# TPL5110 Nano-Power System Timer for Power Gating

## 1 Features

- Supply Voltage From 1.8 V to 5.5 V
- Current Consumption at 2.5 V and 35 nA (Typical)
- Selectable Time Intervals: 100 ms to 7200 s
- Timer Accuracy: 1% (Typical)
- Resistor Selectable Time Interval
- Manual MOSFET Power On
- One-Shot Feature

## 2 Applications

- Battery-Powered Systems
- Internet of Things (IoT)
- Intruder Detection
- Tamper Detection
- Home Automation Sensors
- Thermostats
- Consumer Electronics
- Remote Sensor
- White Goods

## 3 Description

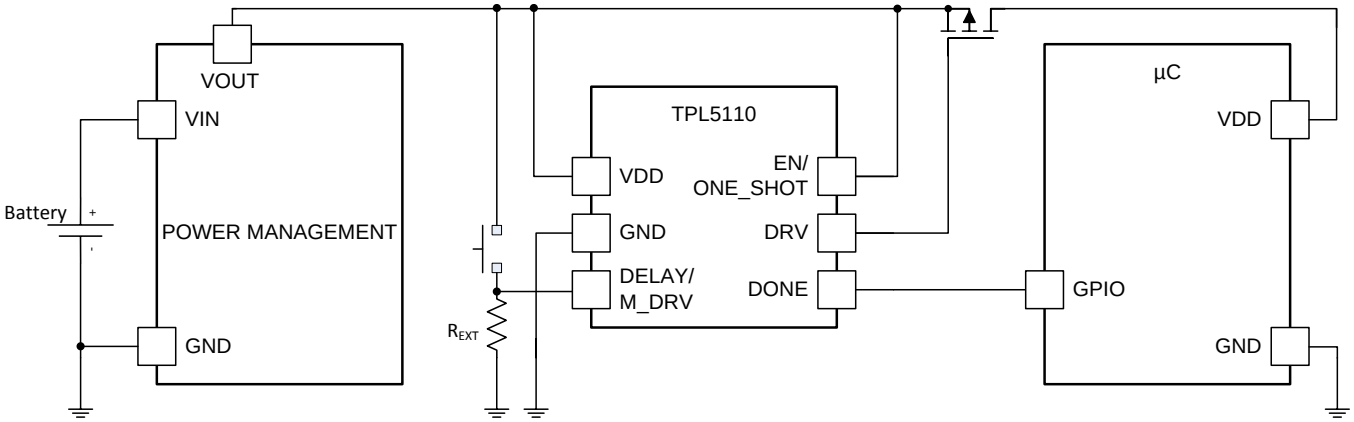
The TPL5110 Nano Timer is a low power timer with an integrated MOSFET driver designed for power gating in duty cycled or battery-powered applications. Consuming only 35 nA, the TPL5110 can enable the power supply line and drastically reduce the overall system stand by current during the sleep time. Such power savings enable the use of significantly smaller batteries for energy harvesting or wireless sensor applications. The TPL5110 provides selectable timing intervals from 100 ms to 7200 s and is designed for power gating applications. In addition, the TPL5110 has a unique One-shot feature where the timer will only power the MOSFET for one cycle. The TPL5110 is available in a 6-pin SOT23 package.

**Device Information**[1]

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TPL5110 | SOT23 (6) | 3.00 mm × 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Application Schematic**




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents



## 4 Revision History

**Changes from Original (January 2015) to Revision A** **Page**

- Changed *Description* text ... 1
- Changed max IDD ... 5
- Changed *TPL5110 Timing* labels ... 6
- Changed *Circuitry* text ... 12
- Changed $T_{ADC}$ and $R_D$ equations in the *Quantization Error* section ... 14
- Added *Receiving Notification of Documentation Updates* section ... 19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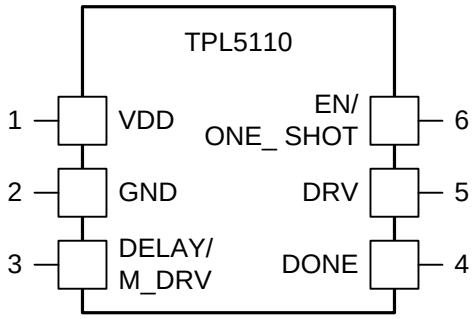
# 5 Pin Configuration and Functions

**DDC Package**
**6-Lead SOT-23**
**Top View**




**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION | APPLICATION INFORMATION |
|---|---|---|---|---|
| NO. | NAME | | | |
| 1 | VDD | P | Supply voltage | |
| 2 | GND | G | Ground | |
| 3 | DELAY/ M_DRV | I | Time interval set and manual MOSFET Power ON | Resistance between this pin and GND is used to select the time interval. The manual MOSFET power ON switch is also connected to this pin. |
| 4 | DONE | I | Logic Input for watchdog functionality | Digital signal driven by the µC to indicate successful processing. |
| 5 | DRV | O | Power Gating output signal generated every $t_{IP}$ | The Gate of the MOSFET is connected to this pin. When DRV = LOW, the MOSFET is ON. |
| 6 | EN/ ONE_SHOT | I | Selector of mode of operation | When EN/ONE_SHOT = HIGH, the TPL5110 works as a TIMER. When EN/ONE_SHOT = LOW, the TPL5110 turns on the MOSFET one time for the programmed time interval. The next power on of the MOSFET is enabled by the manual power ON. |

(1) G= Ground, P= Power, O= Output, I= Input.

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# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage (VDD-GND) | –0.3 | 6 | V |
| Input Voltage at any pin(2) | –0.3 | VDD + 0.3 | V |
| Input Current on any pin | –5 | +5 | mA |
| Junction Temperature, TJ(3) | | 150 | °C |
| Storage Temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The voltage between any two pins should not exceed 6 V.
(3) The maximum power dissipation is a function of $T_J(MAX)$, θJA, and the ambient temperature, $T_A$. The maximum allowable power dissipation at any ambient temperature is PDMAX = ($T_J(MAX)$ - $T_A$)/ θJA. All numbers apply for packages soldered directly onto a printed-circuit board (PCB).

## 6.2 ESD Ratings

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | Human Body Model, per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Ratings

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply Voltage (VDD-GND) | 1.8 | 5.5 | V |
| Temperature | –40 | 105 | °C |

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TPL5110 DDC (SOT-23) 6 PINS | UNIT |
|---|---|---|---|
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 163 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 26 | °C/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 57 | °C/W |
| $ψ_{JT}$ | Junction-to-top characterization parameter | 7.5 | °C/W |
| $ψ_{JB}$ | Junction-to-board characterization parameter | 57 | °C/W |
| $R_{θJC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).


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## 6.5 Electrical Characteristics(1)

Specifications are for $T_A$= 25°C, VDD-GND = 2.5 V, unless otherwise stated.

| PARAMETER | | TEST CONDITIONS | | MIN(2) | TYP(3) | MAX(2) | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| IDD | Supply current(4) | Operation mode | | | 35 | 50 | nA |
| | | Digital conversion of external resistance (Rext) | | | 200 | 400 | µA |
| **TIMER** | | | | | | | |
| $t_{IP}$ | Time interval Period | 1650 selectable Time intervals | Minimum time interval | | 100 | | ms |
| | | | Maximum time interval | | 7200 | | s |
| | Time interval Setting Accuracy(5) | Excluding the precision of Rext | | | ±0.6% | | |
| | Time interval Setting Accuracy over supply voltage | 1.8 V ≤ VDD ≤ 5.5 V | | | ±25 | | ppm/V |
| $t_{OSC}$ | Oscillator Accuracy | | | –0.5% | | 0.5% | |
| | Oscillator Accuracy over temperature(6) | –40°C ≤ $T_A$≤ 105°C | | | ±100 | ±400 | ppm/°C |
| | Oscillator Accuracy over supply voltage | 1.8 V ≤ VDD ≤ 5.5 V | | | ±0.4 | | %/V |
| | Oscillator Accuracy over life time(7) | | | | ±0.24% | | |
| $t_{DONE}$ | DONE Pulse width (6) | | | 100 | | | ns |
| $t_{DRV}$ | DRV Pulse width | DONE signal not received | | | $t_{IP}$-50 ms | | |
| t_Rext | Time to convert Rext | | | | 100 | 120 | ms |
| **DIGITAL LOGIC LEVELS** | | | | | | | |
| VIH | Logic High Threshold DONE pin | | | 0.7 × VDD | | | V |
| VIL | Logic Low Threshold DONE pin | | | | | 0.3 × VDD | V |
| VOH | Logic output High Level DRV pin | Iout = 100 µA | | VDD – 0.3 | | | V |
| | | Iout = 1 mA | | VDD – 0.7 | | | V |
| VOL | Logic output Low Level DRV pin | Iout = -100 µA | | | | 0.3 | V |
| | | Iout = –1 mA | | | | 0.7 | V |
| $VIH_{M\_DRV}$ | Logic High Threshold DELAY/M_DRV pin | | | 1.5 | | | V |

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current excludes load and pullup resistor current. Input pins are at GND or VDD.
(5) The accuracy for time interval settings below 1 second is ±100 ms.
(6) This parameter is specified by design and/or characterization and is not tested in production.
(7) Operational life time test procedure equivalent to 10 years.

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## 6.6 Timing Requirements

| | | | MIN(1) | NOM(2) | MAX(1) | UNIT |
|---|---|---|---|---|---|---|
| $tr_{DRV}$ | Rise Time DRV(3) | Capacitive load 50 pF | | 50 | | ns |
| $tf_{DRV}$ | Fall Time DRV(3) | Capacitive load 50 pF | | 50 | | ns |
| $tD_{DONE}$ | DONE to DRV delay | Minimum delay(4) | | 100 | | ns |
| | | Maximum delay (4) | | $t_{DRV}$ | | |
| $t_{M\_DRV}$ | Valid manual MOSFET Power ON | Observation time 30 ms | 20 | | | ms |
| $t_{DB}$ | De-bounce manual MOSFET Power ON | | | 20 | | ms |

(1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(3) This parameter is specified by design and/or characterization and is not tested in production.
(4) From DRV falling edge.

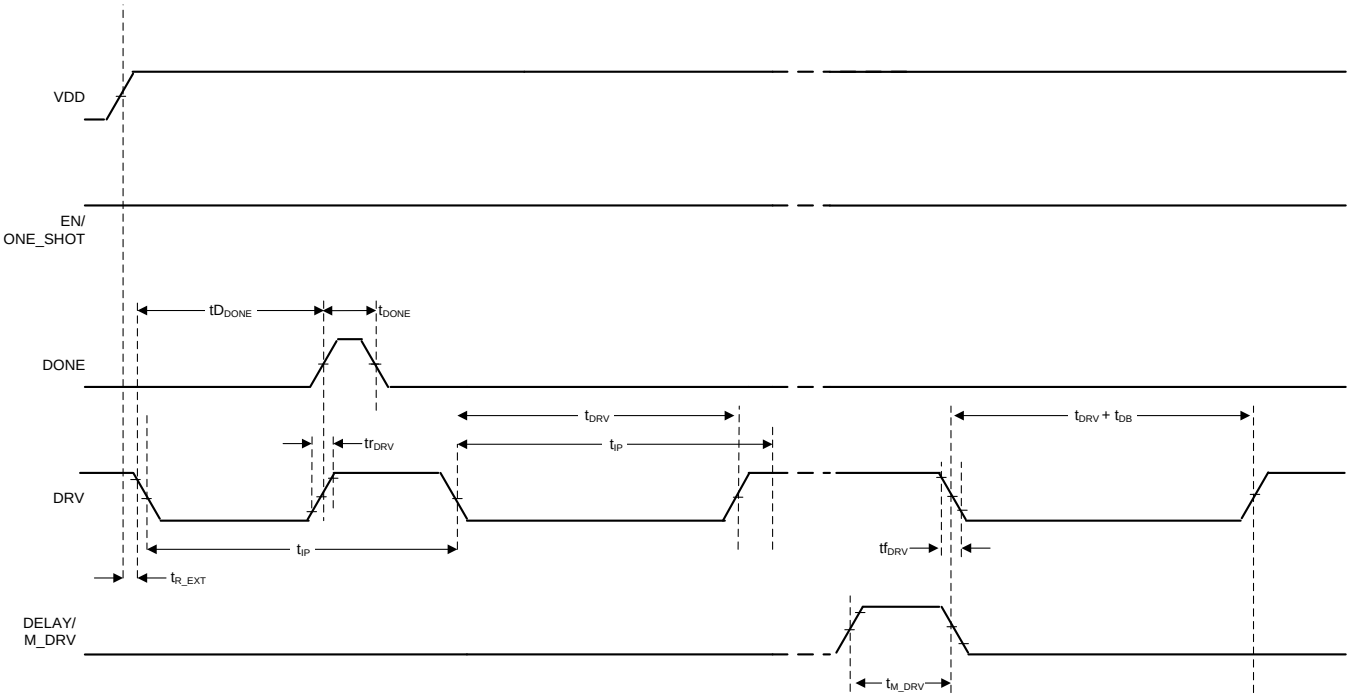


**Figure 1. TPL5110 Timing**


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## 6.7 Typical Characteristics

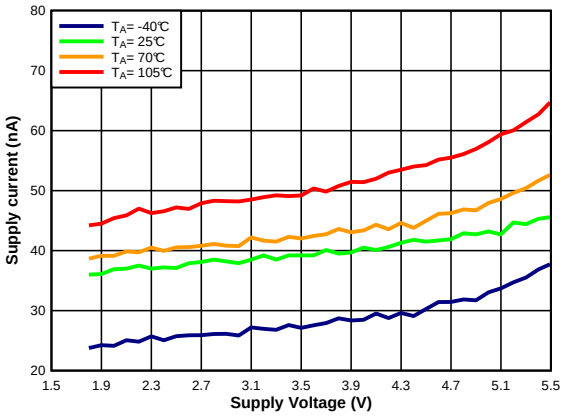



**Figure 2. $I_{DD}$ vs. $V_{DD}$**

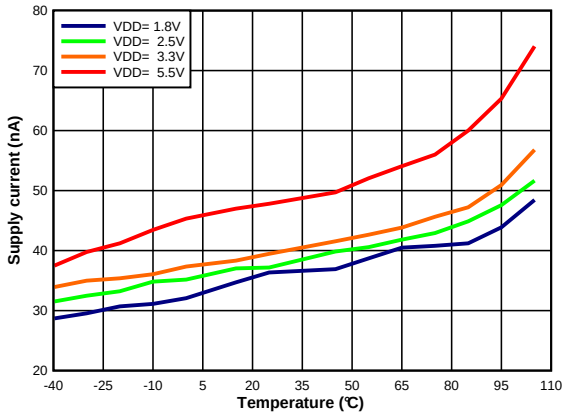



**Figure 3. $I_{DD}$ vs. Temperature**

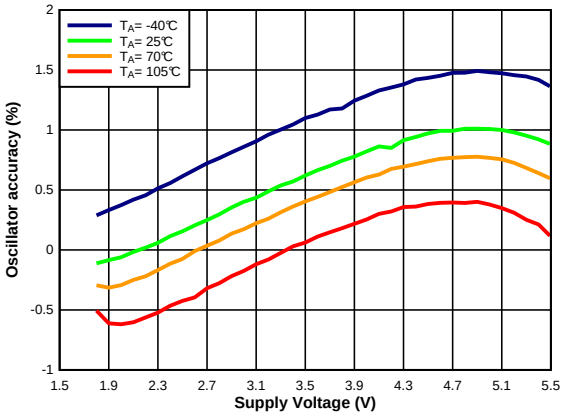



**Figure 4. Oscillator Accuracy vs. $V_{DD}$**

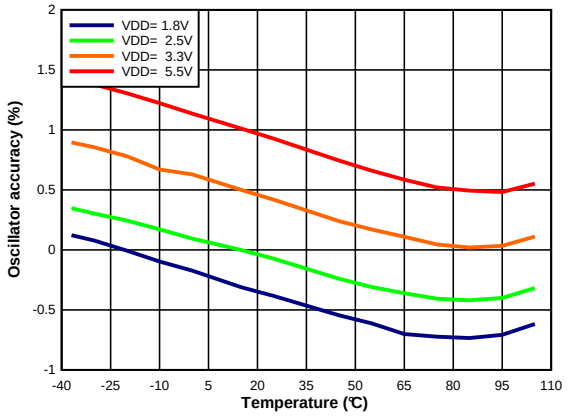



**Figure 5. Oscillator Accuracy vs. Temperature**

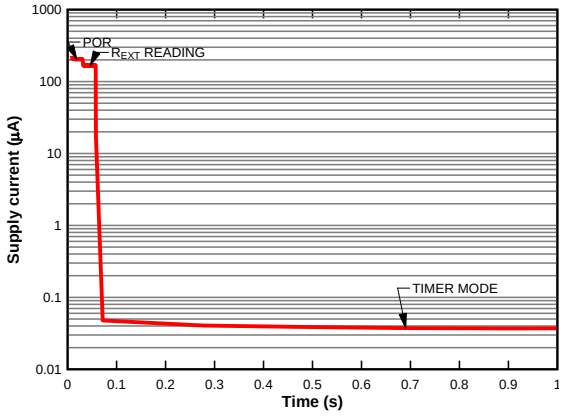
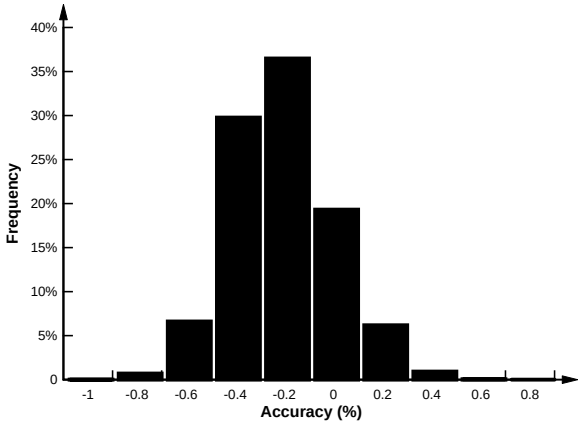



**Figure 6. $I_{DD}$ vs. Time**




number of observations >20000

1s < $t_{IP}$ ≤ 7200s

**Figure 7. Time interval Setting Accuracy**

# 7 Detailed Description

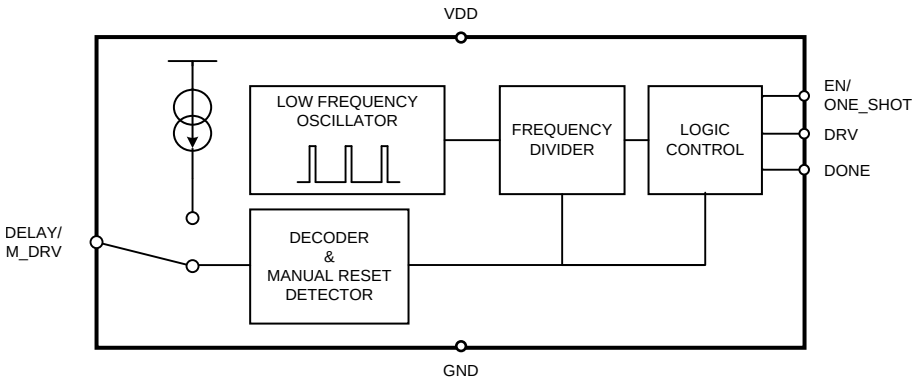
## 7.1 Overview

The TPL5110 is a timer with power gating feature. It is ideal for use in power-cycled applications and provides selectable timing from 100 ms to 7200 s.

Once configured in timer mode (EN/ONE_SHOT= HIGH) the TPL5110 periodically sends out a DRV signal to a MOSFET to turn on the µC. If the µC replies with a DONE signal within the programmed time interval ($t_{DRV}$) the TPL5110 turns off the µC, otherwise the TPL5110 keeps the µC in the on state for a time equal to $t_{DRV}$.

The TPL5110 can work also in a one-shot mode (EN/ONE_SHOT= LOW). In this mode the DRV signal is sent out just one time at the power on of the TPL5110 to turn on the µC. If the µC replies with a DONE signal within the programmed time interval ($t_{DRV}$) the TPL5110 turns off the µC, otherwise the TPL5110 keeps the µC in the on state for a time equal to $t_{DRV}$.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The TPL5110 implements a periodical power gating feature or one shot power gating according to the EN/ONE_SHOT voltage. A manual MOSFET Power ON function is realized by momentarily pulling the DELAY/M_DRV pin to VDD.

### 7.3.1 DRV

The gate of the MOSFET is connected to the DRV pin. When DRV=LOW, the MOSFET is turned ON. The pulse generated at DRV is equal to the selected time interval period, minus 50 ms. It is shorter in the case of a DONE signal received from the µC. If the DONE signal is not received within the programmed time interval (minus 50 ms), the DRV signal will be high for the last 50 ms of the time interval to turn off the MOSFET before the next cycle starts.

The default value (after resistance reading) is HIGH. The signal is sent out from the TPL5110 when the programmed time interval starts. When the DRV is LOW, the manual power ON signal is ignored.

### 7.3.2 DONE

The DONE pin is driven by a µC to signal that the µC is working properly. The TPL5110 recognizes a valid DONE signal as a low to high transition. If two or more DONE signals are received within the time interval, only the first DONE signal is processed. The minimum DONE signal pulse length is 100 ns. When the TPL5110 receives the DONE signal it asserts DRV logic HIGH.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## 7.4 Device Functional Modes

### 7.4.1 Start-Up

During start-up, after POR, the TPL5110 executes a one-time measurement of the resistance attached to the DELAY/M_DRV pin in order to determine the desired time interval for DRV. This measurement interval is $t_{R\_EXT}$. During this measurement a constant current is temporarily flowing into $R_{EXT}$.

Once the reading of the external resistance is complete, the TPL5110 enters automatically in one of the two modes according to the EN/ONE_SHOT value. The EN/ONE_SHOT pin needs to be hard wired to GND or VDD according to the required mode of operation.

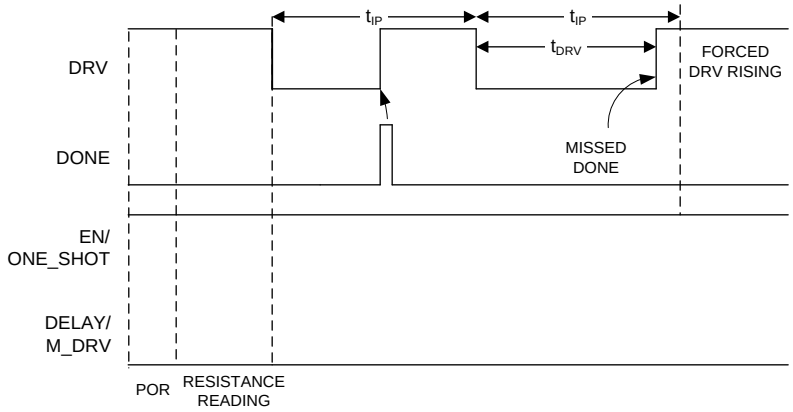


**Figure 8. Start-Up - Timer Mode**

### 7.4.2 Timer Mode

During timer mode (EN/ONE_SHOT = HIGH), the TPL5110 asserts periodic DRV pulses according to the programmed time interval. The length of the DRV pulses is set by the receiving of a DONE pulse from the µC. See Figure 8.

### 7.4.3 One-Shot Mode

During one-shot mode (EN/ONE_SHOT = LOW), the TPL5110 generates just one pulse at the DRV pin which lasts according to the programmed time interval. In one-shot mode, other DRV pulses can be triggered using the DELAY/M_DRV pin. If a valid manual power ON occurs when EN/ONE_SHOT is LOW, the TPL5110 generates just one pulse at the DRV pin. The duration of the pulse is set by the programmed time interval. Also in this case, if a DONE signal is received within the programmed time interval (minus 50 ms), the MOSFET connected to the DRV pin is turned off. See Figure 9 and Figure 10.

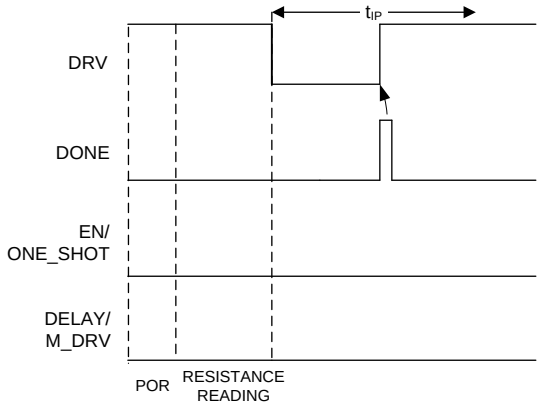


**Figure 9. Start-Up One-Shot Mode (DONE Received Within $t_{IP}$)**

## Device Functional Modes (continued)

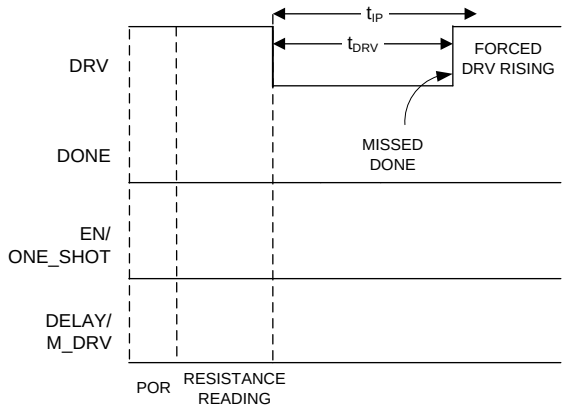


**Figure 10. Start-Up One-Shot Mode (No DONE Received Within $t_{IP}$)**

## 7.5 Programming

### 7.5.1 Configuring the Time Interval With the DELAY/M_DRV Pin

The time interval between two adjacent DRV pulses (falling edges, in timer mode) is selectable through an external resistance ($R_{EXT}$) between the DELAY/M_DRV pin and ground. The resistance ($R_{EXT}$) must be in the range between 500 Ω and 170 kΩ. At least a 1% precision resistance is recommended. See section *Selection of the External Resistance* on how to set the time interval using $R_{EXT}$.

### 7.5.2 Manual MOSFET Power ON Applied to the DELAY/M_DRV Pin

If VDD is connected to the DELAY/M_DRV pin, the TPL5110 recognizes this as a manual MOSFET Power ON condition. In this case the time interval is not set. If the manual MOSFET Power ON is asserted during the POR or during the reading procedure, the reading procedure is aborted and is restarted as soon as the manual MOSFET Power ON switch is released. A pulse on the DELAY/M_DRV pin is recognized as a valid manual MOSFET Power ON only if it lasts at least 20 ms (observation time is 30 ms). The manual MOSFET Power ON may be implemented using a switch (momentary mechanical action).

If the DRV is already LOW (MOSFET ON) the manual MOSFET Power ON is ignored.

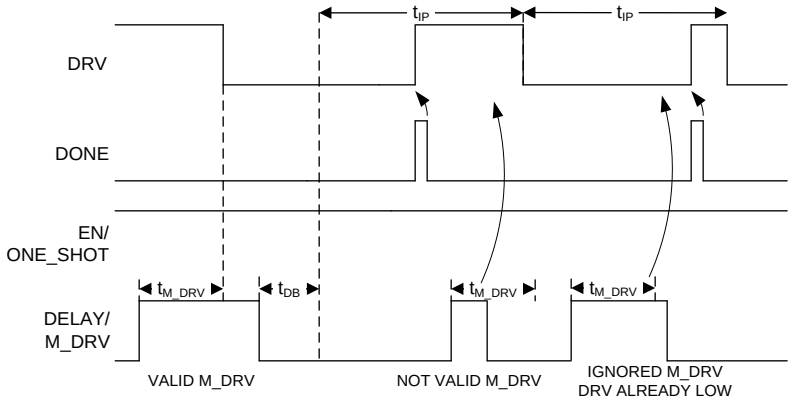


**Figure 11. Manual MOSFET Power ON in Timer Mode**


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## Programming (continued)

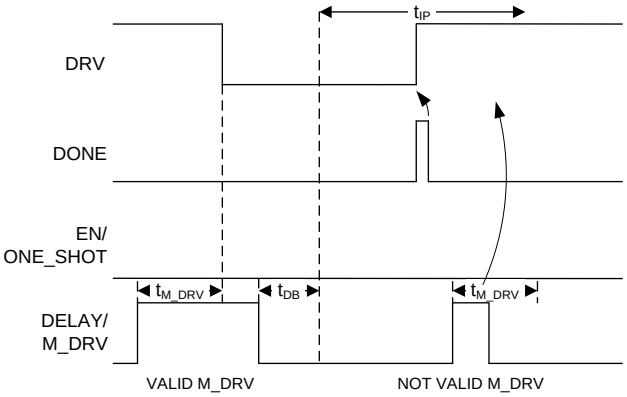


**Figure 12. Manual MOSFET Power ON in One-Shot Mode**

### *7.5.2.1 DELAY/M_DRV*

A resistance in the range between 500 Ω and 170 kΩ must to be connected to the DELAY/M_DRV pin to select a valid time interval. At the POR and during the reading of the resistance, the DELAY/M_DRV is connected to an analog signal chain through a mux. After the reading of the resistance, the analog circuit is switched off and the DELAY/M_DRV is connected to a digital circuit.

In this state, a logic HIGH applied to the DELAY/M_DRV pin is interpreted by the TPL5110 as a manual power ON. The manual power ON detection is provided with a de-bounce feature (on both edges) which makes the TPL5110 insensitive to the glitches on the DELAY/M_DRV.

The M_DRV must stay high for at least 20 ms to be valid. Once a valid signal at DELAY/M_DRV is understood as a manual power on, the DRV signal will be asserted in the next 10 ms. Its duration will be according to the programmed time interval (minus 50 ms), or less if the DONE is received.

A manual power ON signal resets all the counters. The counters will restart as soon as a valid manual power ON signal is recognized and the signal at DELAY/M_DRV pin is asserted LOW. Due to the asynchronous nature of the manual power ON signal and its arbitrary duration, the LOW status of the DRV signal may be affected by an uncertainty of about ±5 ms.

An extended assertion of a logic HIGH at the DELAY/M_DRV pin will turn on the MOSFET for a time longer than the programmed time interval. DONE signals received while the DELAY/M_DRV is HIGH are ignored. If the DRV is already LOW (MOSFET ON) the manual power ON is ignored.

### *7.5.2.2 Circuitry*

The manual Power ON may be implemented using a switch (momentary mechanical action). The TPL5110 offers two possible approaches according to the power consumption constraints of the application.

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## Programming (continued)

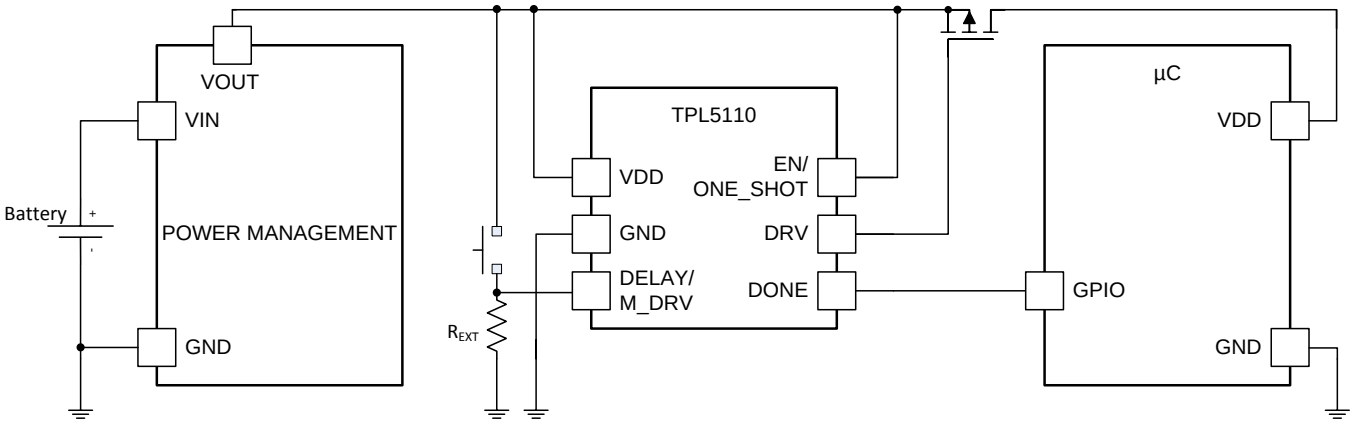


**Figure 13. Manual MOSFET Power ON With SPST Switch**

For use cases that do not require the lowest power consumption, using a single-pole single-throw switch may offer a lower-cost solution. The DELAY/M_DRV pin may be directly connected to VDD with $R_{EXT}$ in the circuit. The current drawn from the supply voltage during the manual power ON is given by VDD/$R_{EXT}$.

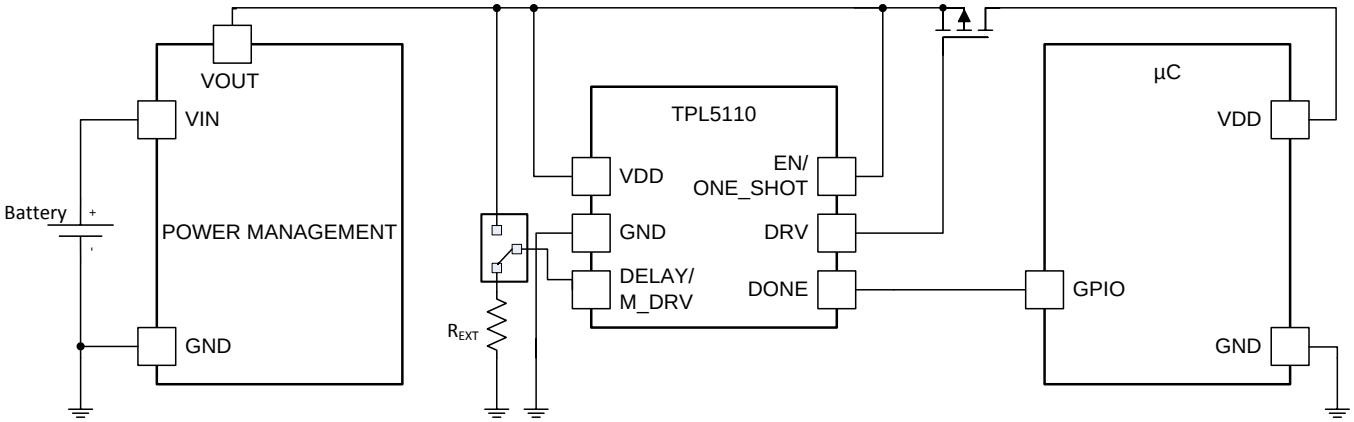


**Figure 14. Manual MOSFET Power ON With SPDT Switch**

The manual MOSFET Power ON function may also be asserted by switching DELAY/M_DRV from $R_{EXT}$ to VDD using a single-pole double-throw switch, which will provide a lower power solution for the manual power ON, because no current flows.

### 7.5.3 Selection of the External Resistance

To set the time interval, the external resistance $R_{EXT}$ is selected according to Equation 1:

$$R_{EXT} = 100 \left( \frac{-b + \sqrt{b^2 - 4a(c - 100\,T)}}{2a} \right) \quad (1)$$

where

- T is the desired time interval in seconds.
- $R_{EXT}$ is the resistance value to use in Ω.
- a, b, c are coefficients depending on the range of the time interval.


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## Programming (continued)

**Table 1. Coefficients for Equation 1**

| SET | Time Interval Range (s) | a | b | c |
|---|---|---|---|---|
| 1 | 1 <T≤ 5 | 0.2253 | -20.7654 | 570.5679 |
| 2 | 5 <T≤ 10 | -0.1284 | 46.9861 | -2651.8889 |
| 3 | 10 <T≤ 100 | 0.1972 | -19.3450 | 692.1201 |
| 4 | 100 <T≤ 1000 | 0.2617 | -56.2407 | 5957.7934 |
| 5 | T> 1000 | 0.3177 | -136.2571 | 34522.4680 |

### EXAMPLE

Required time interval: 8 s

The coefficient set to be selected is the number 2. The formula becomes Equation 2.

$$R_{EXT}=100\left(\frac{46.9861-\sqrt{46.9861^2+4*0.1284\left(-2561.8889-100*8\right)}}{2*0.1284}\right) \quad (2)$$

The resistance value is 10.18 kΩ.

Table 2 and Table 3 contain example values of $t_{IP}$ and their corresponding value of $R_{EXT}$.

**Table 2. First 9 Time Intervals**

| $t_{IP}$ (ms) | Resistance (Ω) | Closest real value (Ω) | Parallel of two 1% tolerance resistors, (kΩ) |
|---|---|---|---|
| 100 | 500 | 500 | 1.0 // 1.0 |
| 200 | 1000 | 1000 | - |
| 300 | 1500 | 1500 | 2.43 // 3.92 |
| 400 | 2000 | 2000 | - |
| 500 | 2500 | 2500 | 4.42 // 5.76 |
| 600 | 3000 | 3000 | 5.36 // 6.81 |
| 700 | 3500 | 3500 | 4.75 // 13.5 |
| 800 | 4000 | 4000 | 6.19 // 11.3 |
| 900 | 4500 | 4501 | 6.19 // 16.5 |

**Table 3. Most Common Time Intervals Between 1s to 2h**

| $t_{IP}$ | Calculated Resistance (kΩ) | Closest Real Value (kΩ) | Parallel of Two 1% Tolerance Resistors,(kΩ) |
|---|---|---|---|
| 1s | 5.20 | 5.202 | 7.15 // 19.1 |
| 2s | 6.79 | 6.788 | 12.4 // 15.0 |
| 3s | 7.64 | 7.628 | 12.7// 19.1 |
| 4s | 8.30 | 8.306 | 14.7 // 19.1 |
| 5s | 8.85 | 8.852 | 16.5 // 19.1 |
| 6s | 9.27 | 9.223 | 18.2 // 18.7 |
| 7s | 9.71 | 9.673 | 19.1 // 19.6 |
| 8s | 10.18 | 10.180 | 11.5 // 8.87 |
| 9s | 10.68 | 10.68 | 17.8 // 26.7 |
| 10s | 11.20 | 11.199 | 15.0 // 44.2 |
| 20s | 14.41 | 14.405 | 16.9 // 97.6 |
| 30s | 16.78 | 16.778 | 32.4 // 34.8 |
| 40s | 18.75 | 18.748 | 22.6 // 110.0 |
| 50s | 20.047 | 20.047 | 28.7 // 66.5 |

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**Table 3. Most Common Time Intervals Between 1s to 2h (continued)**

| $t_{IP}$ | Calculated Resistance (kΩ) | Closest Real Value (kΩ) | Parallel of Two 1% Tolerance Resistors,(kΩ) |
|---|---|---|---|
| 1min | 22.02 | 22.021 | 40.2 // 48.7 |
| 2min | 29.35 | 29.349 | 35.7 // 165.0 |
| 3min | 34.73 | 34.729 | 63.4 // 76.8 |
| 4min | 39.11 | 39.097 | 63.4 // 102.0 |
| 5min | 42.90 | 42.887 | 54.9 // 196.0 |
| 6min | 46.29 | 46.301 | 75.0 // 121.0 |
| 7min | 49.38 | 49.392 | 97.6 // 100.0 |
| 8min | 52.24 | 52.224 | 88.7 // 127.0 |
| 9min | 54.92 | 54.902 | 86.6 // 150.0 |
| 10min | 57.44 | 57.437 | 107.0 // 124.0 |
| 20min | 77.57 | 77.579 | 140.0 // 174.0 |
| 30min | 92.43 | 92.233 | 182.0 // 187.0 |
| 40min | 104.67 | 104.625 | 130.0 // 536.00 |
| 50min | 115.33 | 115.331 | 150.0 // 499.00 |
| 1h | 124.91 | 124.856 | 221.0 // 287.00 |
| 1h30min | 149.39 | 149.398 | 165.0 // 1580.0 |
| 2h | 170.00 | 170.00 | 340.0 // 340.0 |

### 7.5.4 Quantization Error

The TPL5110 can generate 1650 discrete timer intervals in the range of 100 ms to 7200 s. The first 9 intervals are multiples of 100 ms. The remaining 1641 intervals cover the range between 1 s to 7200 s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to Equation 3:

$$Err = 100\frac{\left(T_{DESIRED} - T_{ADC}\right)}{T_{DESIRED}}$$

where

- $T_{ADC} = INT\left[\frac{1}{100}\left(aR_D^2 + bR_D + c\right)\right]$
- $R_D = \frac{R_{EXT}}{100}$ (3)

$R_{EXT}$ is the resistance calculated with Equation 1 and a, b, c are the coefficients of the equation listed in Table 1.

### 7.5.5 Error Due to Real External Resistance

$R_{EXT}$ is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical $R_{EXT}$ using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of $R_{EXT}$ ($R_{EXT\_MIN}$, $R_{EXT\_MAX}$ with Equation 1 using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC\_MIN}[R_{EXT\_MIN}]$, $T_{ADC\_MAX}[R_{EXT\_MAX}]$) with the $T_{ADC}$ equation mentioned in Equation 3.
3. Find the errors using Equation 3 with $T_{ADC\_MIN}$, $T_{ADC\_MAX}$.

The results of the formula indicate the accuracy of the time interval.


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The example below illustrates the procedure.

- Desired time interval, T_desired = 600 s,
- Required $R_{EXT}$ from Equation 1, $R_{EXT}$= 57.44 kΩ.

From Table 3, $R_{EXT}$ can be built with a parallel combination of two commercial values with 1% tolerance: R1 =1 07 kΩ, R2 = 124 kΩ. The uncertainty of the equivalent parallel resistance can be found using Equation 4:

$$uR_{//} = R_{//}\sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2} \quad (4)$$

where

- uRn (n=1,2) represent the uncertainty of a resistance (see Equation 5)

$$u_{Rn} = Rn\frac{Tolerance}{\sqrt{3}} \quad (5)$$

The uncertainty of the parallel resistance is 0.82%, which means the value of $R_{EXT}$ may range between $R_{EXT\_MIN}$ = 56.96 kΩ and $R_{EXT\_MAX}$ = 57.90 kΩ.

Using these value of $R_{EXT}$, the digitized timer intervals calculated by $T_{ADC}$ equation mentioned in Equation 3 are respectively $T_{ADC\_MIN}$ = 586.85 s and $T_{ADC\_MAX}$ = 611.3 s, giving an error range of –1.88% / +2.19%. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

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# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

In battery-powered applications, one design constraint is the need for low current consumption. The TPL5110 is designed for applications where there is a need to monitor environmental conditions at a fixed time interval. Often in these applications a watchdog or other internal timer in a µC is used to implement a wake-up function. Typically, the power consumption of these functions is not optimized. Using the TPL5110 to implement a periodical power gating of the µC or of the entire system the current consumption will be only tens of nA.

## 8.2 Typical Application

The TPL5110 can be used in environment sensor nodes such as humidity and temperature sensor node. The sensor node has to measure the humidity and the temperature and transmit the data through a low power RF micro such as the CC2531. The temperature and the humidity in home application do not change so fast, so the measurement and the transmission of the data can be done at very low rate, such as every 30 seconds. The RF micro should spend most of the time in counting the elapsed time, but using the TPL5110 it is possible to complete turn off the RF micro and extend the battery life. The TPL5110 will turn on the RF micro when the programmed time interval elapses or for debug purpose with the manual MOSFET Power ON switch.

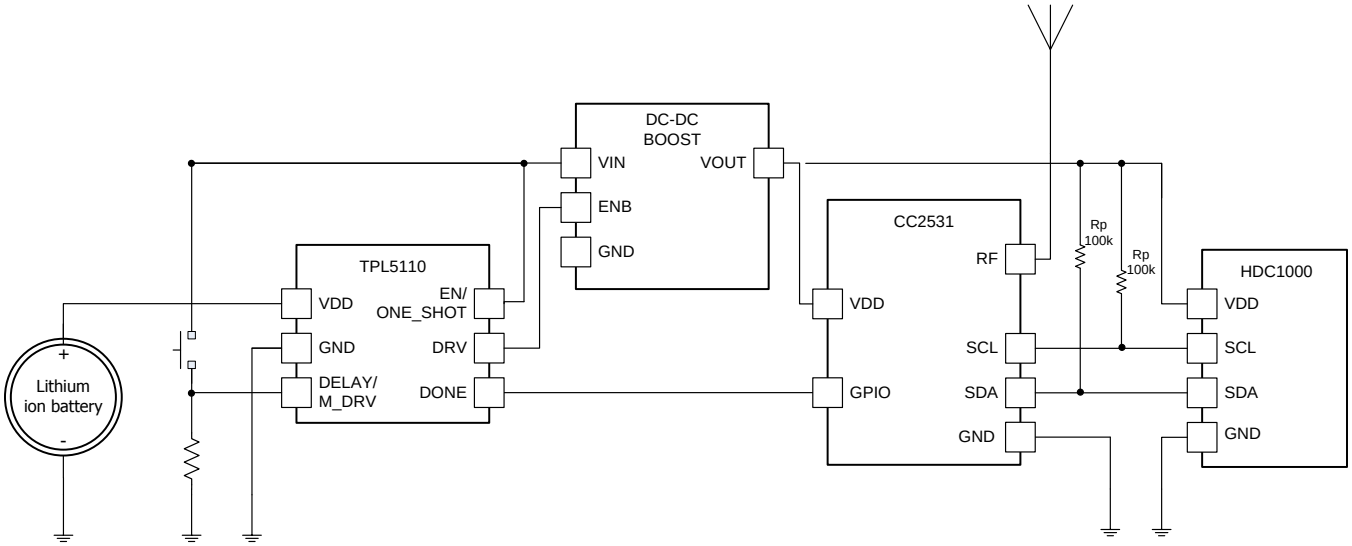


**Figure 15. Sensor Node**

### 8.2.1 Design Requirements

The design is driven by the low current consumption constraint. The data are usually acquired on a rate which is in the range between 30 s and 60 s. The highest necessity is the maximization of the battery life. The TPL5110 helps achieve this goal because it allows turning off the RF micro.

### 8.2.2 Detailed Design Procedure

When the focal constraint is the battery life, the selection of a low power voltage regulator and low leakage MOSFET to power gate the µC is mandatory. The first step in the design is the calculation of the power consumption of each device in the different mode of operations. An example is the HDC1000, in measurement mode the RF micro is in normal operation and transmission. The different modes offer the possibility to select the appropriate time interval which respect the application constraint and maximize the life of the battery.


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## Typical Application (continued)

### 8.2.3 Application Curve

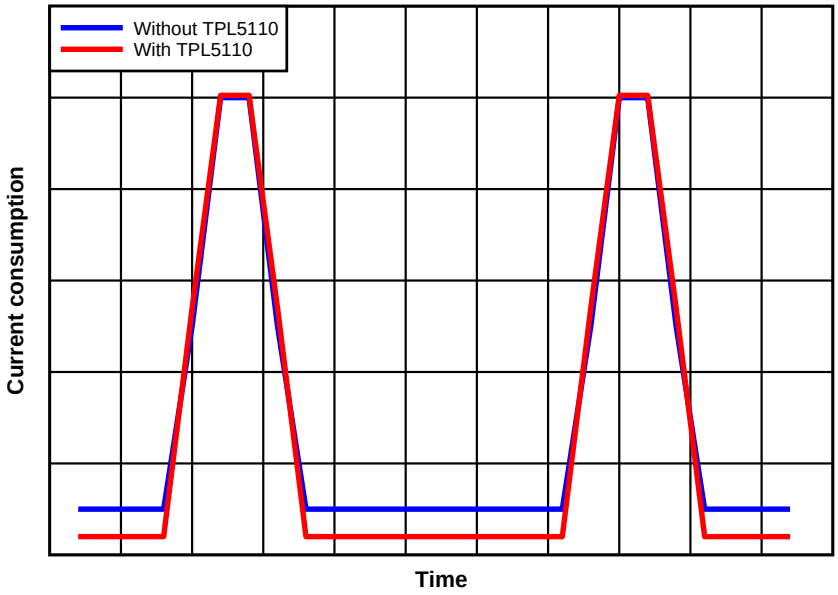


**Figure 16. Effect of TPL5110 on Current Consumption**

## 9 Power Supply Recommendations

The TPL5110 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1 μF between VDD and GND pin is recommended.

## 10 Layout

### 10.1 Layout Guidelines

The DELAY/M_DRV pin is sensitive to parasitic capacitance. TI suggests that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the DRV pin is also improved by keeping the trace length between the TPL5110 and the gate of the MOSFET short to reduce the parasitic capacitance. The EN/ONE_SHOT needs to be tied to GND or VDD with short traces.

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## 10.2 Layout Example

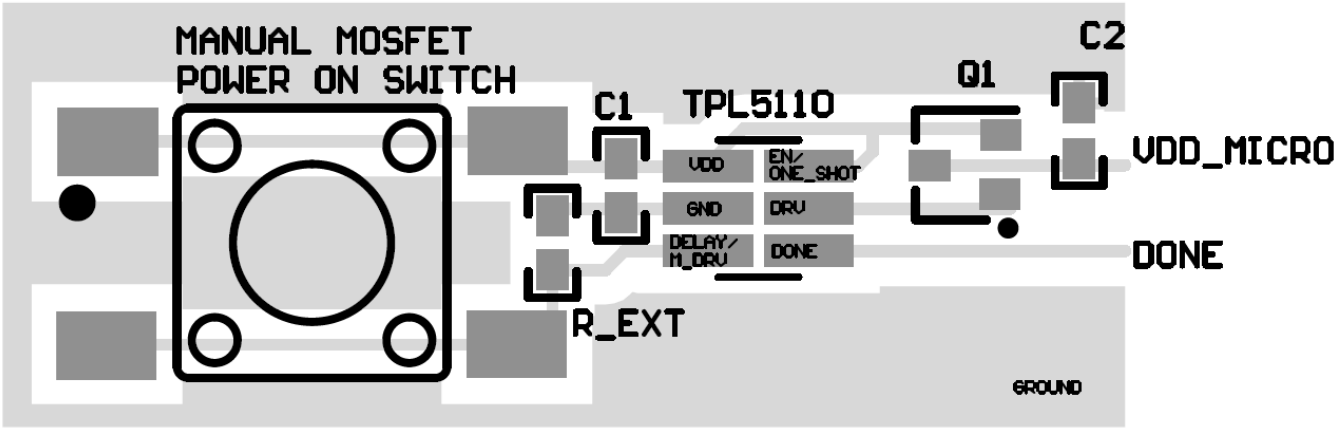


**Figure 17. Layout**


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# 11 Device and Documentation Support

## 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPL5110DDCR | Active | Production | SOT-23-THIN (DDC) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCR.A | Active | Production | SOT-23-THIN (DDC) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCR.B | Active | Production | SOT-23-THIN (DDC) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCT | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCT.A | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCT.B | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCTG4 | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCTG4.A | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |
| TPL5110DDCTG4.B | Active | Production | SOT-23-THIN (DDC) \| 6 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ZALX |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPL5110 :**

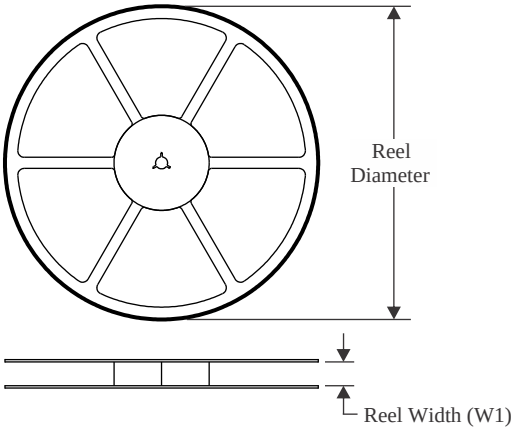
- Automotive : TPL5110-Q1

NOTE: Qualified Version Definitions:

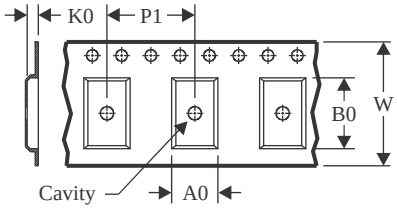
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

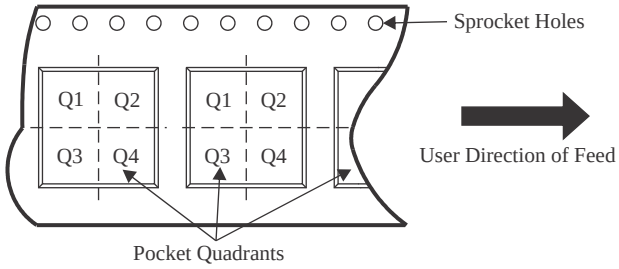



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

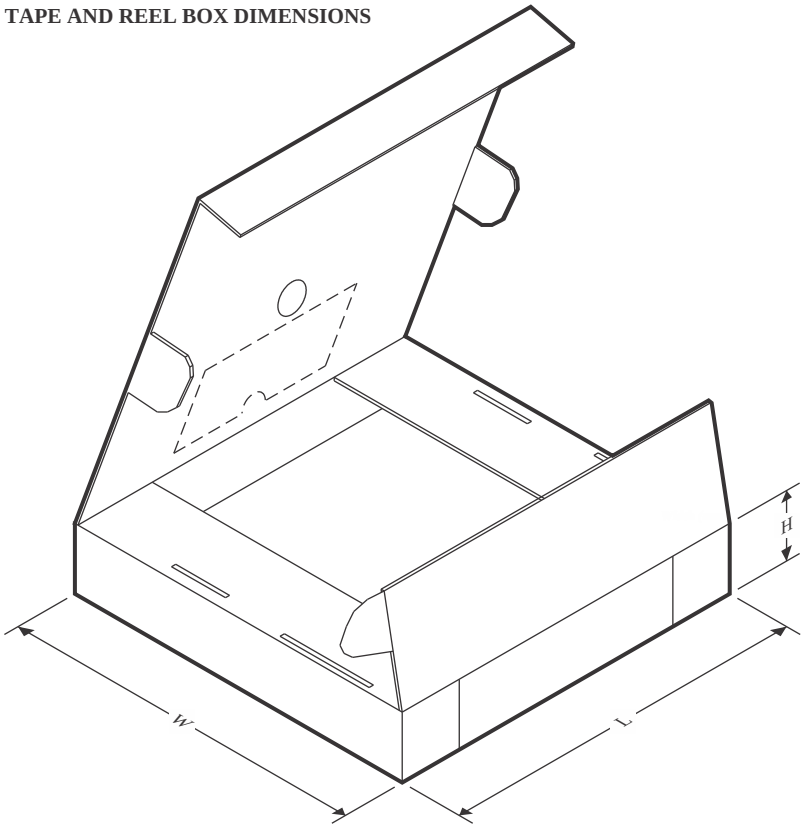
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPL5110DDCR | SOT-23-THIN | DDC | 6 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPL5110DDCT | SOT-23-THIN | DDC | 6 | 250 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPL5110DDCTG4 | SOT-23-THIN | DDC | 6 | 250 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

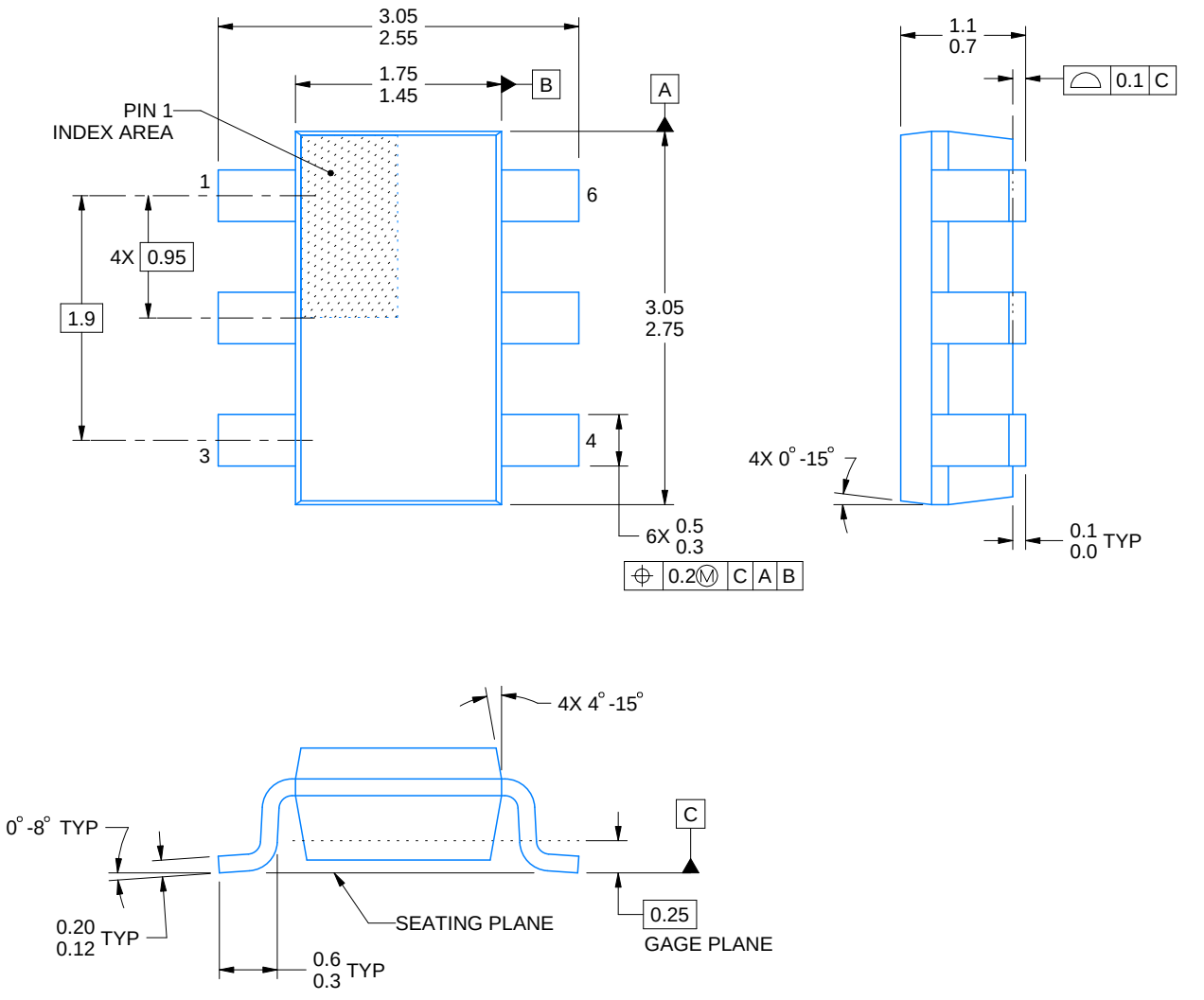
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPL5110DDCR | SOT-23-THIN | DDC | 6 | 3000 | 208.0 | 191.0 | 35.0 |
| TPL5110DDCT | SOT-23-THIN | DDC | 6 | 250 | 208.0 | 191.0 | 35.0 |
| TPL5110DDCTG4 | SOT-23-THIN | DDC | 6 | 250 | 208.0 | 191.0 | 35.0 |

# PACKAGE OUTLINE

## DDC0006A

## SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

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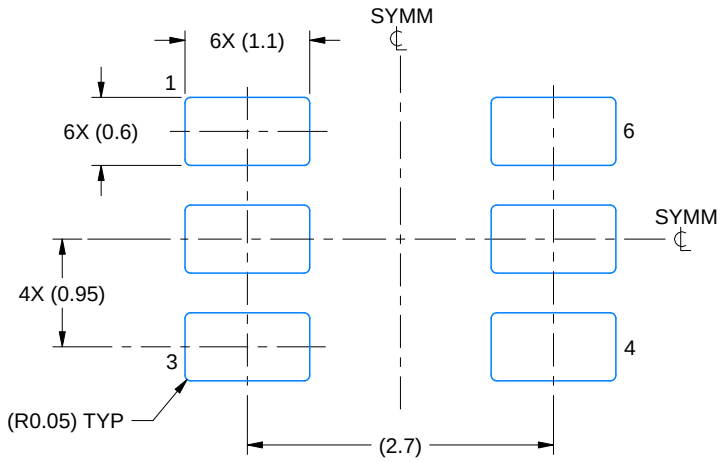
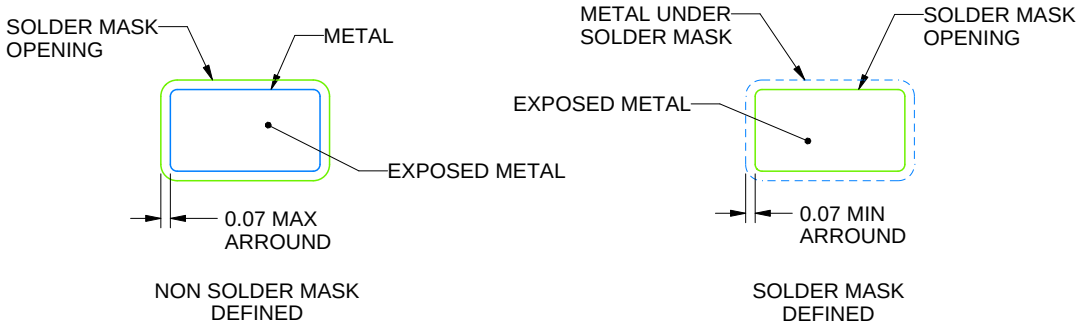
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.




LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X




SOLDERMASK DETAILS

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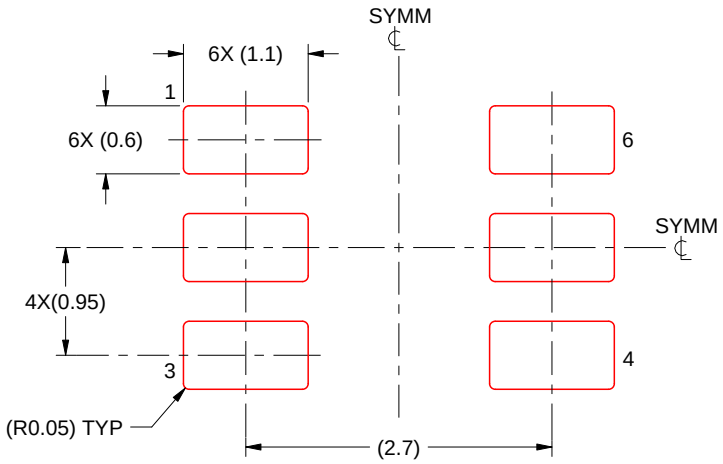
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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