TPL0501 256-Taps, Single-Channel, Digital Potentiometer With SPI Interface

1 Features

- Single-channel, 256-position resolution
- 100-kΩ end-to-end resistance options
- Low temperature coefficient: 35 ppm/°C
- SPI-compatible serial interface
- 2.7-V to 5.5-V single-supply operation
- ±20% resistance tolerance
- Operating temperature: –40°C to +125°C
- ESD performance tested per JESD 22
  - 2000-V human-body model (A114-B, Class II)

2 Applications

- Pulse oximeter
- Water meter
- Camera
- Medical sensor patches
- Building security gateway

3 Description

The TPL0501 device is a single-channel, linear-taper, digital potentiometer with 256 wiper positions. This device can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0501 is currently offered with end-to-end resistance of 100 kΩ. The internal registers of the TPL0501 can be accessed using a SPI-compatible interface. The TPL0501 has a nominal temperature coefficient of 35 ppm/°C.

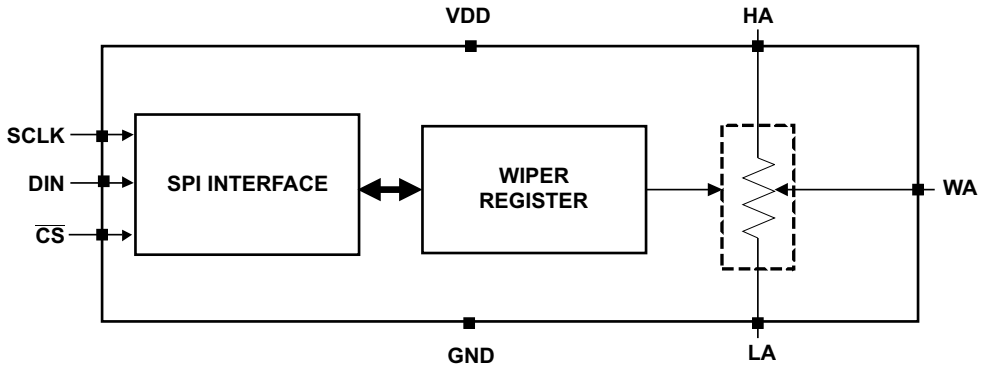
The TPL0501 is available in 8-pin SOT-23 and 8-pin UQFN packages, with a specified temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPL0501	UQFN (8)	1.50 mm × 1.50 mm
	SOT-23 (8)	1.63 mm × 2.90 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2016) to Revision C — **Page**

- Changed maximum temp range in last sentence of *Description* section from 85°C to 125°C (typo) ... 1

Changes from Revision A (September 2011) to Revision B — **Page**

- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added register map default value in Table 1 ... 11
- Changed ratio to correct form in *Ideal Resistance Values* section and in Table 2; registers names for RWL and RHW were reversed. ... 12

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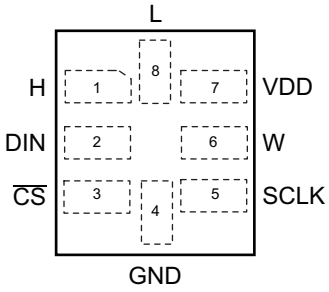
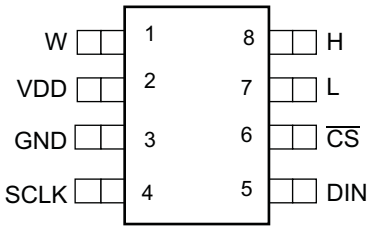
5 Pin Configuration and Functions

RSE Package
8-Pin UQFN
Top View



DCN Package
8-Pin SOT-23
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	SOT-23	UQFN		
$\overline{CS}$	6	3	I	SPI chip select (active low)
DIN	5	2	I	SPI input
GND	3	4	G	Ground
H	8	1	I/O	High terminal
L	7	8	I/O	Low terminal
SCLK	4	5	I	SPI clock
VDD	2	7	P	Positive supply voltage
W	1	6	I/O	Wiper terminal

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

		MIN	MAX	UNIT
Supply voltage	V_{DD} to GND	–0.3	7	V
	V_H, V_L, V_W	–0.3	V_{DD} + 0.3	
Pulse current, I_H, I_L, I_W			±20	mA
Continuous current, I_H, I_L, I_W (TPL0501-100)			±5	mA
Digital input voltage, V_I		–0.3	7	V
Operating temperature, T_j			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Thermal Information

THERMAL METRIC[1]		TPL0501		UNIT
		DCN (SOT-23)	RSE (UQFN)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	205.6	118.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	122.3	62.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.9	26.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.7	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	97.8	26.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.4 Electrical Characteristics: Analog Specifications

typical values are specified at VDD = 5 V and operating temperature is 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TOTAL}	End-to-end resistance	Between Hi and Li terminals	80	100	120	kΩ
V_H, V_L	Terminal voltage		0		VDD	V
R_H, R_L	Terminal resistance			50	150	Ω
R_W	Wiper resistance	H terminal floating, V_L = GND, Force I_W = (V_{DD}/2) / R_{TOTAL}, input code = 0x80h		25	100	Ω
C_H, C_L	Terminal capacitance	f = 1 MHz, measured to GND, input code = 0x80h		15		pF
C_W	Wiper capacitance	f = 1 MHz, measured to GND, input code = 0x80h		12		pF
I_{LKG}	Terminal leakage current	V_H = GND to V_{DD}, V_L = floating *or* V_L = GND to V_{DD}, V_H = floating		0.1	1	µA
TC_R	Resistance temperature coefficient			35		ppm/°C
VOLTAGE DIVIDER MODE[1]						
INL	Integral non-linearity		–1		1	LSB
DNL	Differential non-linearity		–0.5		0.5	LSB
ZS_{ERROR}	Zero-scale error		0	0.5	2	LSB
FS_{ERROR}	Full-scale error		–2	–0.5	0	LSB
T_{CV}	Ratiometric temperature coefficient	Wiper set at mid-scale		4		ppm/°C
BW	Bandwidth	Wiper set at mid-scale (TPL0501-100), C_{LOAD}= 10 pF		265		kHz
T_{SW}	Wiper settling time	TPL0501-100		3		µS
THD	Total harmonic distortion	V_H = 1 V_{RMS} at 1 kHz, V_L = V_{DD}/2, measurement at W		0.005%		
RHEOSTAT MODE[2]						
RINL	Integral non-linearity		–1		1	LSB
RDNL	Differential non-linearity		–0.5		0.5	LSB
R_{OFFSET}	Offset		0	0.5	2	LSB
RBW	Bandwidth	Code = 0x00h, L floating, input applied to W, 10 pF on H		60		kHz

(1) V_H = V_{DD}, V_L = GND, V_W = not loaded
(2) Measurements between Wi and Li with Hi not connected, or between Wi and Hi with Li not connected.

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6.5 Electrical Characteristics: Operating Specifications

typical values are specified at VDD = 5 V and operating temperature is 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(STBY)}$	V_{DD} standby current			0.3	8	µA
I_{IN-DIG}	Digital pins leakage current	SCLK, DIN, $\overline{CS}$ inputs	–1		1	µA
$I_{DD(SUPPLY)}$	V_{DD} supply current	Digital input = 1.8 V, VDD = 2.7 V		5		µA
		Digital input = 1.8 V, VDD = 5 V		500		
SERIAL INTERFACE(1)						
V_{IH}	Input high voltage	V_{DD} = 2.7 V to 5.5 V	1.8		5.5	V
V_{IL}	Input low voltage	SCLK, DIN, $\overline{CS}$ inputs	0		0.6	V
C_{IN}	Pin capacitance	SCLK, DIN, $\overline{CS}$ inputs		7	10	pF

(1) SCLK, DIN, $\overline{CS}$ Inputs

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
f_{SCLK}	SCLK frequency			25	MHz
t_{SCP}	SCLK period	40			ns
t_{SCH}	SCLK high time	20			ns
t_{SCL}	SCLK low time	20			ns
t_{DS}	DIN to SCLK set-up time	5			ns
t_{DH}	DIN hold after SCLK	5			ns
t_{CSS}	$\overline{CS}$ fall to SCLK rise setup time	15			ns
t_{CSW}	$\overline{CS}$ pulse width high	40			ns

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6.7 Typical Characteristics

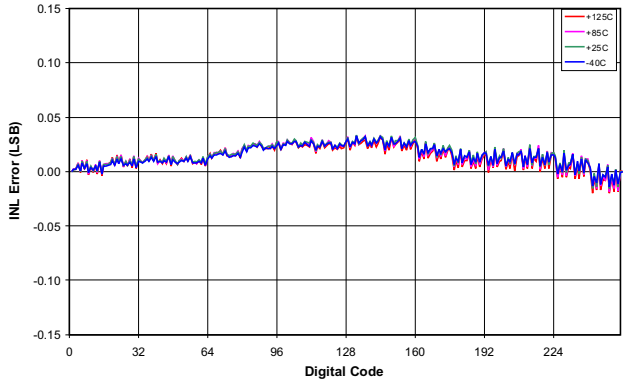

Figure 1. INL vs Tap Position (Potentiometer Mode)

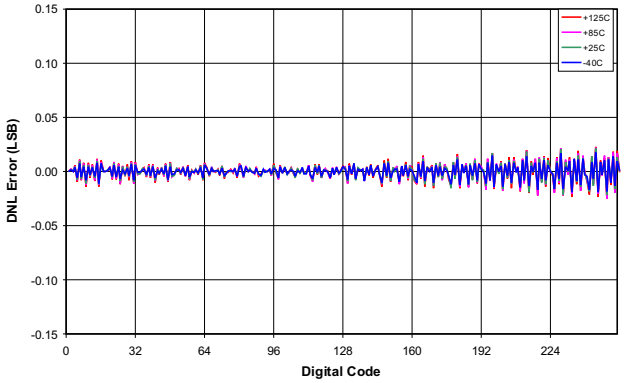

Figure 2. DNL vs Tap Position (Potentiometer Mode)

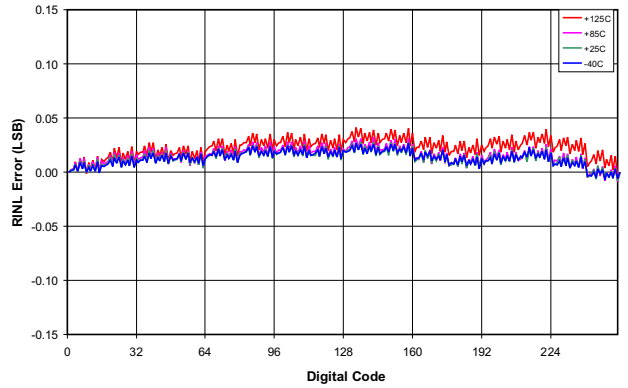

Figure 3. INL vs Tap Position (Rheostat Mode)

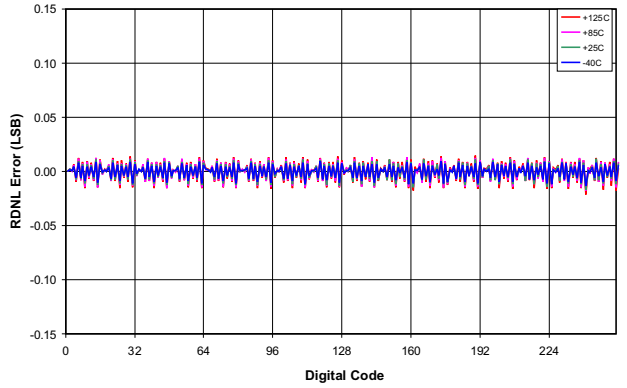

Figure 4. DNL vs Tap Position (Rheostat Mode)

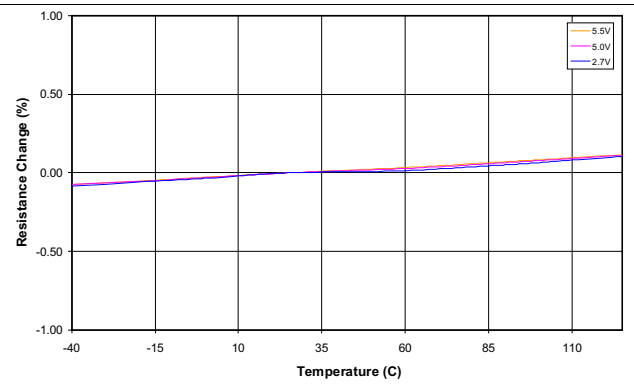

Figure 5. End-to-End Resistance Change vs Temperature

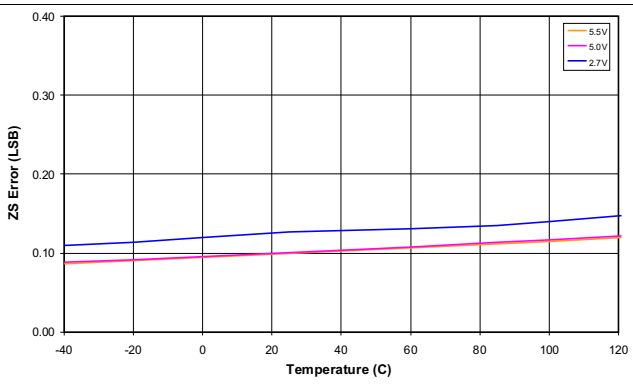

Figure 6. Zero Scale Error vs Temperature

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Typical Characteristics (continued)

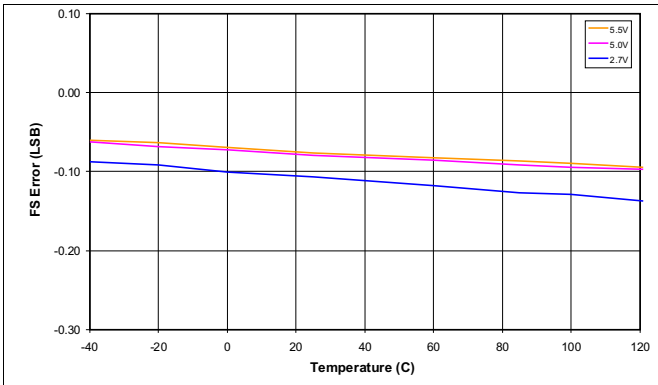


Figure 7. Full Scale Error vs Temperature

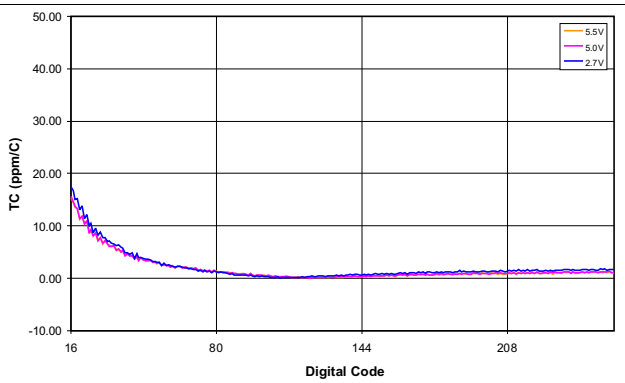


Figure 8. Temperature Coefficient vs Tap Position (Potentiometer Mode)

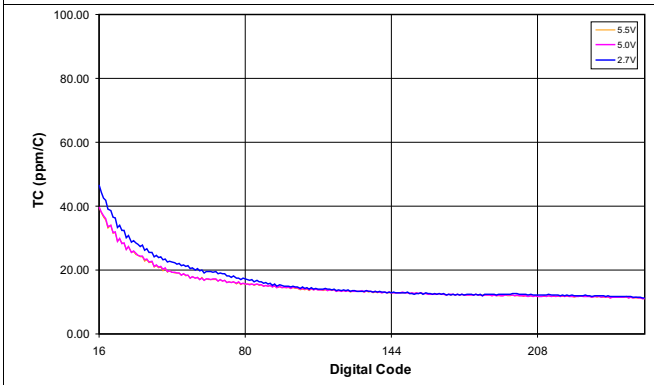


Figure 9. Temperature Coefficient vs Tap Position (Rheostat Mode)

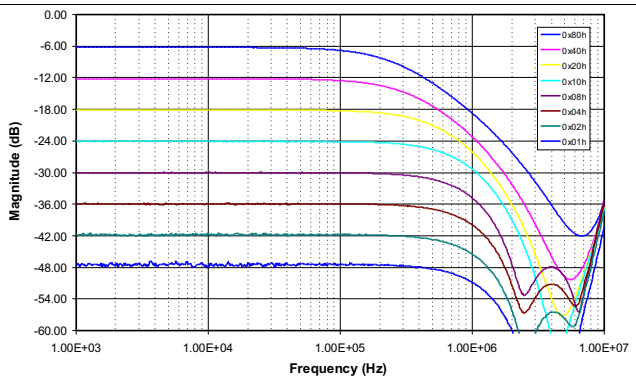


Figure 10. Bandwidth (Potentiometer Mode)

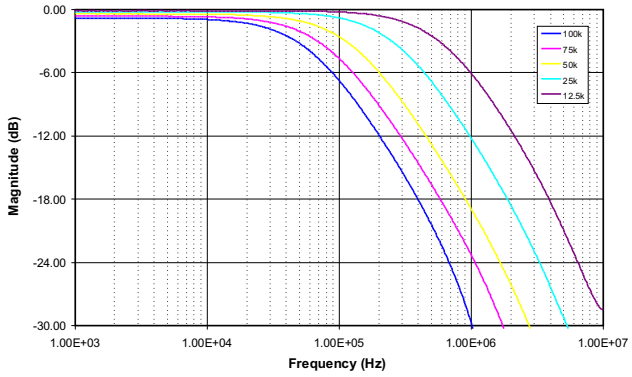


Figure 11. Bandwidth (Rheostat Mode)

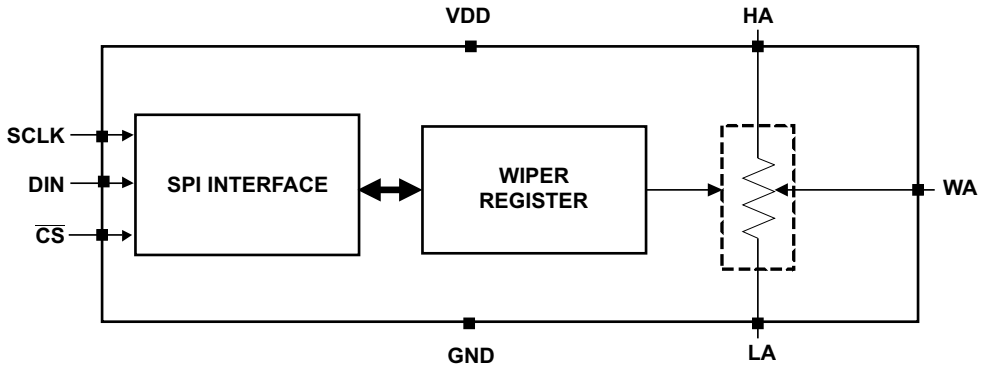
7 Detailed Description

7.1 Overview

The TPL0501 has a single linear-taper digital potentiometer with 256 wiper positions and an end-to-end resistance of 100 kΩ. The potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The potentiometer can be used in either voltage divider mode or rheostat mode.

The high (H) and low (L) terminals of the TPL0501 are equivalent to the fixed terminals of a mechanical potentiometer. The H and L terminals do not have any polarity restrictions (H can be at a higher voltage than L, or L can be at a higher voltage than H). The position of the wiper (W) terminal is controlled by the value in the 8-bit Wiper Resistance (WR) register. When the WR register contains all zeroes (zero-scale), the wiper terminal is closest to its L terminal. As the value of the WR register increases from all zeroes to all ones (full-scale), the wiper moves from the position closest to the L terminal, to the position closest to the H terminal. At the same time, the resistance between W and L increases, whereas the resistance between W and H decreases.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Single-Channel, 256-Position Resolution

The TPL0501 features a single independent DPOT. The DPOT is capable of being used and controlled independently.

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7.4 Device Functional Modes

7.4.1 Voltage Divider Mode

The digital potentiometer generates a voltage divider when all three terminals are used. The voltage divider at wiper-to-H and wiper-to-L is proportional to the input voltage at H to L (see Figure 12).

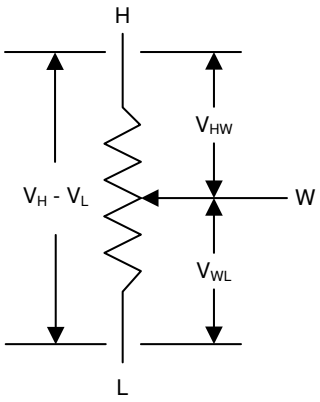

Figure 12. Equivalent Circuit for Voltage Divider Mode

For example, connecting terminal H to 5 V and terminal L to ground, the output voltage at terminal W can range from 0 V to 5 V (see Equation 1).

$$V_W = V_{WL} = (V_H - V_L) \times \frac{D}{256} \quad (1)$$

The voltage difference between terminal H and terminal W can also be calculated in Equation 2.

$$V_{HW} = (V_H - V_L) \times \left(1 - \left(\frac{D}{256}\right)\right) \quad (2)$$

where

- D is the decimal value of the wiper code.

7.4.2 Rheostat Mode

The TPL0501 operates in rheostat mode when only two terminals are used as a variable resistor. The variable resistance can either be between terminal H and terminal W or between terminal L and terminal W. The unused terminal can be left floating or it can be tied to terminal W. The nominal resistance between terminal H and terminal L is 10 kΩ and has 256 tap points accessed by the wiper terminal. The 8-bit volatile register value is used to determine one of the 256 possible wiper positions.

To set the resistance between terminal H and terminal W in rheostat mode, the potentiometer can be configured in two possible ways (see Figure 13).

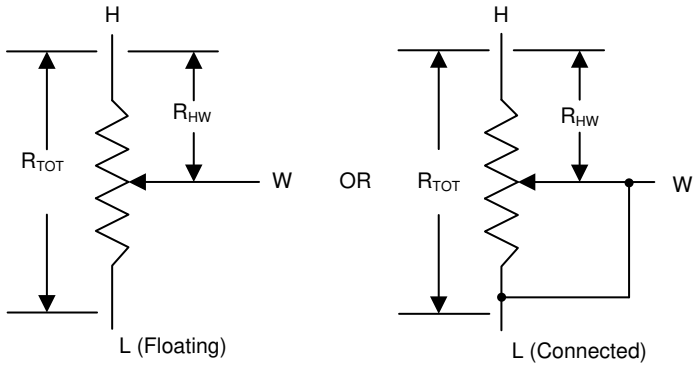

Figure 13. Equivalent Circuit for Rheostat Mode With Terminal H to Terminal W Resistance

Device Functional Modes (continued)

The general equation for determining the digitally programmed output resistance between Terminal H and Terminal W is Equation 3:

$$R_{HW} = R_{TOT} \times \left(1 - \left(\frac{D}{256}\right)\right) \quad (3)$$

where

- R_{TOT} is the end-to-end resistance between terminal H and terminal L.
- D is the decimal value of the wiper code

Similarly, to set the resistance between terminal L and terminal W, the potentiometer can be configured in two possible ways.

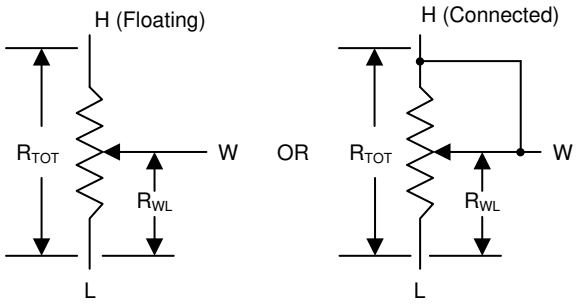

Figure 14. Equivalent Circuit for Rheostat Mode With Terminal L to Terminal W Resistance

The general equation for determining the digitally programmed output resistance between terminal L and terminal W is Equation 4:

$$R_{WL} = R_{TOT} \times \frac{D}{256} \quad (4)$$

where

- R_{TOT} is the end-to-end resistance between terminal H and terminal L
- D is the decimal value of the wiper code.

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7.5 Programming

7.5.1 SPI Digital Interface

The TPL0501 uses a 3-wire SPI compatible serial data interface. This write-only interface has three inputs: chip-select ($\overline{CS}$), data clock (SCLK), and data input (DIN). Drive $\overline{CS}$ low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge. After loading data into the shift register, drive $\overline{CS}$ high to latch the data into the appropriate potentiometer control register and disable the serial interface. Keep $\overline{CS}$ low during the entire serial data stream to avoid corruption of the data.

Table 1. Register Map - Default Value 0x80

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

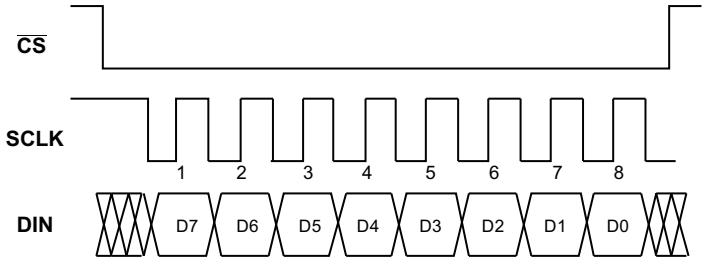


Figure 15. SPI Write Sequence

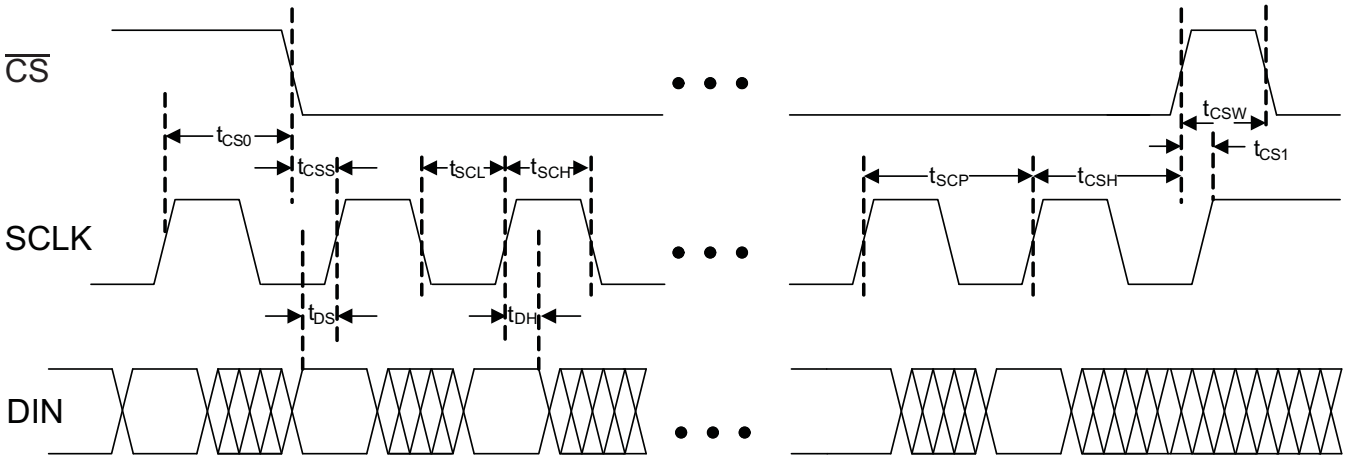
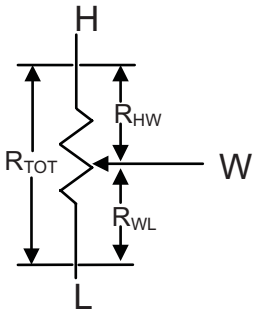


Figure 16. Digital Interface Timing Diagram

7.5.2 Ideal Resistance Values



$R_{WL} = R_{TOT} \times D/256$

$R_{HW} = R_{TOT} \times (1 - (D/256))$

Where D = Decimal Value of Wiper Code

Figure 17. Digital Potentiometer Measurements

Table 2 shows the ideal values for DPOT with end-to-end resistance of 100 kΩ. The absolute values of resistance can vary significantly but the Ratio (R_{WL}/R_{HW}) is extremely accurate.

Table 2. DPOT Ideal Values

STEP	BINARY	100 kΩ		R_{WL}/R_{HW}
		R_{WL} (kΩ)	R_{HW} (kΩ)	
0	00000000	0.00	100.00	0.00
1	00000001	0.39	99.61	0.00
2	00000010	0.78	99.22	0.01
3	00000011	1.17	98.83	0.01
4	00000100	1.56	98.44	0.02
5	00000101	1.95	98.05	0.02
6	00000110	2.34	97.66	0.02
7	00000111	2.73	97.27	0.03
8	00001000	3.13	96.88	0.03
9	00001001	3.52	96.48	0.04
10	00001010	3.91	96.09	0.04
11	00001011	4.30	95.70	0.04
12	00001100	4.69	95.31	0.05
13	00001101	5.08	94.92	0.05
14	00001110	5.47	94.53	0.06
15	00001111	5.86	94.14	0.06
16	00010000	6.25	93.75	0.07
17	00010001	6.64	93.36	0.07
18	00010010	7.03	92.97	0.08
19	00010011	7.42	92.58	0.08
20	00010100	7.81	92.19	0.08
21	00010101	8.20	91.80	0.09
22	00010110	8.59	91.41	0.09
23	00010111	8.98	91.02	0.10
24	00011000	9.38	90.63	0.10
25	00011001	9.77	90.23	0.11
26	00011010	10.16	89.84	0.11
27	00011011	10.55	89.45	0.12
28	00011100	10.94	89.06	0.12
29	00011101	11.33	88.67	0.13
30	00011110	11.72	88.28	0.13

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Table 2. DPOT Ideal Values (continued)

STEP	BINARY	100 kΩ		R_{WL}/R_{HW}
		R_{WL} (kΩ)	R_{HW} (kΩ)	
31	00011111	12.11	87.89	0.14
32	00100000	12.50	87.50	0.14
33	00100001	12.89	87.11	0.15
34	00100010	13.28	86.72	0.15
35	00100011	13.67	86.33	0.16
36	00100100	14.06	85.94	0.16
37	00100101	14.45	85.55	0.17
38	00100110	14.84	85.16	0.17
39	00100111	15.23	84.77	0.18
40	00101000	15.63	84.38	0.19
41	00101001	16.02	83.98	0.19
42	00101010	16.41	83.59	0.20
43	00101011	16.80	83.20	0.20
44	00101100	17.19	82.81	0.21
45	00101101	17.58	82.42	0.21
46	00101110	17.97	82.03	0.22
47	00101111	18.36	81.64	0.22
48	00110000	18.75	81.25	0.23
49	00110001	19.14	80.86	0.24
50	00110010	19.53	80.47	0.24
51	00110011	19.92	80.08	0.25
52	00110100	20.31	79.69	0.25
53	00110101	20.70	79.30	0.26
54	00110110	21.09	78.91	0.27
55	00110111	21.48	78.52	0.27
56	00111000	21.88	78.13	0.28
57	00111001	22.27	77.73	0.29
58	00111010	22.66	77.34	0.29
59	00111011	23.05	76.95	0.30
60	00111100	23.44	76.56	0.31
61	00111101	23.83	76.17	0.31
62	00111110	24.22	75.78	0.32
63	00111111	24.61	75.39	0.33
64	01000000	25.00	75.00	0.33
65	01000001	25.39	74.61	0.34
66	01000010	25.78	74.22	0.35
67	01000011	26.17	73.83	0.35
68	01000100	26.56	73.44	0.36
69	01000101	26.95	73.05	0.37
70	01000110	27.34	72.66	0.38
71	01000111	27.73	72.27	0.38
72	01001000	28.13	71.88	0.39
73	01001001	28.52	71.48	0.40
74	01001010	28.91	71.09	0.41
75	01001011	29.30	70.70	0.41
76	01001100	29.69	70.31	0.42

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Table 2. DPOT Ideal Values (continued)

STEP	BINARY	100 kΩ		R_{WL}/R_{HW}
		R_{WL} (kΩ)	R_{HW} (kΩ)	
77	01001101	30.08	69.92	0.43
78	01001110	30.47	69.53	0.44
79	01001111	30.86	69.14	0.45
80	01010000	31.25	68.75	0.45
81	01010001	31.64	68.36	0.46
82	01010010	32.03	67.97	0.47
83	01010011	32.42	67.58	0.48
84	01010100	32.81	67.19	0.49
85	01010101	33.20	66.80	0.50
86	01010110	33.59	66.41	0.51
87	01010111	33.98	66.02	0.51
88	01011000	34.38	65.63	0.52
89	01011001	34.77	65.23	0.53
90	01011010	35.16	64.84	0.54
91	01011011	35.55	64.45	0.55
92	01011100	35.94	64.06	0.56
93	01011101	36.33	63.67	0.57
94	01011110	36.72	63.28	0.58
95	01011111	37.11	62.89	0.59
96	01100000	37.50	62.50	0.60
97	01100001	37.89	62.11	0.61
98	01100010	38.28	61.72	0.62
99	01100011	38.67	61.33	0.63
100	01100100	39.06	60.94	0.64
101	01100101	39.45	60.55	0.65
102	01100110	39.84	60.16	0.66
103	01100111	40.23	59.77	0.67
104	01101000	40.63	59.38	0.68
105	01101001	41.02	58.98	0.70
106	01101010	41.41	58.59	0.71
107	01101011	41.80	58.20	0.72
108	01101100	42.19	57.81	0.73
109	01101101	42.58	57.42	0.74
110	01101110	42.97	57.03	0.75
111	01101111	43.36	56.64	0.77
112	01110000	43.75	56.25	0.78
113	01110001	44.14	55.86	0.79
114	01110010	44.53	55.47	0.80
115	01110011	44.92	55.08	0.82
116	01110100	45.31	54.69	0.83
117	01110101	45.70	54.30	0.84
118	01110110	46.09	53.91	0.86
119	01110111	46.48	53.52	0.87
120	01111000	46.88	53.13	0.88
121	01111001	47.27	52.73	0.90
122	01111010	47.66	52.34	0.91

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Table 2. DPOT Ideal Values (continued)

STEP	BINARY	100 kΩ		R_{WL}/R_{HW}
		R_{WL} (kΩ)	R_{HW} (kΩ)	
123	01111011	48.05	51.95	0.92
124	01111100	48.44	51.56	0.94
125	01111101	48.83	51.17	0.95
126	01111110	49.22	50.78	0.97
127	01111111	49.61	50.39	0.98
128	10000000	50.00	50.00	1.00
129	10000001	50.39	49.61	1.02
130	10000010	50.78	49.22	1.03
131	10000011	51.17	48.83	1.05
132	10000100	51.56	48.44	1.06
133	10000101	51.95	48.05	1.08
134	10000110	52.34	47.66	1.10
135	10000111	52.73	47.27	1.12
136	10001000	53.13	46.88	1.13
137	10001001	53.52	46.48	1.15
138	10001010	53.91	46.09	1.17
139	10001011	54.30	45.70	1.19
140	10001100	54.69	45.31	1.21
141	10001101	55.08	44.92	1.23
142	10001110	55.47	44.53	1.25
143	10001111	55.86	44.14	1.27
144	10010000	56.25	43.75	1.29
145	10010001	56.64	43.36	1.31
146	10010010	57.03	42.97	1.33
147	10010011	57.42	42.58	1.35
148	10010100	57.81	42.19	1.37
149	10010101	58.20	41.80	1.39
150	10010110	58.59	41.41	1.42
151	10010111	58.98	41.02	1.44
152	10011000	59.38	40.63	1.46
153	10011001	59.77	40.23	1.49
154	10011010	60.16	39.84	1.51
155	10011011	60.55	39.45	1.53
156	10011100	60.94	39.06	1.56
157	10011101	61.33	38.67	1.59
158	10011110	61.72	38.28	1.61
159	10011111	62.11	37.89	1.64
160	10100000	62.50	37.50	1.67
161	10100001	62.89	37.11	1.69
162	10100010	63.28	36.72	1.72
163	10100011	63.67	36.33	1.75
164	10100100	64.06	35.94	1.78
165	10100101	64.45	35.55	1.81
166	10100110	64.84	35.16	1.84
167	10100111	65.23	34.77	1.88
168	10101000	65.63	34.38	1.91

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Table 2. DPOT Ideal Values (continued)

STEP	BINARY	100 kΩ		R_{WL}/R_{HW}
		R_{WL} (kΩ)	R_{HW} (kΩ)	
169	10101001	66.02	33.98	1.94
170	10101010	66.41	33.59	1.98
171	10101011	66.80	33.20	2.01
172	10101100	67.19	32.81	2.05
173	10101101	67.58	32.42	2.08
174	10101110	67.97	32.03	2.12
175	10101111	68.36	31.64	2.16
176	10110000	68.75	31.25	2.20
177	10110001	69.14	30.86	2.24
178	10110010	69.53	30.47	2.28
179	10110011	69.92	30.08	2.32
180	10110100	70.31	29.69	2.37
181	10110101	70.70	29.30	2.41
182	10110110	71.09	28.91	2.46
183	10110111	71.48	28.52	2.51
184	10111000	71.88	28.13	2.56
185	10111001	72.27	27.73	2.61
186	10111010	72.66	27.34	2.66
187	10111011	73.05	26.95	2.71
188	10111100	73.44	26.56	2.76
189	10111101	73.83	26.17	2.82
190	10111110	74.22	25.78	2.88
191	10111111	74.61	25.39	2.94
192	11000000	75.00	25.00	3.00
193	11000001	75.39	24.61	3.06
194	11000010	75.78	24.22	3.13
195	11000011	76.17	23.83	3.20
196	11000100	76.56	23.44	3.27
197	11000101	76.95	23.05	3.34
198	11000110	77.34	22.66	3.41
199	11000111	77.73	22.27	3.49
200	11001000	78.13	21.88	3.57
201	11001001	78.52	21.48	3.65
202	11001010	78.91	21.09	3.74
203	11001011	79.30	20.70	3.83
204	11001100	79.69	20.31	3.92
205	11001101	80.08	19.92	4.02
206	11001110	80.47	19.53	4.12
207	11001111	80.86	19.14	4.22
208	11010000	81.25	18.75	4.33
209	11010001	81.64	18.36	4.45
210	11010010	82.03	17.97	4.57
211	11010011	82.42	17.58	4.69
212	11010100	82.81	17.19	4.82
213	11010101	83.20	16.80	4.95
214	11010110	83.59	16.41	5.10

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Table 2. DPOT Ideal Values (continued)

STEP	BINARY	100 kΩ		R_{WL}/R_{HW}
		R_{WL} (kΩ)	R_{HW} (kΩ)	
215	11010111	83.98	16.02	5.24
216	11011000	84.38	15.63	5.40
217	11011001	84.77	15.23	5.56
218	11011010	85.16	14.84	5.74
219	11011011	85.55	14.45	5.92
220	11011100	85.94	14.06	6.11
221	11011101	86.33	13.67	6.31
222	11011110	86.72	13.28	6.53
223	11011111	87.11	12.89	6.76
224	11100000	87.50	12.50	7.00
225	11100001	87.89	12.11	7.26
226	11100010	88.28	11.72	7.53
227	11100011	88.67	11.33	7.83
228	11100100	89.06	10.94	8.14
229	11100101	89.45	10.55	8.48
230	11100110	89.84	10.16	8.85
231	11100111	90.23	9.77	9.24
232	11101000	90.63	9.38	9.67
233	11101001	91.02	8.98	10.13
234	11101010	91.41	8.59	10.64
235	11101011	91.80	8.20	11.19
236	11101100	92.19	7.81	11.80
237	11101101	92.58	7.42	12.47
238	11101110	92.97	7.03	13.22
239	11101111	93.36	6.64	14.06
240	11110000	93.75	6.25	15.00
241	11110001	94.14	5.86	16.07
242	11110010	94.53	5.47	17.29
243	11110011	94.92	5.08	18.69
244	11110100	95.31	4.69	20.33
245	11110101	95.70	4.30	22.27
246	11110110	96.09	3.91	24.60
247	11110111	96.48	3.52	27.44
248	11111000	96.88	3.13	31.00
249	11111001	97.27	2.73	35.57
250	11111010	97.66	2.34	41.67
251	11111011	98.05	1.95	50.20
252	11111100	98.44	1.56	63.00
253	11111101	98.83	1.17	84.33
254	11111110	99.22	0.78	127.00
255	11111111	99.61	0.39	255.00

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Many applications require using a digital potentiometer such as the TPL0501 for variable resistance or voltage division. *Typical Application* shows one of these examples. In conjunction with various amplifiers, the TPL0501 can effectively be used in rheostat mode to modify the gain of an amplifier in voltage divider mode to create a digital-to-analog converter (DAC).

8.2 Typical Application

Figure 18 shows a DAC.

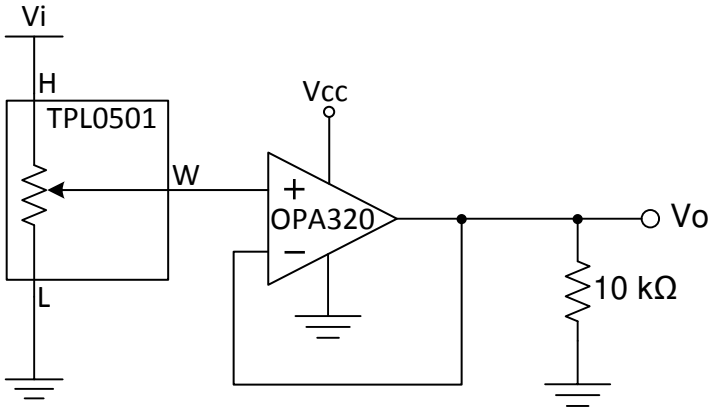

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Figure 18. DAC Schematic

8.2.1 Design Requirements

Table 3 lists the design parameters for this application.

Table 3. Example Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	0 V to 5 V
Output voltage	0 V to 5 V

8.2.2 Detailed Design Procedure

The TPL0501 can be used in voltage divider mode with a unity-gain operational amplifier buffer to create an 8-bit DAC. The analog output voltage of the circuit is determined by the wiper setting programmed through the SPI Interface.

The operational amplifier is required to buffer the high-impedance output of the TPL0501 or else loading placed on the output of the voltage divider affects the output voltage.

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8.2.3 Application Curve

The voltage at terminal H determines the maximum analog voltage at the output. As the TPL0501 moves from zero-scale to full-scale, the voltage divider adjusts with relation to the voltage divider formula (see Figure 12), resulting in the desired voltage at terminal W. The voltage at terminal W ranges linearly from 0 V to the terminal H voltage. In this example, V_{IN} at terminal H is 5 V and 2.7 V.

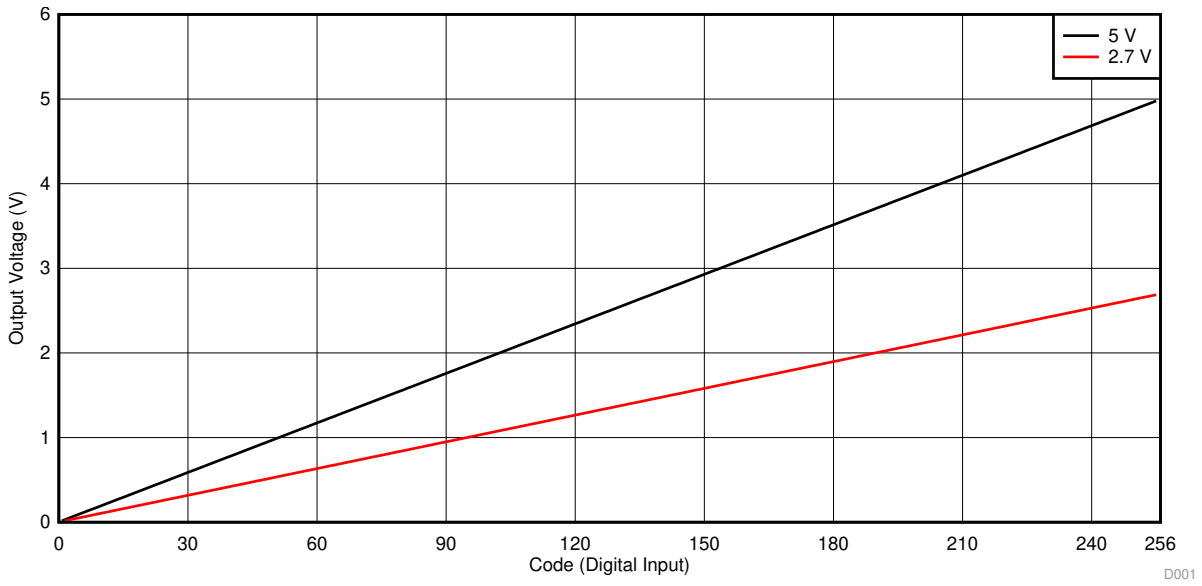

Figure 19. TPL0501 Digital Input vs OPA320 Analog Output (DAC)

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9 Power Supply Recommendations

9.1 Power Sequence

Protection diodes limit the voltage compliance at terminal H, terminal L, and terminal W, making it important to power up V_{DD} first before applying any voltage to terminal H, terminal L, and terminal W. The diodes are forward-biasing, meaning V_{DD} is not powered first. The ideal power up sequence is V_{DD}, digital inputs, and V_H, V_L, and V_W. The order of powering digital inputs, V_H, V_L, and V_W does not matter as long as they are powered after V_{DD}.

9.2 Wiper Position Upon Power Up

It is prudent to know that when DPOT is powered off, the impedance of the device is not known. Upon power up, the device will return to 0x80h code because this device does not contain non-volatile memory.

10 Layout

10.1 Layout Guidelines

To maintain reliability of the device, follow common printed-circuit board (PCB) layout guidelines.

- Leads to the input must be as direct as possible with a minimum conductor length.
- The ground path must have low resistance and low inductance.
- Use short trace-lengths to avoid excessive loading.
- It is common to have a dedicated ground plane on an inner layer of the board.
- Terminals that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias.
- Use bypass capacitors on power supplies and placed them as close as possible to the V_{DD} pin.
- Apply low equivalent series resistance (0.1-µF to 10-µF tantalum or electrolytic capacitors) at the supplies to minimize transient disturbances and to filter low frequency ripple.

10.2 Layout Example

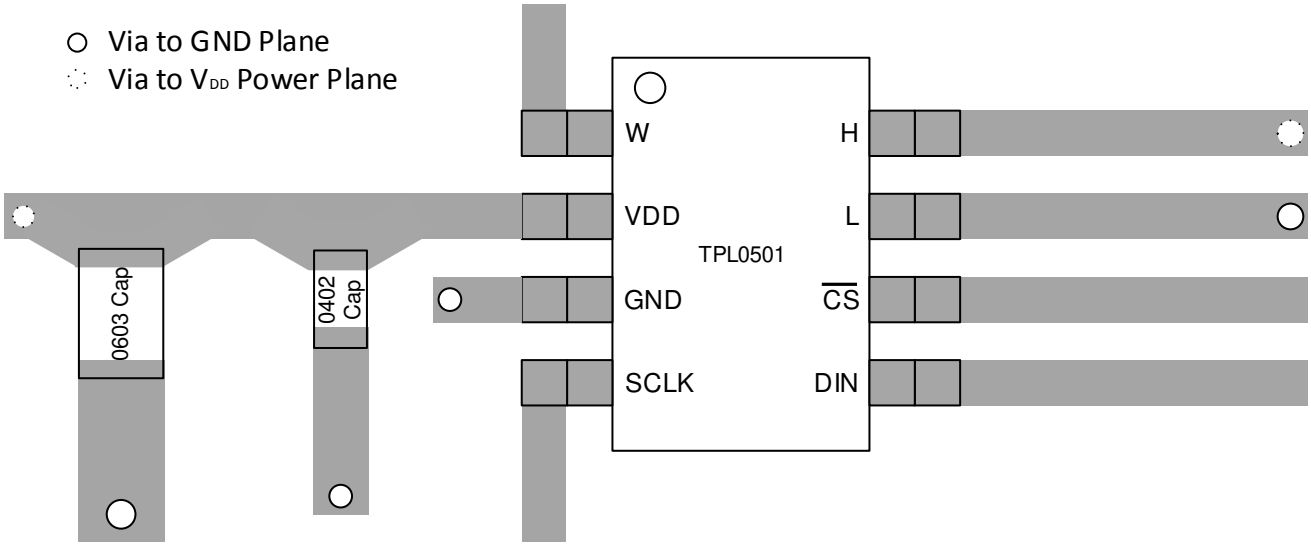

Figure 20. Example Layout for DCN Package

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPL0501-100DCNR	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(NF5J, NF5T)
TPL0501-100DCNR.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(NF5J, NF5T)
TPL0501-100DCNRG4	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NF5T
TPL0501-100DCNRG4.A	Active	Production	SOT-23 (DCN) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NF5T
TPL0501-100RSER	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7M
TPL0501-100RSER.A	Active	Production	UQFN (RSE) | 8	5000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

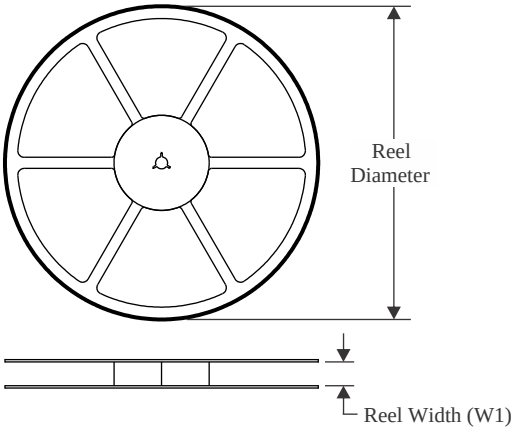
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

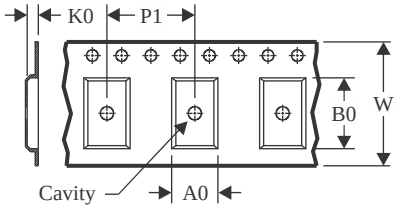
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

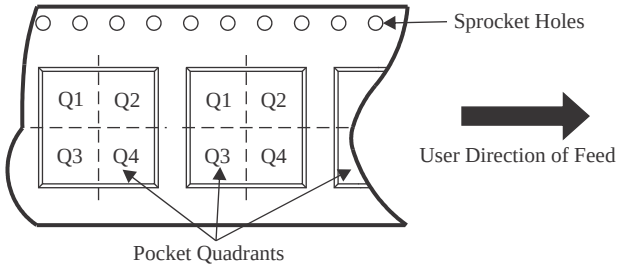


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

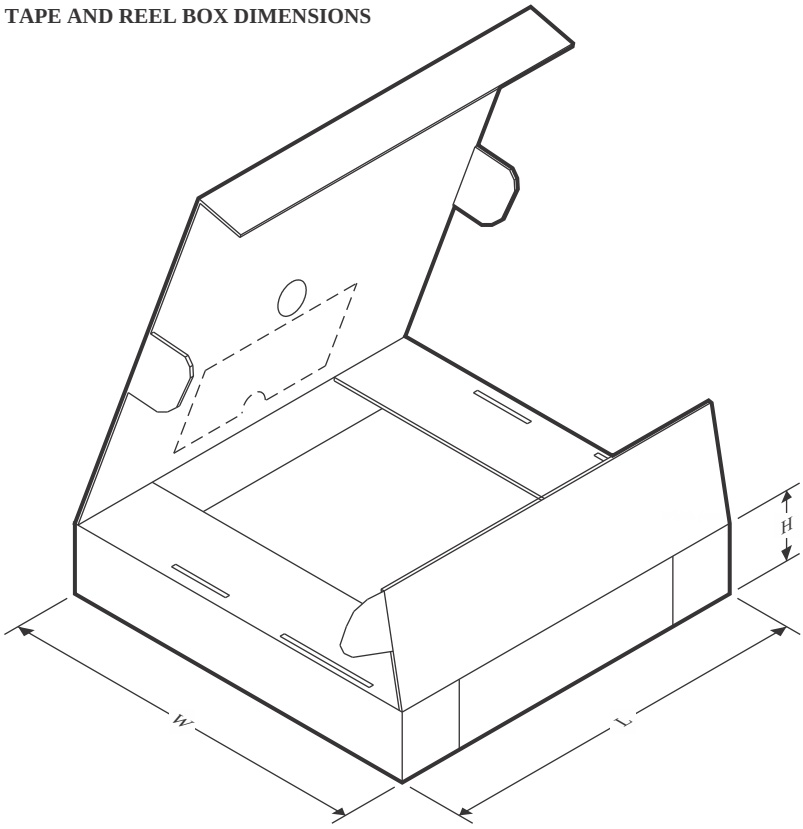
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL0501-100DCNR	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPL0501-100DCNRG4	SOT-23	DCN	8	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPL0501-100RSER	UQFN	RSE	8	5000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q1

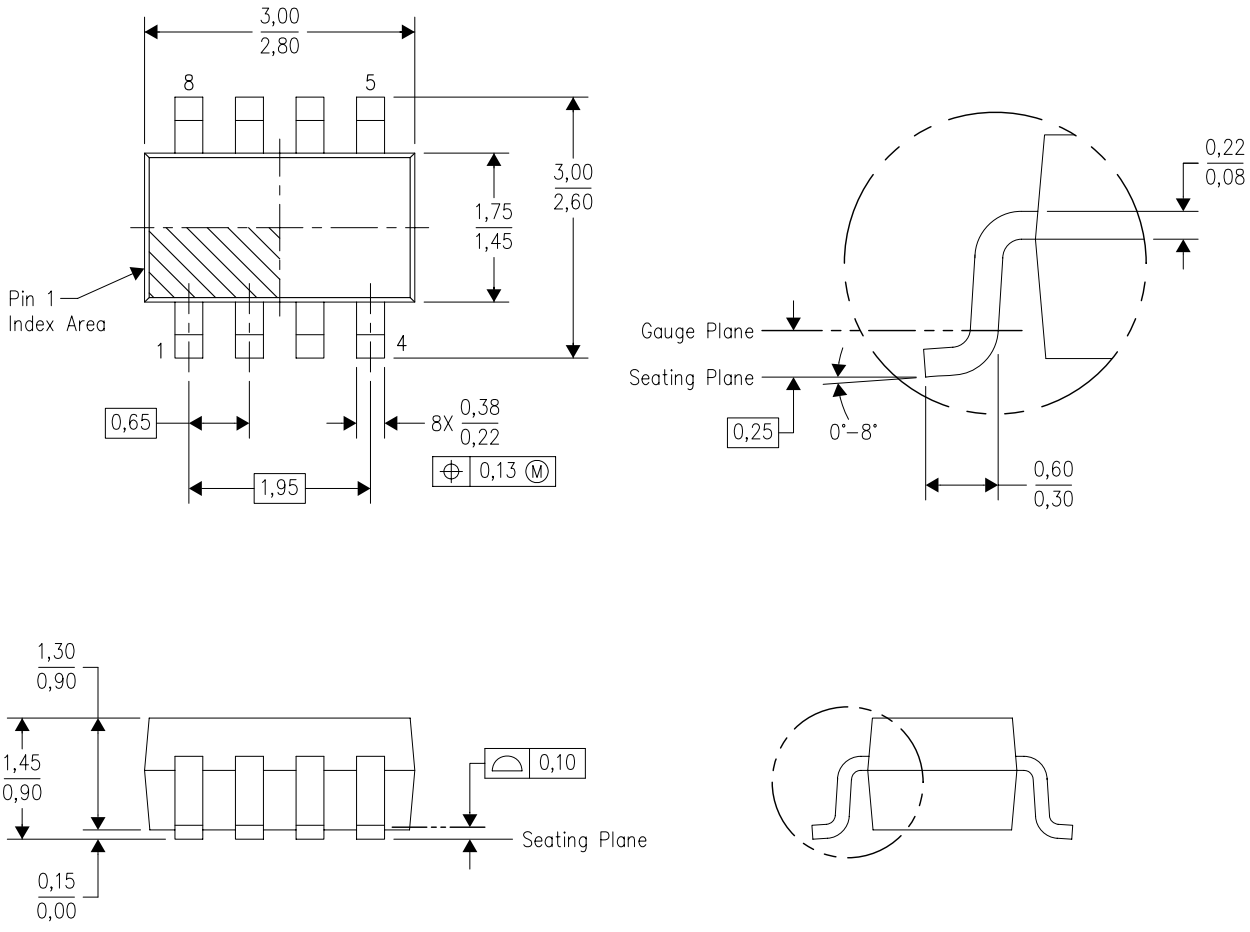
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

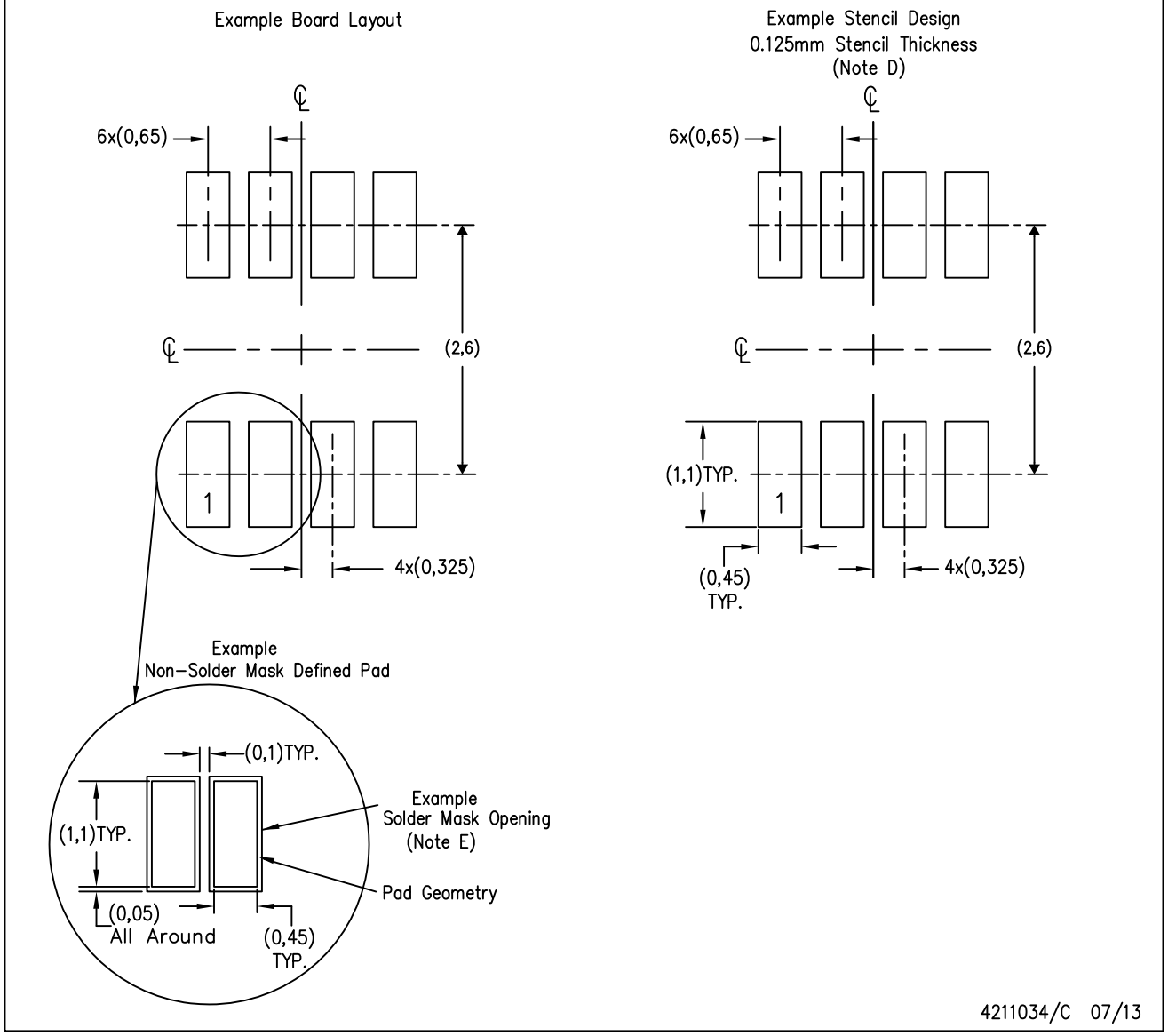
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL0501-100DCNR	SOT-23	DCN	8	3000	202.0	201.0	28.0
TPL0501-100DCNRG4	SOT-23	DCN	8	3000	202.0	201.0	28.0
TPL0501-100RSER	UQFN	RSE	8	5000	202.0	201.0	28.0

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO–178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



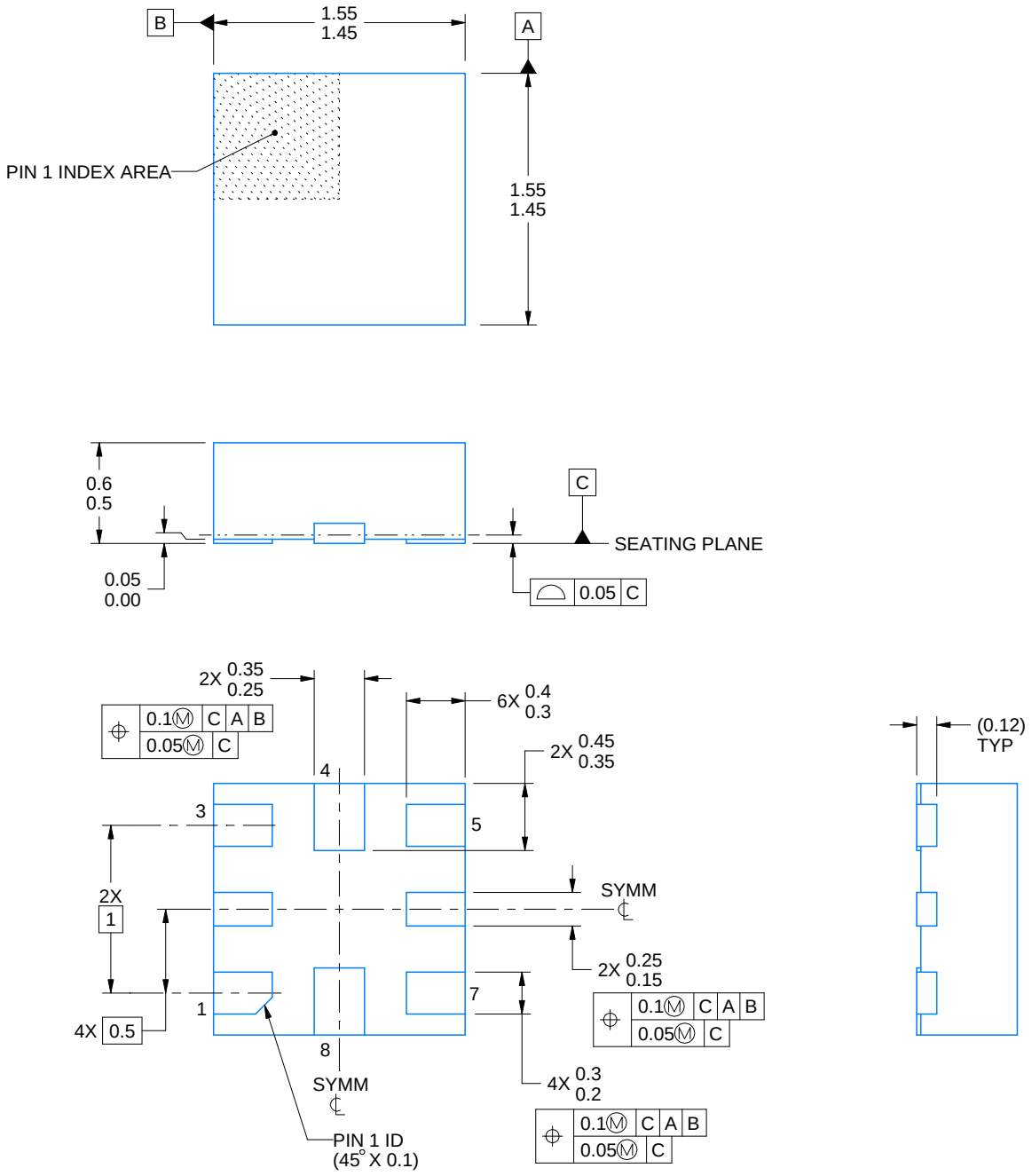
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RSE0008A

PACKAGE OUTLINE

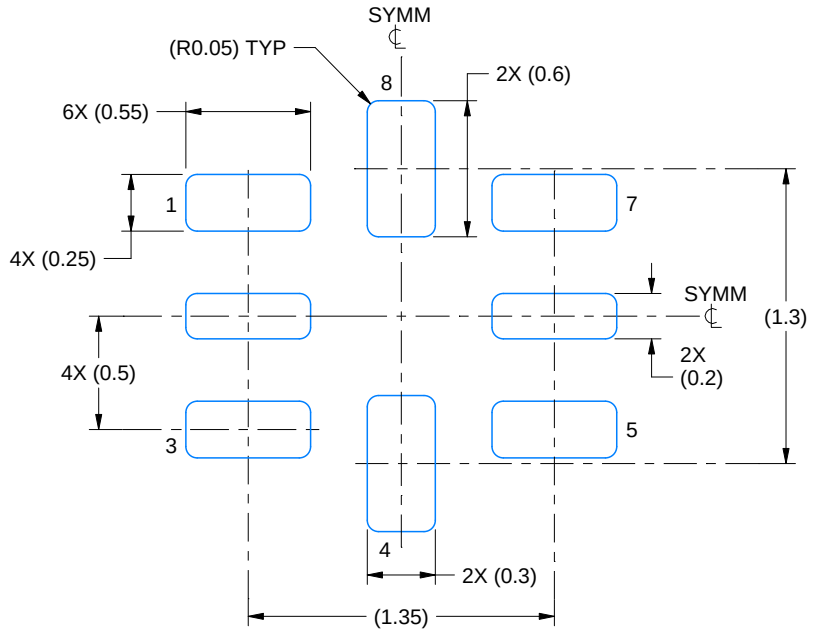
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

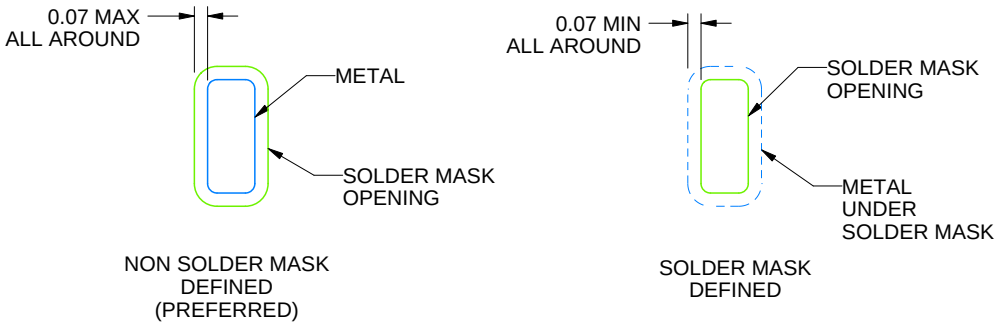


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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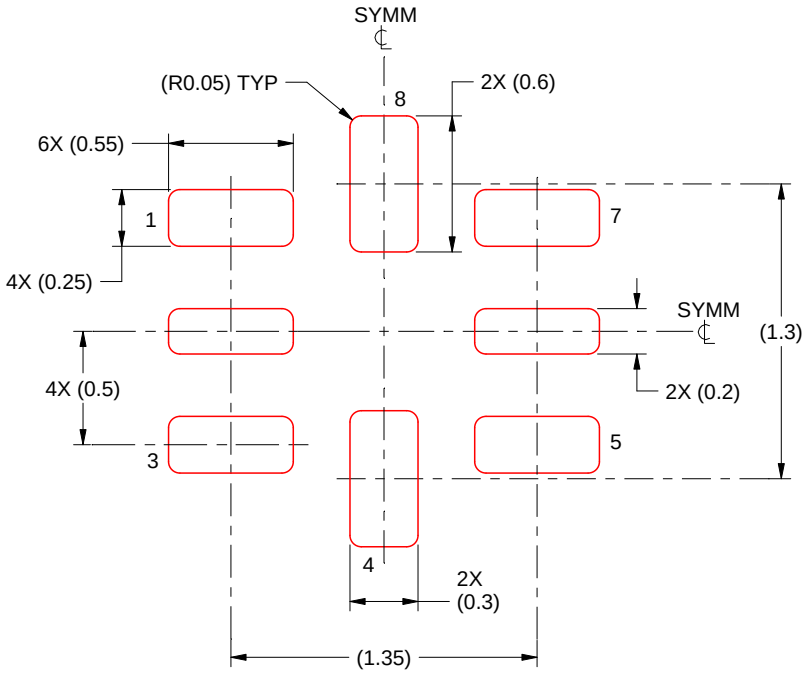
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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