TPD6F002-Q1 Automotive ESD Protection and EMI Filter for LCD Displays and FPD-Link

1 Features

- AEC-Q101 Qualified
- Six-Channel EMI Filtering for Data Ports
  - –47 dB Crosstalk Attenuation at 100 MHz
  - –30 dB Insertion Loss at 800 MHz
  - –3 dB Bandwidth 100 MHz
- Pi-Style (C-R-C) Filter Configuration ($R = 100\ \Omega$, $C_{TOTAL} = 34$ pF)
- Robust ESD Protection Exceeds IEC 61000-4-2 (Level 4)
  - ±20-kV IEC 61000-4-2 Contact Discharge
  - ±30-kV IEC 61000-4-2 Air-Gap Discharge
- Low Leakage Current 20 nA (Max)
- Space-Saving SON Package (3 mm × 1.35 mm)

2 Applications

- LCD Display Interface
- GPIO
- Memory Interface
- Data Lines at Flex Cable
- FPD-Link

3 Description

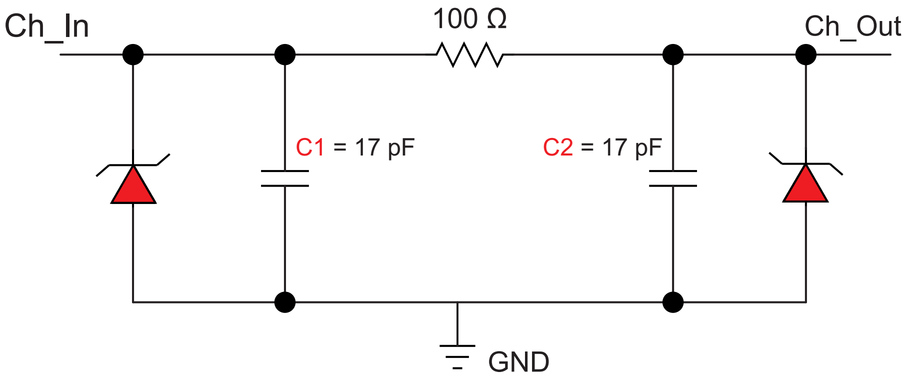
The TPD6F002-Q1 is a highly integrated device that provides a six channel Electromagnetic Interference (EMI) filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD6F002-Q1	SON (12)	3.00 mm × 1.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

5 Revision History

Changes from Original (December 2014) to Revision A	**Page**
• Initial release of full version datasheet.	1

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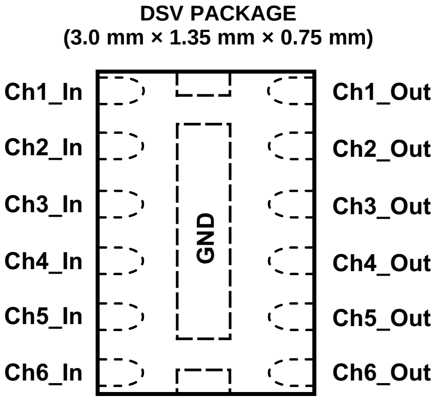
6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ChX_In	1, 2, 3, 4, 5, 6	IO	ESD-protected channel, connected to corresponding ChX_Out
ChX_Out	7, 8, 9, 10, 11, 12	IO	ESD-protected channel, connected to corresponding ChX_In
GND	G	G	Ground

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	IO to GND		5.75	V
T_J	Junction temperature		125	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins(1)	±10	kV
		Charged device model (CDM), per AEC Q101-005, all pins	±1.5	
		IEC 61000-4-2 Contact Discharge	±20	
		IEC 61000-4-2 Air-Gap Discharge	±30	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	0		5.5	V
T_A	Operating free-air temperature	-40		125	°C

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7.4 Thermal Information

THERMAL METRIC(1)		TPD6F002-Q1 DSV 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	78.5	
ψ_{JT}	Junction-to-top characterization parameter	13.0	
ψ_{JB}	Junction-to-board characterization parameter	77.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	66.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

T_A = –40°C to 125°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{BR}	DC breakdown voltage	I_{IO} = 10 µA	6			V
R	Resistance	V_{IN} = 3.3 V, $I_{In\text{-}to\text{-}out}$ = 1mA	85	100	115	Ω
C	Capacitance (C1 or C2)	V_{IO} = 2.5 V		17		pF
I_{IO}	Channel leakage current	V_{IO} = 3.3 V		1	20	nA
f_C	Cut-off frequency	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω		100		MHz

(1) Typical values are at T_A = 25°C.

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7.6 Typical Characteristics

T_A = 25°C unless otherwise noted

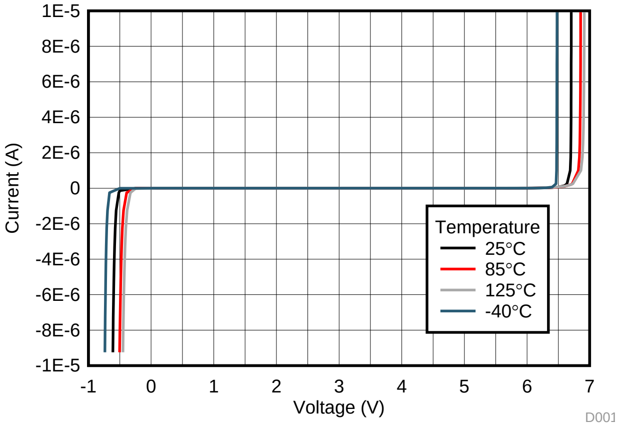

Figure 1. DC Voltage-Current Sweep across Input, Output Pins

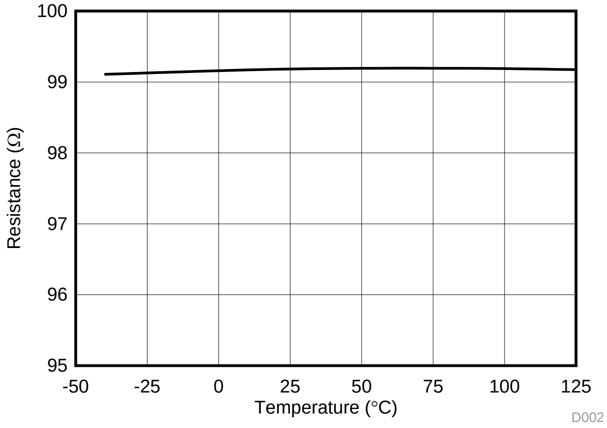

Figure 2. Series Resistance vs Temperature

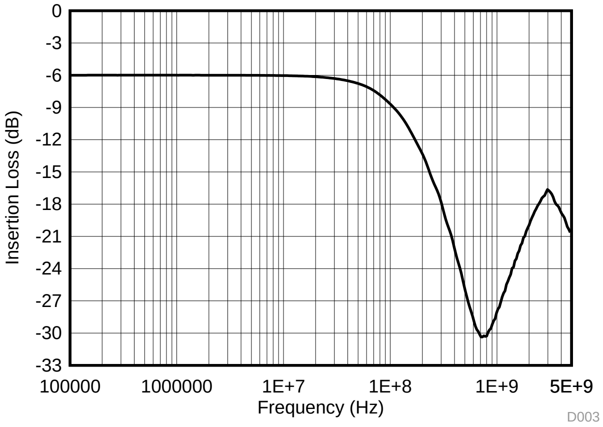

Figure 3. Typical Insertion-loss Characteristics (DC Bias = 0 V, 50 Ω Environment)

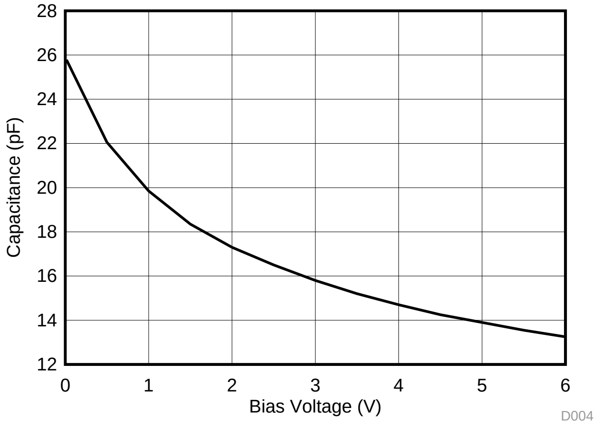

Figure 4. Capacitance (C1 or C2) vs. Bias Voltage

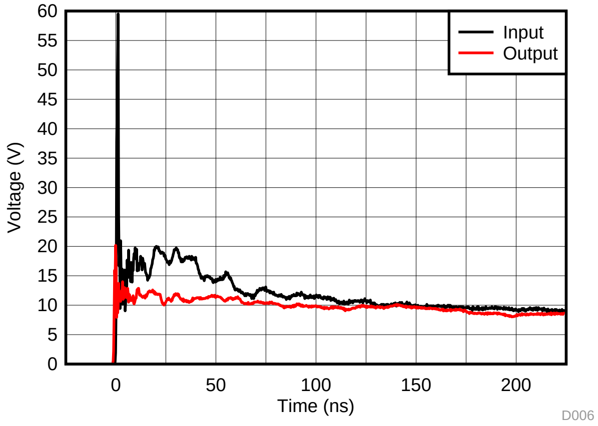

Figure 5. +8-kV IEC Waveform

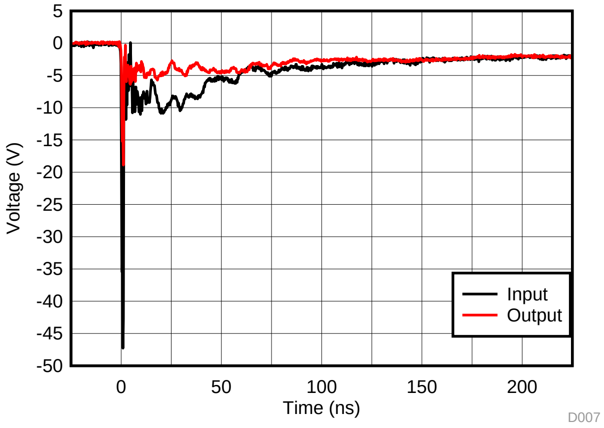

Figure 6. -8-kV IEC Waveform

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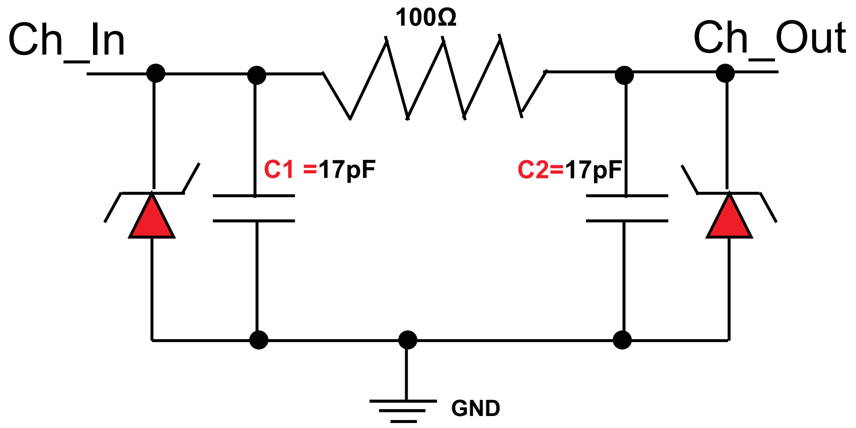
8 Detailed Description

8.1 Overview

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TPD6F002-Q1 is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, makes this device ideal for protecting interfaces like LCD displays, memory interfaces, and FPD-Link.

8.2 Functional Block Diagram



8.3 Feature Description

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

8.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards. It passes HBM H3B (±8 kV) and CDM C5 (±1 kV) ESD ratings and is qualified to operate from –40°C to 125°C.

8.3.2 Six-Channel EMI Filtering

This device provides six channels for EMI filtering of data lines with the following parameters:

- –47 dB Crosstalk Attenuation at 100 MHz
- –30 dB Insertion Loss at 800 MHz
- –3 dB Bandwidth: 100 MHz

8.3.3 Pi-Style Filter Configuration

This device has a pi-style filtering configuration composed of a series resistor and two capacitors in parallel with the I/O pins. The typical resistor value is 100 Ω and the typical capacitor values are 17 pF each.

8.3.4 Robust ESD Protection

The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact ESD is rated at ±20 kV and Air-gap ESD is rated at ±30 kV.

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Feature Description (continued)

8.3.5 Low Leakage Current

The I/O pins feature an ultra-low leakage current of 20-nA (max) with a bias of 3.3 V

8.3.6 Space-Saving SON Package

The layout of this device makes it easy to add protection to existing layouts. The packages offer flow-through routing which requires minimal changes to existing layout for addition of these devices. Additionally, the device offers a small space-saving package that takes a minimal footprint on the board.

8.4 Device Functional Modes

The TPD6F002-Q1 is a passive integrated circuit that passively filters EMI and triggers when voltages are above V_{BR} or below the lower diode voltage (–0.6 V). During ESD events, voltages as high as ±30 kV (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels, the device reverts to passive.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPD6F002-Q1 is a highly integrated device that provides a six channel EMI filter and a TVS based ESD protection diode array. The low-pass filter array suppresses EMI/RFI emissions for data ports subject to electromagnetic interference. The TVS diode array is rated to dissipate ESD strikes above the maximum level specified in the IEC 61000-4-2 international standard. The high level of integration, combined with its small easy-to-route DSV package, allows this device to provide great circuit protection for LCD displays, memory interfaces, GPIO lines, and FPD-Link.

9.2 Typical Application

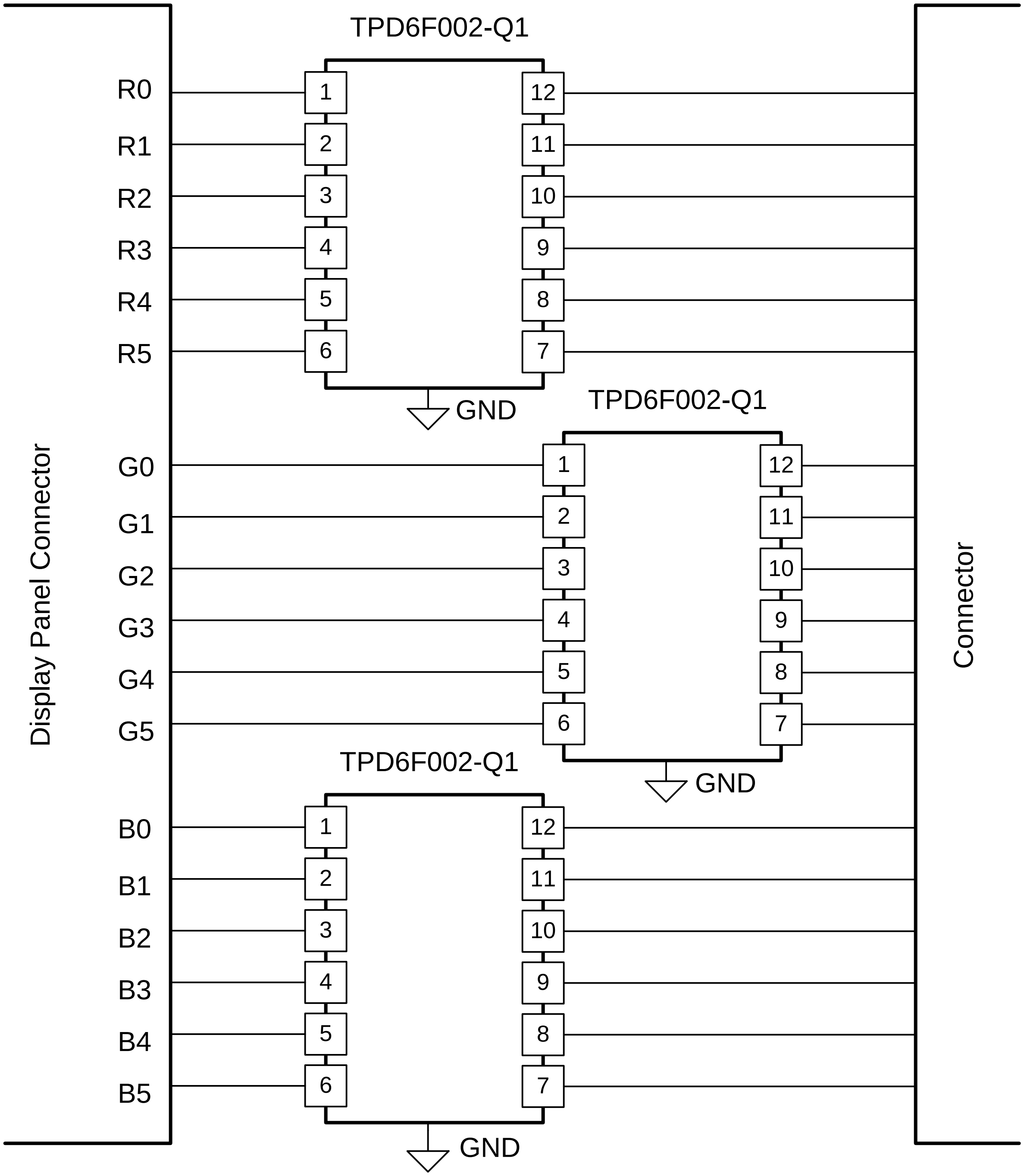

Figure 7. Display Panel Schematic

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Typical Application (continued)

9.2.1 Design Requirements

For this design example, three TPD6F002-Q1 devices are being used in an 18-bit display panel application. This will provide a complete ESD and EMI protection solution for the display connector.

Given the display panel application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on all pins except GND	0 V to 5 V
Operating Frequency	50 MHz

9.2.2 Detailed Design Procedure

To begin the design process, some design parameters must be decided; the designer needs to know the following:

- Signal range of all the protected lines
- Operating frequency
- Crosstalk response

9.2.2.1 Signal Range on All Protected Lines

The TPD6F002-Q1 has 6 identical protection channels for signal lines. All I/O pins will support a signal range from 0 to 5.5 V.

9.2.2.2 Operating Frequency

The TPD6F002-Q1 has a 100 MHz –3 dB bandwidth, which supports the operating frequency for this display.

9.2.2.3 Crosstalk Response

The TPD6F002-Q1 has a –47 dB near-side crosstalk attenuation at 100 MHz, sufficient for this display.

9.2.3 Application Curves

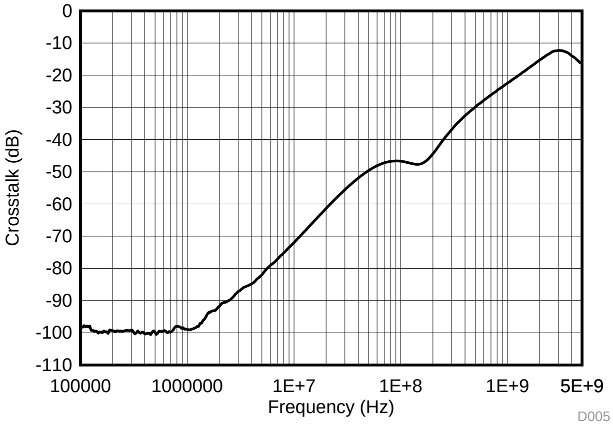

Figure 8. Near-Side Crosstalk

10 Power Supply Recommendations

This device is a passive EMI and ESD device so there is no need to power it. Care should be taken to not violate the recommended V_{IO} specification (5.5 V) to ensure the device functions properly.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

This application is typical of an 18-bit RGB display panel layout.

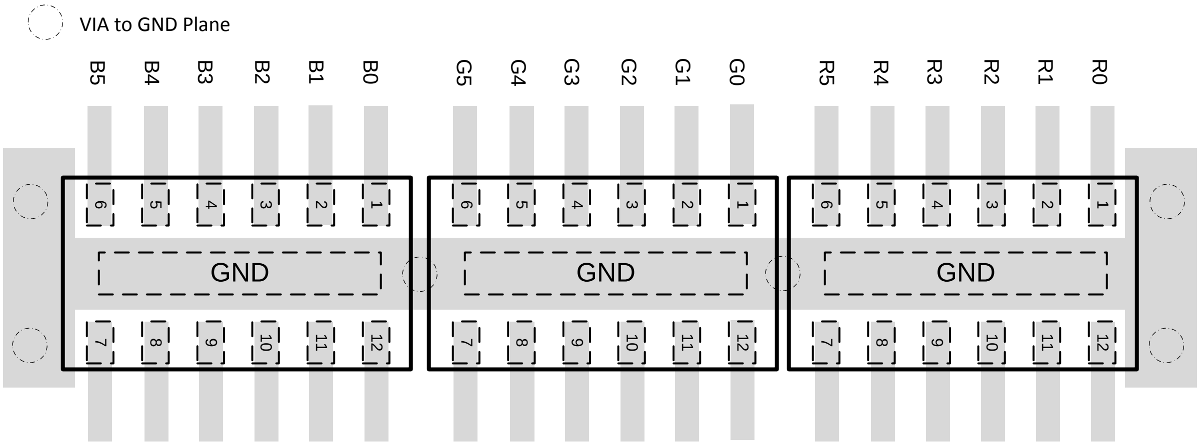

Figure 9. TPD6F002-Q1 Layout

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12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD6F002QDSVRQ1	Active	Production	SON (DSV) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UNS
TPD6F002QDSVRQ1.A	Active	Production	SON (DSV) | 12	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UNS
TPD6F002QDSVRQ1.B	Active	Production	SON (DSV) | 12	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPD6F002-Q1 :

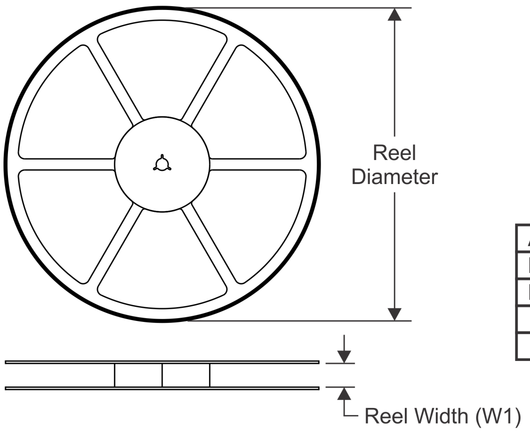
- Catalog : TPD6F002

NOTE: Qualified Version Definitions:

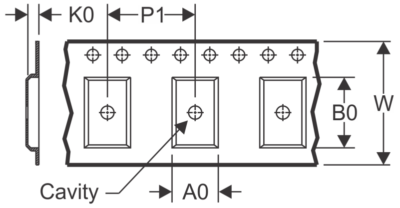
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

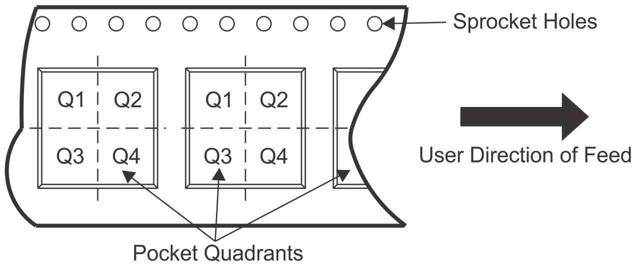


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

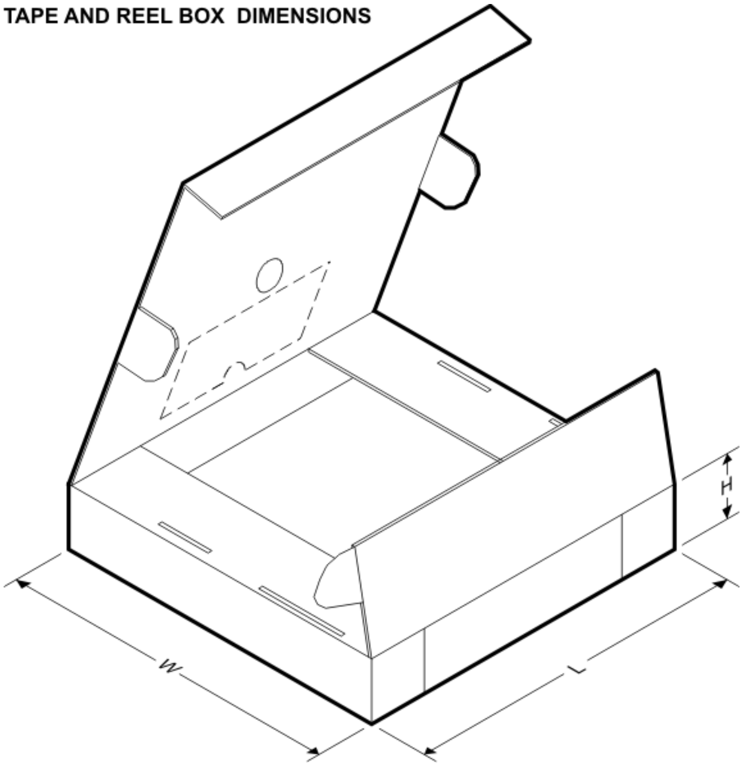
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6F002QDSVRQ1	SON	DSV	12	3000	180.0	8.4	1.74	3.33	1.05	4.0	8.0	Q1

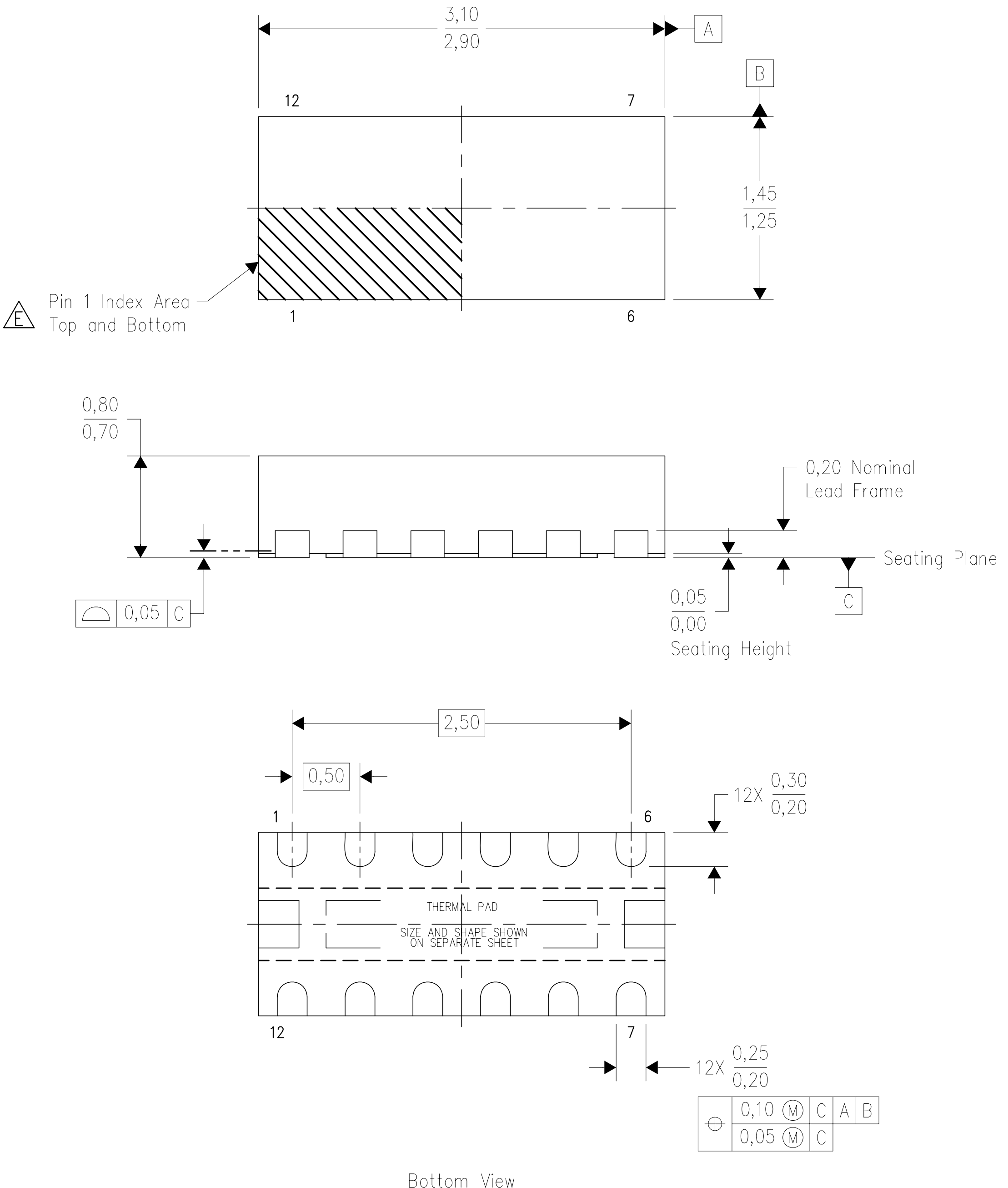
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6F002QDSVRQ1	SON	DSV	12	3000	213.0	191.0	35.0

DSV (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4209279/B 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

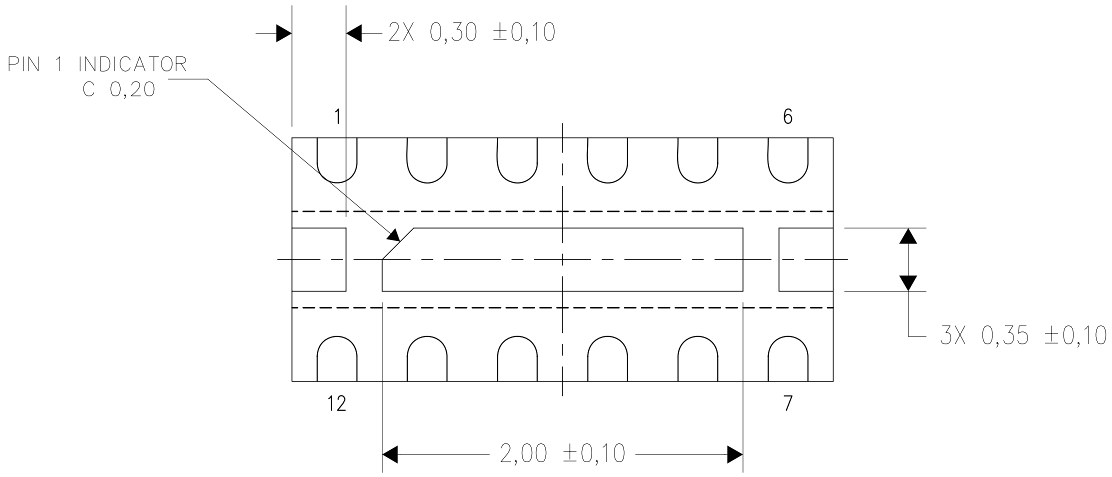
DSV (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



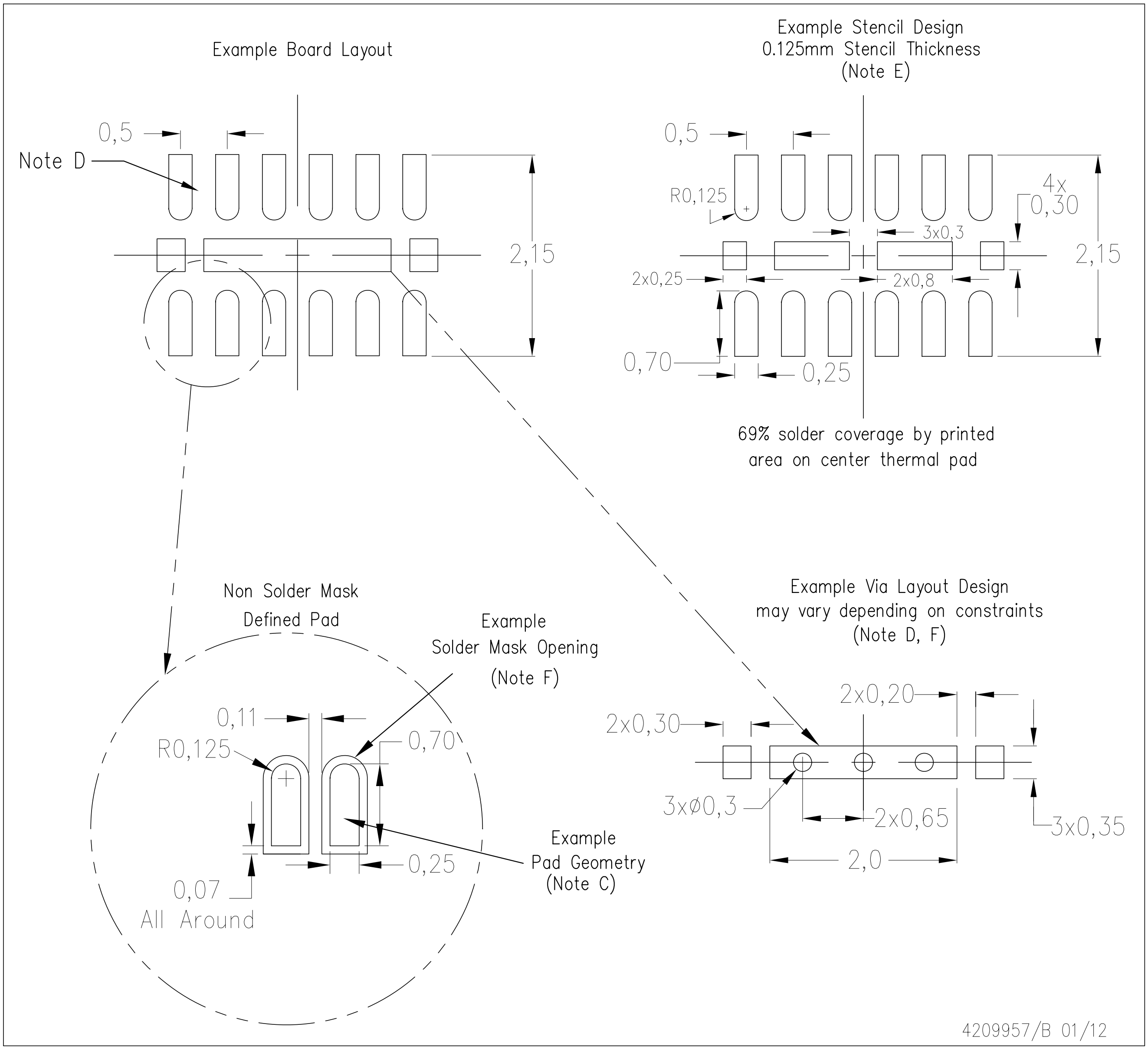
Bottom View

Exposed Thermal Pad Dimensions

4209318/B 12/11

NOTE: All linear dimensions are in millimeters

DSV (R-PWSON-N12) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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