TPD6E004 Low-Capacitance, 6-Channel ±15-kV ESD Protection Array for High-Speed Data Interfaces

1 Features

- ESD protection exceeds JESD:
  - ±15-kV human-body model (HBM)
  - ±8-kV IEC 61000-4-2 contact discharge
  - ±12-kV IEC 61000-4-2 air-gap discharge
- Low 1.6-pF I/O capacitance
- 0.9-V to 5.5-V supply-voltage range
- 6-channel device
- Space-saving UQFN (RSE) package

2 Applications

- USB
- Ethernet™
- FireWire™
- Video
- Cell phones
- SVGA video connections
- Glucose meters

3 Description

The TPD6E004 device is a low-capacitance, ±15-kV ESD protection diode array designed to protect sensitive electronics attached to communication lines. Each channel consists of a pair of diodes that steers ESD current pulses to V_{CC} or GND. The TPD6E004 protects against ESD pulses up to ±15-kV human-body model (HBM), ±8-kV contact ESD, and ±12-kV air-gap ESD as specified in IEC 61000-4-2. This device has a typical 1.6-pF capacitance per channel, making it an excellent choice for use in high-speed data I/O interfaces.

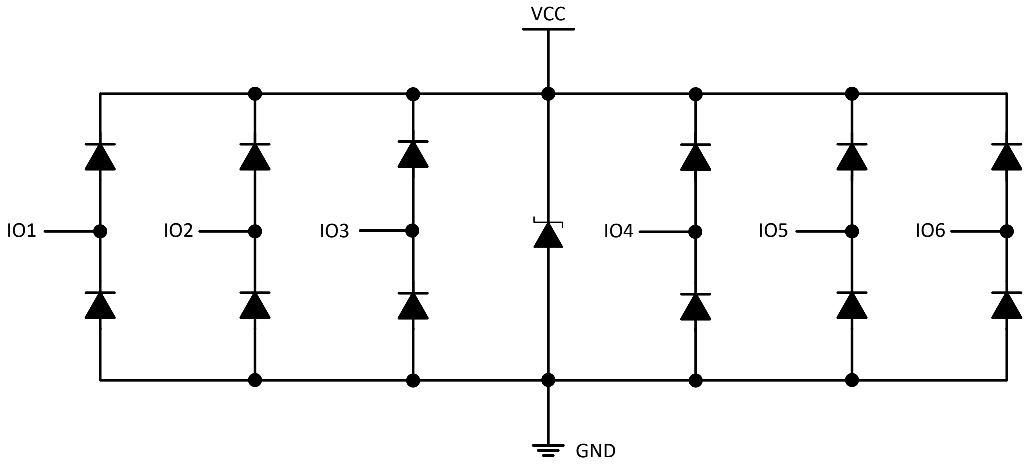
The TPD6E004 device is available in the RSE package and is specified for –40°C to +85°C operation.

The TPD6E004 device is a 6-channel ESD structure designed for USB, Ethernet, and FireWire applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPD6E004	RSE (UQFN, 8)	1.5 mm × 1.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2016) to Revision C (July 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the *Package Information* table to include package lead size	1

Changes from Revision A (February 2008) to Revision B (February 2016)	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

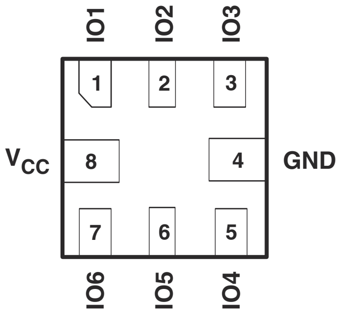


Figure 5-1. RSE Package, 8-Pin UQFN (Bottom View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IO1	1	I/O	ESD-protected channel
IO2	2	I/O	ESD-protected channel
IO3	3	I/O	ESD-protected channel
GND	4	GND	Ground
IO4	5	I/O	ESD-protected channel
IO5	6	I/O	ESD-protected channel
IO6	7	I/O	ESD-protected channel
V_{CC}	8	PWR	Power-supply input. Bypass V_{CC} to GND with a 0.1-μF ceramic capacitor.

(1) I = input, O = output, GND = ground, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Operating voltage for pin VCC		–0.3	5.5	V
$V_{I/O}$	Operating voltage for pins IO1, IO2, IO3, IO4, IO5 and IO6		–0.3	V_{CC} + 0.3	V
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±15000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Surge Protection

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8000	V
		IEC 61000-4-2 air-gap discharge	±12000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	85	°C
V_{CC}	Operating voltage for pin VCC	0.9	5.5	V
$V_{I/O}$	Operating voltage for pins IO1, IO2, IO3, IO4, IO5 and IO6	0	Minimum of: (5.8, V_{CC})	V

6.5 Thermal Information

THERMAL METRIC[1]		TPD6E004	UNIT
		RSE (UQFN)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

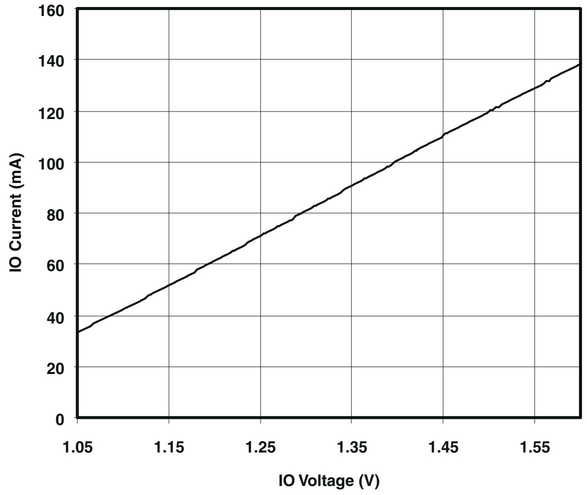
6.6 Electrical Characteristics

V_{CC} = 5 V ± 10%, T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{CC}	Supply voltage		0.9		5.5	V
I_{CC}	Supply current				500	nA
V_F	Diode forward voltage	I_F = 1 mA		0.8		V
I_I	Channel leakage current			±1		nA
V_{BR}	Break-down voltage	I_I = 10 µA	6		8	V
$C_{I/O}$	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC}/2, f = 10 MHz		1.6	2	pF

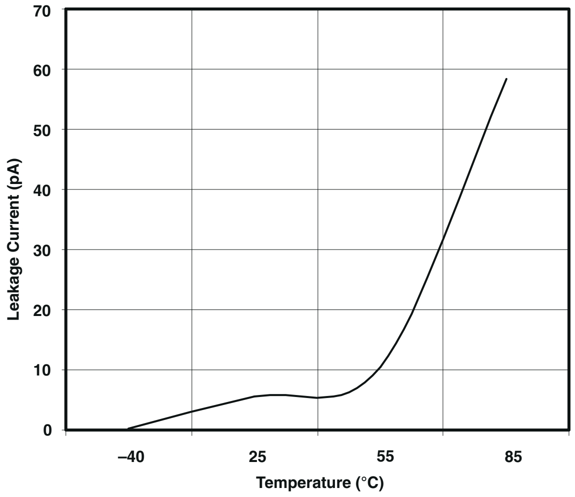
(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.

6.7 Typical Characteristics



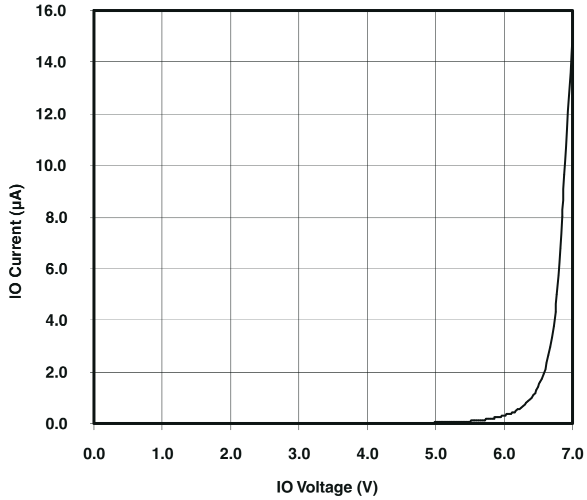
V_{CC} = 0 V, DC Sweep Across the I/O Pin

Figure 6-1. Forward Diode Voltage (Upper Clamp Diode)



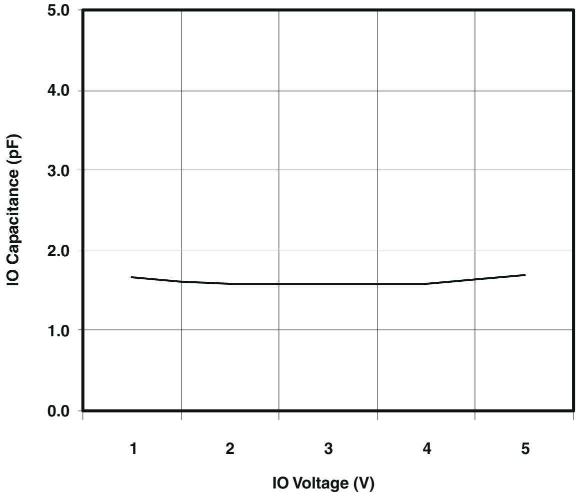
$V_{I/O}$ = 2.5 V

Figure 6-2. Leakage Current vs Temperature



V_{CC} = Open

Figure 6-3. Reverse Diode Curve Current I/O to GND



V_{CC} = 5 V

Figure 6-4. I/O Capacitance vs Input Voltage

7 Detailed Description

7.1 Overview

The TPD6E004 device is a six-channel TVS protection diode array. The TPD6E004 is rated to dissipate ESD strikes of ±8-kV contact and ±12-kV air-gap, as specified in the IEC 61000-4-2 international standard. This device has 1.6-pF capacitance per I/O channel, making it an excellent choice for use in high-speed data I/O interfaces.

7.2 Functional Block Diagram

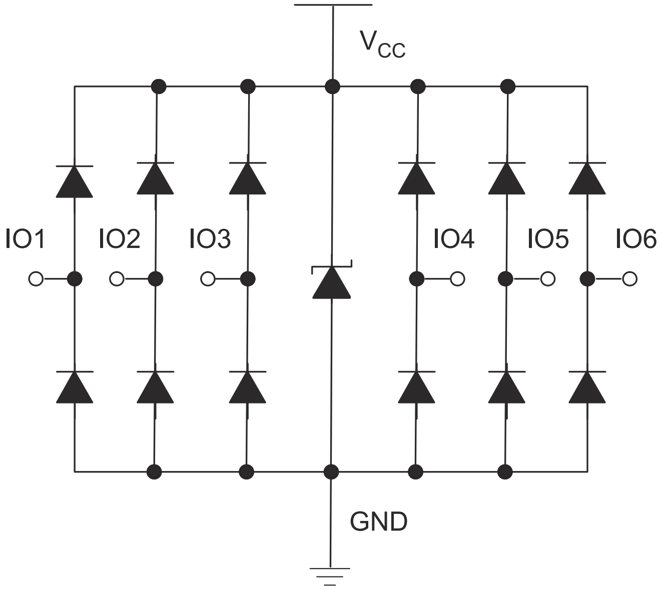


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Figure 7-1. Logic Block Diagram

7.3 Feature Description

The TPD6E004 is a TVS that provides ESD protection for up to six channels, withstanding up to ±8-kV contact and ±12-kV air-gap ESD per IEC 61000-4-2. The monolithic technology yields exceptionally small variations in capacitance between any I/O pin of the TPD6E004. The small footprint is an excellent choice for applications where space-saving designs are important.

7.4 Device Functional Modes

The TPD6E004 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the diodes V_F of approximately –0.8 V. During ESD events, voltages as high as ±8-kV contact and ±12-kV air-gap ESD can be directed to ground through the internal diodes. When the voltages on the protected line fall below the trigger levels of TPD6E004 (usually within 10s of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPD6E004 device is a TVS diode array typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected integrated circuit (IC). The triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

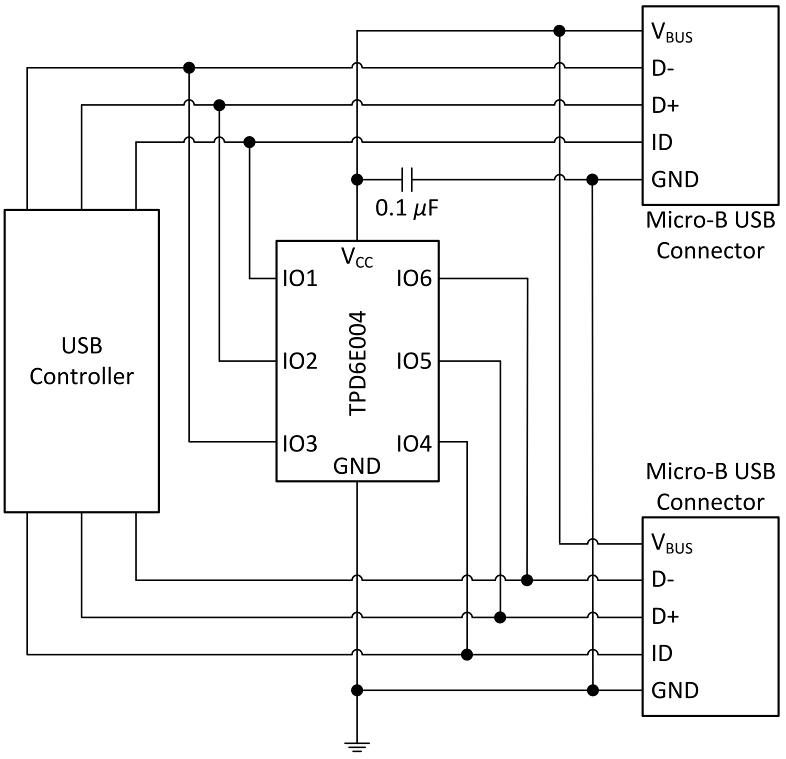

Figure 8-1. Two-Port Micro-B USB 2.0 Application

8.2.1 Design Requirements

For this design example, a single TPD6E004 is used to protect all the pins of two USB 2.0 Micro-B connectors. Table 8-1 lists the design parameters for the USB application.

Table 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, IO4, IO5 and IO6	0 V to 3.6 V
Signal voltage range on V_{CC}	0 V to 5.5 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD6E004 ESD solution offers little or no signal distortion during normal operation due to low I/O capacitance and ultra-low leakage current specifications. The TPD6E004 is designed to protect the core circuitry and allow the system to function properly in the event of an ESD strike. For proper operation, the *Layout Guidelines* and following design guidelines must be followed:

1. Place the TPD6E004 solution close to the connectors. This allows the TPD6E004 to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
2. Place a 0.1-μF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the I/O pin during the ESD strike event.
3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD6E004 consumes only μA of leakage current, but during an ESD event, V_{CC} and GND may see 15-A to 30-A of current, depending on the ESD level. A sufficient current path enables the safe discharge of all the energy associated with the ESD strike.
4. Leave any unused I/O pins floating. In this example of protecting two Micro-B USB ports, none of the I/O pins are left unused.
5. The V_{CC} pin can be connected in two different ways:
   a. If the V_{CC} pin is connected to the system power supply, then the TPD6E004 works as a transient suppressor for any signal swing above V_{CC} + V_F. TI recommends a 0.1-μF capacitor on the device V_{CC} pin for ESD bypass.
   b. If the V_{CC} pin is not connected to the system power supply, then the TPD6E004 can tolerate a higher signal swing in the range of up to 5.8 V.

Note

A 0.1-μF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.3 Application Curve

Figure 8-2 is a capture of the voltage clamping waveform of the TPD6E004 during a +8-kV contact IEC 61000-4-2 ESD strike.

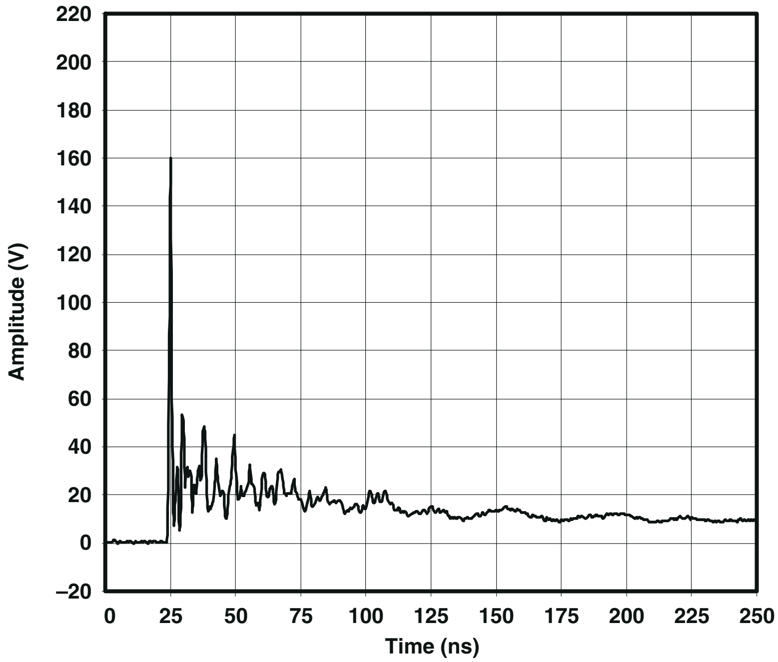

Figure 8-2. IEC 61000-4-2 +8-kV Contact ESD Clamping Waveform

8.3 Power Supply Recommendations

The TPD6E004 device is a passive ESD protection device, so there is no need to power it. Do not violate the maximum voltage specifications for each pin.

8.4 Layout

8.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any corners less than 135° on the protected traces between the TVS and the connector. Best practice is using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Connect the ground pin to a same layer ground pour which is connected to an internal ground plane with a via. Place the via very near the ground pin.

8.4.2 Layout Example

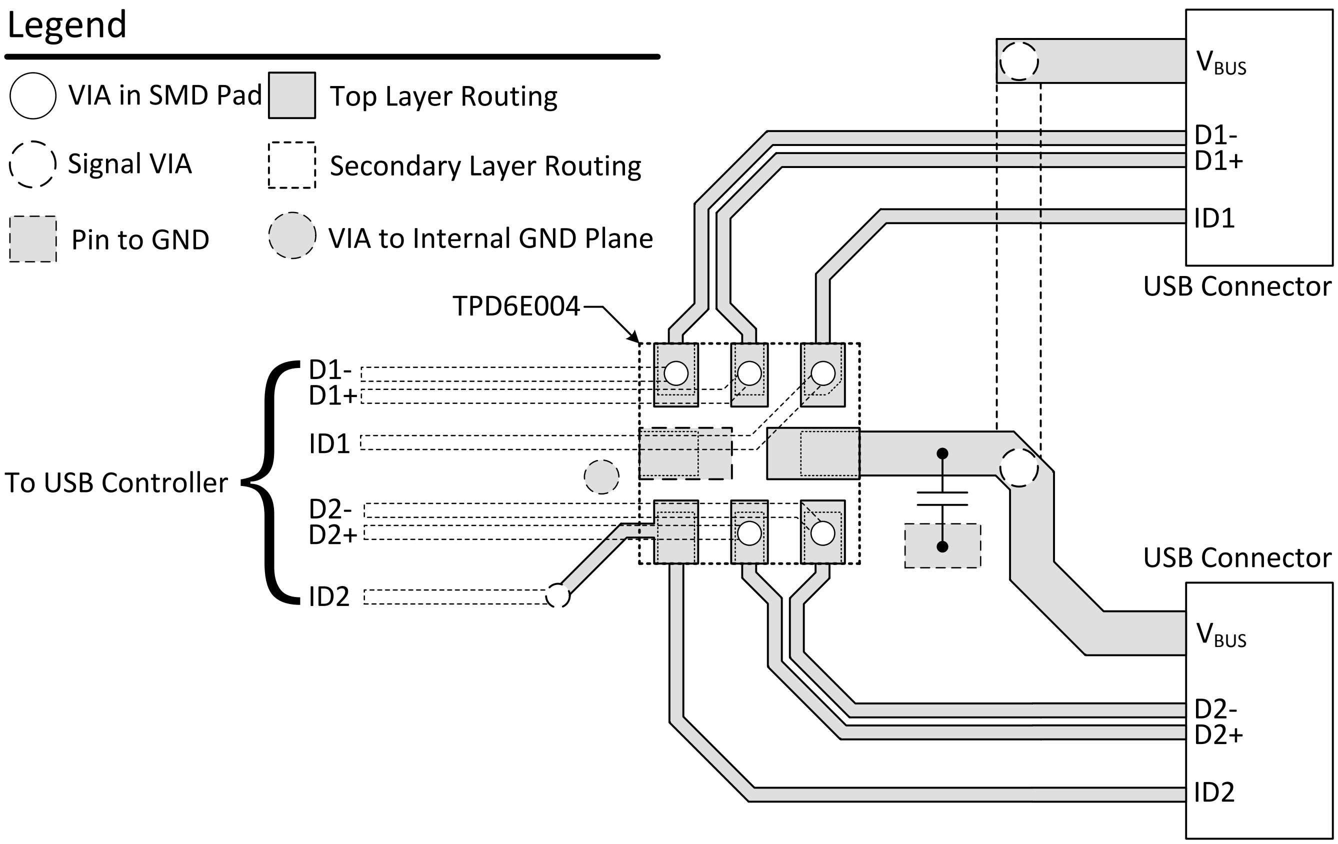

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Figure 8-3. TPD6E004 Layout Example for Two USB 2.0 Micro-B Connectors

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection Data Sheet*
- Texas Instrument, *ESD Protection Layout Guide*

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD6E004RSER	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2V
TPD6E004RSER.A	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2V
TPD6E004RSER.B	Active	Production	UQFN (RSE) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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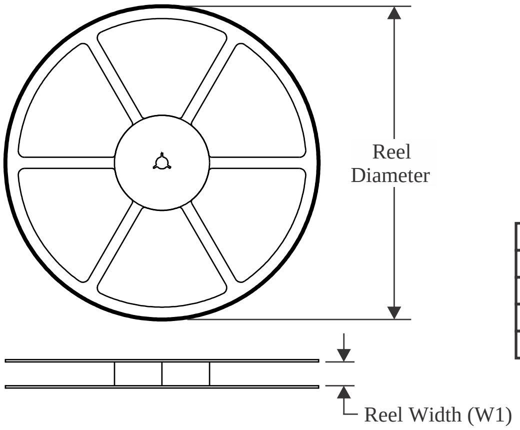
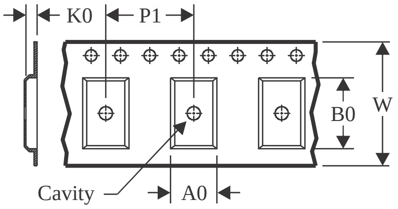
TAPE AND REEL INFORMATION

REEL DIMENSIONS

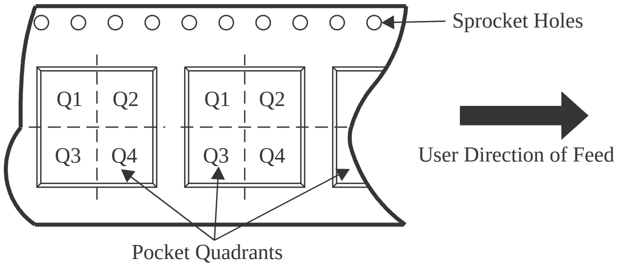


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

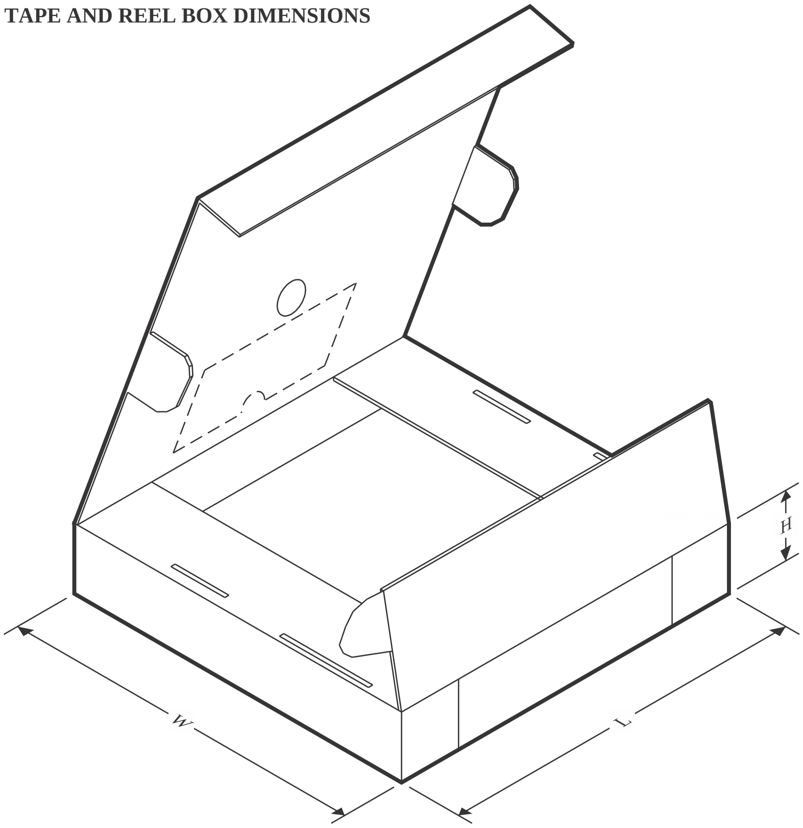
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD6E004RSER	UQFN	RSE	8	3000	180.0	9.5	1.7	1.7	0.75	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

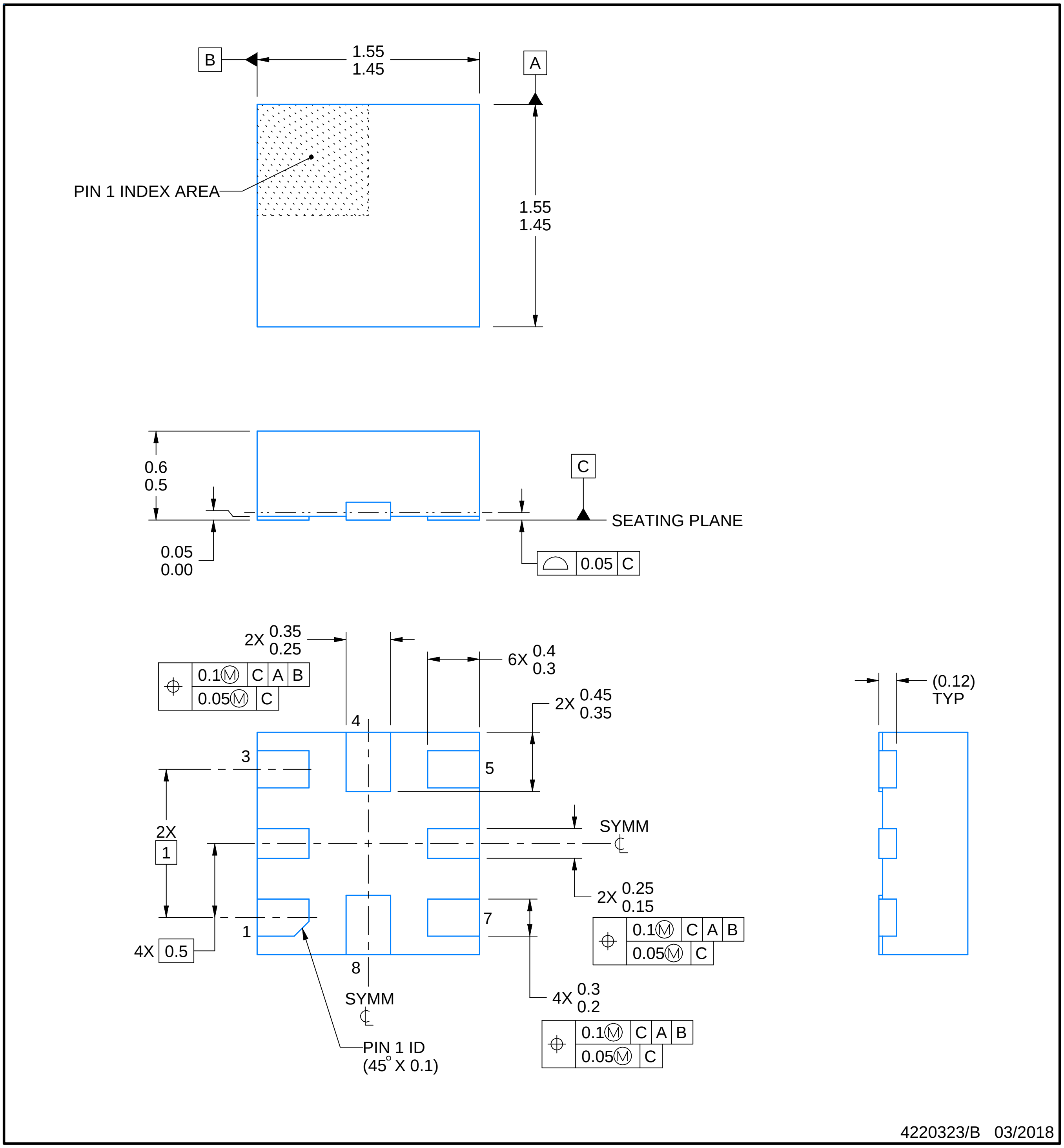
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6E004RSER	UQFN	RSE	8	3000	184.0	184.0	19.0

RSE0008A

PACKAGE OUTLINE

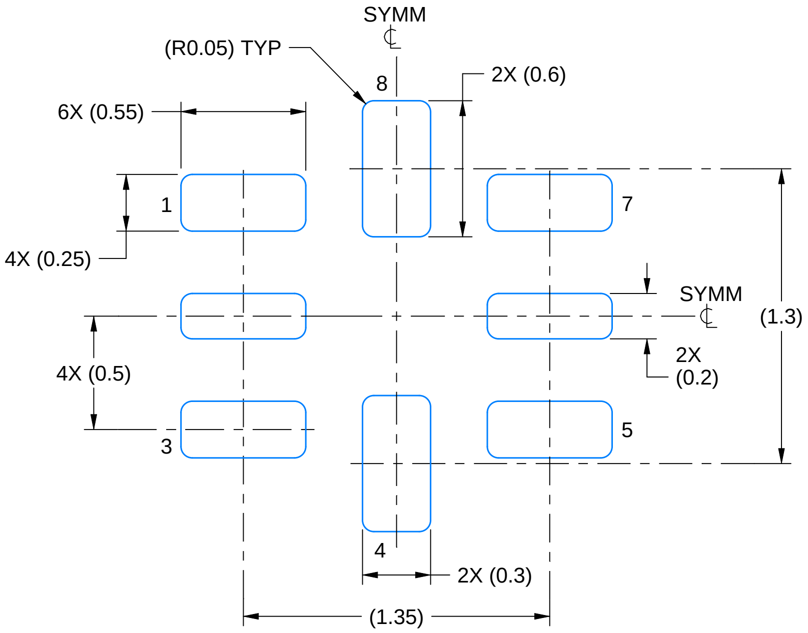
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

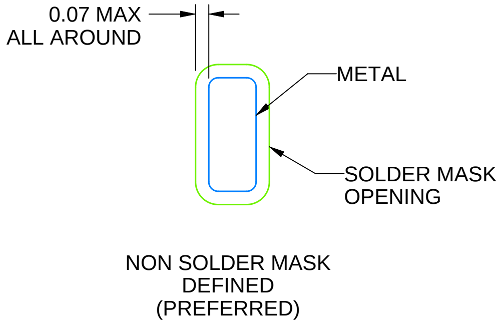


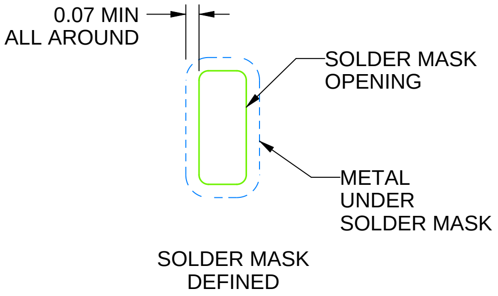
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

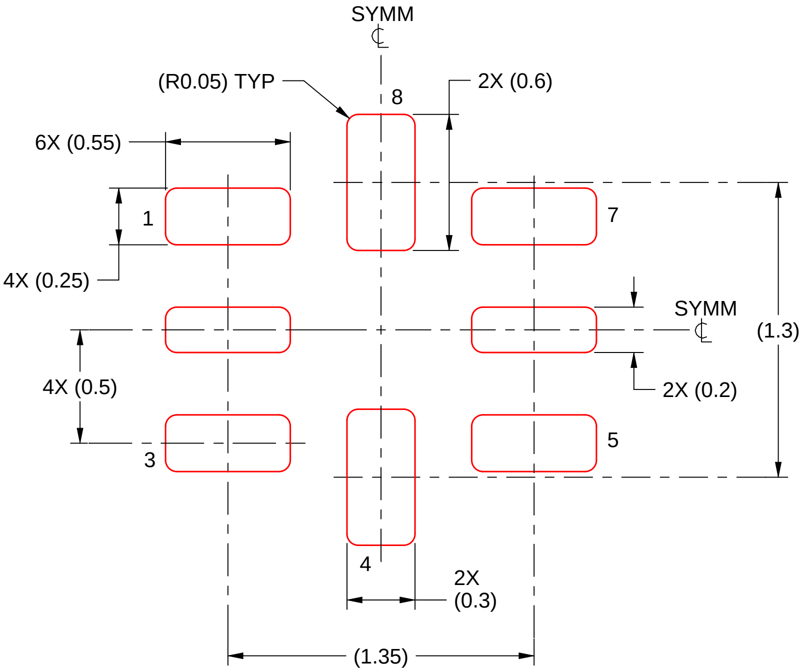




SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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