

# TPD5S115 HDMI Companion Chip With Step-Up DC-DC Converter, Level-Shifter, and ESD Clamp

## 1 Features

- Conforms to HDMI Compliance Tests Without Any External Components
- Supports HDMI 2.0, HDMI 1.4, and HDMI 1.3 Standards
- Matches HDMI Connector Pin Mapping
- Internal DC-DC Converter to Generate 5 V From a Battery Voltage as Low as 2.3 V
- Auto-Direction Sensing, Level Shifting, and Buffering in the CEC, SDA, and SCL Paths
- IEC 61000-4-2 (Level 4) System Level ESD Compliance
- Reverse Current Blocking and Short-Circuit Protection to Protect Against Fault Conditions
- Industrial Temperature Range: –40°C to 85°C

## 2 Applications

- Set-Top Boxes
- TVs
- Smart Phones
- Digital Camcorders
- Portable Game Consoles
- Digital Still Cameras

## 3 Description

The TPD5S115 device is an integrated HDMI companion chip solution. The device provides a regulated 5-V output (5VOUT) for sourcing the HDMI power line. The regulated 5-V output supplies up to 55 mA to the HDMI receiver with a current limiting function. The TPD5S115 features two control signals: EN and LS\_OE. The control of 5VOUT and the hot plug detect (HPD) circuitry is independent of the LS\_OE control signal and is controlled by the EN pin. The EN pin allows the detection scheme (5VOUT + HPD) to be active before turning on the whole HDMI link. The LS\_OE activates the internal LDO, CEC, SCL, and SDA buffers only when EN is also activated. This dual stage enable scheme ensures optimized power saving for portable applications.

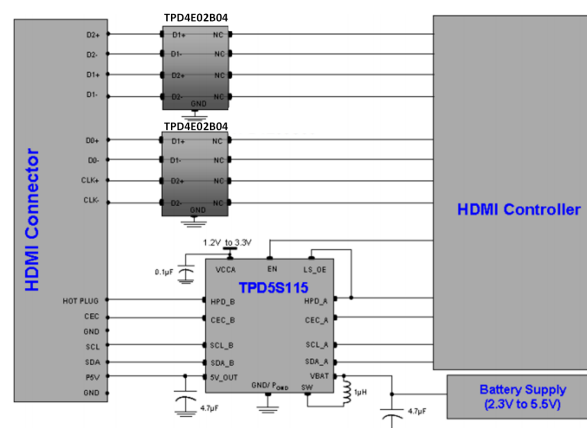
There are three noninverting, bidirectional, voltage level translation circuits for the SDA, SCL, and CEC lines. Each have a common power rail (VCCA) on the A side from 1.1 V to 3.6 V. On the B side, the SCL\_B and SDA\_B each have an internal 1.75-kΩ pullup connected to the regulated 5-V rail (5VOUT). The DDC (SCL\_B and SDA\_B) pins meet the I<sup>2</sup>C specification and drive up to 750-pF loads with the buffers. The CEC\_B pin has an internal 27-kΩ pullup to an internal 3.3-V supply. The TPD5S115 exceeds the IEC61000-4-2 (Level 4) ESD protection level. This device features a space saving, 1.72-mm × 1.72-mm, YFF package with 0.4-mm pitch.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD5S115	DSBGA (16)	1.72 mm × 1.72 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical System Diagram



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## 4 Revision History

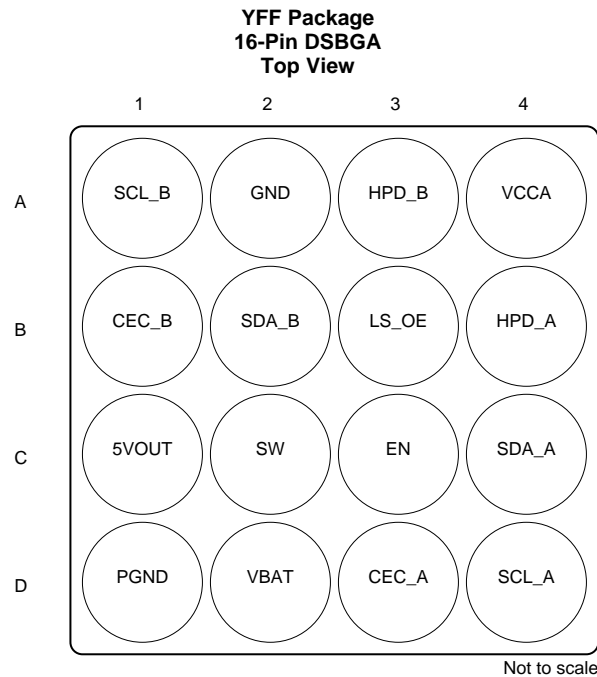
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2016) to Revision D	Page
• Updated Pinout image .....	3

Changes from Revision B (March 2013) to Revision C	Page
• Added <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>Specifications</i> section, <i>ESD Ratings</i> table, <i>Detailed Description</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet .....	1
• Added <i>Thermal Information</i> table .....	5
• Moved the passive components parameters from <i>Recommended Operating Conditions</i> table to the <i>Output Capacitor</i> section .....	18

Changes from Revision A (February 2013) to Revision B	Page
• Changed Board Layout section .....	21

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
5VOUT	C1	O	DC-DC output. The 5-V power pin can supply a 55-mA regulated current to the HDMI receiver. A separate DC-DC converter control pin (EN) disables the DC-DC converter when operating at low-power mode
CEC_A	D3	I/O	LS system side CEC bus I/O. This pin is bidirectional and referenced to VCCA
CEC_B	B1	I/O	LS HDMI connector side CEC bus I/O. This pin is bidirectional and referenced to the 3.3-V internal supply
EN	C3	C	DC-DC enable. Enables the DC-DC converter and HPD circuitry when EN is HIGH. The EN is referenced based off VCCA
GND	A2	G	Device ground
HPD_A	B4	O	System side output for the hot plug detect. This pin is unidirectional and is referenced to VCCA
HPD_B	A3	I	HDMI side input for the hot plug detect. This pin is unidirectional and is referenced to 5VOUT
LS_OE	B3	C	Level shifter enable. This pin is referenced to VCCA. Enables level shifters and LDO when EN is HIGH and LS_OE is HIGH
PGND	D1	G	DC-DC converter ground. These pins are isolated from the GND pins. This pin should be tied to system GND
SCL_A, SDA_A	D4, C4	I/O	LS system side input and output for I <sup>2</sup> C Bus. These pins are bidirectional and referenced to VCCA
SCL_B, SDA_B	A1, B2	I/O	LS HDMI side connector side input and output for I <sup>2</sup> C Bus. These pins are bidirectional and referenced to 5VOUT
SW	C2	I	Switch input. This pin is the inductor input for the DC-DC converter
VBAT	D2	P	Battery supply. This voltage is typically 2.3 V to 5.5 V
VCCA	A4	P	System side supply. This voltage is typically 1.2 V to 3.3 V from the core microcontroller

(1) C = Control, G = Ground, I = Input, O = Output, P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage	VCCA		4	V
	VBAT	−0.3	6	V
Input voltage, $V_I$ <sup>(2)</sup>	SCL_A, SDA_A, CEC_A	−0.3	4	V
	SCL_B, SDA_B, CEC_B, HPD_B	−0.3	6	
	EN, LS_OE	−0.3	4	
Voltage applied to any output in the high-impedance or power-off state, $V_O$ <sup>(2)</sup>	SCL_A, SDA_A, CEC_A	−0.3	4	V
	SCL_B, SDA_B, CEC_B	−0.3	6	
Voltage applied to any output in the high or low state, $V_O$ <sup>(2)</sup>	SCL_A, SDA_A, CEC_A	−0.3	VCCA + 0.3	V
	SCL_B, SDA_B, CEC_B	−0.3	5VOUT + 0.3	
Input clamp current ( $I_V < 0$ )			−50	mA
Output clamp current ( $V_O < 0$ )			−50	mA
Continuous current through 5VOUT, or GND			±100	mA
Storage temperature, $T_{stg}$		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	All pins except pins 4A, B3, C3, C4, D3, and D4	500	V
		Pins 4A, B3, C3, C4, D3, and D4	2000	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		1000	
	IEC 61000-4-2 Contact Discharge	Pins A1, A3, B1, B2, and C1	±14000	
	IEC 61000-4-2 Air-gap Discharge	Pins A1, A3, B1, B2, and C1	±16000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{CCA}$	Supply voltage, VCCA	1.2		3.6	V
$V_{BAT}$	Supply voltage, VBAT	2.3		5.5	V
$V_{IH}$ High-level input voltage	$V_{CCA} = 1.2 \text{ V to } 3.6 \text{ V}$	SCL_A, SDA_A	$0.7 \times V_{CCA}$	$V_{CCA}$	V
		CEC_A	$0.7 \times V_{CCA}$	$V_{CCA}$	
		EN, LS_OE	1	$V_{CCA}$	
	5VOUT = 5 V	SCL_B, SDA_B	$0.7 \times 5VOUT$	5VOUT	
		CEC_B	$0.7 \times 3.3 \text{ V (internal)}^{(1)}$	3.3 V (internal) <sup>(1)</sup>	
		HPD_B	2		

(1) 3.3 V (internal) is an internally generated voltage node for the CEC\_B output buffer supply reference. An LDO generates this 3.3 V from 5VOUT when LS\_OE and EN are HIGH.

## Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{IL}$	Low-Level input voltage	SCL_A, SDA_A	−0.5	$0.082 \times V_{CCA}$		V
		CEC_A	−0.5	$0.082 \times V_{CCA}$		
		EN, LS_OE	−0.5	0.4		
	5VOUT = 5 V	SCL_B, SDA_B	−0.5	$0.3 \times 5V_{OUT}$		
		CEC_B	−0.5	$0.3 \times 3.3$ (internal) <sup>(1)</sup>		
		HPD_B	0	0.8		
$V_{ILC}$	Low-level input voltage		−0.5	$0.065 \times V_{CCA}$		V
$V_{OL} - V_{ILC}$	Delta between $V_{OL}$ and $V_{ILC}$ ( $V_{IO} = 2.5$ V)			$0.1 \times V_{CCA}$		V
$T_A$	Operating free-air temperature		−40		85	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD5S115	UNIT
		YFF (DSBGA)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.2	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	2.5	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	13	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OHA</sub>			I <sub>OH</sub> = −10 μA, V <sub>I</sub> = V <sub>IH</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V	V <sub>CCA</sub> × 0.8			V
V <sub>OLA</sub>			I <sub>OL</sub> = 10 μA, V <sub>I</sub> = V <sub>IL</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V	V <sub>CCA</sub> × 0.16			V
V <sub>OHB</sub>			I <sub>OH</sub> = −10 μA, V <sub>I</sub> = V <sub>IH</sub>				V
V <sub>OLB</sub>			I <sub>OL</sub> = 3 mA, V <sub>I</sub> = V <sub>IL</sub>			0.4	V
R <sub>PU</sub>	Internal pullup	SCL_A, SDA_A	Pullup connected to VCCA rail	10			kΩ
		SCL_B, SDA_B	Pullup connected to 5-V rail	1.75			
I <sub>PULLUPAC</sub>	Transient boosted pullup current (rise-time accelerator)	SCL_B, SDA_B	Pullup connected to 5-V rail	15			mA
I <sub>OFF</sub>	Leakage current	A port	V <sub>CCA</sub> = 0 V, V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V, V <sub>CCA</sub> = 0 V			±5	μA
		B port	5VOUT = 0 V, V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V, V <sub>CCA</sub> = 0 V to 3.6 V			±5	
I <sub>OZ</sub>		A port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>CCA</sub> = 1.2 V to 3.6 V			±5	
		B port	V <sub>I</sub> = V <sub>CCI</sub> or GND, V <sub>CCA</sub> = 1.2 V to 3.6 V			±5	
C <sub>L</sub>	Bus load capacitance	A port				15	pF
		B port				750	
SUPPLY CURRENT							
I <sub>CCA</sub>	VCCA supply current	Standby	I/Os = HIGH			2	μA
		Active	I/Os = HIGH			15	μA
I <sub>CCB</sub>	VBAT supply current	Standby	EN = LOW, LS_OE = LOW	0.5			μA
		DC-DC and HPD active	EN = HIGH, LS_OE = LOW	30		50	μA
		DC-DC, HPD, DDC, CEC Active	EN = HIGH, LS_OE = LOW, I/Os = HIGH	225		300	μA

## Electrical Characteristics (continued)

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC CONVERTER						
V <sub>BAT</sub>	Input voltage		2.3		5.5	V
V <sub>OUT</sub>	Total DC output voltage <sup>(1)</sup>		4.9	5	5.13	V
T <sub>OVA</sub>	Total output voltage accuracy <sup>(2)</sup>		4.8	5	5.3	V
V <sub>IO_Ripple</sub>	Output voltage ripple, loaded	I <sub>O</sub> = 65 mA		50.6		mV <sub>PP</sub>
		I <sub>O</sub> = 150 mA		16		
f <sub>CLK</sub>	Internal operating frequency	V <sub>BAT</sub> = 2.3 V to 5.5 V		3.5		MHz
t <sub>START</sub>	Start-up time	From EN input to 5-V power output 90% point		187		μs
I <sub>O</sub>	Output current	V <sub>BAT</sub> = 2.3 V to 5.5 V	55			mA
	Reverse leakage current, V <sub>O</sub>	EN = LOW, V <sub>O</sub> = 5.5 V			2.5	μA
	Leakage current from battery to V <sub>O</sub>	EN = LOW			5	μA
V <sub>BATUV</sub>	Undervoltage lockout threshold	Falling		2		V
		Rising		2.1		V
Line transient response		V <sub>BAT</sub> = 3.4 V, I <sub>O</sub> = 20 mA to 65 mA, A 217 Hz, 600 mV <sub>PP</sub> square wave pulse		17.1		mV <sub>pk</sub>
Load transient response		V <sub>BAT</sub> = 3.4 V, I <sub>O</sub> = 5 mA to 65 mA, 10-μs pulse, t <sub>RISE</sub> = t <sub>FALL</sub> = 0.1 μs		63.5		mV <sub>pk</sub>
I <sub>INRUSH</sub>	Inrush current, average over t <sub>START</sub>	V <sub>BAT</sub> = 2.3 V to 5.5 V, I <sub>OUT</sub> = 65 mA		168		mA
I <sub>SC</sub>	Short-circuit current limit from output			90		mA
VOLTAGE LEVEL SHIFTER CEC LINE (x_A & x_B PORTS)						
V <sub>OHA</sub>		I <sub>OH</sub> = −10 μA, V <sub>I</sub> = V <sub>IH</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V	V <sub>CCA</sub> × 0.8			V
V <sub>OLA</sub>		I <sub>OL</sub> = 10 μA, V <sub>I</sub> = V <sub>IL</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V	V <sub>CCA</sub> × 0.16			V
V <sub>OHB</sub>		I <sub>OH</sub> = −20 μA, V <sub>I</sub> = V <sub>IH</sub>	V <sub>CCA</sub> × 0.8			V
V <sub>OLB</sub>		I <sub>OL</sub> = 3 mA, V <sub>I</sub> = V <sub>IL</sub>			0.4	V
R <sub>PU</sub>	Internal pullup	CEC_A	Pullup connected to V <sub>CCA</sub> rail		10	kΩ
		CEC_B	Pullup connected to 3.3 V rail		22	
R <sub>PD</sub>	Internal pulldown	CEC_B	Pullup connected to GND		14	MΩ
I <sub>OFF</sub>	A port	V <sub>CCA</sub> = 0 V, V <sub>I</sub> or V <sub>O</sub> = 0 to 3.6 V, V <sub>CCA</sub> = 0 V			±5	μA
	B port	5V <sub>OUT</sub> = 0 V, V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V, V <sub>CCA</sub> = 0 V to 3.6 V			±1.8	
I <sub>OZ</sub>	A port	V <sub>O</sub> = V <sub>CCO</sub> or GND, V <sub>CCA</sub> = 1.2 V to 3.6 V			±5	
	B port	V <sub>I</sub> = V <sub>CCI</sub> or GND, V <sub>CCA</sub> = 1.2 V to 3.6 V			±5	
VOLTAGE LEVEL SHIFTER - HPD LINE (X_A & x_B)						
V <sub>OHA</sub>		I <sub>OH</sub> = −3 mA, V <sub>I</sub> = V <sub>IH</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V	V <sub>CCA</sub> × 0.7			V
V <sub>OLA</sub>		I <sub>OL</sub> = 3 mA, V <sub>I</sub> = V <sub>IL</sub> , V <sub>CCA</sub> = 1.2 V to 3.6 V			0.4	V
R <sub>PD</sub>	Internal pulldown	HPD_B	Pullup connected to GND		100	kΩ
I <sub>OZ</sub>	A port	V <sub>I</sub> = V <sub>CCI</sub> or GND, V <sub>CCA</sub> = 3.6 V			±5	μA
LS_OE, EN						
I <sub>I</sub>		V <sub>I</sub> = V <sub>CCA</sub> or GND, V <sub>CCA</sub> = 1.2 V to 3.6 V			±12	

(1) Includes voltage references, DC load and line regulations, process and temperature.

(2) Includes voltage references, DC load and line regulations, transient load and line regulations, ripple, process, and temperature.

## 6.6 Electrical Characteristics – I/O Capacitances

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Capacitance	EN, LS_OE	$V_{BIAS} = 1.8\text{ V}$ , $f = 1\text{ MHz}$ , 30-mV <sub>pp</sub> AC signal	$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$		7.1	9.5	pF
	SCL_A, SDA_A, CEC_A		$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW		7		pF
	HPD_A, HPD_B		$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW		4		pF
	SCL_B, SDA_B	$V_{BIAS} = 2.5\text{ V}$ , $f = 100\text{ kHz}$ , 3.5-V <sub>pp</sub> AC signal	$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW, LS_OE = HIGH		10		pF
	CEC_B		$V_{CCA} = 3.6\text{ V}$ , $V_{BAT} = 5\text{ V}$ , EN = LOW, LS_OE = HIGH		7		pF
	CEC_B		$V_{CCA} = 0\text{ V}$ , $5V_{IN} = 0\text{ V}$		7		pF

## 6.7 Switching Characteristics – $V_{CCA} = 1.2\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SCL and SDA LINES (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	DDC channels enabled	394		ns	
		B to A	DDC channels enabled	347			
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	DDC channels enabled	504		ns	
		B to A	DDC channels enabled	171			
t <sub>FALL</sub>	Fall time	A port	DDC channels enabled	146		ns	
		B port	DCC channels enabled	135			
t <sub>RISE</sub>	Rise time	A port	DCC channels enabled	190		ns	
		B port	DCC channels enabled	93			
f <sub>MAX</sub>	Maximum switching frequency		DCC channels enabled	400		kHz	
CEC LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	CEC channels enabled	550		ns	
		B to A	CEC channels enabled	350			
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	CEC channels enabled	13		μs	
		B to A	CEC channels enabled	290			
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled	146		ns	
		B port	CEC channels enabled	200			
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled	190		ns	
		B port	CEC channels enabled	16.4			
HPD LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	Propagation delay	B to A	CEC channels enabled	10.4		ns	
t <sub>PLH</sub>	Low-to-high propagation delay	B to A	CEC channels enabled	9.9		ns	
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled	0.7		ns	
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled	0.8		ns	

## 6.8 Switching Characteristics – $V_{CCA} = 1.5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SCL, SDA LINES (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	DDC channels enabled		375		ns
		B to A	DDC channels enabled		272		
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	DDC channels enabled		488		ns
		B to A	DDC channels enabled		166		
t <sub>FALL</sub>	Fall time	A port	DDC channels enabled		114		ns
		B port	DCC channels enabled		135		
t <sub>RISE</sub>	Rise time	A port	DCC channels enabled		186		ns
		B port	DCC channels enabled		93		
f <sub>MAX</sub>	Maximum switching frequency		DCC channels enabled		400		kHz
CEC Line (x_A & x_B Ports)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	CEC channels enabled		536		ns
		B to A	CEC channels enabled		272		
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	CEC channels enabled		13		μs
		B to A	CEC channels enabled		285		ns
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled		113		ns
		B port	CEC channels enabled		201		
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled		187		ns
		B port	CEC channels enabled		16		μs
HPD LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	B to A	CEC channels enabled		10		ns
t <sub>PLH</sub>	Low-to-high propagation delay	B to A	CEC channels enabled		10		ns
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled		0.46		ns
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled		0.5		ns

## 6.9 Switching Characteristics – $V_{CCA} = 1.8\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SCL, SDA LINES (x_A &amp; x_B PORTS)</b>						
$t_{PHL}$	High-to-low propagation delay	A to B	DDC channels enabled	370		ns
		B to A	DDC channels enabled	230		
$t_{PLH}$	Low-to-high propagation delay	A to B	DDC channels enabled	480		ns
		B to A	DDC channels enabled	163		
$t_{FALL}$	Fall time	A port	DDC channels enabled	100		ns
		B port	DCC channels enabled	135		
$t_{RISE}$	Rise time	A port	DCC channels enabled	180		ns
		B port	DCC channels enabled	93		
$f_{MAX}$	Maximum switching frequency	DCC channels enabled	400			kHz
<b>CEC LINE (x_A &amp; x_B PORTS)</b>						
$t_{PHL}$	High-to-low propagation delay	A to B	CEC channels enabled	530		ns
		B to A	CEC channels enabled	230		
$t_{PLH}$	Low-to-high propagation delay	A to B	CEC channels enabled	13		$\mu\text{s}$
		B to A	CEC channels enabled	280		ns
$t_{FALL}$	Fall time	A port	CEC channels enabled	98		ns
		B port	CEC channels enabled	200		



## Switching Characteristics – $V_{CCA} = 1.8\text{ V}$ (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled		180		ns
		B port	CEC channels enabled		16		μs
HPD LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	B to A	CEC channels enabled		10		ns
t <sub>PLH</sub>	Low-to-high propagation delay	B to A	CEC channels enabled		10		ns
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled		0.41		ns
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled		0.41		ns

## 6.10 Switching Characteristics – $V_{CCA} = 2.5\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SCL, SDA LINES (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	DDC channels enabled	370		ns	
		B to A	DDC channels enabled	185			
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	DDC channels enabled	467		ns	
		B to A	DDC channels enabled	160			
t <sub>FALL</sub>	Fall time	A port	DDC channels enabled	80		ns	
		B port	DCC channels enabled	135			
t <sub>RISE</sub>	Rise time	A port	DCC channels enabled	179		ns	
		B port	DCC channels enabled	93			
f <sub>MAX</sub>	Maximum switching frequency		DCC channels enabled	400		kHz	
CEC LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	CEC channels enabled	530		ns	
		B to A	CEC channels enabled	185			
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	CEC channels enabled	13		μs	
		B to A	CEC channels enabled	275			
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled	80		ns	
		B port	CEC channels enabled	200			
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled	180		ns	
		B port	CEC channels enabled	16			
HPD LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	B to A	CEC channels enabled	10		ns	
t <sub>PLH</sub>	Low-to-high propagation delay	B to A	CEC channels enabled	10		ns	
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled	0.35		ns	
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled	0.35		ns	

## 6.11 Switching Characteristics – $V_{CCA} = 3.3\text{ V}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SCL, SDA LINES (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	DDC channels enabled		370		ns
		B to A	DDC channels enabled		160		
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	DDC channels enabled		460		ns
		B to A	DDC channels enabled		155		
t <sub>FALL</sub>	Fall time	A port	DDC channels enabled		75		ns
		B port	DCC channels enabled		135		
t <sub>RISE</sub>	Rise time	A port	DCC channels enabled		180		ns
		B port	DCC channels enabled		93		
f <sub>MAX</sub>	Maximum switching frequency		DCC channels enabled		400		kHz
CEC LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	A to B	CEC channels enabled		530		ns
		B to A	CEC channels enabled		160		
t <sub>PLH</sub>	Low-to-high propagation delay	A to B	CEC channels enabled		13		μs
		B to A	CEC channels enabled		275		ns
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled		73		ns
		B port	CEC channels enabled		200		
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled		180		ns
		B port	CEC channels enabled		16		μs
HPD LINE (x_A & x_B PORTS)							
t <sub>PHL</sub>	High-to-low propagation delay	B to A	CEC channels enabled		10		ns
t <sub>PLH</sub>	Low-to-high propagation delay	B to A	CEC channels enabled		10		ns
t <sub>FALL</sub>	Fall time	A port	CEC channels enabled		0.34		ns
t <sub>RISE</sub>	Rise time	A port	CEC channels enabled		0.36		ns

## 6.12 Typical Characteristics

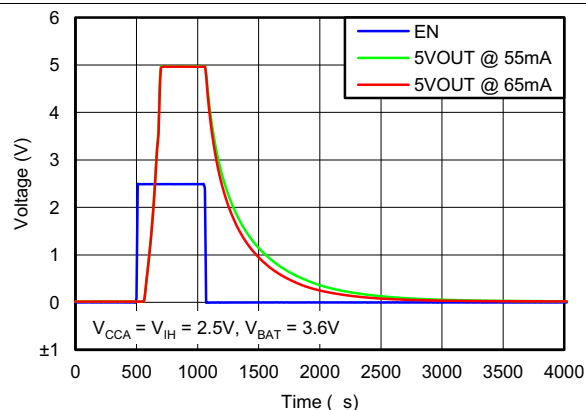


Figure 1. Voltage vs Time

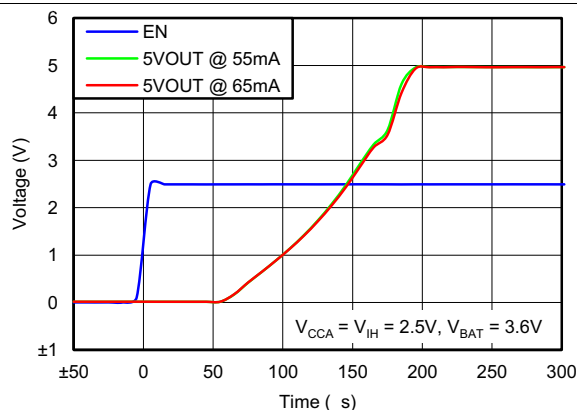


Figure 2. Voltage vs Time

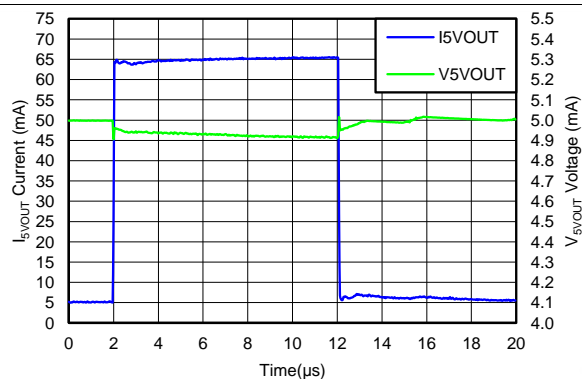


Figure 3. Current vs Time

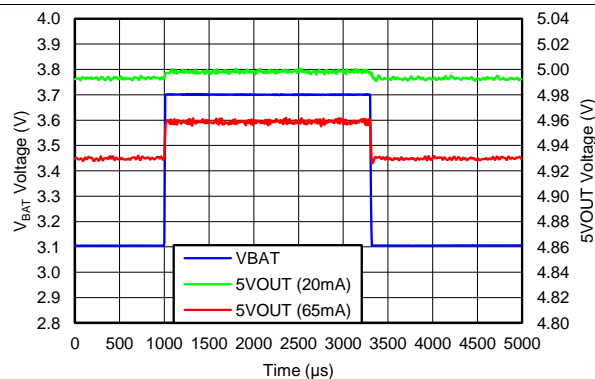


Figure 4. Voltage vs Time

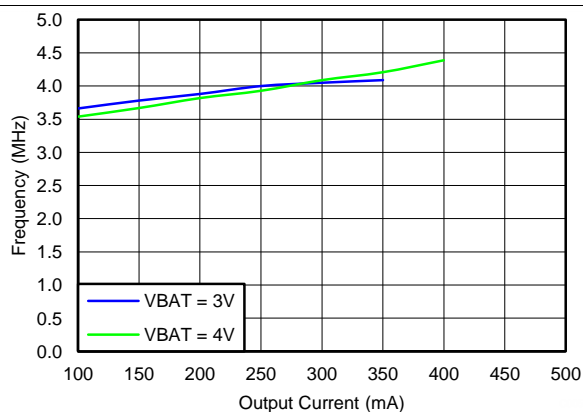


Figure 5. Frequency vs Output Current

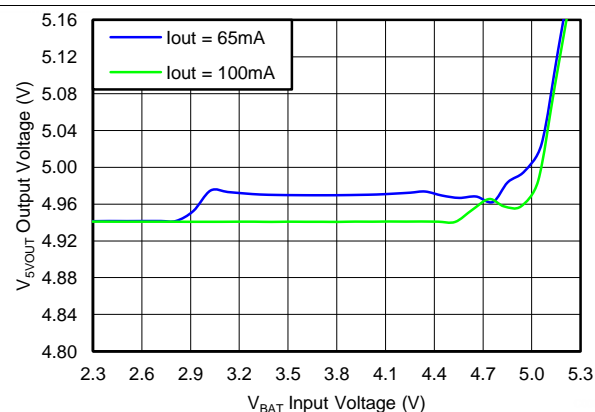


Figure 6. Output Voltage vs Input Voltage

## Typical Characteristics (continued)

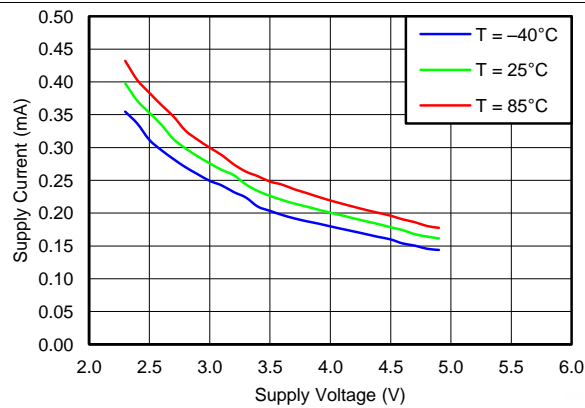


Figure 7. Supply Current vs Supply Voltage

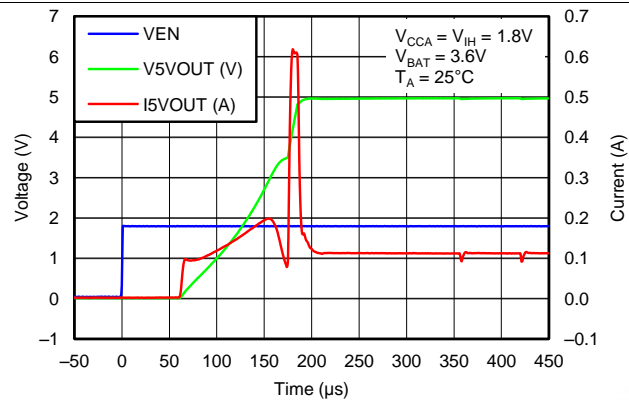


Figure 8. Voltage and Current vs Time

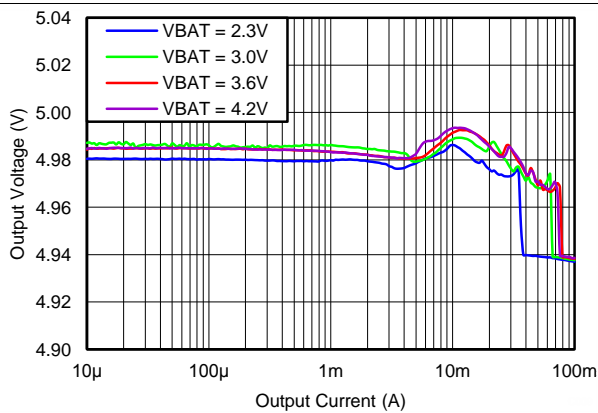


Figure 9. Output Voltage vs Output Current

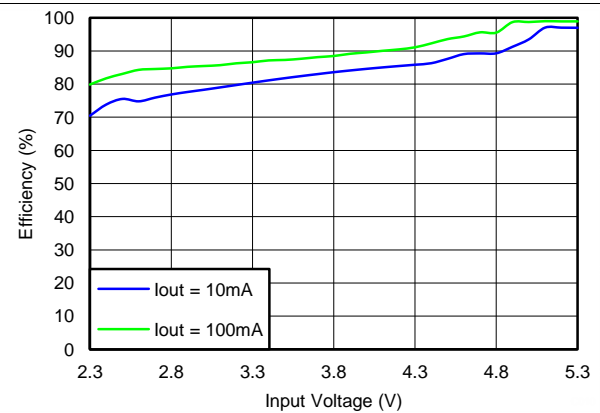


Figure 10. Efficiency vs Input Voltage

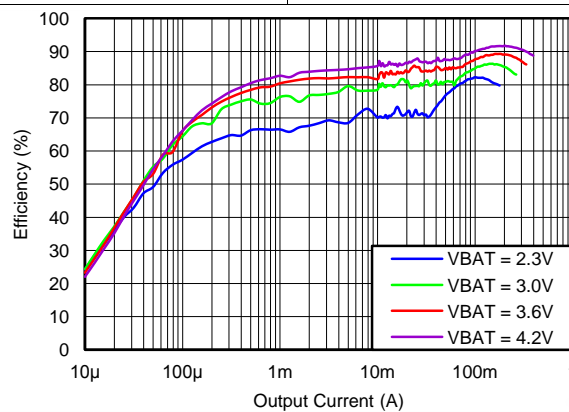


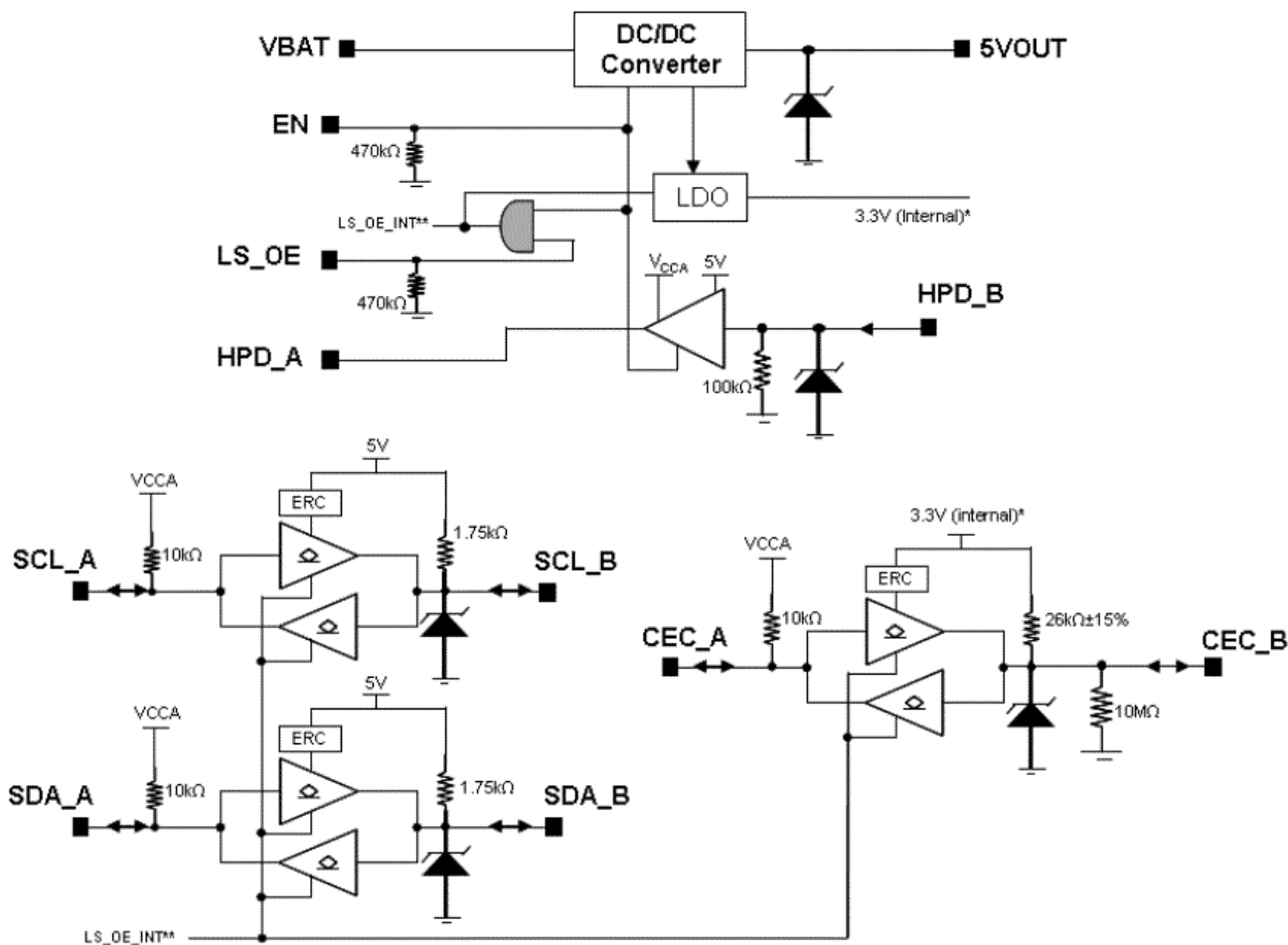
Figure 11. Efficiency vs Output Current

## 7 Detailed Description

### 7.1 Overview

The TPD5S115 is an integrated interface solution that covers HDMI versions' 2.0, 1.4, and 1.3 need for power supply voltage management and control line level translation. On the power supply line, it has a DC-DC converter that takes the internal power supply from 2.3 V to 5.5 V, and outputs a regulated and current-limited, 5-V voltage to the connector. The drivers support level translation on HPD, ECE, SCL, and SDA lines in both transmission directions. Moreover, the rise-time acceleration feature helps drive the high capacitive load on the cable side. Every channel comes with robust ESD protection with  $\pm 14$ -kV contact and  $\pm 16$ -kV air-gap IEC61000-4-2 capability.

### 7.2 Functional Block Diagram



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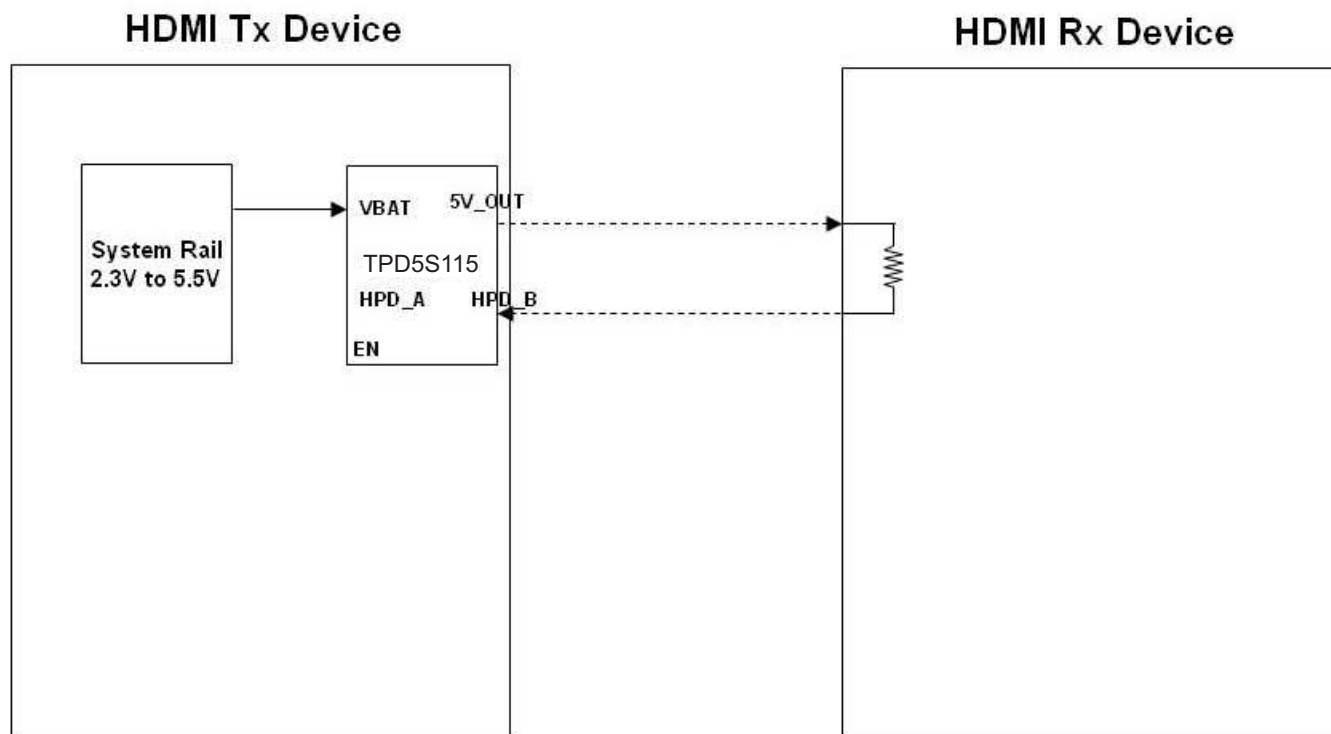
- (1) 3.3 V (internal) is an internal 3.3-V supply rail which is generated from 5VOUT when EN and LS\_OE are HIGH.
- (2) LS\_OE\_INT is an internal control signal generated from EN and LS\_OE signals. LS\_OE\_INT is active when both EN and LS\_OE are HIGH.

### 7.3 Feature Description

#### 7.3.1 Rise-Time Accelerators

The HDMI cable side of the DDC lines incorporates rise-time accelerators to support the high capacitive load on the HDMI cable side. The rise-time accelerator boosts the cable-side DDC signal, independent of which side of the bus is releasing the signal.

## Feature Description (continued)



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**Figure 12. Receiving and Transmitting Interaction**

### 7.3.2 Hot Plug Detect

After the TPD5S115's DC-DC converter and HPD block are enabled through the EN pin, the TPD5S115 is ready for continual HDMI receiver detection. After a HDMI cable connects a receiving and transmitting device together, the 5-V signal from the DC-DC output flows through the receiving device's internal resistor and into HPD's input. The HPD buffer's output then goes high, indicating to the transmitter that a receiving device is connected. To save power, periodic detection can be done by turning on and off the DC-DC converter before a receiving device is connected.

#### NOTE

Ground offset between the TPD5S115 ground and the ground of devices on port A of the TPD5S115 must be avoided. A CMOS or NMOS open-drain capable of sinking 3 mA of current at 0.4 V has an output resistance of 133  $\Omega$  or less ( $R = E / I$ ). Such a driver shares enough current with the port A output pulldown of the TPD5S115 to be detected as a LOW while the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Because  $V_{ILC}$  can be as low as 90 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 50 mV. Bus repeaters that use an output offset are not interoperable with the port A of the TPD5S115 as their output LOW levels are not recognized by the TPD5S115 as a LOW. If the TPD5S115 is placed in an application where the  $V_{IL}$  of port A of the TPD5S115 does not go below its  $V_{ILC}$  it will pull port B LOW initially when port A input transitions LOW but the port B will return HIGH, so it does not reproduce the port A input on port B. Such applications must be avoided. Port B is interoperable with all I<sup>2</sup>C-bus slaves, masters, and repeaters.

## Feature Description (continued)

### 7.3.3 CEC Level Shift Operation

The CEC level shift function operates in the same manner as the DDC lines except that the CEC line does not need the rise time accelerator function.

### 7.3.4 Pullup Resistor

The system is designed to work properly with no external pullup resistors on the DDC, CEC, and HPD lines.

### 7.3.5 Undervoltage Lockout

The undervoltage-lockout circuit prevents the DC-DC converter from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling  $V_{IN}$  trips the undervoltage-lockout threshold ( $V_{BATUV}$ ). The undervoltage-lockout threshold for falling  $V_{IN}$  is typically 2 V. The device starts operation once the rising  $V_{IN}$  trips the under-voltage-lockout threshold again at 2.1 V (typical).

### 7.3.6 Soft Start

The DC-DC converter has an internal soft-start circuit that controls the ramp-up of the output voltage. The output voltage reaches its nominal value within 250  $\mu$ s (typical) after EN has been pulled high. The output voltage ramps up from 5% to its nominal value within 300  $\mu$ s (typical). This limits the in-rush current in the converter during start-up and prevents possible input voltage drops when a battery or high impedance power source is used. During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches  $V_{IN}$ . Once the output voltage trips this threshold, the device operates with its nominal current limit.

## 7.4 Device Functional Modes

### 7.4.1 Power-Save Mode

The TPD5S115 integrates a power-save mode to improve efficiency at light loads. In power-save mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power-save mode once the output voltage exceeds the set threshold voltage. The PFM mode is ended and PWM mode begins in case the output current can no longer be supported in PFM mode.

### 7.4.2 Enable

The DC-DC converter is enabled when the EN is set to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches its nominal value in 250  $\mu$ s (typical) after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter to drive the EN pin high and create a sequencing of supply rails. When EN = GND, the converter enters shutdown mode.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

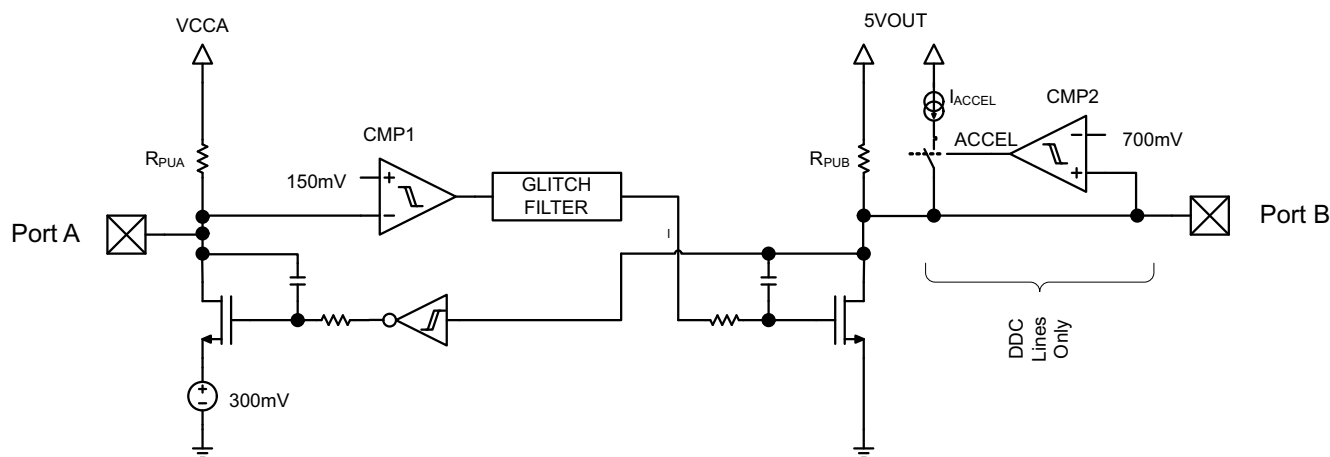
### 8.1 Application Information

The TPD5S115 is an integrated solution for HDMI 2.0, 1.3, and 1.4 interfaces. The device has a boost converter on the power supply, signal conditioning circuits on CEC, SCL, SDA, and HPD lines, and ESD protection on all the connector-facing lines.

### 8.2 Typical Applications

#### 8.2.1 DDC or CEC Level Shifter

The TPD5S115 enables DDC translation from VCCA (system side) voltage levels to 5-V (HDMI cable side) voltage levels without degradation of system performance. The TPD5S115 contains 2 bidirectional, open-drain buffers specifically designed to support up and down-translation between the low voltage, VCCA side DDC-bus and the 5-V DDC-bus. The port B I/Os are overvoltage tolerant to 5.5 V, even when the device is shutdown. After power up and with the LS\_OE and EN pins HIGH, a LOW level on port A (below  $V_{ILC} = 0.08 \times V_{CCA}$ ) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to  $V_{OLB}$ . When port A rises above approximately  $0.10 \times V_{CCA}$ , the port B pulldown driver is turned off and the internal pullup resistor pulls the pin HIGH. When port B falls first and goes below  $0.3 \times V_{OUT}$ , a CMOS hysteresis input buffer detects the falling edge, turns on the port A driver, and pulls port A down to approximately  $V_{OLA} = 0.16 \times V_{CCA}$ . The port B pulldown is not enabled unless the port A voltage goes below  $V_{ILC}$ . If the port A low voltage goes below  $V_{ILC}$ , the port B pulldown driver is enabled until port A rises above  $(V_{ILC} + \Delta V_{T-HYSTA})$ , then port B, if not externally driven LOW, continues to rise being pulled up by the internal pullup resistor.



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**Figure 13. DDC or CEC Level Shifter Block Diagram**



## Typical Applications (continued)

### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

**Table 1. Design Parameters**

PARAMETER	VALUE
5VOUT DC current	55 mA
CEC_A, HPD_A, SCL_A, SDA_A voltage level	V <sub>CCA</sub>
HDMI 2.0 data rate per TMDS signal pair	6 Gbps
Required IEC 61000-4-2 ESD Protection	±8-kV contact

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 DDC or CEC Level Shifter Operational Notes for V<sub>CCA</sub> = 1.8 V

- The threshold of CMP1 is approximately 150 mV ± the 40 mV of total hysteresis
- The comparator trips for a falling waveform at approximately 130 mV
- The comparator trips for a rising waveform at approximately 170 mV
- To be recognized as a zero, the level at port A must first go below 130 mV (V<sub>ILC</sub> in spec) and then stay below 170 mV (V<sub>ILA</sub> in spec)
- To be recognized as a one, the level at A must first go above 170 mV and then stay above 130 mV
- V<sub>ILC</sub> is specified as 110 mV in [Electrical Characteristics](#) to give some margin to the 130 mV
- V<sub>ILA</sub> is specified as 140 mV in [Electrical Characteristics](#) to give some margin to the 170 mV
- V<sub>IHA</sub> is specified as 70% of V<sub>CCA</sub> to be consistent with standard CMOS levels

#### 8.2.1.2.2 Input Capacitor

Due to the nature of the boost converter having a pulsating input current, a low-ESR input capacitor is required to prevent large voltage transients that can cause poor performance of the device or interference with other circuits in the system. TI recommends a 1.2-μF (minimum) input capacitor to improve transient behavior of the regulator and EMI behavior of the total power-supply circuit. TI recommends placing a ceramic capacitor (4.7 μF) as close as possible to the V<sub>IN</sub> and GND pins to improve the input noise filtering.

#### 8.2.1.2.3 Output Capacitor

TI recommends using a small ceramic capacitors placed as close as possible to the V<sub>OUT</sub> and GND pins of the IC. If the application requires the use of large capacitors which can not be placed close to the IC, TI recommends using a smaller ceramic capacitor in parallel to the large capacitor. This small capacitor must be placed as close as possible to the V<sub>OUT</sub> and GND pins of the IC. Use [Equation 1](#) to estimate the recommended minimum output capacitance.

$$C_{\min} = \frac{I_{\text{OUT}} \times (V_{\text{OUT}} - V_{\text{IN}})}{f \times \Delta V \times V_{\text{OUT}}}$$

where

- f is the switching frequency
- ΔV is the maximum allowed ripple

(1)

If a ripple voltage of 10 mV is chosen, a minimum effective capacitance of 2.7 μF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using [Equation 2](#).

$$\Delta V_{\text{ESR}} = I_{\text{OUT}} \times R_{\text{ESR}}$$

(2)

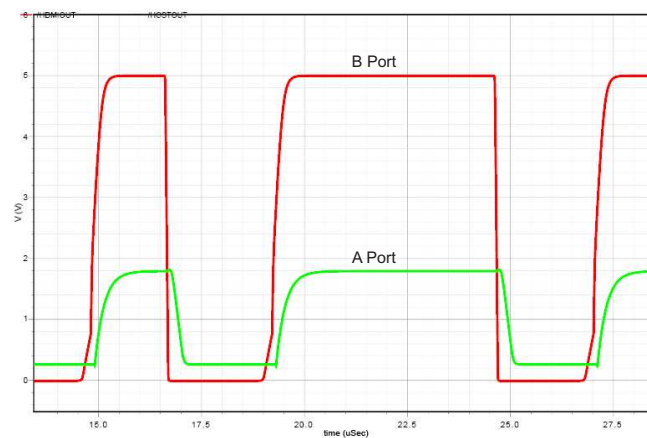
To maintain control loop stability, a capacitor with a value in the range of the calculated minimum must be used. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Ceramic capacitors have a DC-bias effect, which has a strong influence on the final effective capacitance needed. Therefore the appropriate capacitor value must be chosen very carefully. Package size, voltage rating, and material are responsible for differences between the rated capacitor value and the effective capacitance. The minimum effective capacitance value is 1.2  $\mu\text{F}$ , but the recommended value is 4.7  $\mu\text{F}$ .

**Table 2. Passive Components: Recommended Effective Values**

COMPONENT	MIN	TYP	MAX	UNIT
$C_{\text{IN}}$	1.2	4.7	6.5	$\mu\text{F}$
$C_{\text{OUT}}$	1.2	4.7	10	$\mu\text{F}$
$L_{\text{IN}}$	0.7	1	1.3	$\mu\text{H}$
$C_{\text{VCCA}}$		0.1		$\mu\text{F}$

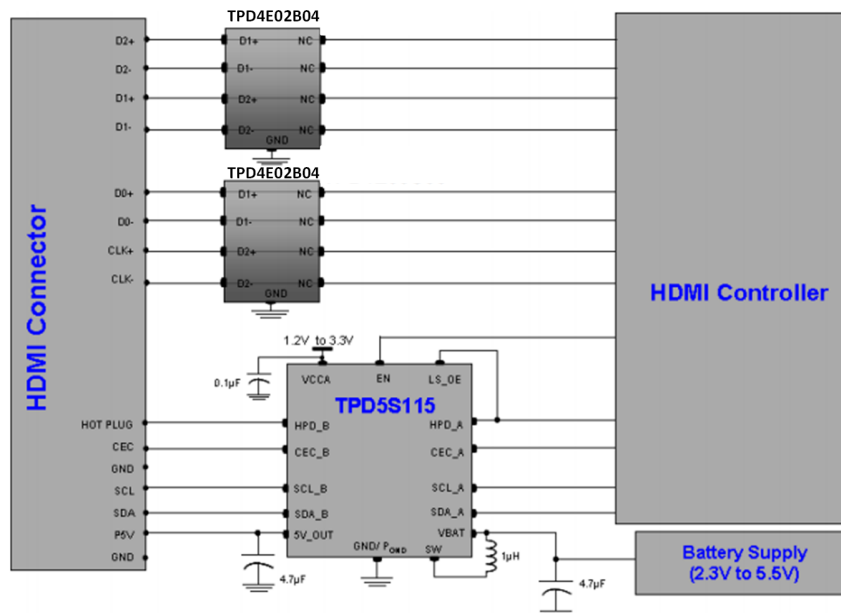
### 8.2.1.3 Application Curve



**Figure 14. DDC Level Shifter Operation (B to A Direction)**

## 8.2.2 Other Application Circuits

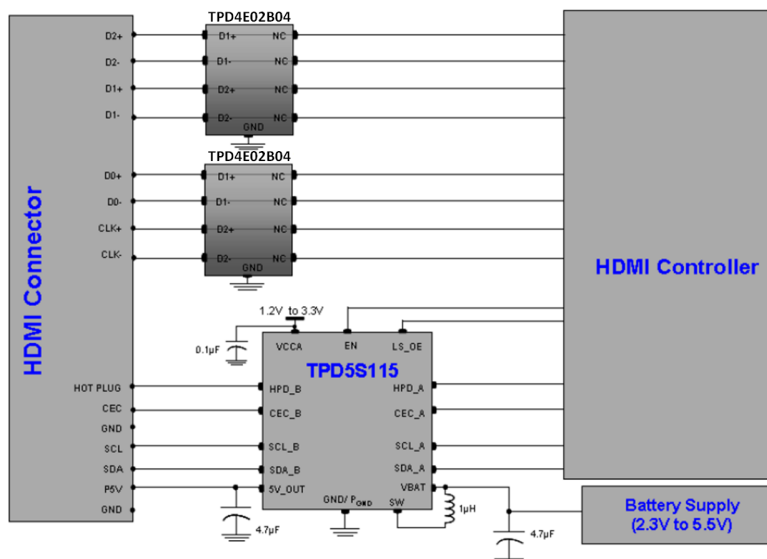
Figure 15 and Figure 16 show application examples using the TPD5S115 devices. Customers must fully validate and test any circuit before implementing a design based on an example in this section. Unless otherwise noted, the design procedures in [DDC or CEC Level Shifter](#) are applicable.



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Figure 15. Application Schematic for HDMI Controllers With One GPIO for HDMI Interface Control

Some HDMI controllers may have only one GPIO to control the HDMI interface, thus, the HDMI driver chip controls the TPD5S115 through only one control line (EN). In this mode the HPD\_A to LS\_OE pins are connected to each other (see Figure 15).



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Figure 16. Application Schematic for HDMI Controllers With Two GPIOs for HDMI Interface Control

## TPD5S115

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Some HDMI driver chips may have two GPIOs to control the HDMI interface chip. In this case a flexible power saving mode can be implemented. The LS\_OE and EN are active-high enable pins. They control the TPD5S115 power-saving options according to [Table 3](#) and [Table 4](#).

**Table 3. Device Status – Part 1**

LS_OE	EN	V <sub>CCA</sub>	V <sub>BAT</sub>	5VOUT	A-SIDE PULLUPS	DCC, B-SIDE PULLUPS	CEC, B-SIDE PULLUPS
L	L	1.8 V	5 V	Off	Off	Off	Off
L	H	1.8 V	5 V	On	On	On	Off
H	L	1.8 V	5 V	Off	Off	Off	Off
H	H	1.8 V	5 V	On	On	On	On
X	X	0 V	0 V	High-Z	High-Z	High-Z	High-Z
X	X	1.8 V	0 V	Low	Low	High-Z	High-Z
X	X	0 V	5 V	High-Z	High-Z	High-Z	High-Z

**Table 4. Device Status – Part 2**

LS_OE	EN	CEC LDO	DC-DC AND HPD	DDC OR CEC VLTS	I <sub>CCA</sub> TYP	I <sub>CC</sub> V <sub>BAT</sub> TYP	COMMENT
L	L	Off	Off	OFF and High-Z	1 µA	1 µA	Fully disabled
L	H	Off	On	OFF and High-Z	1 µA	30 µA	DC-DC (30 µA) ON
H	L	Off	Off	OFF and High-Z	1 µA	1 µA	Not valid state
H	H	On	On	ON	13 µA	225 µA	Fully ON
X	X	Off	Off	High-Z	0 µA	0 µA	Power down
X	X	Off	Off	High-Z	0 µA	0 µA	Power down
X	X	Off	Off	High-Z	0 µA	0 µA	Power down

## 9 Power Supply Recommendations

To keep the normal function of TPD5S115, the designer needs to make sure that both VBAT and VCCA are within the recommended operating range. See [Detailed Design Procedure](#) for power supply recommendations.

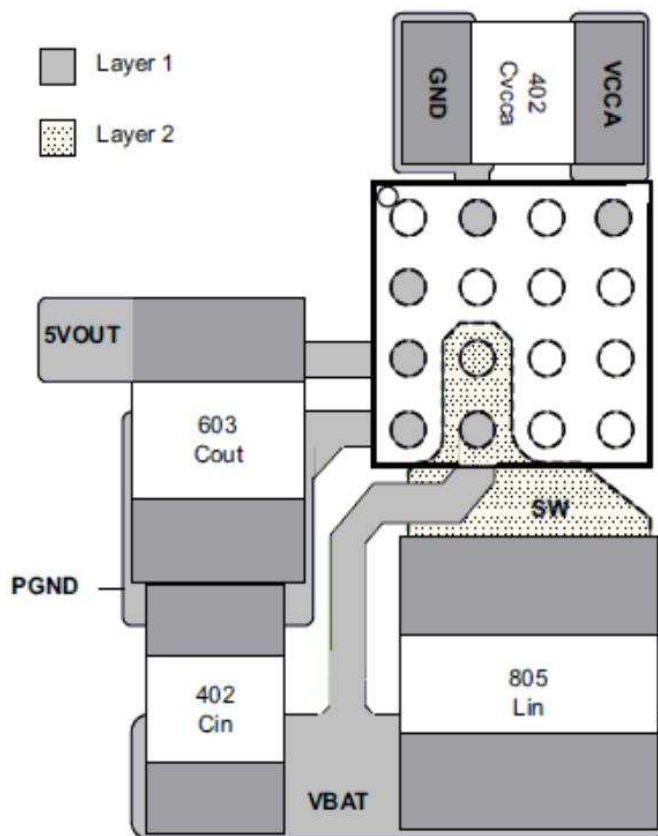
## 10 Layout

### 10.1 Layout Guidelines

For proper operation, follow these layout and design guidelines:

- Place the TPD5S115 as close to the connector as possible. This allows it to remove the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place power line capacitors and inductors close to the pins with wide traces to allow enough current to flow through with less trace parasitics. Ensure that there is enough metallization for the GND pad. A sufficient current path enables safe discharge of all the energy associated with the ESD strike.

### 10.2 Layout Example



**Figure 17. Board Layout With DC-DC Components (Top View)**

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- [Reading and Understanding an ESD Protection Datasheet](#)
- [ESD Layout Guide](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPD5S115YFFR</a>	Active	Production	DSBGA (YFF)   16	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RE115
TPD5S115YFFR.A	Active	Production	DSBGA (YFF)   16	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	RE115

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD5S115YFFR	DSBGA	YFF	16	3000	180.0	8.4	1.84	1.84	0.69	4.0	8.0	Q1



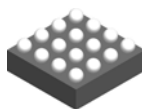
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD5S115YFFR	DSBGA	YFF	16	3000	182.0	182.0	20.0

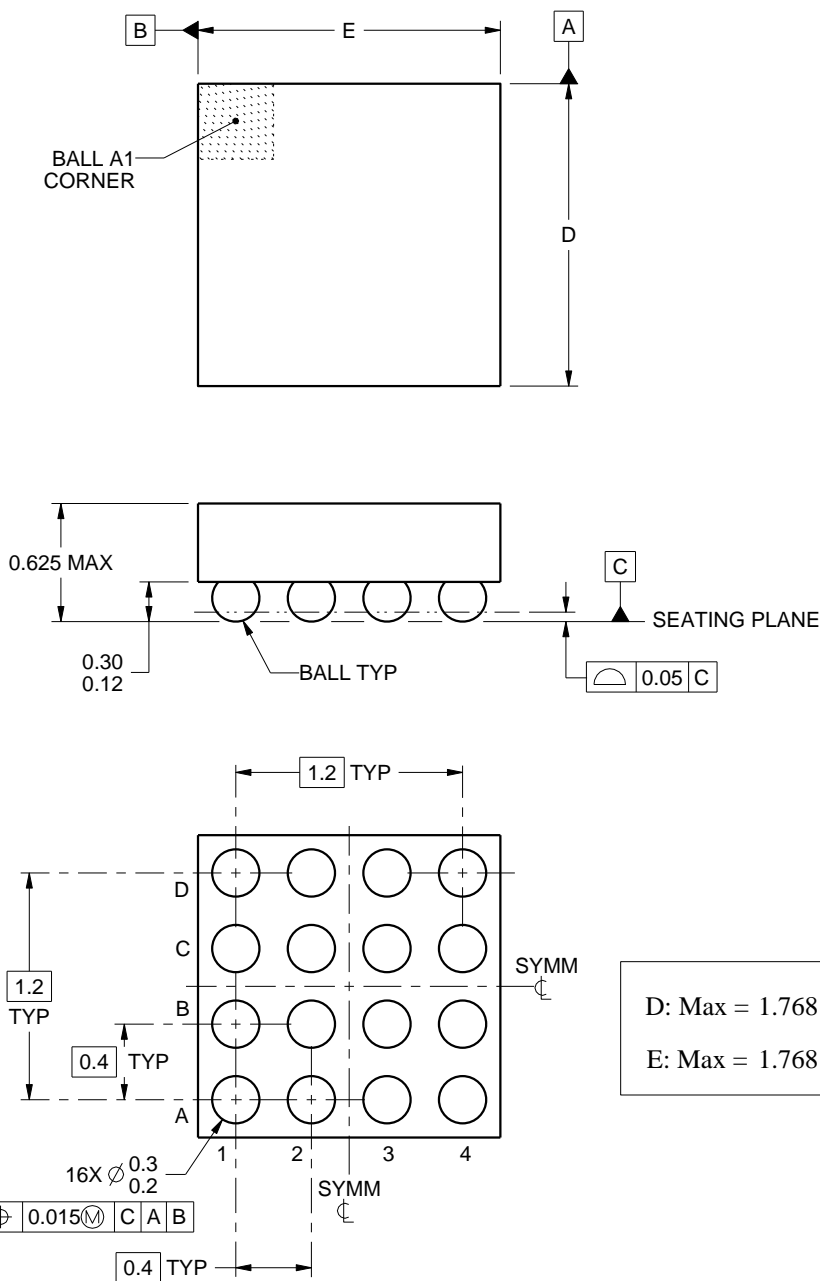
YFF0016



# PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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## NOTES:

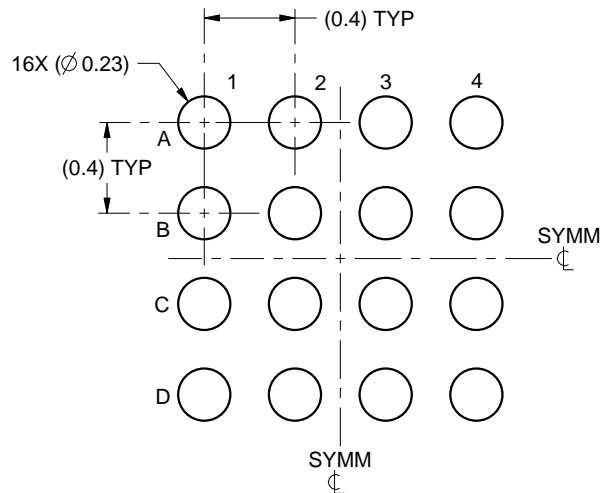
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

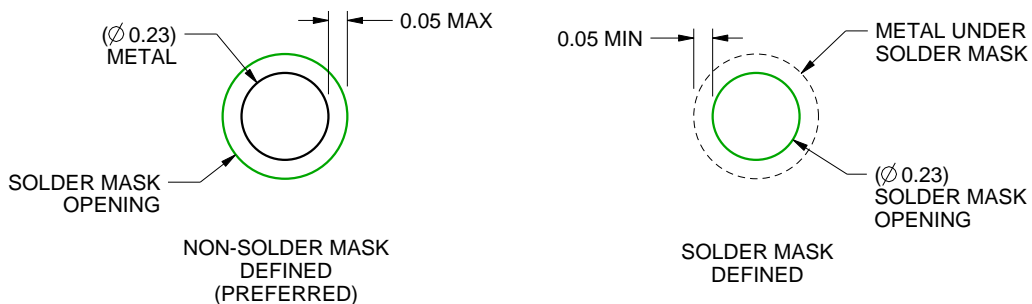
YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

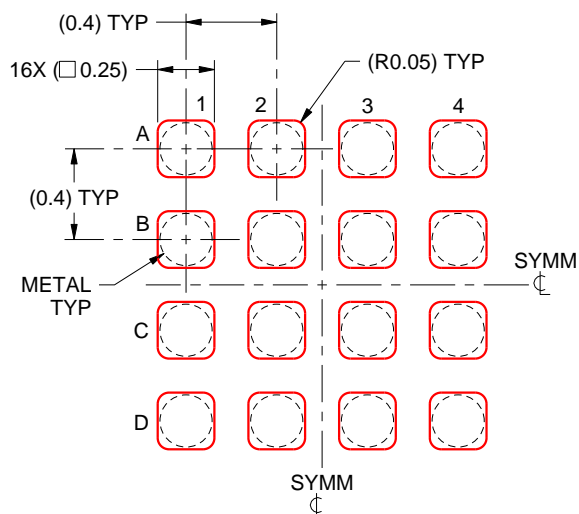
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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