

# TPD4S481-Q1 USB Type-C® 48V EPR Port Protector: Short-to-VBUS Overvoltage and IEC ESD Protection

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 2: -40°C to +105°C Ambient Operating Temperature Range
- 4-channels of short-to- $V_{BUS}$  overvoltage protection (CC1, CC2, SBU1, SBU2): 63V<sub>DC</sub> tolerant
- 4-channels of IEC 61000-4-2 ESD protection (CC1, CC2, SBU1, SBU2)
- CC1 and CC2 overvoltage protection FETs for passing  $V_{CONN}$  power
- ±65V surge protection on CC pins
- +65/-35V surge protection on SBU pins
- CC dead battery resistors integrated for handling dead battery use case
- 3.5mm x 3.5mm QFN package

## 2 Applications

- [Automotive USB charging](#)
- [Automotive media hub](#)
- [Automotive head unit](#)
- [Automotive display module](#)

## 3 Description

The TPD4S481-Q1 is a single-chip USB Type-C port protection device that provides 48V short-to- $V_{BUS}$  overvoltage and IEC ESD protection.

Since the release of the USB Type-C connector, many products and accessories for USB Type-C have been released that do not meet the USB Type-C specification. Another concern for USB Type-C is that mechanical twisting and sliding of the connector shorting pins due to the pins close proximity in the small connector. This mechanical twisting and sliding can cause 48V  $V_{BUS}$  to be shorted to the CC and SBU pins. Also due to the proximity of the pins in the Type-C connector, there is a heightened concern that debris and moisture will cause the 48V  $V_{BUS}$  pin to be shorted to the CC, SBU, or USB2 pins.

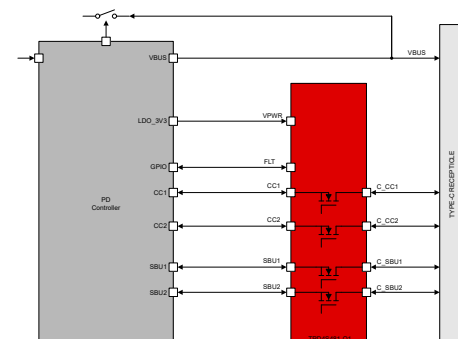
These mechanical events and non-ideal equipment make it necessary for the CC and other pins to be 48V tolerant, even though the pins only operate at 5V or lower. The TPD4S481-Q1 enables the CC and SBU or USB2 pins to be 48V tolerant without interfering with normal operation by providing overvoltage protection on the CC and SBU pins. The device places high voltage FETs in series on the SBU and CC lines. For systems not utilizing alternate modes with SBU communication, use the SBU pins of the TPD4S481-Q1 to protect the USB2 data lines instead. When a voltage above the OVP threshold is detected on these lines, the high voltage switches are opened up, isolating the rest of the system from the high voltage condition present on the connector.

Finally, most systems require IEC 61000-4-2 system level ESD protection for external pins. The TPD4S481-Q1 integrates IEC 61000-4-2 ESD protection for the CC1, CC2, SBU1, and SBU2 pins, eliminating the need to place high voltage TVS diodes externally on the connector.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
TPD4S481-Q1	RGR (VQFN, 20)	3.5mm x 3.5mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



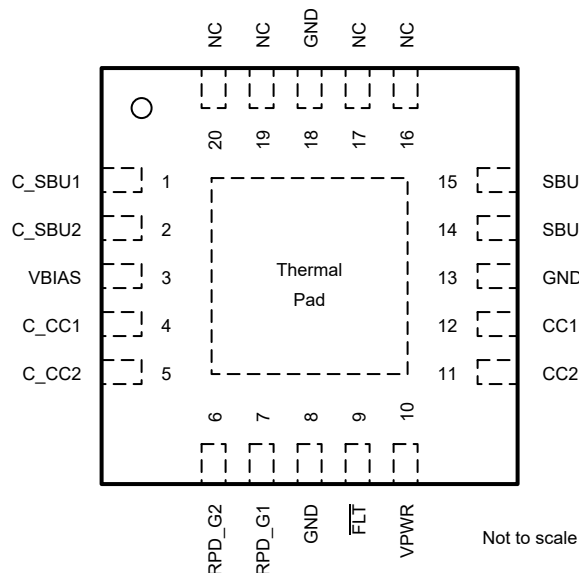
**CC and SBU Overvoltage Protection**



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## 4 Pin Configuration and Functions



**Figure 4-1. TPD4S481-Q1 RGR Package, 20-Pin QFN**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
12	CC1	I/O	System side of the CC1 OVP FET. Connect to either CC pin of the CC/PD controller.
11	CC2	I/O	System side of the CC2 OVP FET. Connect to either CC pin of the CC/PD controller.
4	C_CC1	I/O	Connector side of the CC1 OVP FET. Connect to either CC pin of the USB Type-C connector.
5	C_CC2	I/O	Connector side of the CC2 OVP FET. Connect to either CC pin of the USB Type-C connector.
1	C_SBU1	I/O	Connector side of the SBU1 OVP FET. Connect to either SBU pin of the USB Type-C connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins.
2	C_SBU2	I/O	Connector side of the SBU2 OVP FET. Connect to either SBU pin of the USB Type-C connector. Alternatively, connect to either USB2.0 pin of the USB Type-C connector to protect the USB2.0 pins instead of the SBU pins.
15	SBU1	I/O	System side of the SBU1 OVP FET. Connect to either SBU pin of the SBU MUX. Alternatively, connect to either USB2.0 pin of the USB2.0 Phy when protecting the USB2.0 pins instead of protecting the SBU pins.
14	SBU2	I/O	System side of the SBU2 OVP FET. Connect to either SBU pin of the SBU MUX. Alternatively, connect to either USB2.0 pin of the USB2.0 Phy when protecting the USB2.0 pins instead of protecting the SBU pins.
7	RPD_G1	I/O	Short to C_CC1 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
6	RPD_G2	I/O	Short to C_CC2 if dead battery resistors are needed. If dead battery resistors are not needed, short pin to GND.
9	FLT	O	Open drain for fault reporting.
8, 13, 18	GND	GND	Ground
3	VBIAS	P	Pin for ESD support capacitor. Place a 0.1µF capacitor on this pin to ground.
10	VPWR	P	2.7V to 4.5V power supply.
20	NC	-	No Connect, may be left floating or grounded

**Table 4-1. Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
19	NC	-	No Connect, may be left floating or grounded
16	NC	-	No Connect, may be left floating or grounded
17	NC	-	No Connect, may be left floating or grounded
-	Thermal Pad	GND	Internally connected to GND. Used as a heatsink. Connect to the PCB GND plane

(1) I = input, O = output, I/O = input and output, GND = ground, P = power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>I</sub>	Input voltage	VPWR	-0.3	5	V
		RPD_G1, RPD_G2, VBUS	-0.3	63	V
V <sub>O</sub>	Output voltage	FLT	-0.3	6	V
		VBIAS	-0.3	63	V
V <sub>IO</sub>	I/O voltage	CC1, CC2, SBU1, SBU2	-0.3	6	V
		C_CC1, C_CC2, C_SBU1, C_SBU2	-0.3	63	V
t <sub>rise</sub>	Input voltage rise time (V <sub>I</sub> > 36V)	CC1, CC2, SBU1, SBU2	400		ns
T <sub>J</sub>	Operating junction temperature		-40	125	°C
T <sub>stg</sub>	Storage temperature		-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 5.2 ESD Ratings—JEDEC Specification

				VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
V <sub>(ESD)</sub>	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101	Charged-device model (CDM), per JEDEC specification JESD22-C101	±500	V

### 5.3 ESD Ratings—IEC Specification

				VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2, C_CC1, C_CC2	Contact discharge	±8000	V
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2, C_CC1, C_CC2	Air-gap discharge	±15000	V
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2, C_SBU1, C_SBU2	Contact discharge	±8000	V
V <sub>(ESD)</sub>	Electrostatic discharge	IEC 61000-4-2, C_SBU1, C_SBU2	Air-gap discharge	±15000	V
V <sub>(Surge)</sub>	Lightning and Surge	IEC 61000-4-5, C_CC1, C_CC2	IEC 61000-4-5, C_CC1, C_CC2	±65	V
V <sub>(Surge)</sub>	Lightning and Surge	IEC 61000-4-5, C_SBU1, C_SBU2	IEC 61000-4-5, C_SBU1, C_SBU2	+65/-35	V

### 5.4 ESD Ratings—ISO Specification

				VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	ISO 10605 330 pF, 330 Ω, C_CC1, C_CC2	Contact discharge	±8000	V
V <sub>(ESD)</sub>	Electrostatic discharge	ISO 10605 330 pF, 330 Ω, C_CC1, C_CC2	Air-gap discharge	±15000	V
V <sub>(ESD)</sub>	Electrostatic discharge	ISO 10605 330 pF, 330 Ω, C_SBU1, C_SBU2	Contact discharge	±8000	V
V <sub>(ESD)</sub>	Electrostatic discharge	ISO 10605 330 pF, 330 Ω, C_SBU1, C_SBU2	Air-gap discharge	±15000	V

### 5.5 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V <sub>I</sub>	Input voltage	VPWR	2.7	3.3	4.5	V

## 5.5 Recommended Operating Conditions (continued)

			MIN	NOM	MAX	UNIT
V <sub>I</sub>	Input voltage	RPD_G1, RPD_G2	0		5.5	V
V <sub>I</sub>	Input voltage	VBUS	0		51	V
V <sub>O</sub>	Output voltage	FLT Pull-up resistor power rail	2.7		5.5	V
V <sub>IO</sub>	I/O voltage	CC1, CC2, C_CC1, C_CC2	0		5.5	V
		SBU1, SBU2, C_SBU1, C_SBU2	0		4.3	V
I <sub>VCONN</sub>	V <sub>CONN</sub> Current	Current flowing into CC1/2 and flowing out of C_CC1/2, T <sub>J</sub> ≤ 105 °C			600	mA
I <sub>VCONN</sub>	V <sub>CONN</sub> Current	Current flowing into CC1/2 and flowing out of C_CC1/2, T <sub>J</sub> ≤ 85 °C			1.25	A
T <sub>J</sub>	Operating Junction Temperature		-40		125	°C
External Components <sup>(1)</sup>	External Components <sup>(1)</sup>	FLT Pull-up resistance			300	kΩ
		VBIAS capacitance <sup>(2)</sup>	0.04	0.1		μF
		VPWR Capacitance	0.3	1		μF
		VBUS_LV Capacitance		0.1		μF

- (1) For recommended values for capacitors and resistors, the typical values assume a component placed on the board near the pin. Minimum and maximum values listed are inclusive of manufacturing tolerances, voltage derating, board capacitance, and temperature variation. The effective value presented should be within the minimum and maximums listed in the table.
- (2) The VBIAS pin requires a minimum 63-VDC rated capacitor. A 100-VDC rated capacitor is recommended to reduce capacitance derating.  
See the VBIAS Capacitor Selection section for more information on selecting the VBIAS capacitor.

## 5.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DEVICE	UNIT
		QFN	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	43.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	43.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	18.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	19.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	5.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.7 Electrical Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CC OVP Switches</b>					
R <sub>ON</sub>	On Resistance of CC OVP FETs	CCx = 5.5V, T <sub>J</sub> ≤ 85 °C		272	420 mΩ
C <sub>ON_CC</sub>	Equivalent on Capacitance	Capacitance from CCx or C_CCx to GND when device is powered. Measure at V <sub>C_CCx</sub> /V <sub>CCx</sub> = 0V to 1.2V, f = 400kHz.		40	74 120 pF
RD_DB	Dead Battery Pull-Down Resistors (only present when device is unpowered)	V <sub>C_CCx</sub> = 2.6V		4.1	5.1 6.1 kΩ
V <sub>TH_DB</sub>	Threshold voltage of the pull-down FET in series with RD during dead battery	I <sub>C_CCx</sub> = 80μA		0.5	0.9 1.2 V
V <sub>OVPCC</sub>	OVP Threshold on CC Pins	Place 5.5V on C_CCx. Step up C_CCx until FLT pin is asserted. Put 100mA load through the CC FET and see the FET shuts off.		5.6	5.9 6.2 V

## 5.7 Electrical Characteristics (continued)

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OVPCC_HYS</sub>	Hysteresis on CC OVP Place 6.5 V on C <sub>CCx</sub> . Step down the voltage on C <sub>CCx</sub> until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C <sub>CCx</sub> .		50		mV
BW <sub>ON</sub>	On Bandwidth Single Ended (-3dB) Measure the -3 dB bandwidth from C <sub>CCx</sub> to CCx. Single ended measurement, 50-Ω system. V <sub>cm</sub> = 0.1V to 1.2 V.		125		MHz
V <sub>STBUS_CC</sub>	Short-to-VBUS tolerance on the CC pins Hot-Plug C <sub>CCx</sub> with a 1 meter USB Type C Cable, place a 30-Ω load on CCx			51	V
V <sub>STBUS_CC_CLAMP</sub>	Short-to-VBUS System-Side Clamping Voltage on the CC pins (CCx) Hot-Plug C <sub>CCx</sub> with a 1 meter USB Type C Cable. Hot-Plug voltage C <sub>CCx</sub> = 51 V. VPWR = 3.3 V. Place a 30-Ω load on CCx.		7		V
<b>SBU OVP Switches</b>					
R <sub>ON</sub>	On Resistance of SBU OVP FETs SBUx = 3.6 V. -40°C ≤ T <sub>J</sub> ≤ +85°C		4	6.8	Ω
C <sub>ON_SBU</sub>	Equivalent on Capacitance Capacitance from SBUx or C <sub>SBUx</sub> to GND when device is powered. Measure at V <sub>C_SBUx</sub> /V <sub>SBUx</sub> = 0.3V to 4.0V.		6		pF
V <sub>OVP_SBU</sub>	OVP Threshold on SBU Pins Place 3.6V on C <sub>SBUx</sub> . Step up C <sub>SBUx</sub> until FLT pin is asserted.	4.0	4.2	4.41	V
V <sub>OVP_SBU_HYS</sub>	Hysteresis on SBU OVP Place 5 V on C <sub>CCx</sub> . Step down the voltage on C <sub>CCx</sub> until the FLT pin is deasserted. Measure difference between rising and falling OVP threshold for C <sub>SBUx</sub> .		50		mV
BW <sub>ON</sub>	On Bandwidth Single Ended (-3dB) Measure the -3 dB bandwidth from C <sub>SBUx</sub> to SBUx. Single ended measurement, 50Ω system. V <sub>cm</sub> = 0.1V to 3.6V.	600	760		MHz
X <sub>TALK</sub>	Crosstalk Measure crosstalk at f = 1 MHz from SBU1 to C <sub>SBU2</sub> or SBU2 to C <sub>SBU1</sub> . V <sub>cm1</sub> = 3.6 V, V <sub>cm2</sub> = 0.3 V. Terminate open sides to 50Ω.		-70		dB
V <sub>STBUS_SBU</sub>	Short-to-VBUS tolerance on the SBU pins Hot-Plug C <sub>SBUx</sub> with a 1 meter USB Type C Cable. Put a 100-nF capacitor in series with a 40-Ω resistor to GND on SBUx.			51	V
V <sub>STBUS_SBU_CLAMP</sub>	Short-to-VBUS System-Side Clamping Voltage on the SBU pins (SBUx) Hot-Plug C <sub>SBUx</sub> with a 1 meter USB Type C Cable. Hot-Plug voltage C <sub>SBUx</sub> = 51V. VPWR = 3.3 V. Put a 150-nF capacitor in series with a 40-Ω resistor to GND on SBUx.		7		V
<b>Power Supply and Leakage Currents</b>					
V <sub>PWR_UVLO</sub>	V <sub>PWR</sub> Undervoltage Lockout Place 1 V on VPWR and raise voltage until SBU or CC FETs turn-on.	2.1	2.3	2.6	V
V <sub>PWR_UVLO_HYS</sub>	V <sub>PWR</sub> UVLO Hysteresis Place 3 V on VPWR and lower voltage until SBU or CC FETs turnoff; measure difference between rising and falling UVLO to calculate hysteresis.	70	100	130	mV
I <sub>VPWR</sub>	V <sub>PWR</sub> supply current VPWR = 3.3 V (typical), VPWR = 4.5 V (maximum). -40°C ≤ T <sub>J</sub> ≤ +85°C.		112	160	μA
I <sub>C_CC_LEAK</sub>	Leakage current for C <sub>CCx</sub> pins when device is powered VPWR = 3.3 V, V <sub>C_CCx</sub> = 3.6 V, CCx pins are floating, measure leakage current into C <sub>CCx</sub> pins.			5	μA
I <sub>C_SBU_LEAK</sub>	Leakage current for C <sub>SBUx</sub> pins when device is powered VPWR = 3.3 V, V <sub>C_SBUx</sub> = 3.6 V, SBUx pins are floating, measure leakage current into C <sub>SBUx</sub> pins. Result should be same if SBUx side is biased and C <sub>SBUx</sub> is left floating. -40°C ≤ T <sub>J</sub> ≤ +85°C			3.2	μA

## 5.7 Electrical Characteristics (continued)

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC_LEAK_OVP</sub>	Leakage current for C <sub>CCx</sub> pins when device is in OVP	VPWR = 0 V or 3.3 V, V <sub>C_CCx</sub> = 51 V, CCx pins are set to 0 V, measure leakage current into C <sub>CCx</sub> pins.			1200	μA
I <sub>C_SBU_LEAK_OVP</sub>	Leakage current for C <sub>SBUx</sub> pins when device is in OVP	VPWR = 0 V or 3.3 V, V <sub>C_SBUx</sub> = 51 V, SBUx pins are set to 0 V, measure leakage current into C <sub>SBUx</sub> pins.			720	μA
I <sub>CC_LEAK_OVP</sub>	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, V <sub>C_CCx</sub> = 51 V, CCx pins are set to 0 V, measure leakage current out of CCx pins.			30	μA
I <sub>SBU_LEAK_OVP</sub>	Leakage current for SBU pins when device is in OVP	VPWR = 0 V, V <sub>C_SBUx</sub> = 51 V, SBUx pins are set to 0 V, measure leakage current into SBUx pins.	-1		1	μA
/FLT Pin						
V <sub>OL</sub>	Low-level output voltage	IOL = 3mA. Measure voltage at $\overline{\text{FLT}}$ pin.			0.4	V
Over Temperature Protection						
T <sub>SD_RISING</sub>	The rising over-temperature protection shutdown threshold		150	175		°C
T <sub>SD_FALLING</sub>	The falling over-temperature protection shutdown threshold		130	140		°C
T <sub>SD_HYST</sub>	The over-temperature protection shutdown threshold hysteresis			35		°C

## 5.8 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>Power-On and Off Timings</b>					
$t_{ON\_FET}$	Time from Crossing Rising VPWR UVLO until CC and SBU OVP FETs are on.		1.3	3.5	ms
$t_{ON\_FET\_DB}$	Time from Crossing Rising VPWR UVLO until CC and SBU OVP FETs are on and the dead battery resistors are off.		5.7	9.5	ms
$dV_{PWR\_OFF}/dt$	Minimum slew rate allowed to specify CC and FETs turn off during a power off.	-0.5			V/ $\mu s$
<b>Overvoltage Protection</b>					
$t_{OVP\_RESPONSE\_CC}$	OVP response time on the CCx pins. Time from OVP asserted until OVP FETs turn off.		70		ns
$t_{OVP\_RESPONSE\_SBU}$	OVP response time on the SBUx pins. Time from OVP asserted until OVP FETs turn off.		80		ns
$t_{OVP\_RECOVERY\_CC}$	OVP recovery time on the CCx pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on. Remove OVP for CC FETs to turn back on.		0.93	2.3	ms
$t_{OVP\_RECOVERY\_CC\_DB}$	OVP recovery time on the CCx pins. Once an OVP has occurred, the minimum time duration until the CC FETs turn back on and the dead battery resistors turn off. Remove OVP for CC FETs to turn back on.		5		ms
$t_{OVP\_RECOVERY\_SBU}$	OVP recovery time on the SBUx pins. Once an OVP has occurred, the minimum time duration until the SBU FETs turn back on. Remove OVP for SBU FETs to turn back on.		0.62		ms
$t_{OVP\_FLT\_ASSERTION}$	Time from OVP Asserted to /FLT assertion. FLT assertion is 10% of the maximum value. Set C_CCx or C_SBUx above the maximum OVP threshold. Start the time where it passes the typical OVP threshold value.		20		$\mu s$
$t_{OVP\_FLT\_DEASSERTION}$	Time from CC FET turn on after an OVP to FLT deassertion.		5		ms



## 5.9 Typical Characteristics

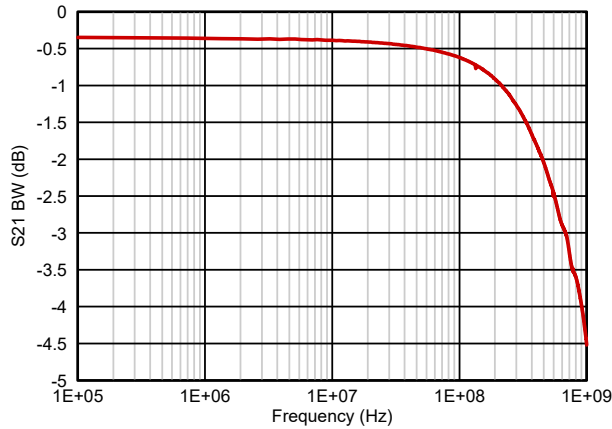


Figure 5-1. SBU Bandwidth

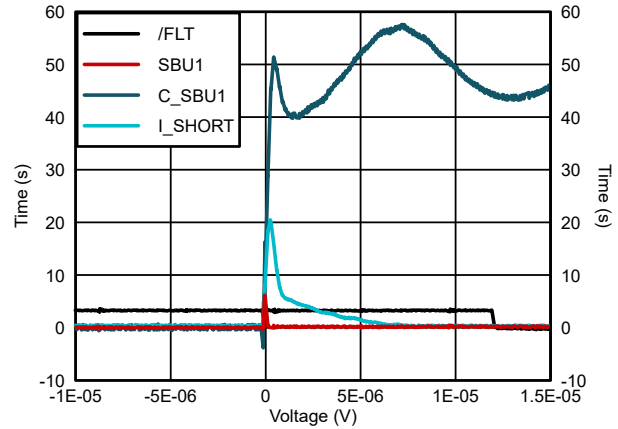


Figure 5-2. SBU Short-to- $V_{BUS}$  48V

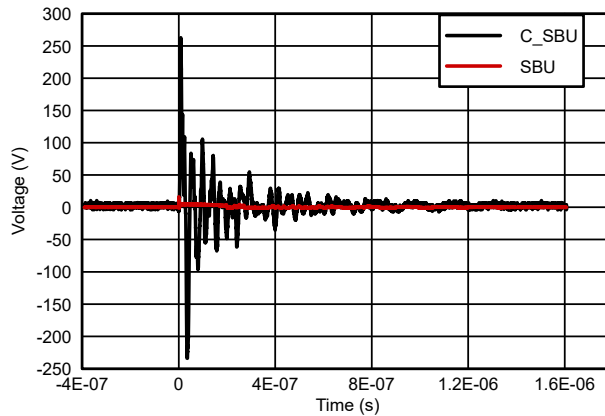


Figure 5-3. SBU IEC 61000-4-2 4kV Response Waveform

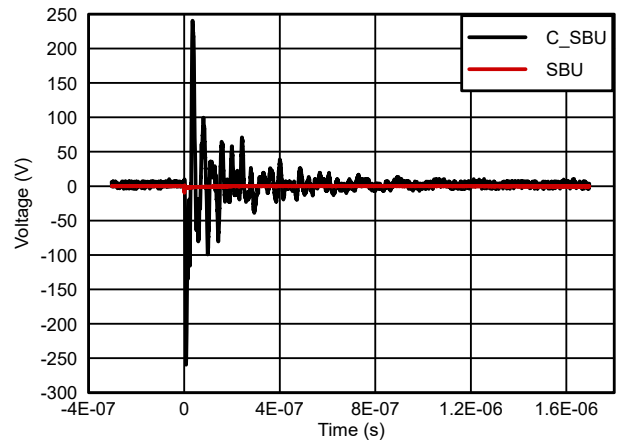


Figure 5-4. SBU IEC 61000-4-2 -4kV Response Waveform

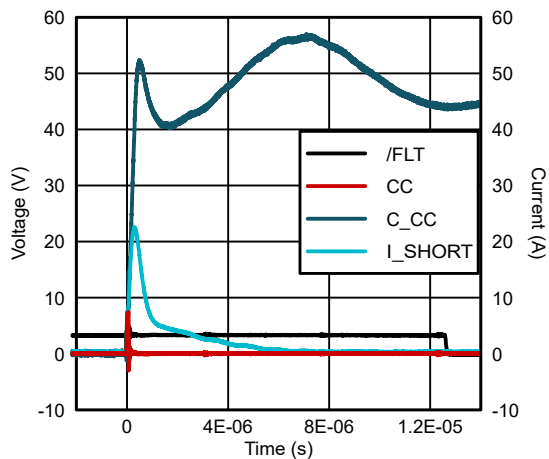


Figure 5-5. CC Short-to- $V_{BUS}$  48V

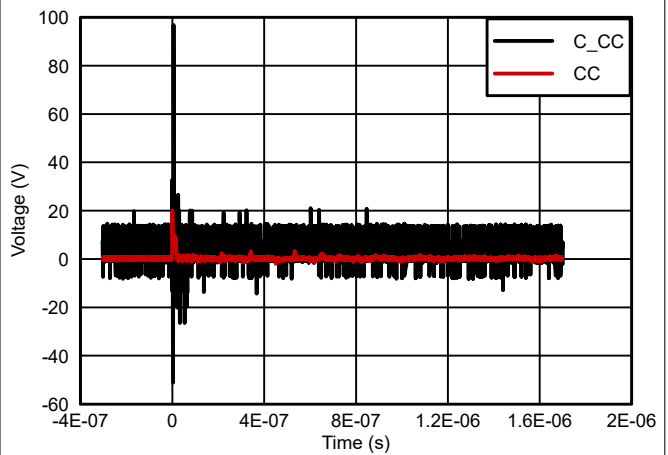


Figure 5-6. CC IEC 61000-4-2 8kV Response Waveform

## 5.9 Typical Characteristics (continued)

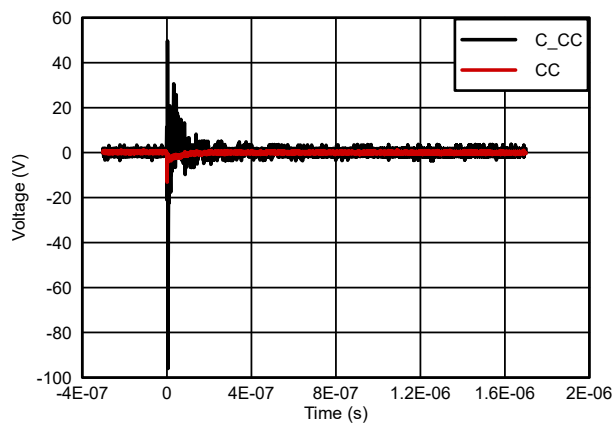


Figure 5-7. CC IEC 61000-4-2 -8kV Response Waveform

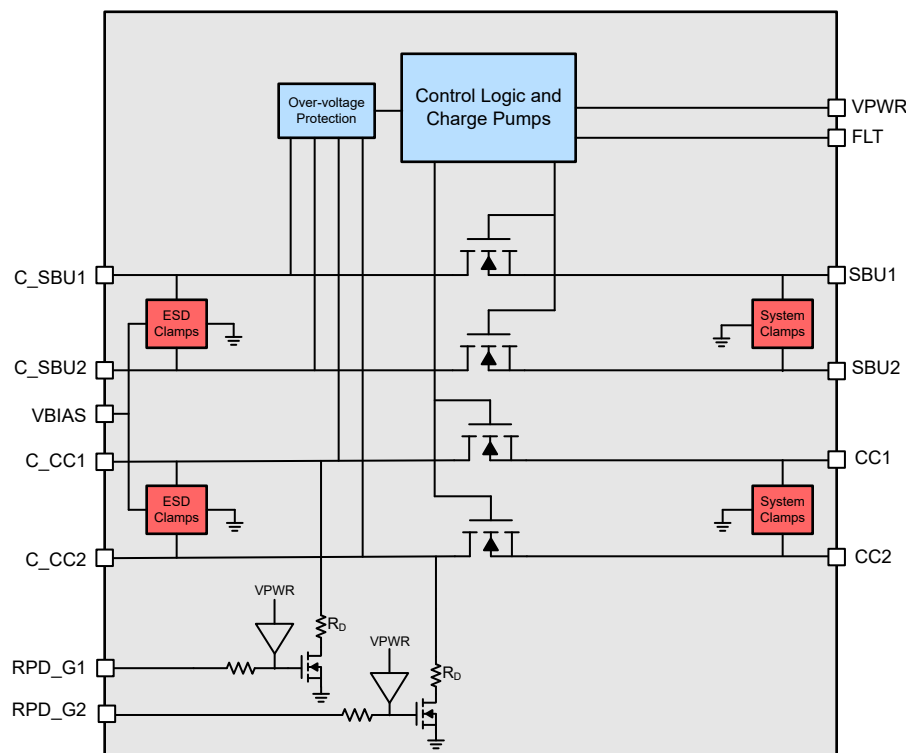
## 6 Detailed Description

### 6.1 Overview

The TPD4S481-Q1 is a single chip USB Type-C port protector that provides 48V short-to- $V_{BUS}$  overvoltage and ESD protection. The  $V_{BUS}$  pins short to the CC and SBU pins inside the USB Type-C connector due to the small pin pitch of the USB Type-C connector and non-compliant USB Type-C cables and accessories. Because of this short-to- $V_{BUS}$  event, the CC and SBU pins need to be 48V tolerant, to support protection on the full USB PD-EPR voltage range. The TPD4S481-Q1 integrates four channels of 48V short-to- $V_{BUS}$  overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector.

Additionally, IEC 61000-4-2 system level ESD protection is required to protect a USB Type-C port from ESD strikes generated by end product users. The TPD4S481-Q1 integrates four channels of IEC61000-4-2 ESD protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector, all of the low-speed pins on the USB Type-C connector. Additionally, high-voltage ESD protection that is 55V DC tolerant is required for the CC and SBU lines to simultaneously support ESD and short-to- $V_{BUS}$  protection. The TPD4S481-Q1 integrates a high-voltage ESD diode designed to work in conjunction with the overvoltage protection FETs inside the device.

### 6.2 Functional Block Diagram



### 6.3 Feature Description

#### 6.3.1 4-Channels of Short-to- $V_{BUS}$ Overvoltage Protection (CC1, CC2, SBU1, SBU2 Pins or CC1, CC2, DP, DM Pins): 63V<sub>DC</sub> Tolerant

The TPD4S481-Q1 provides 4-channels of short-to- $V_{BUS}$  Overvoltage Protection for the CC1, CC2, SBU1, and SBU2 pins (or the CC1, CC2, DP, and DM pins) of the USB Type-C connector. The TPD4S481-Q1 is able to handle 63V<sub>DC</sub> on its C\_CC1, C\_CC2, C\_SBU1, and C\_SBU2 pins. This level of protection is necessary because according to the USB PD specification, with  $V_{BUS}$  set for 48-V operation, the  $V_{BUS}$  voltage is allowed to legally swing up to 50.4V and 50.9V on voltage transitions from a different USB PD  $V_{BUS}$  voltage. To support possible ringing during a short event, the TPD4S481-Q1 builds in tolerance up to 63V<sub>BUS</sub> to provide margin above this 50.9V specification.

When a short-to- $V_{BUS}$  event occurs, ringing happens due to the RLC elements in the hot-plug event. Ringing up to twice the settling voltage appears on the connector if the resistance is low in the RLC circuit. Ringing of more than twice the DC level is generated if any capacitor on the line derates in capacitance value during the short-to- $V_{BUS}$  event. This behavior means that more than 90V is seen on a USB Type-C pin during a short-to- $V_{BUS}$  event. The TPD4S481-Q1 has built in circuit protection to handle this ringing. The diode clamps used for IEC ESD protection also clamp the ringing voltage during the short-to- $V_{BUS}$  event to limit the peak ringing to approximately 53V. Additionally, the overvoltage protection FETs integrated inside the TPD4S481-Q1 are 63V tolerant, therefore being capable of supporting the high-voltage ringing waveform that is experienced during the short-to- $V_{BUS}$  event. The TPD4S481-Q1 handles short-to- $V_{BUS}$  hot-plug events with hot-plug voltages as high as  $51V_{DC}$  because of the well-designed combination of voltage clamps and 63V tolerant OVP FETs.

The TPD4S481-Q1 has an extremely fast turnoff time of 70ns typical. Furthermore, additional voltage clamps are placed after the OVP FET on the system side (CC1, CC2, SBU1, SBU2) pins of the TPD4S481-Q1, to further limit the voltage and current that are exposed to the USB Type-C CC/PD controller during the 70ns interval while the OVP FET is turning off. The combination of connector side voltage clamps, OVP FETs with extremely fast turnoff time, and system side voltage clamps all work together to enable the level of stress seen on a CC1, CC2, SBU1, or SBU2 pin during a short-to- $V_{BUS}$  event to be less than or equal to an HBM event.

The SBU OVP FETs are designed to be able to optionally protect the DP, DM (USB2.0) pins in lieu of the SBU pins. Some systems designers also prefer to protect the DP, DM pins from short-to- $V_{BUS}$  events due to the potential for moisture/water in the connector to short the  $V_{BUS}$  pins to DP, DM pins. This protection is applicable in cases where the end equipment with a USB Type-C connector is trying to be made water-proof. If desiring to protect the DP, DM pins on the USB Type-C connector from a short-to- $V_{BUS}$  event, connect the C\_SBUx pins to the DP, DM pins on the USB Type-C connector, and the SBUx pins to the USB2.0 pins of the system device being protected from the short-to- $V_{BUS}$  event.

#### **6.3.2 4-Channels of IEC 61000-4-2 ESD Protection (CC1, CC2, SBU1, SBU2 Pins)**

The TPD4S481-Q1 integrates 4-Channels of IEC 61000-4-2 system level ESD protection for the CC1, CC2, SBU1, and SBU2 pins. USB Type-C ports on end-products need system level IEC ESD protection in order to provide adequate protection for the ESD events that the connector can be exposed to from end users. The TPD4S481-Q1 integrates IEC ESD protection for all of the low-speed pins on the USB Type-C connector in a single chip. Also note, that while the RPD\_Gx pins are not individually rated for IEC ESD, when they are shorted to the C\_CCx pins, the C\_CCx pins provide protection for both the C\_CCx pins and the RPD\_Gx pins. Additionally, high-voltage IEC ESD protection that is 63V DC tolerant is required for the CC and SBU lines in order to simultaneously support IEC ESD and Short-to- $V_{BUS}$  protection; there are not many discrete market solutions that can provide this kind of protection. The TPD4S481-Q1 integrates this type of high-voltage ESD protection so a system designer can meet both IEC ESD and Short-to- $V_{BUS}$  protection requirements in a single device.

#### **6.3.3 CC1, CC2 Overvoltage Protection FETs 600-mA Capable for Passing VCONN Power**

The CC pins on the USB Type-C connector serve many functions; one of the functions is to be a provider of power to active cables. Active cables are required when desiring to pass greater than 3 A of current on the  $V_{BUS}$  line or when the USB Type-C port uses the super-speed lines (TX1+, TX2-, RX1+, RX1-, TX2+, TX2-, RX2+, RX2-). When CC is configured to provide power, it is called VCONN. VCONN is a DC voltage source in the range of 3V to 5.5V. If supporting VCONN, enable the VCONN provider to have the capability to provide 1.5 W of power to a cable; this translates into a current range of 273mA to 500mA (depending on the VCONN voltage level).

When a USB Type-C port is configured for VCONN and using the TPD4S481-Q1, this VCONN current flows through the OVP FETs of the TPD4S481-Q1. Therefore, the TPD4S481-Q1 has been designed to handle these currents and have an RON low enough to provide a specification compliant VCONN voltage to the active cable.

### 6.3.4 CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices

An important feature of USB Type-C and USB PD is the ability for this connector to serve as the sole power source to mobile devices. With support up to 240W, the USB Type-C connector supporting USB PD powers a whole new range of mobile devices not previously possible with legacy USB connectors.

When the USB Type-C connector is the sole power supply for a battery powered device, enable the device to charge from the USB Type-C connector even when its battery is dead. In order for a USB Type-C power adapter to supply power on  $V_{BUS}$ , expose RD pulldown resistors on the CC pins. These RD resistors are typically included inside a USB Type-C CC/PD controller. However, when the TPD4S481-Q1 is used to protect the USB Type-C port, the OVP FETs inside the device isolate these RD resistors in the CC/PD controller when the mobile device has no power. When the TPD4S481-Q1 has no power, the OVP FETs are turned off to provide overvoltage protection in a dead battery condition. Therefore, the TPD4S481-Q1 integrates high-voltage, dead battery RD pull-down resistors to allow dead battery charging simultaneously with high-voltage OVP protection.

If dead battery support is required, short the RPD\_G1 pin to the C\_CC1 pin, and short the RPD\_G2 pin to the C\_CC2 pin. This short connects the dead battery resistors to the connector CC pins. When the TPD4S481-Q1 is unpowered, and the RP pull-up resistor is connected from a power adapter, this RP pull-up resistor activates the RD resistor inside the TPD4S481-Q1, and enables  $V_{BUS}$  to be applied from the power adapter even in a dead battery condition. Once power is restored back to the system and back to the TPD4S481-Q1 on its VPWR pin, the TPD4S481-Q1 turns ON its OVP FETs in 3.5ms and then turns OFF its dead battery RD. The TPD4S481-Q1 first turns ON its CC OVP FETs fully, and then removes its dead battery RDs to make sure the PD controller RD is fully exposed before removing the RD of the TPD4S481-Q1.

If desiring to power the CC/PD controller during dead battery mode and if the CC/PD Controller is configured as a DRP, it is critical that the TPD4S481-Q1 be powered before or at the same time that the CC/PD controller is powered. It is also critical that when unpowered, the CC/PD controller also expose its dead battery resistors. When the TPD4S481-Q1 gets powered, it exposes the CC pins of the CC/PD controller within 3.5ms, and then removes its own RD dead battery resistors. Once the TPD4S481-Q1 turns on, present the RD pull-down resistors of the CC/PD controller immediately in order to maintain a connection. If the power adapter does not see RD present, the  $V_{BUS}$  disconnects. This event removes power from the device with its battery still not sufficiently charged, which consequently removes power from the CC/PD controller and the TPD4S481-Q1. Then the RD resistors of the TPD4S481-Q1 are exposed again, and connects the  $V_{BUS}$  of the power adapter to start the cycle over.

If the CC/PD Controller is configured for DRP and has started to DRP toggle before the TPD4S481-Q1 turns on, this DRP toggle is unable to maintain a connection with a power adapter. If the CC/PD controller is configured for DRP, the dead battery resistors of the PD controller need to be exposed as well, and that the resistors remain exposed until the TPD4S481-Q1 turns on. This behavior is typically accomplished by powering the TPD4S481-Q1 at the same time as the CC/PD controller when powering the CC/PD controller in dead battery operation.

If dead battery charging is not required in your application, connect the RPD\_G1 and RPD\_G2 pins to ground.

## 6.4 Device Functional Modes

[Table 6-1](#) describes all of the functional modes for the TPD4S481-Q1. The "X" in the below table are "don't care" conditions, meaning the value present maintains functional mode and is within the absolute maximum ratings of the data sheet.

**Table 6-1. Device Mode Table**

Device Mode Table		Inputs					Outputs		
MODE		VPWR	C_CCx	C_SBUx	RPD_Gx	T <sub>J</sub>	FLT	CC FETs	SBU FETs
<b>Normal Operating Conditions</b>	Unpowered, no dead battery support	<UVLO	X	X	Grounded	X	High-Z	OFF	OFF
	Unpowered, dead battery support	<UVLO	X	X	Shorted to C_CCx	X	High-Z	OFF	OFF
	Powered on, SPR mode	>UVLO	<OVP	<OVP	X, forced OFF	<TSD	High-Z	ON	ON
	Powered on, EPR mode	>UVLO	<OVP	<OVP	X, forced OFF	<TSD	High-Z	ON	ON
<b>Fault Conditions</b>	Thermal shutdown	>UVLO	X	X	X, forced OFF	>TSD	Low (Fault Asserted)	OFF	OFF
	CC overvoltage condition	>UVLO	>OVP	X	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF
	SBU overvoltage condition	>UVLO	X	>OVP	X, forced OFF	<TSD	Low (Fault Asserted)	OFF	OFF
	IEC ESD generated overvoltage condition <sup>(1)</sup> (1)	>UVLO	X	X	R <sub>D</sub> ON if RPD_Gx is shorted to C_CCx	<TSD	Low (Fault Asserted)	OFF	OFF

- (1) This row describes the state of the device while still in OVP after the IEC ESD strike which put the device into OVP is over, and the voltages on the C\_CCx and C\_SBUx pins have returned to their normal voltage levels.

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

The TPD4S481-Q1 provides 4-channels of short-to- $V_{BUS}$  overvoltage protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector, and 4-channels of IEC ESD protection for the CC1, CC2, SBU1, and SBU2 pins of the USB Type-C connector. The TPD4S481-Q1 provides adequate system protection as well as ensuring that proper system operation is maintained. The following application example explains how to properly design the TPD4S481-Q1 into a USB Type-C system.

### 7.2 Typical Application

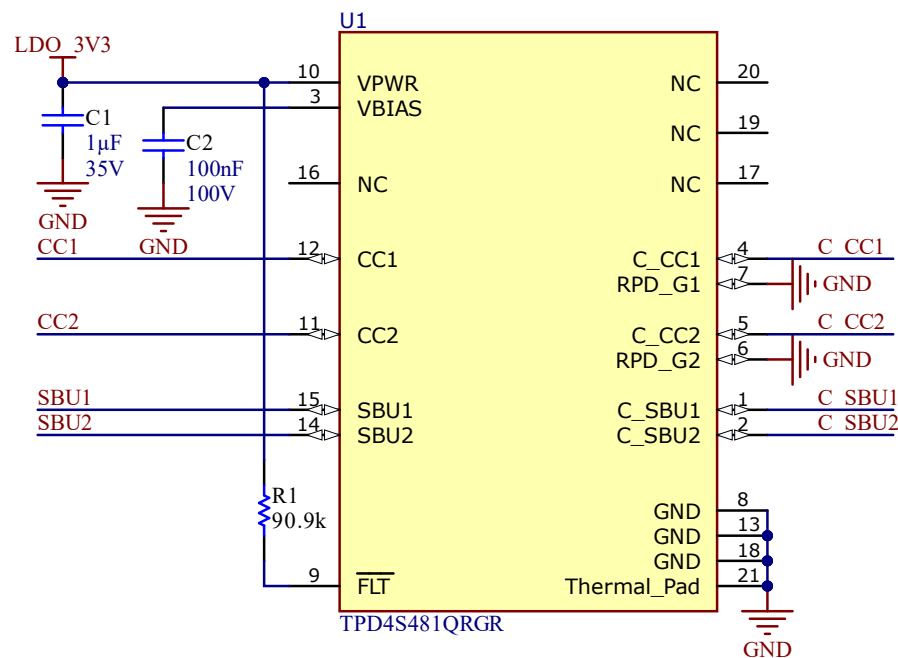


Figure 7-1. TPD4S481-Q1 No Dead Battery

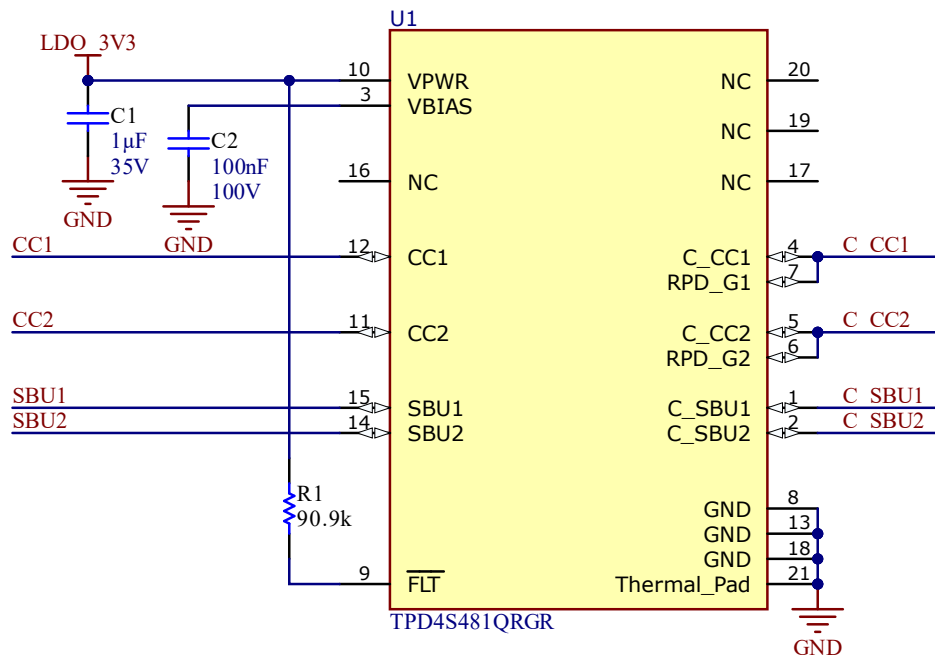


Figure 7-2. TPD4S481-Q1 Dead Battery



### 7.2.1 Design Requirements

In this application example, we study the protection requirements for a USB Type-C DRP Port, fully equipped with USB-PD, and 240W charging. The TPS2674x-Q1 is used to easily enable a DRP port. Both the CC and SBU pins are susceptible to short-to-Vbus events. With 240W charging,  $V_{BUS}$  operates at 48V, requiring the CC and SBU pins to tolerate  $48V_{DC}$ . With these protection requirements present for the USB Type-C connector, the TPD4S481-Q1 is used.

The Design Parameters table lists the TPD4S481-Q1 design parameters.

**Table 7-1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
$V_{BUS}$ nominal operating voltage	48V
Short-to- $V_{BUS}$ tolerance for the CC and SBU pins	63V
VBIAS nominal capacitance	0.1 $\mu$ F
Dead battery charging	240W

#### 7.2.1.1 EPR Design Requirements

The TPD4S481-Q1 works in conjunction with the PD controller to provide the following functionality in USB-PD EPR:

- Short to VBUS protection for direct shorts to CC1 and CC2 pins of the Type-C connector.
- Short to VBUS protection for the SBU1 and SBU2 pins of the Type-C connector.
- Short to VBUS protection for the liquid detection circuitry of the PD controller that is connected to the LQD pin of the Type-C connector, if the liquid detection feature is implemented.
- Voltage level translation from the EPR maximum voltage down to the operation range of the VBUS pins of the PD controller.

## 7.2.2 Detailed Design Procedure

### 7.2.2.1 VBIAS Capacitor Selection

As noted in the [Section 5.5](#) table, a minimum of  $63V_{BUS}$  rated capacitor is required for the VBIAS pin, and a  $100V_{BUS}$  capacitor is recommended. The VBIAS capacitor is in parallel with the central diode clamp integrated inside the TPD4S481-Q1. A forward biased hiding diode connects the VBIAS pin to the C\_CCx and C\_SBUx pins. Therefore, when a short-to- $V_{BUS}$  event occurs at 48V,  $48V_{BUS}$  minus a forward biased diode drop is exposed to the VBIAS pin. Additionally, during the short-to- $V_{BUS}$  event, ringing almost doubles the settling voltage of 48V, allowing a potential 96V to be exposed to the C\_CCx and C\_SBUx pins. However, the internal diode clamps limit the voltage exposed to the C\_CCx and C\_SBUx pins to around 63V. Therefore, at least a 63V capacitor is required to avoid the destruction of the VBIAS capacitor during short-to- $V_{BUS}$  events.

A 100V, X7R capacitor is recommended to further improve the derating performance of the capacitors. When the voltage across a real capacitor is increased, the capacitance value derates. The more the capacitor derates, the larger the ringing in the short-to- $V_{BUS}$  RLC circuit. The 100V X7R capacitors have great derating performance, allowing for the best short-to- $V_{BUS}$  performance of the TPD4S481-Q1.

### 7.2.2.2 CC Line Capacitance

USB PD has a specification for the total amount of capacitance that is required for proper USB PD BMC operation on the CC lines.

**Table 7-2. USB PD cReceiver Specification**

NAME	DESCRIPTION	MIN	MAX	UNIT	COMMENT
cReceiver	CC receiver capacitance	200	600	pF	The DFP or UFP system have capacitance within this range when not transmitting on the line

When USB PD is in use, keep the capacitance of the CC lines between 200pF and 600pF. The combination of capacitances added to the system by the TPS2674x-Q1, the TPD4S481-Q1, and any external capacitor need to fall within these limits.

### 7.2.2.3 $\overline{FLT}$ Pin Operation

Once a short-to- $V_{BUS}$  occurs on the C\_CCx or C\_SBUx pins, the  $\overline{FLT}$  pin is asserted in 20 $\mu$ s (typical) to quickly notify the PD controller. If  $V_{BUS}$  is being shorted to CC or SBU, it is recommended to respond to the event by forcing a detach in the USB PD controller to remove  $V_{BUS}$  from the port. The TPD4S481-Q1 provides protection from these shorting events, but does not protect the other device connected through the USB Type-C Cable or any active circuitry in the cable. Although shutting the  $V_{BUS}$  off through a detach does not always stop the other device or cable from being damaged, it mitigates any high current paths from causing further damage after the initial damage. Additionally, even if the active cable or other device does have proper protection, the short-to- $V_{BUS}$  event is capable of corrupting a configuration in an active cable or in the other PD controller, so it is best to detach and reconfigure the port.

### 7.2.2.4 Dead Battery Operation

For most automotive applications, PD dead battery operation is not required. Short the RPD\_G1 and RPD\_G2 pins to ground so that the dead battery resistors are not provided to the connector CC1 and CC2 pins.

For this application, dead battery support is required, so short RPD\_G1 to CC1 and short RPD\_G2 to CC2. Shorting the pins is done to ensure the dead battery resistors are present, even when no system power is provided.

For more information on the TPD4S481-Q1 dead battery operation, see the [CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices](#) section of the data sheet.

### 7.2.3 Application Curves

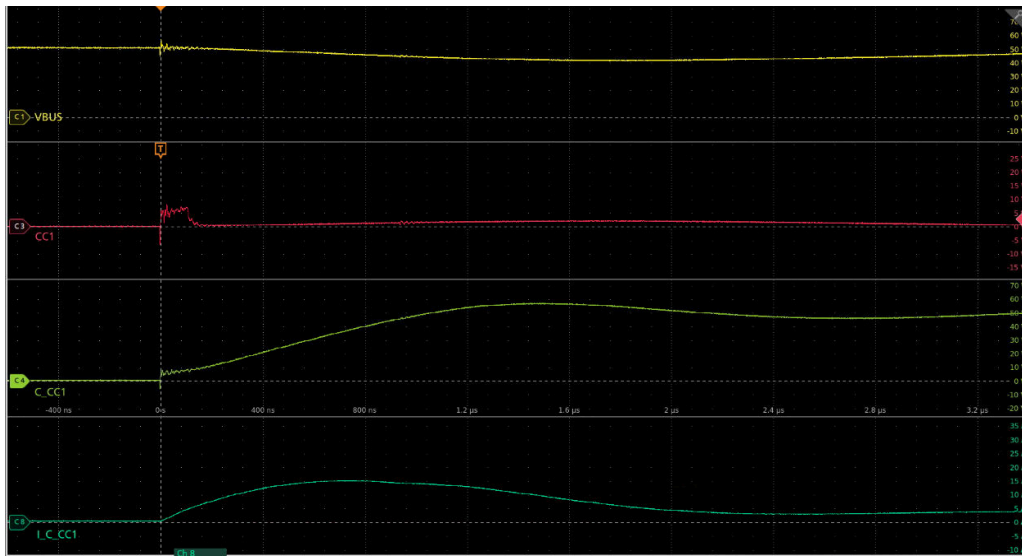


Figure 7-3. Short to VBUS Protection Example

## 7.3 Power Supply Recommendations

The  $V_{PWR}$  pin provides power to all the circuitry in the TPD4S481-Q1. It is recommended a 1- $\mu$ F decoupling capacitor is placed as close as possible to the  $V_{PWR}$  pin. If USB PD is desired to be operated in dead battery conditions, it is critical that the TPD4S481-Q1 share the same power supply as the PD controller in dead battery boot-up (such as sharing the same dead battery LDO). See the [CC Dead Battery Resistors Integrated for Handling the Dead Battery Use Case in Mobile Devices](#) section for more details.

## 7.4 Layout

### 7.4.1 Layout Guidelines

Proper routing and placement is important to maintain the signal integrity the USB2.0, SBU, CC line signals. The following guidelines apply to the TPD4S481-Q1 device:

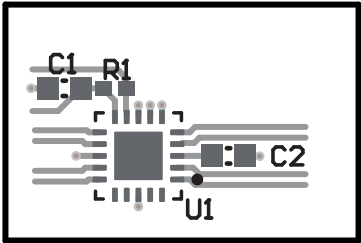
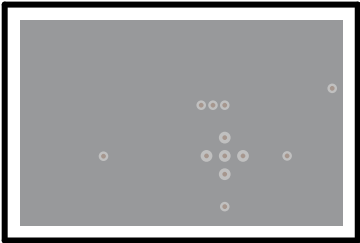
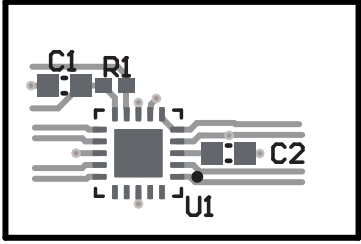
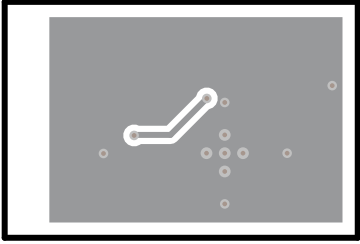
- Place the bypass capacitors as close as possible to the  $V_{PWR}$  pin, and ESD protection capacitor as close as possible to the  $V_{BIAS}$  pin. Attach capacitors to a solid ground to minimize voltage disturbances during transient events such as short-to- $V_{BUS}$  and ESD strikes.
- Route the USB2.0 and SBU lines as straight as possible and minimize any sharp bends.

Standard ESD recommendations apply to the C\_CC1, C\_CC2, C\_SBU1, and C\_SBU2 as well:

- The optimum placement for the device is as close to the connector as possible:
  - EMI during an ESD event couples from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer minimizes the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TPD4S481-Q1 device and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

7.4.2 Layout Example

Table 7-3. Typical Layout

System Configuration	Top	Bottom/Ground Plane
No Dead Battery		
Dead Battery		

## 8 Device and Documentation Support

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

For related documentation see the following:

[TPS26744E-Q1 Automotive Dual Port USB Type-C® PD Controller With 240W EPR and DisplayPort™ over USB Type-C®](#)

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.4 Trademarks

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### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2025) to Revision A (August 2025)	Page
• Updated Features to clarify functions of device and include automotive grade information.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4S481TRGRRQ1	Active	Production	VQFN (RGR)   20	5000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	4S481

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S481TRGRRQ1	VQFN	RGR	20	5000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPD4S481TRGRRQ1	VQFN	RGR	20	5000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S481TRGRRQ1	VQFN	RGR	20	5000	367.0	367.0	35.0
TPD4S481TRGRRQ1	VQFN	RGR	20	5000	346.0	346.0	33.0



## GENERIC PACKAGE VIEW

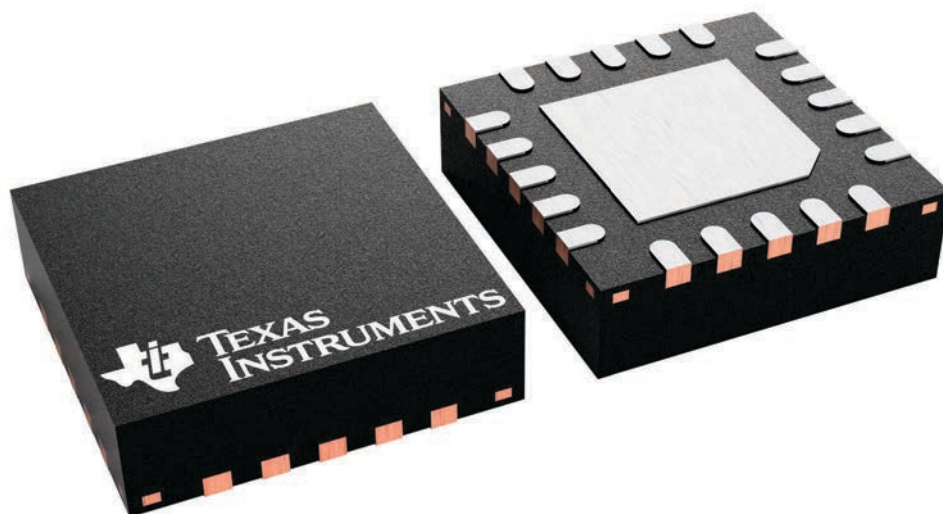
**RGR 20**

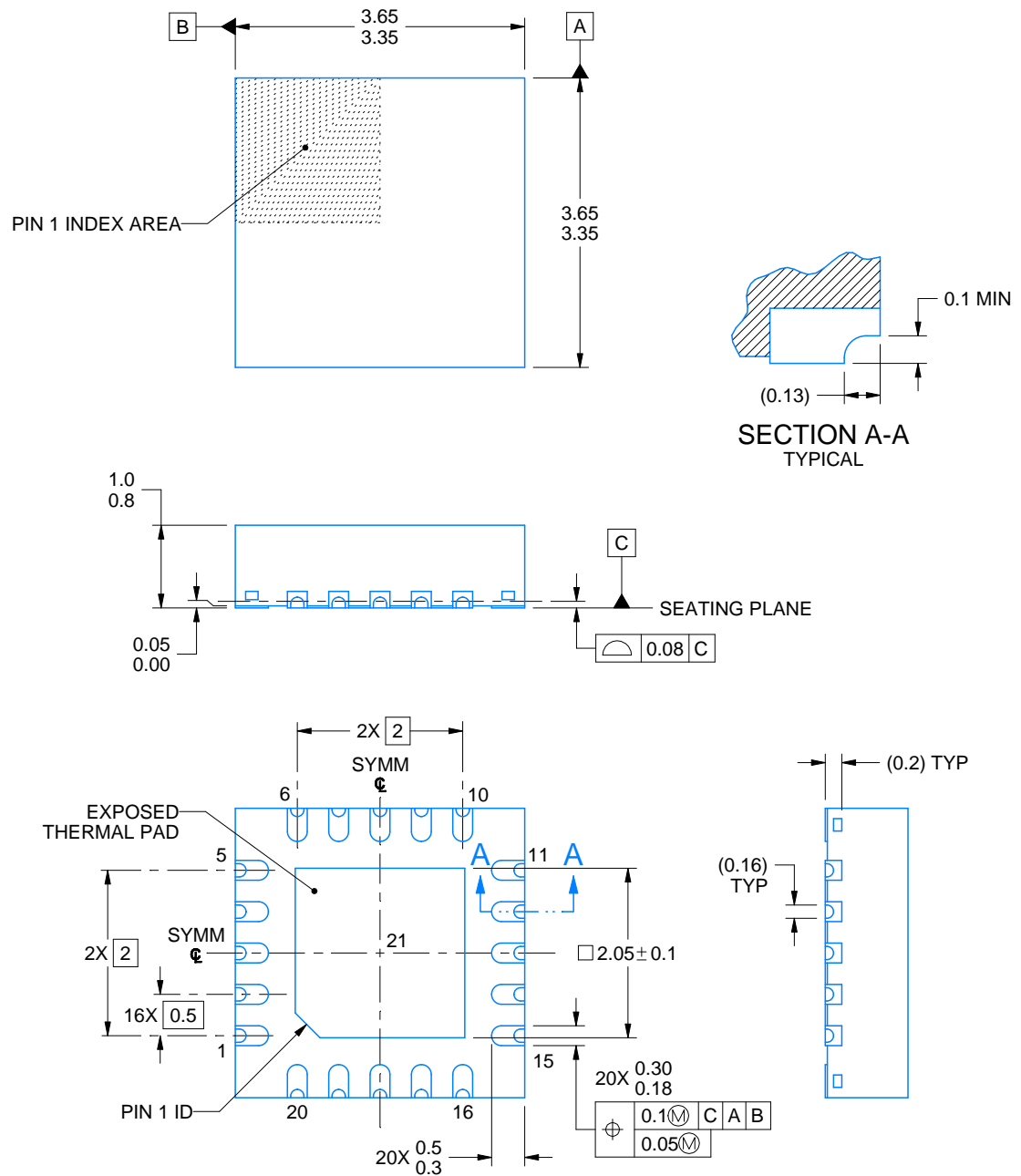
**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





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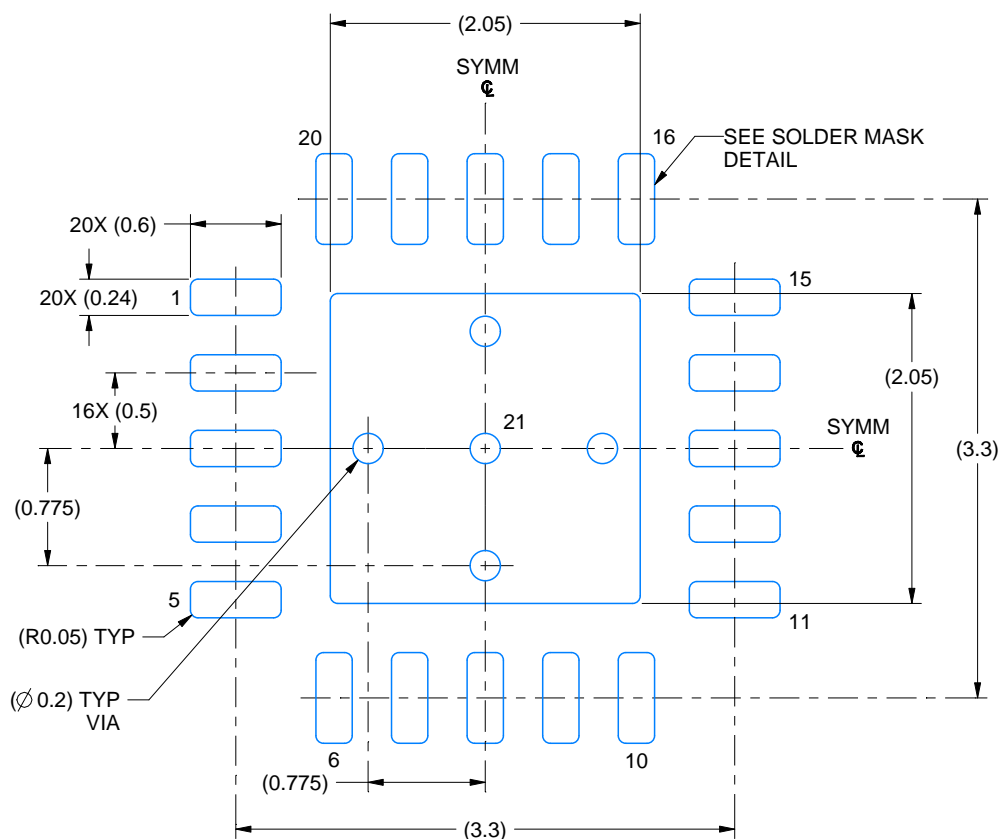
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

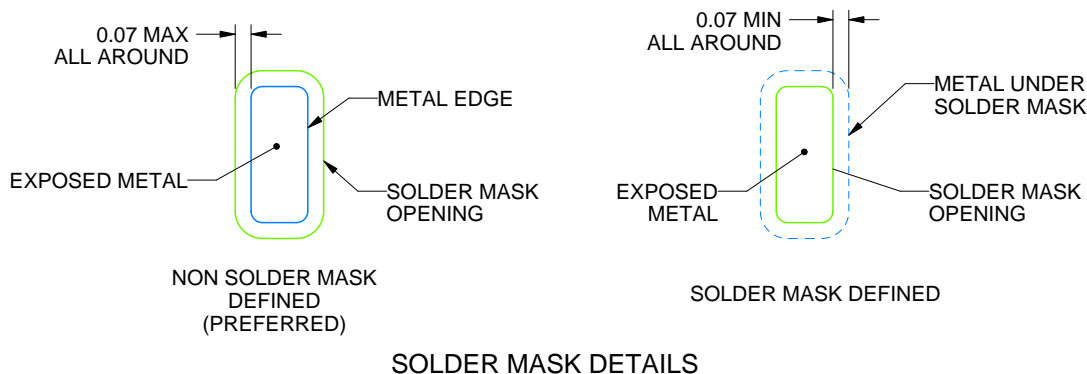
**RGR0020C**

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



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NOTES: (continued)

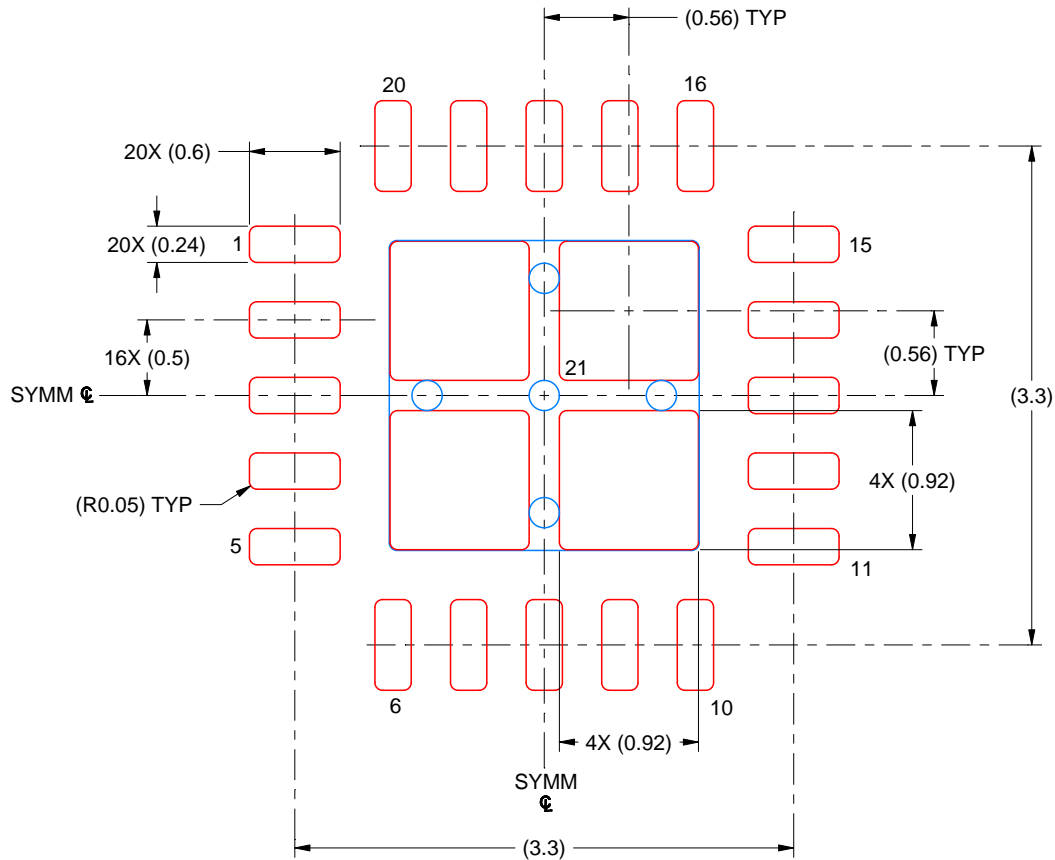
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGR0020C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 21  
81% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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