TPD4E001-Q1 4-Channel ESD Protection Array With 1.5-pF I/O Capacitance

1 Features

- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3B
  - HBM Level 15 kV
  - Device CDM ESD Classification Level C5
- IEC 61000-4-2 Level 4 ESD Protection
  - ±8-kV Contact Discharge
  - ±15-kV Air-Gap Discharge
- IEC 61000-4-5 Surge Protection
  - 5.5 A (8/20 µs)
- Low 1.5-pF Input Capacitance
- Low 10-nA Maximum Leakage Current
- 0.9-V to 5.5-V Supply Voltage Range

2 Applications

- End Equipment
  - Automotive Head Unit
  - Automotive Rear Seat Entertainment
  - Automotive Rear Camera Systems
- Interfaces
  - USB 2.0
  - Ethernet
  - Precision Analog Interfaces

3 Description

The TPD4E001-Q1 device is a low-capacitance TVS diode array designed for ESD protection in sensitive electronics connected to communication lines. Each channel consists of a pair of transient-voltage-suppression diodes that steer ESD pulses to V_{CC} or GND. The TPD4E001-Q1 protects against ESD events up to ±8-kV contact discharge and ±15-kV air-gap discharge, as specified in IEC 61000-4-2 international standard. This device has a low capacitance of 1.5-pF per channel making it ideal for use in high-speed data interfaces. The low leakage current (10 nA maximum) ensures minimum power consumption for the system and high accuracy for analog interfaces.

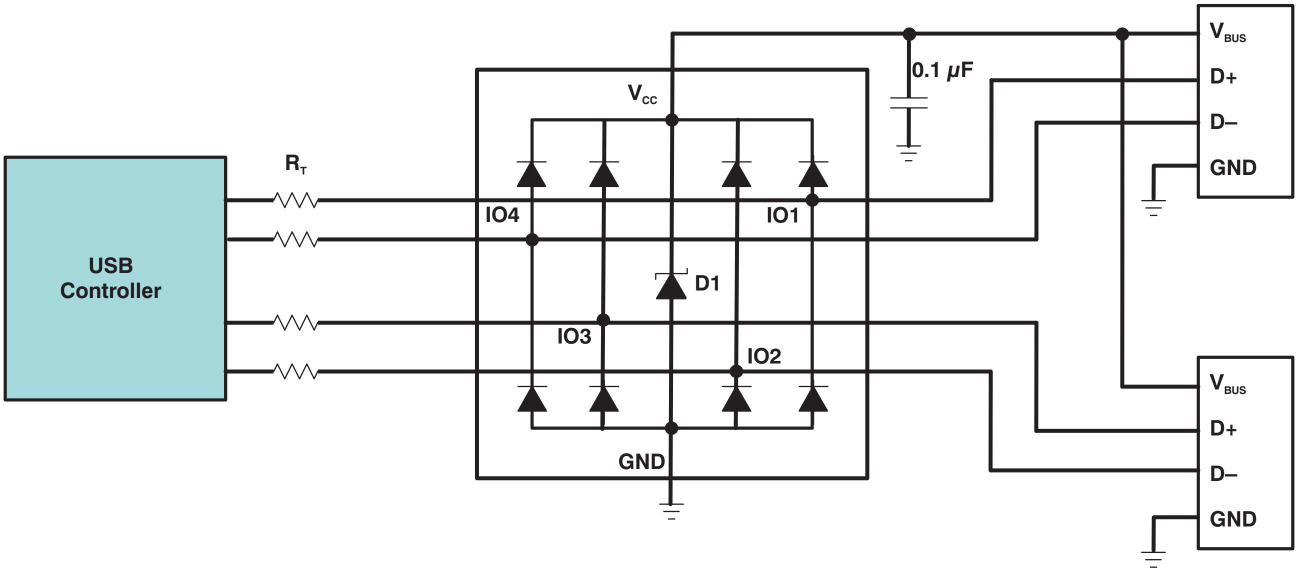
Additionally, this device is ideal for protecting automotive head units, automotive rear seat entertainment, and automotive rear camera systems that use USB 2.0, Ethernet, or precision analog interfaces.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E001-Q1	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2017) to Revision F	Page
• Added ISO Specification	4

Changes from Revision D (March 2015) to Revision E	Page
• Updated *Typical Application Schematic*	9

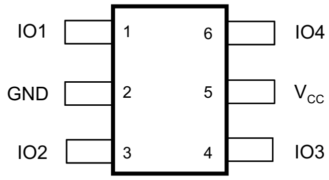
Changes from Revision C (June 2013) to Revision D	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed Device CDM ESD Classification Level from C4B to C5	1

Changes from Revision B (February 2012) to Revision C	Page
• Changed maximum I_{CC} supply current in Electrical Characteristics	5

Changes from Revision A (April 2013) to Revision B	Page
• Revised text in DESCRIPTION section	1
• Revised Figure 2 graph	5
• Revised APPLICATION INFORMATION schematic	9

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	2	GND	Ground
IO1	1	I/O	ESD-protected channel
IO2	3		
IO3	4		
IO4	6		
V_{CC}	5	I	Power-supply input. Bypass V_{CC} to GND with a 0.1-μF ceramic capacitor

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	7	V
V_{IO}	I/O voltage tolerance	–0.3	V_{CC} + 0.3	V
I_{PP}	Peak pulse current (Tp = 8/20 µs) [2]		5.5	A
P_{PP}	Peak pulse power (Tp = 8/20 µs) [2]		100	W
T_A	Free air operating temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

[1] SStresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 [1]	±15000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

[1] AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±8000	V
		IEC 61000-4-2 air-gap discharge	±15000	

6.4 ESD Ratings—ISO Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 (330 pF, 330 Ω) contact discharge	±8000	V
		ISO 10605 (330 pF, 330 Ω) air-gap discharge	±15000	

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Free air operating temperature	–40	125	°C
V_{CC} pin	Operating voltage	0.9	5.5	V
IO1, IO2, IO3, IO4 pins	Operating voltage	0	V_{CC}	V

6.6 Thermal Information

THERMAL METRIC[1]		TPD4E001-Q1	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	146.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

V_{CC} = 5 V ± 10%, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
I_{CC}	Supply current				1	200	nA
V_F	Diode forward voltage	I_F = 10 mA		0.65		0.95	V
V_{BR}	Breakdown voltage	I_{BR} = 10 mA		11			V
V_{CLAMP}	Clamping voltage	Surge strike[2] on IO pin, GND pin grounded, V_{CC} = 5.5 V, I_{PP} = 5.5 A	Positive transients		16		V
V_{RWM}	Reverse standoff voltage	IO pin to GND pin				5.5	V
I_{IO}	Channel leakage current	V_{IO} = GND to V_{CC}				±10	nA
C_{IO}	Channel input capacitance	V_{CC} = 5 V, bias of V_{CC}/2, f = 10 MHz			1.5		pF

(1) Typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

6.8 Typical Characteristics

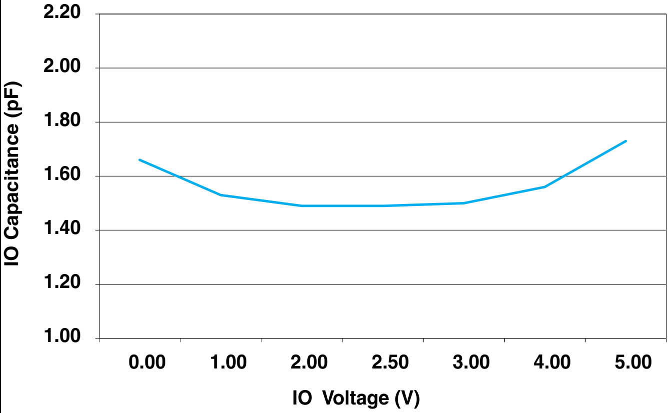


Figure 1. IO Capacitance vs IO Voltage (V_{CC} = 5 V)

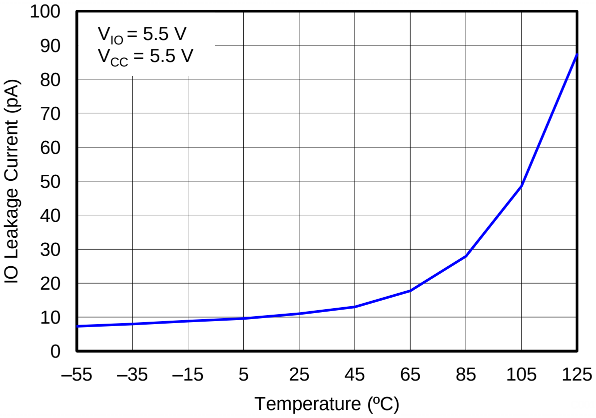


Figure 2. IO Leakage Current vs Temperature

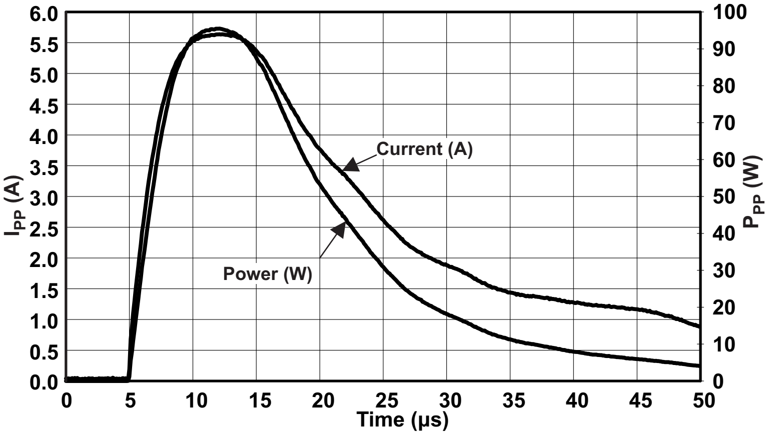


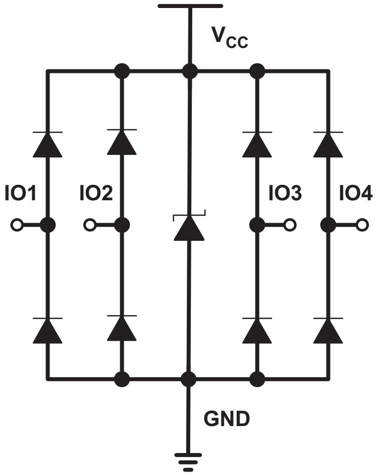
Figure 3. Peak Pulse Waveform, V_{CC} = 5.5 V

7 Detailed Description

7.1 Overview

The TPD4E001-Q1 device is a low-capacitance, TVS diode array designed for ESD protection in sensitive electronics connected to communication lines. Each channel consists of a pair of transient voltage suppression diodes that steer ESD pulses to V_{CC} or GND. The TPD4E001-Q1 device protects against ESD events up to ±8-kV contact discharge and ±15-kV air-gap discharge, as specified in IEC 61000-4-2 international standard. This device has a low capacitance of 1.5-pF per channel making it ideal for use in high-speed data interfaces. The low-leakage current (10 nA maximum) ensures minimum power consumption for the system and high accuracy for analog interfaces.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 AEC-Q100 Qualified

This device is qualified according to the AEC-Q100 standard. The device temperature rating is Grade 1 (–40°C to +125°C). The HBM Classification Level passed is 3B (> 8 kV). The CDM Classification Level passed is C5 (all pins 750 V to <1000 V).

7.3.2 IEC 61000-4-2 Level 4 ESD Protection

The device is specified at ±8-kV contact discharge and ±15-kV air gap discharge.

7.3.3 IEC 61000-4-5 Surge Protection

This device is rated to pass at least 5.5-A of peak pulse current according to the IEC 61000-4-5 (8/20-µs pulse) standard.

7.3.4 Low 1.5-pF Input Capacitance

This device has a typical capacitance of 1.5-pF on each of the four IO pins. This allows for high speed signals on the IO pins in excess of 1 Gbps.

7.3.5 Low 10-nA (Maximum) Leakage Current

This device is rated to have a maximum leakage current of 10-nA on each of the four IO pins.

7.3.6 0.9-V to 5.5-V Supply Voltage Range

This device is specified to operate with a supply voltage (on V_{CC}) between 0.9-V and 5.5-V to ensure sufficient signal integrity.

7.4 Device Functional Modes

The TPD4E001-Q1 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the lower diodes V_F (–0.6 V). During ESD events, voltages as high as ±8 kV (contact) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E001-Q1 (usually within 10s of nano-seconds) the device reverts back to its high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E001-Q1 device is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

For this design example, one TPD4E001-Q1 device is being used in a dual USB 2.0 application. This provides a complete port protection scheme.

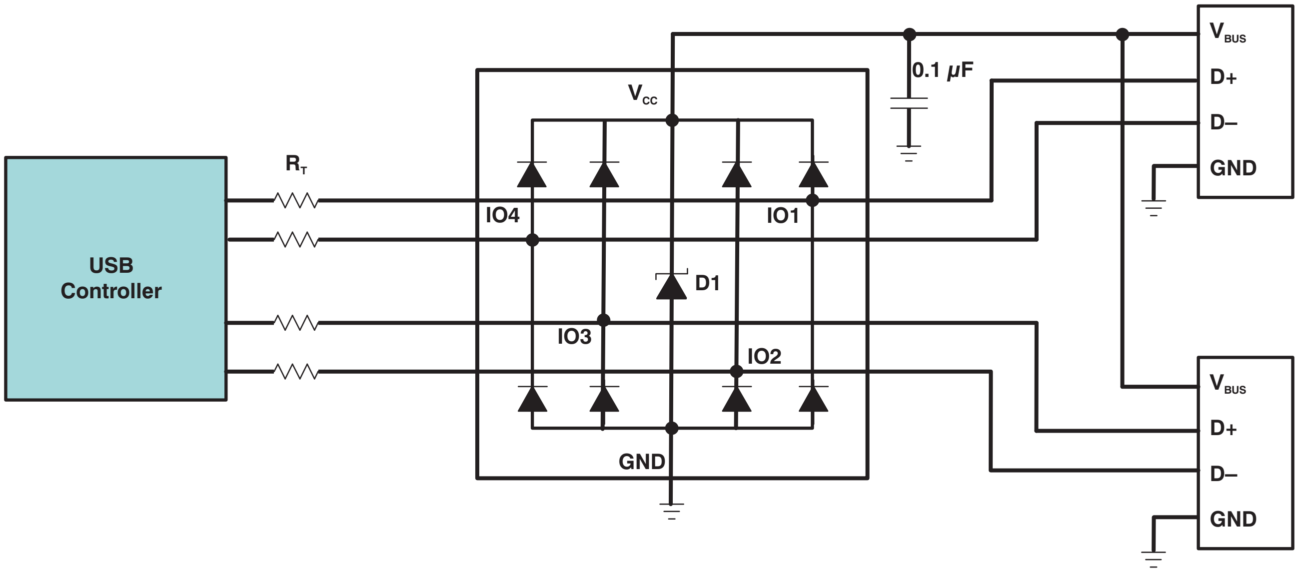


Figure 4. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

For this design example, a single TPD4E001-Q1 device is used to protect all the pins on two USB2.0 connectors.

Given the USB application, known parameters are listed in the Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, or IO4	0 V to 3.6 V
Voltage range on V_{CC}	0 V to 5.25 V
Operating Frequency on IO1, IO2, IO3, or IO4	240 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range on all protected lines
- Operating frequency on all protected lines

8.2.2.1 Signal Range on IO1 Through IO4

The TPD4E001-Q1 device has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 IO channels protects which signal lines. Any IO supports a signal range of 0 to (V_{CC} + 0.3) V. Therefore, this device supports the USB 2.0 signal swing assuming V_{CC} is set appropriately.

8.2.2.2 Voltage Range on V_{CC}

The V_{CC} pin can be connected in one of two ways:

- If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 device works as a transient suppressor for any signal swing above $V_{CC} + V_F$. TI recommends a 0.1-µF capacitor on the device V_{CC} pin for ESD bypass.
- If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 device can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-µF capacitor at the V_{CC} pin for ESD bypass.

If this pin is connected to the USB 2.0 V_{BUS} supply or left floating, the allowable signal swing is enough for a USB 2.0 application.

8.2.2.3 Bandwidth on IO1 Through IO4

Each IO pin on the TPD4E001-Q1 device has a typical capacitance of 1.5 pF. This capacitance is low enough to easily support USB 2.0 data rates.

8.2.3 Application Curve

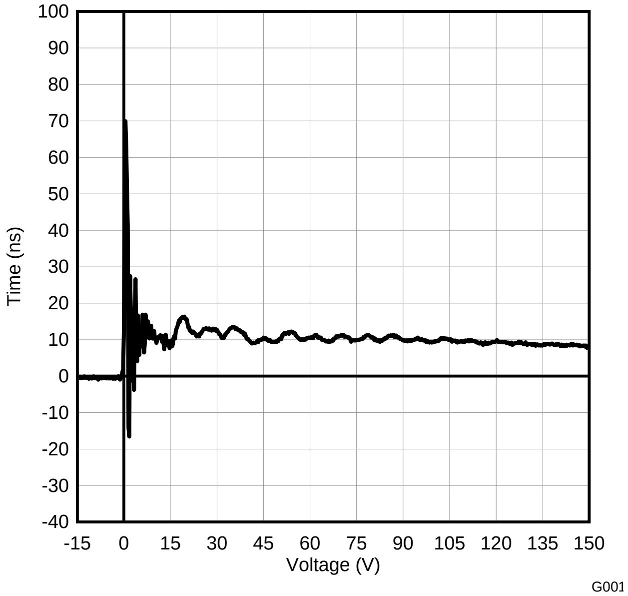


Figure 5. IEC 61000-4-2 Voltage Clamp Waveform 8-kV Contact

9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Do not violate the maximum voltage specifications for each pin.

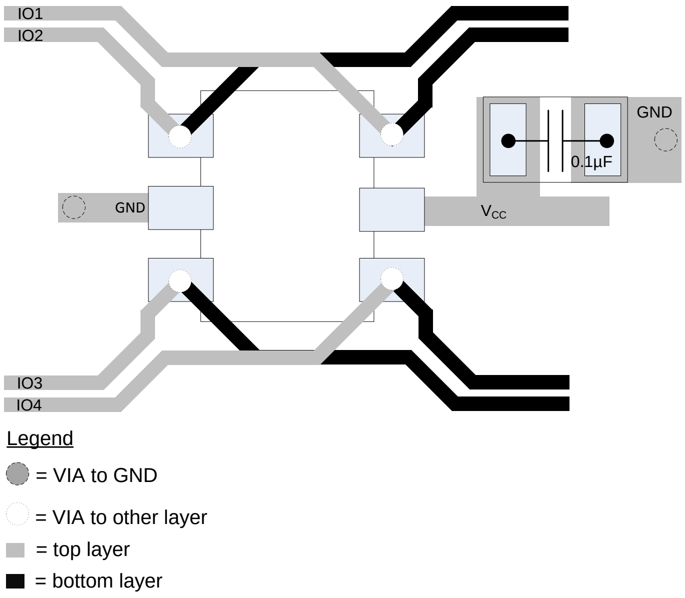
10 Layout

10.1 Layout Guidelines

When placed near the connector, the TPD4E001-Q1 device's ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage-current specifications. The TPD4E001-Q1 device ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, observe the following layout and design guidelines:

- Place the TPD4E001-Q1 device solution close to the connector. This allows the device to take away the energy associated with ESD strike before it reaches the internal circuitry of the system board.
- Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.
- Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E001-Q1 device consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15 A to 30 A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.
- Leave the unused IO pins floating.
- One can connect the V_{CC} pin in two different ways:
  a. If the V_{CC} pin connects to the system power supply, the TPD4E001-Q1 works as a transient suppressor for any signal swing above V_{CC} + V_F. TI recommends a 0.1-µF capacitor on the device V_{CC} pin for ESD bypass.
  b. If the V_{CC} pin does not connect to the system power supply, the TPD4E001-Q1 can tolerate higher signal swing in the range up to 10 V. Note that TI still recommends a 0.1-µF capacitor at the V_{CC} pin for ESD bypass.
- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example



11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Reading and Understanding an ESD Protection Datasheet*
- *ESD Layout Guide*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E001QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AAXQ
TPD4E001QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AAXQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD4E001-Q1 :

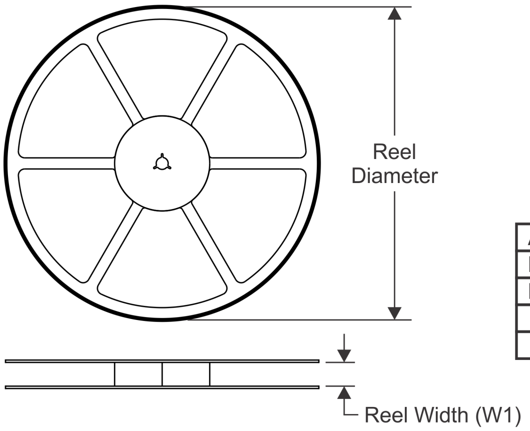
- Catalog : TPD4E001

NOTE: Qualified Version Definitions:

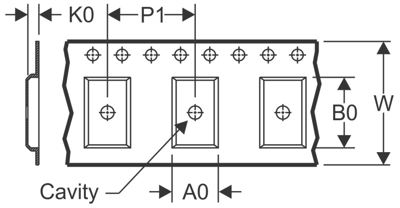
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

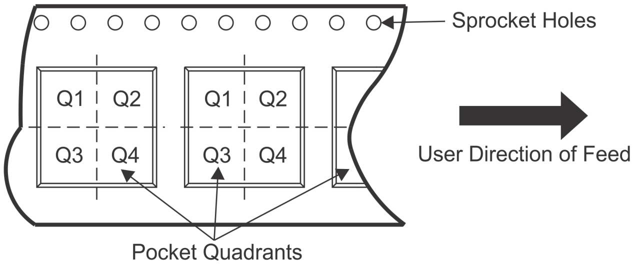


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

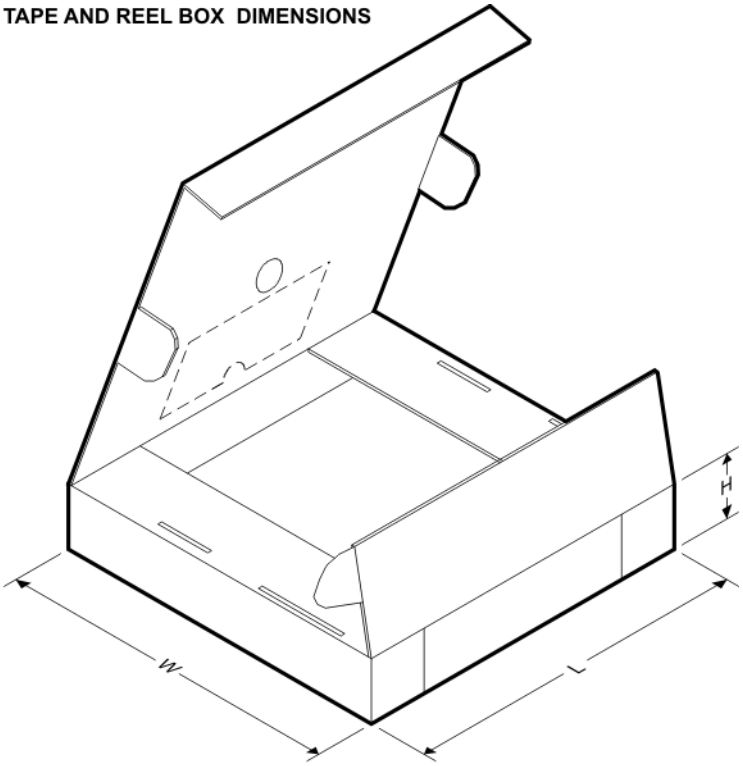
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

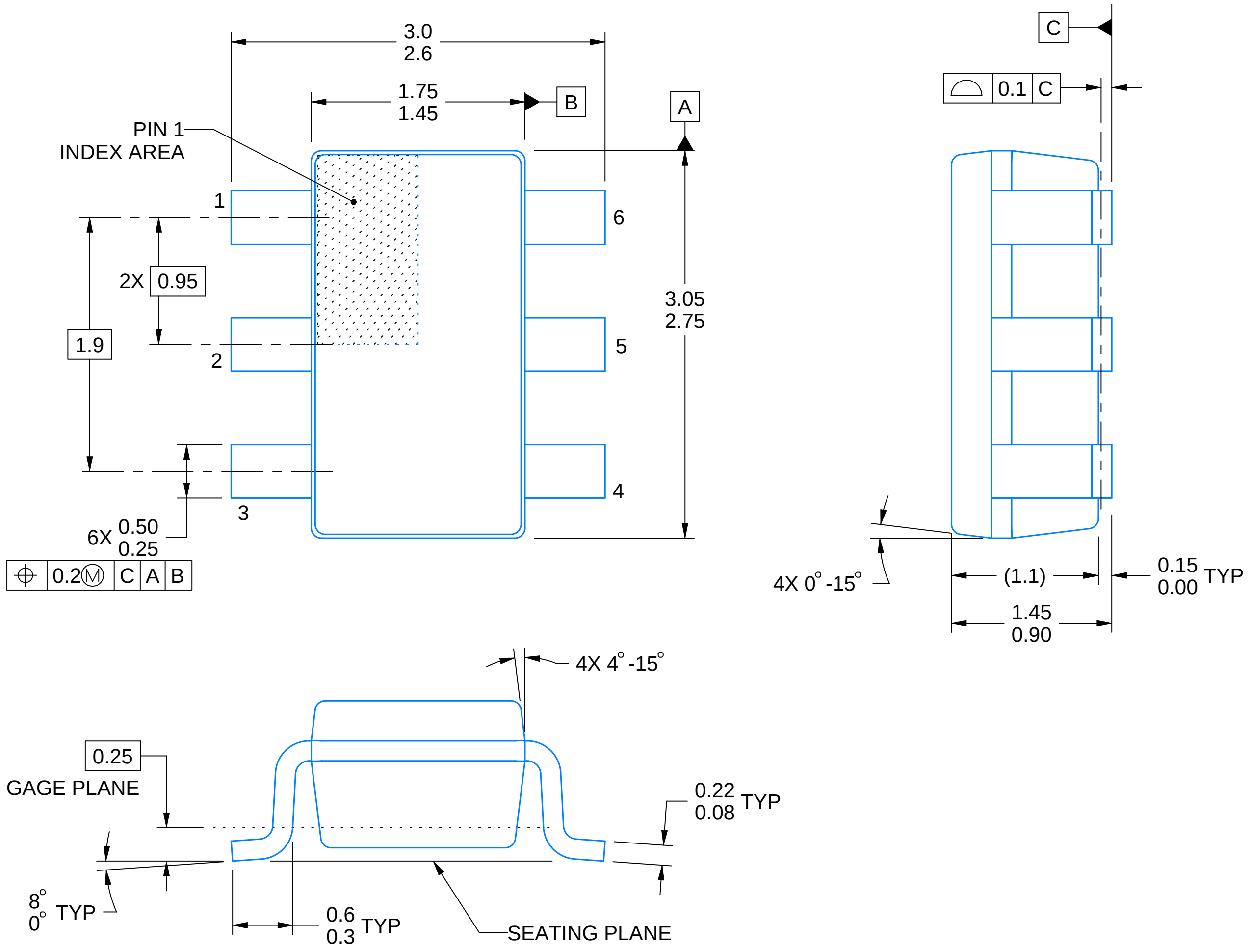
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E001QDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0



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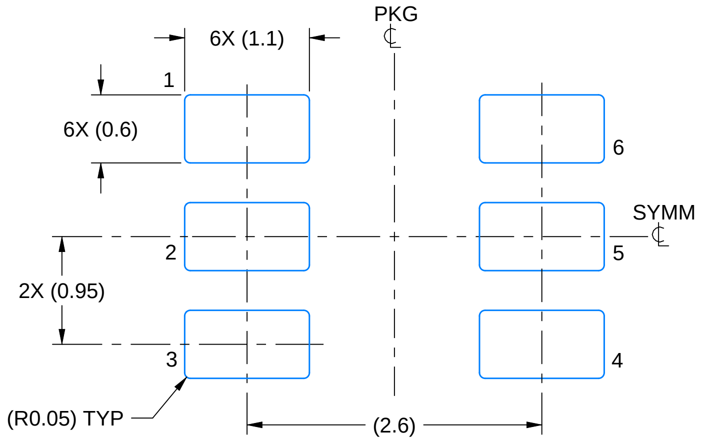
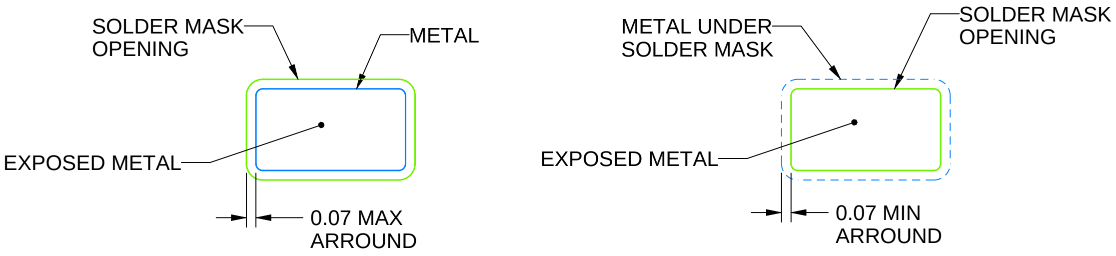
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



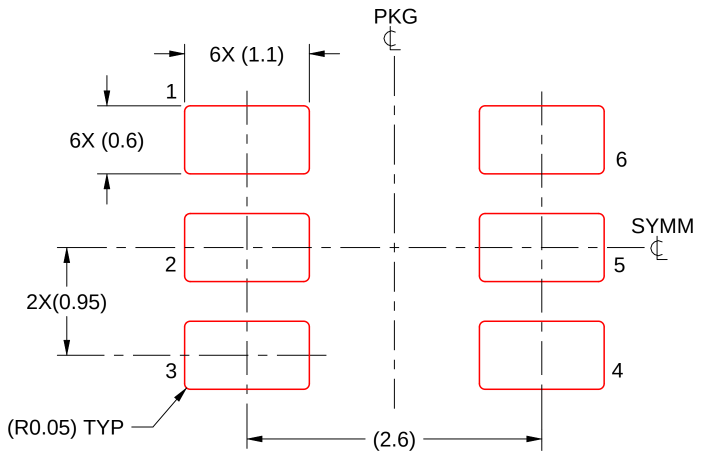
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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