TPA6404-Q1 45W, 2MHz Analog Input 4-Channel Automotive Class-D Audio Amplifier with Load Dump Protection and I²C Diagnostics

1 Features

- Advanced load diagnostics
  - AC diagnostic for tweeter detection with impedance and phase response
  - Integrated sine wave generator
- Easy to meet CISPR25-L5 EMC specification
- AEC-Q100 Qualified for automotive applications:
  - Temperature Grade 1: –40°C to 125°C T_A
  - Device HBM ESD classification level: 3A
  - Device CDM ESD classification level: C4B
- Audio Inputs
  - 4 Channel differential analog input
  - Four I²C-controlled gain options
  - High input impedance for low value AC-coupling capacitor
- Audio outputs
  - Four-channel Bridge-tied load (BTL), with option of parallel BTL (PBTL)
  - Up to 2.1 MHz Output switching frequency
  - 27 W, 10% THD into 4Ω at 14.4V
  - 45W, 10% THD into 2Ω at 14.4V
  - 85W, 10% THD into 1Ω at 14.4V PBTL
- Audio performance into 4Ω at 14.4V, 1kHz
  - THD+N < 0.01%
  - 42μV_{RMS} Output noise
  - - 90dB Crosstalk
- Load Diagnostics
  - Output open and shorted load
  - Output-to-battery or ground shorts
  - Line output detection up to 6kΩ
  - Runs without input clocks
- Protection
  - Output current limiting
  - Output short protection
  - 40V Load dump
  - Fortuitous Open ground and power tolerant
  - DC Offset
  - Over temperature
  - Undervoltage and overvoltage
- General operation
  - 4.5V to 18V supply voltage
  - I²C Control With 4 Address Options
  - Clip Detection and Thermal Foldback

2 Applications

- Automotive Head Units
- Automotive External Amplifier Modules

3 Description

The TPA6404-Q1 device is a four-channel analog-input Class-D audio amplifier that implements a 2.1MHz PWM switching frequency that enables a cost optimized solution in a very small 4.5cm² PCB size, full operation down to 4.5V for start/stop events, and exceptional sound quality with up to 100kHz audio bandwidth.

The TPA6404-Q1 Class-D audio amplifier has an optimal design for use in entry level automotive head units that provide analog audio input signals as part of their system design.

The Class-D topology dramatically improves efficiency over traditional linear amplifier solutions.

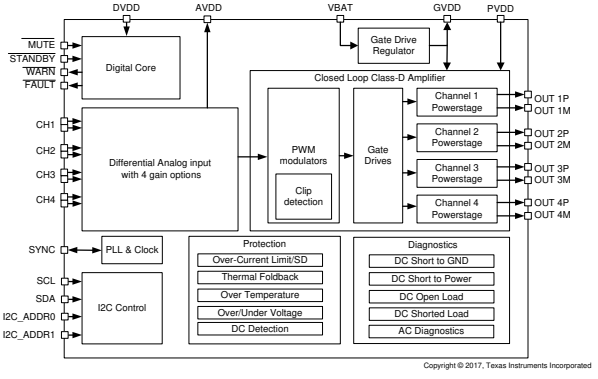
The output switching frequency operates above the AM band, which eliminates the AM band interference and reduces the output filter size and cost.

The device is offered in a 56 pin HSSOP package with the exposed thermal pad up.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPA6404-Q1	HSSOP (56)	18.41mm × 7.49mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Block Diagram

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4 Pin Configuration and Functions

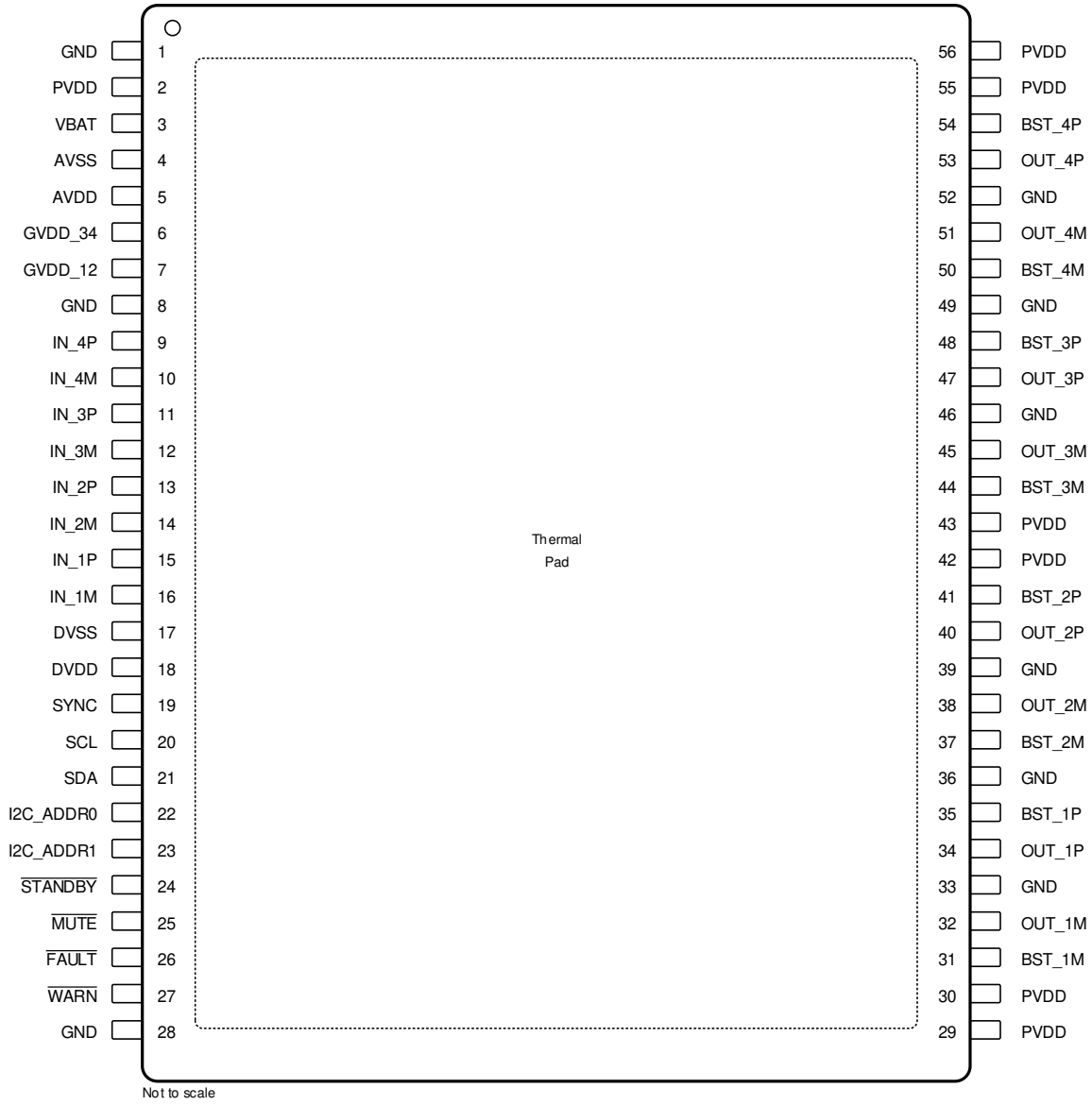

Figure 4-1. DKQ Package 56-Pin HSSOP With Exposed Thermal Pad Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AVDD	5	PWR	Voltage regulator bypass. Connect 1µF capacitor from AVDD to AVSS
AVSS	4	PWR	AVDD bypass capacitor return
BST_1M	31	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_1P	35	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2M	37	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2P	41	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_3M	44	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_3P	48	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_4M	50	PWR	Bootstrap capacitor connection pins for high-side gate driver

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Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BST_4P	54	PWR	Bootstrap capacitor connection pins for high-side gate driver
DVDD	18	PWR	DVDD supply input. Connect 1 µF capacitor from DVDD to DVSS
DVSS	17	GND	DVDD Ground Reference
$\overline{\text{FAULT}}$	26	DO	Reports a fault (active low, open drain), 100-kΩ internal pull-up resistor
GND	1, 8, 28, 33, 36, 39, 46, 49, 52	GND	Ground
GVDD_34	6	PWR	Gate drive voltage regulator for channel 3 and 4, derived from VBAT input pins. Connect 2.2µF capacitor to GND
GVDD_12	7	PWR	Gate drive voltage regulator for channel 1 and 2, derived from VBAT input pins. Connect 2.2µF capacitor to GND
I2C_ADDR0	22	DI	I^2C address pins. Refer to Table 7-7
I2C_ADDR1	23		
IN_1M	16	AI	Negative input for the channel
IN_1P	15	AI	Positive input for the channel
IN_2M	14	AI	Negative input for the channel
IN_2P	13	AI	Positive input for the channel
IN_3M	12	AI	Negative input for the channel
IN_3P	11	AI	Positive input for the channel
IN_4M	10	AI	Negative input for the channel
IN_4P	9	AI	Positive input for the channel
$\overline{\text{MUTE}}$	25	DI	Mutes the device outputs (active low), 100-kΩ internal pull-down resistor
OUT_1M	32	NO	Negative output for the channel
OUT_1P	34	PO	Positive output for the channel
OUT_2M	38	NO	Negative output for the channel
OUT_2P	40	PO	Positive output for the channel
OUT_3M	45	NO	Negative output for the channel
OUT_3P	47	PO	Positive output for the channel
OUT_4M	51	NO	Negative output for the channel
OUT_4P	53	PO	Positive output for the channel
PVDD	2, 29, 30, 42, 43, 55, 56	PWR	PVDD voltage input (can be connected to battery)
SCL	20	DI	I^2C clock input
SDA	21	DI/O	I^2C data input and output
$\overline{\text{STANDBY}}$	24	DI	Enables low power standby state (active Low), 1MΩ internal pull-down resistor
SYNC	19	DI/O	Sync clock input or output
VBAT	3	PWR	Battery voltage input
$\overline{\text{WARN}}$	27	DO	Clip and overtemperature warning (active low, open drain), 100kΩ internal pull-up resistor
Thermal Pad	—	GND	Provides both electrical and thermal connection for the device. Heatsink must be connected to GND.

(1) AI = analog input, GND = ground, PWR = power, PO = positive output, NO = negative output, DI = digital input, DO = digital output, DI/O = digital input and output, NC = No Connection

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
PVDD, VBAT	DC supply-voltage range relative to GND		-0.3	30	V
V_{MAX}	Transient supply-voltage range - PVDD, VBAT	t ≤ 400 ms exposure	–1	40	
V_{RAMP}	Supply-voltage ramp rate - PVDD, VBAT			75	V/ms
V_{IN}	Audio differential input pins: IN_xP, IN_xM		–0.3	6.5	V
DVDD	DC supply voltage range relative to GND		–0.3	3.5	V
I_{MAX}	Maximum current per pin (PVDD, VBAT, Out xP, Out xM, GND)			±8	A
I_{MAX_PULSED}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms		±12	
V_{LOGIC}	Input voltage for logic pins (SCL, SDA, $\overline{MUTE}$, $\overline{STANDBY}$, I2C ADDRx)		–0.3	DVDD + 0.5	V
V_{GND}	Maximum voltage between GND pins			±0.3	
T_J	Maximum operating junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±4000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 28, 29 and 56)	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
PVDD	Output FET Supply Voltage Range	Relative to GND	4.5	14.4	18	V
VBAT	Battery Supply Voltage Input	Relative to GND	4.5	14.4	18	V
DVDD	DC Logic supply	Relative to GND	3.0	3.3	3.5	V
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature	An adequate thermal design is required	–40		150	°C
R_L	Nominal speaker load impedance	BTL Mode	2	4		Ω
		PBTL Mode	1	2		Ω
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
C_{Bypass}	External capacitance on bypass pins	Pin 2, 3, 5, 18		1		µF
C_{GVDD}	External capacitance on GVDD pins	Pin 6, 7		2.2		µF
C_{OUT}	External capacitance to GND on OUT pins	Limit set by DC-diagnostic timing		1	3.3	µF
L_O	Output filter inductance - I_{SD}	Minimum output filter inductance at I_{SD} current levels. Applies to short to ground or short to power protection.	1			µH
L_O	Output filter inductance - I-LIMIT	Minimum output filter inductance at I-LIMIT current levels. Applies to current limiting.	2			µH

5.4 Thermal Information

THERMAL METRIC(1)		TPA6404-Q1(2) DKQ (HSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	–	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	–	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	–	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.
(2) JEDEC standard 4 layer PCB.

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5.5 Electrical Characteristics

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, AES17 Filter, reconstruction filter inductor used: DFEG7030D-3R3M from MuRata Toko, default I^2C settings, see application diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All channels playing, no audio input		65	80	mA
$I_{PVDD+VBAT\_IDLE}$	PVDD+VBAT idle current	All channels playing, no audio input		155	190	mA
I_{VBAT_IDLE}	VBAT idle current	All channels playing, no audio input		90	110	mA
I_{PVDD_STBY}	PVDD standby current	$\overline{STANDBY}$Active, DVDD= 0 V		0.08		µA
I_{VBAT_STBY}	VBAT standby current	$\overline{STANDBY}$Active, DVDD= 0 V		3.0		µA
I_{TOTAL_STBY}	PVDD+VBAT standby current	$\overline{STANDBY}$Active, DVDD = 0 V		3.0	7.0	µA
I_{DVDD}	DVDD supply current	All channels playing, -60 dB Signal		6.2	7.0	mA
OUTPUT POWER						
P_{O_BTL}	Output power per channel, BTL	4 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	20	22		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	24	27		
P_{O_BTL}	Output power per channel, BTL	2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	31	38		W
		2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	40	45		
P_{O_BTL}	Output power per channel, BTL	4 Ω, PVDD = 18 V, THD+N = 1%, T_C = 75°C	32	35		W
		4 Ω, PVDD = 18 V, THD+N = 10%, T_C = 75°C	40	44		
P_{O_PBTL}	Output power per channel in parallel mode, PBTL	2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	40	44		W
		2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	50	54		
P_{O_PBTL}	Output power per channel in parallel mode, PBTL	1 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	62	70		W
		1 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	78	85		
P_{O_PBTL}	Output power per channel in parallel mode, PBTL	2 Ω, PVDD = 18 V, THD+N = 1%, T_C = 75°C	63	68		W
		2 Ω, PVDD = 18 V, THD+N = 10%, T_C = 75°C	78	83		
EFF_P	Power efficiency	4 channels operating, 25 W output power/ch 4 Ω load, PVDD = 14.4 V, T_C = 25°C; (includes output filter losses)		86%		
AUDIO PERFORMANCE						
V_n	Output Noise Voltage	Zero input, A-weighting, 10 dB gain, PVDD = 14.4 V		42		µV
		Zero input, A-weighting, 16 dB gain, PVDD = 14.4 V		48		
		Zero input, A-weighting, 22 dB gain, PVDD = 18 V		58		
		Zero input, A-weighting, 28 dB gain, PVDD = 18 V		79		
Crosstalk	Channel crosstalk	PVDD = 14.4 Vdc + 1 V_{RMS}, f = 1 kHz		90		dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 V_{RMS}, f = 1 kHz		75		dB
THD+N	Total harmonic distortion + noise			0.01		%
G	Gain	Level 1	9.0	9.5	10.0	dB
		Level 2	15.0	15.5	16.0	
		Level 3 (default)	21.0	21.5	22.0	
		Level 4	27.0	27.5	28.0	
G_{CH}	Channel-to-channel gain variation		–0.5	0	0.5	dB
G_{MUTE}	Output Attenuation	Assert $\overline{MUTE}$ and compare to amp playing 1W audio into 4 Ω	100	110		dB
V_{CLICK}	Click & Pop	Zero input, ITU-filter, 22dB gain, PVDD = 14.4 V		5		mV
LINE OUTPUT PERFORMANCE						
$V_{n\_LINEOUT}$	LINE Output Noise Voltage	Zero input, A-weighting, channel set to LINE MODE, PVDD = 14.4 V, RL = 600 Ω		42		µV
THD+N	Line output Total harmonic distortion + noise	V_O = 2Vrms , channel set to LINE MODE, PVDD = 14.4 V		0.02		%
ANALOG INPUT PINS						
R_{IN}	Input impedance	10 dB gain		80		kΩ
		16 dB gain		40		kΩ
		22 dB gain		20		kΩ
		28 dB gain		10		kΩ

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Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, AES17 Filter, reconstruction filter inductor used: DFEG7030D-3R3M from MuRata Toko, default I^2C settings, see application diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Maximum input voltage swing, Single Ended			1		V_{RMS}
	Maximum input voltage swing, Differential	Positive input equals negative input		2		
I_{IN}	Maximum input current				±1	mA
DIGITAL INPUT PINS						
V_{IH}	Input logic level high		70			%DVDD
V_{IL}	Input logic level low				30	
I_{IH}	Input logic current	V_I = DVDD			15	uA
I_{IL}		V_I= 0			-15	
PWM OUTPUT STAGE						
$R_{DS(on)}$	FET drain-to-source resistance	25°C, Including bond wire and package resistance		120		mΩ
$R_{DS(on)}$	FET drain-to-source resistance	25°C, Not including bond wire and package resistance		90		mΩ
OVERVOLTAGE (OV) PROTECTION						
V_{PVDD_OV}	PVDD overvoltage shutdown		18.5	21	23	V
$V_{PVDD\_OV\_HYS}$	PVDD overvoltage shutdown hysteresis			0.5		V
V_{VBAT_OV}	VBAT overvoltage shutdown		18.5	21	23	V
$V_{VBAT\_OV\_HYS}$	VBAT overvoltage shutdown hysteresis			0.5		V
UNDERVOLTAGE (UV) PROTECTION						
$VBAT_{UV\_SET}$	VBAT undervoltage shutdown set			4	4.5	V
$VBAT_{UV\_CLEAR}$	VBAT undervoltage shutdown clear			4.2		
$PVDD_{UV\_SET}$	PVDD undervoltage shutdown set			4	4.5	
$PVDD_{UV\_CLEAR}$	PVDD undervoltage shutdown clear			4.2		
BYPASS VOLTAGES						
V_{GVDD}	Gate Drive Bypass pin voltage			7		V
V_{AVDD}	Analog Bypass Pin Voltage			6		
POWER-ON RESET (POR)						
V_{POR}	DVDD voltage for POR			1.8	2.1	V
V_{POR_HY}	DVDD POR recovery hysteresis voltage			0.5		
OVERTEMPERATURE (OT) PROTECTION						
OTW(i)	Channel Over-Temperature Warning			150		°C
OTSD(i)	Channel Over-Temperature Shutdown			175		
OTW	Global Junction Over-Temperature Warning	set by register 0x01 bit 5-6, default value		130		
OTSD	Global Junction Over-Temperature Shutdown			160		
OT_{HYS}	Over-Temperature Hysterisis			15		
LOAD OVER CURRENT PROTECTION						
I_{LIM}	Overcurrent limit	OC Level 1, Load current		4.8		A
		OC Level 2, Load current	6	6.5		
I_{SD}	Overcurrent Shutdown	OC Level 1, Any short to supply, ground, or other channels		7		
		OC Level 2, Any short to supply, ground, or other channels		9		

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Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, AES17 Filter, reconstruction filter inductor used: DFEG7030D-3R3M from MuRata Toko, default I^2C settings, see application diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC DETECT						
DC_{FAULT}	Output DC Fault Protection	PVDD = 14.4 V		2	2.5	V
DIGITAL OUTPUT PINS						
V_{OH}	Output voltage for logic level high	I = ±2mA	90			%DVDD
V_{OL}	Output voltage for logic level low				10	
SYNC						
f_{sync}	Supported SYNC Frequencies, controller mode	Reg 0x02 bit 6-4: 101		1.8		Mhz
		Reg 0x02 bit 6-4: 110		2.1		Mhz
		Reg 0x02 bit 6-4: 111		2.3		Mhz
Δf_{sync}	Supported SYNC Frequency deviation, target mode		-10		10	%
D_{sync}	Supported SYNC dutycycle, target mode		45%	50%	55%	
LOAD DIAGNOSTICS						
S2P	Maximum resistance to detect a short from OUT pin(s) to PVDD				500	Ω
S2G	Maximum resistance to detect a short from OUT pin(s) to ground				200	
SL	Shorted Load Detection Tolerance	R_L = 4 Ω, Other Channels in Hi-Z		±0.5		
OL	Minimum Impedance Detected as Open Load	Other Channels in Hi-Z		70		
T_{DC_DIAG}	DC Diagnostic time	4 channels, no faults		231		ms
LO	Line Output Maximum Detectable Impedance	For load resistance below this value, the device will report the LO load			6	kΩ
T_{LINE_DIAG}	Line output Diagnostic time			40		ms
AC_{IMP}	AC Impedance Accuracy	f = 19 kHz, R_L = 4 Ω		±0.75		Ω
		Z_{OUT} (including LC filter), f = 19 kHz		25%		
T_{AC_DIAG}	AC Diagnostic time	4 channels, f = 19 kHz		550		ms
F_{AC}	AC Diagnostic Test frequency	Default		18.75		kHz
I2C_ADDR PINS						
t_{I2C_ADDR}	Time delay needed for I2C Address set-up	From release of Standby pin until Address set-up	300			µs
I2C CONTROL PORT						
t_{BUS}	Bus free time between start and stop conditions		1.3			µs
t_{HOLD1}	Hold Time, SCL to SDA		0			ns
t_{HOLD2}	Hold Time, start condition to SCL		0.6			µs
t_{START}	I2C Startup Time After DVDD Power On Reset				12	ms
t_{RISE}	Rise Time, SCL and SDA				300	ns
t_{FALL}	Fall Time, SCL and SDA				300	ns
t_{SU1}	Setup, SDA to SCL		100			ns
t_{SU2}	Setup, SCL to Start Condition		0.6			µs
t_{SU3}	Setup, SCL to Stop Condition		0.6			µs
$t_{W(H)}$	Required Pulse Duration SCL "High"		0.6			µs
$t_{W(L)}$	Required Pulse Duration SCL "Low"		1.3			µs

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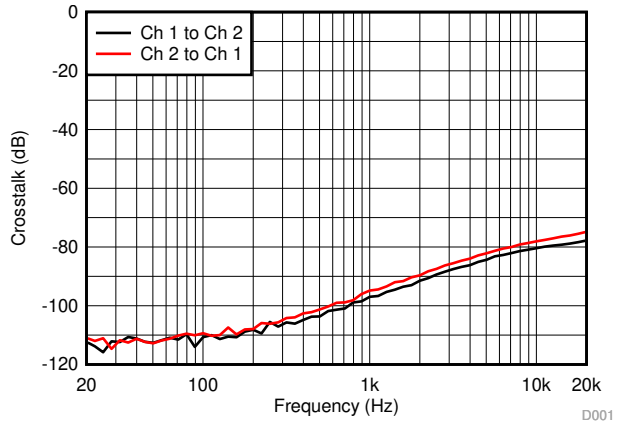
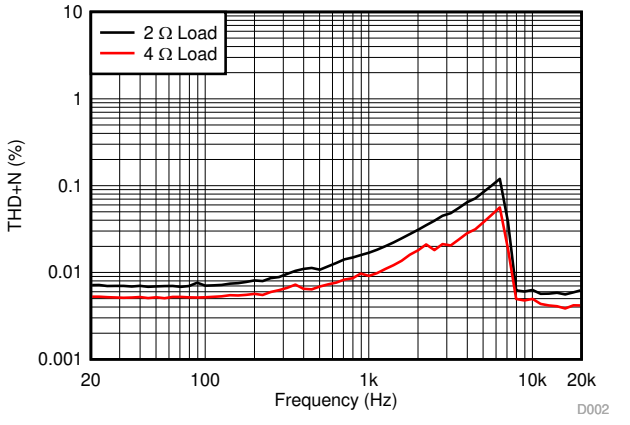
5.6 Typical Characteristics

T_A = 25 °C, DVDD = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, AES17 filter, default I^2C settings, reconstruction filter inductor used: DFEG7030D-3R3M from MuRata Toko, see application diagram in Section 9.2.1.4 Figure 9-2 (unless otherwise noted)



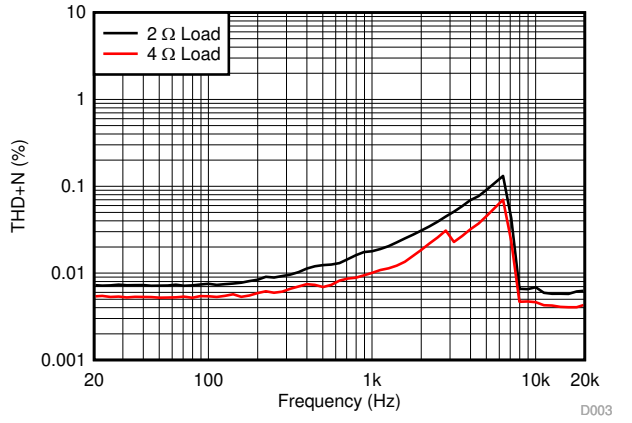
1W, BTL mode 4Ω

Figure 5-1. Crosstalk vs Frequency



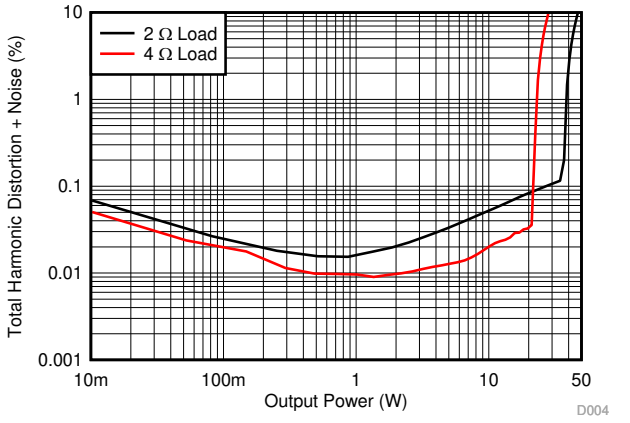
Pout = 1W PVDD = 14.4V 2.1MHz

Figure 5-2. THD+N vs Frequency



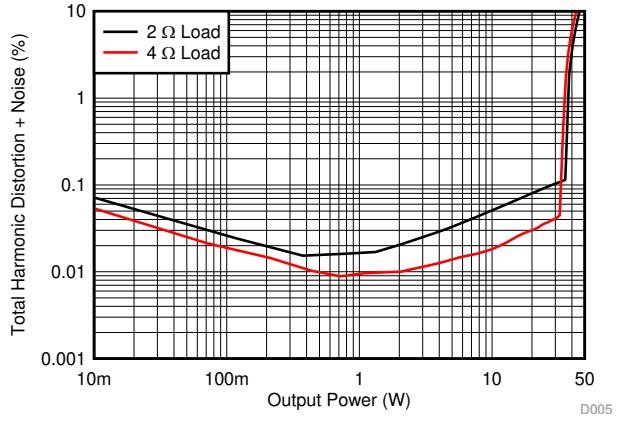
Pout = 1W PVDD = 18V 2.1MHz

Figure 5-3. THD+N vs Frequency



PVDD = 14.4V

Figure 5-4. THD+N vs Power



PVDD = 18V

Figure 5-5. THD+N vs Power

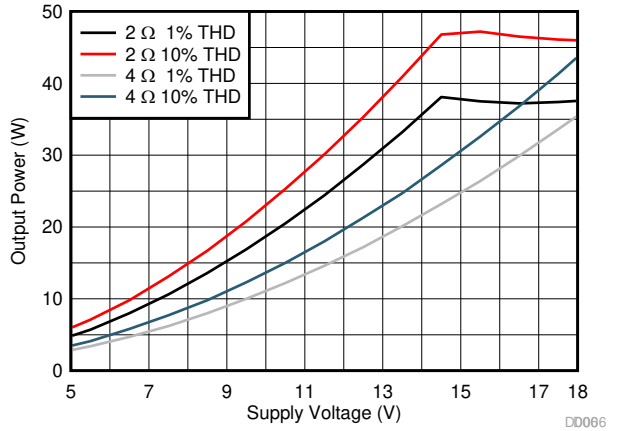


Figure 5-6. Output Power vs Supply Voltage

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5.6 Typical Characteristics (continued)

T_A = 25 °C, DVDD = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, AES17 filter, default I^2C settings, reconstruction filter inductor used: DFEG7030D-3R3M from MuRata Toko, see application diagram in Section 9.2.1.4 Figure 9-2 (unless otherwise noted)

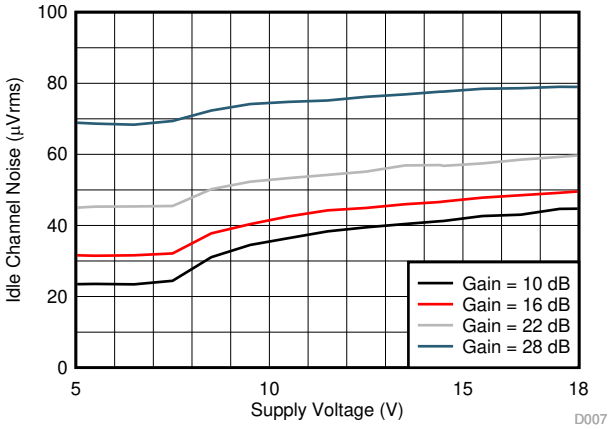
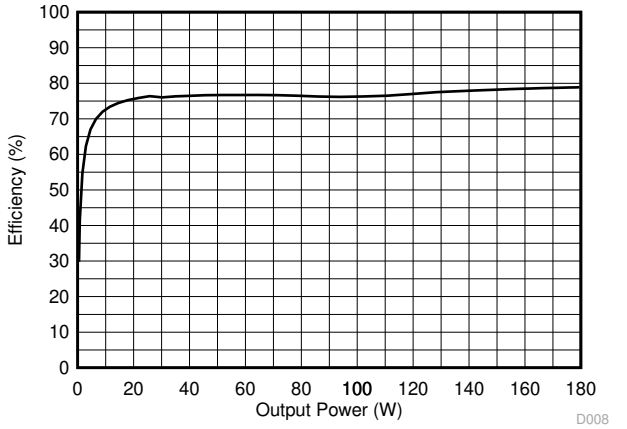
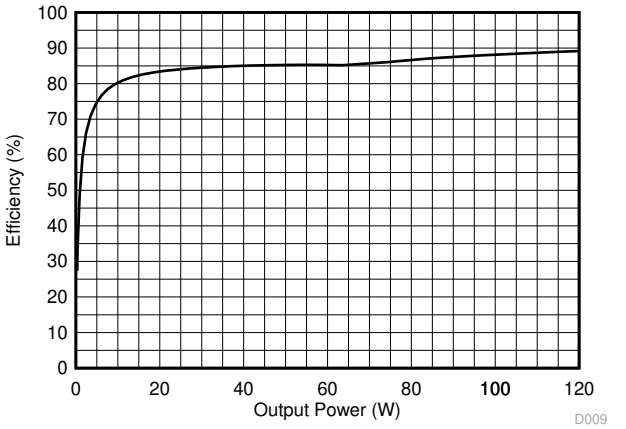


Figure 5-7. Noise vs Supply Voltage



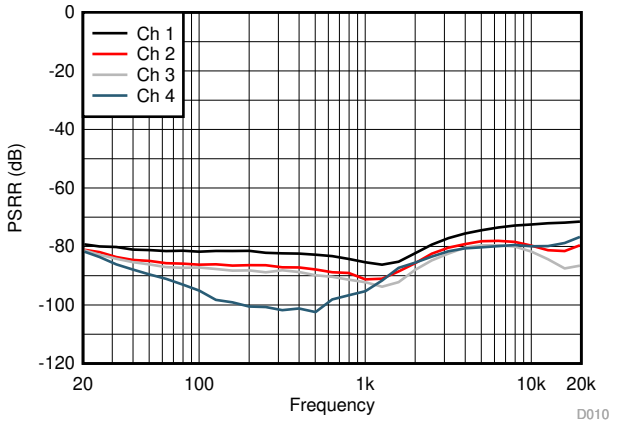
F_O= 1kHz 2Ω

Figure 5-8. Efficiency vs Output Power



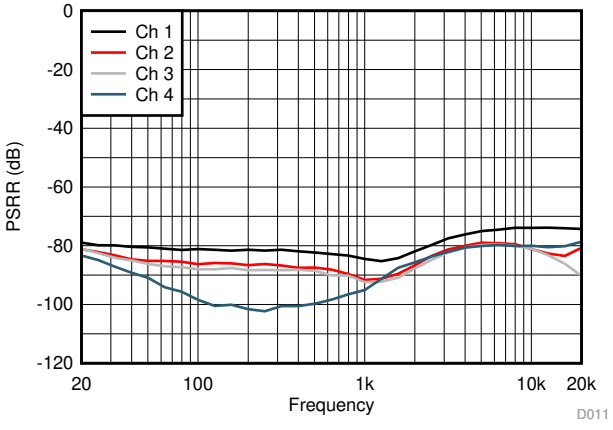
F_O= 1kHz 4Ω

Figure 5-9. Efficiency vs Output Power



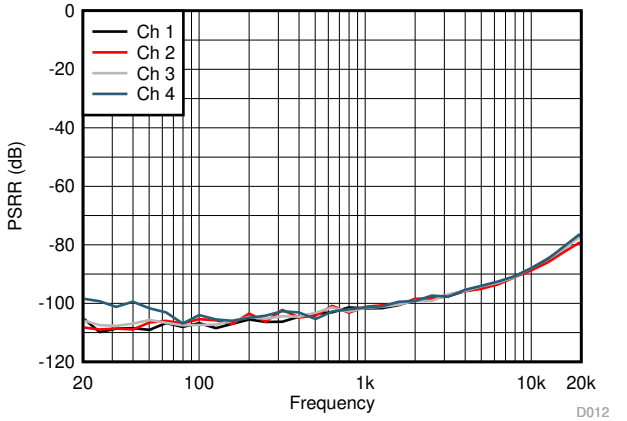
PVDD = 14.4VDC + 1Vrms

Figure 5-10. PVDD PSRR vs Frequency



PVDD = VBAT = 14.4VDC + 1Vrms

Figure 5-11. PVDD + VBAT PSRR vs Frequency



VBAT = 14.4VDC + 1Vrms

Figure 5-12. VBAT PSRR vs Frequency

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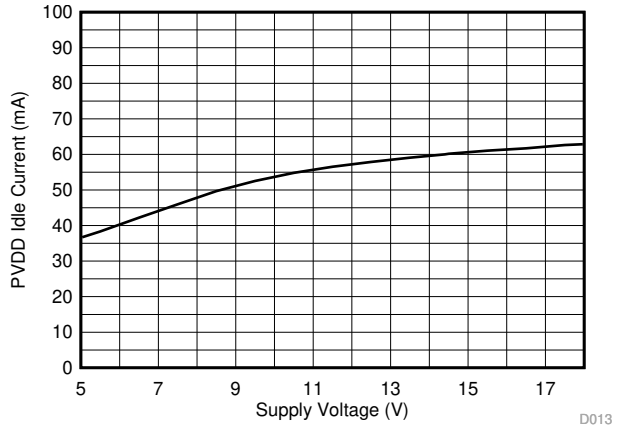
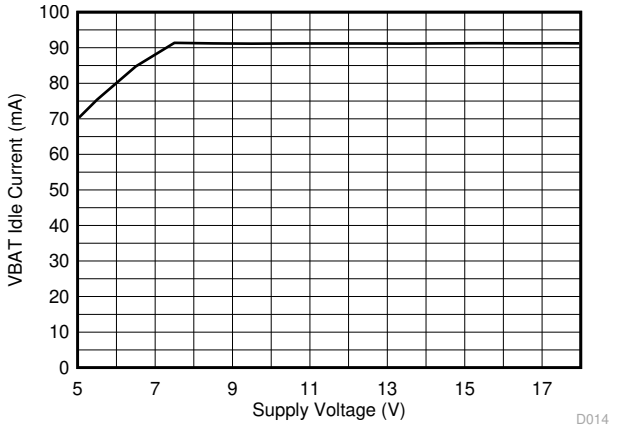
5.6 Typical Characteristics (continued)

T_A = 25 °C, DVDD = 3.3 V, VBAT = PVDD = 14.4 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, AES17 filter, default I^2C settings, reconstruction filter inductor used: DFEG7030D-3R3M from MuRata Toko, see application diagram in Section 9.2.1.4 Figure 9-2 (unless otherwise noted)



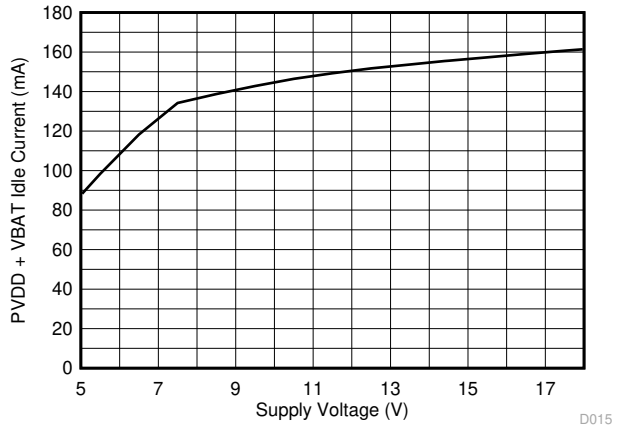
VBAT = 14.4V

Figure 5-13. PVDD Idle Current vs Supply Voltage



4Ω PVDD = 14.4V

Figure 5-14. VBAT Idle Current vs Supply Voltage



4Ω

Figure 5-15. PVDD + VBAT Idle Current vs Supply Voltage

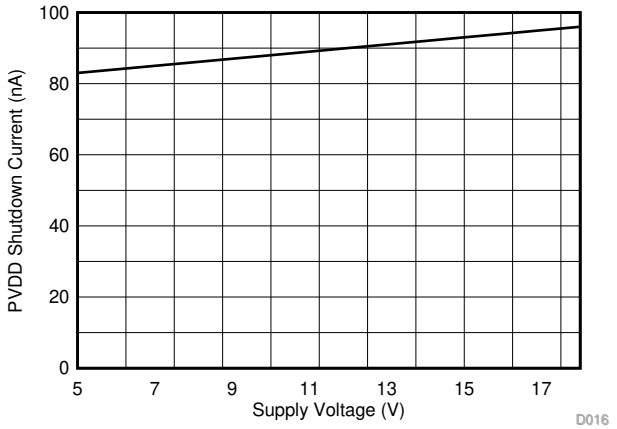


Figure 5-16. PVDD Standby Current vs Supply Voltage

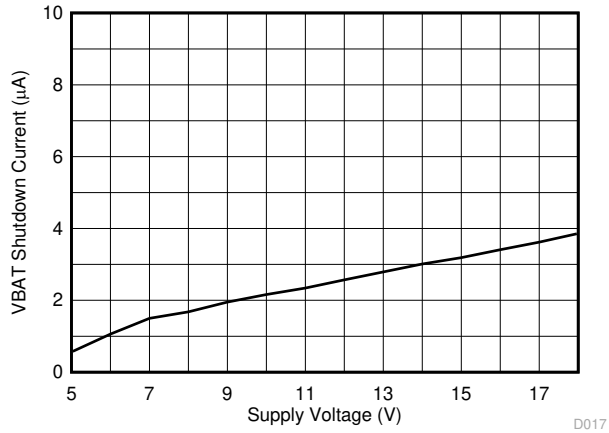


Figure 5-17. VBAT Standby Current vs Supply Voltage

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6 Parameter measurement Information

The parameters for the TPA6404-Q1 device were measured using the circuit in Section 9.2.1.

7 Detailed description

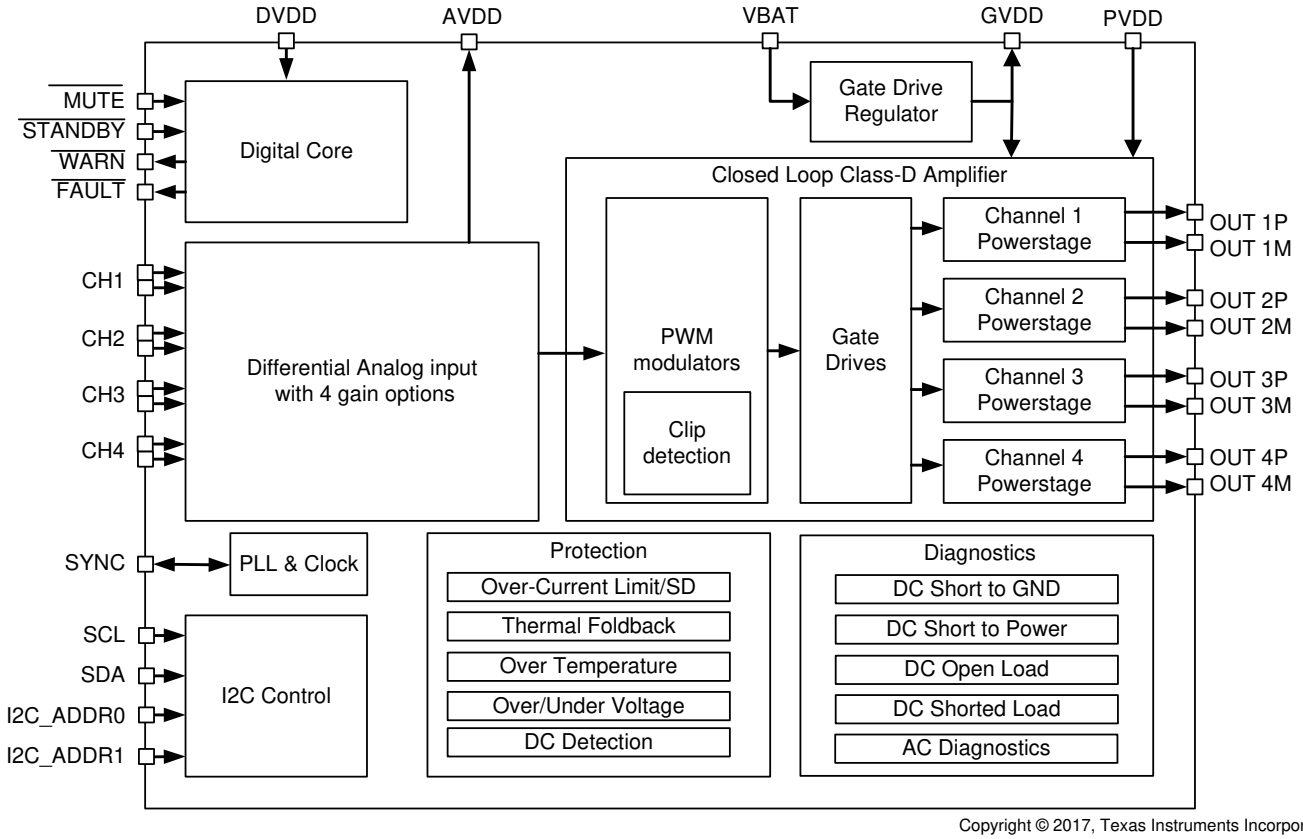
7.1 Overview

The TPA6404-Q1 device is a four-channel analog input Class-D audio amplifier, specifically tailored for use in the automotive industry. The device is designed for vehicle battery operation . The ultra-efficient Class-D technology allows for reduced power consumption, reduced PCB area, heat, and peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional Class-AB solutions.

The core design blocks are:

- Differential Analog Input
- Clock management
- Pulse width modulator (PWM) with output stage feedback
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Differential Analog inputs

The TPA6404-Q1 features balanced analog audio inputs to optimize audio performance. The differential inputs give maximum hum and noise suppression.

With a single-ended analog input it is recommended to connect the inputs as pseudo balanced for best hum and noise suppression. Figure 7-1 shows the proposed balanced and single ended connections.

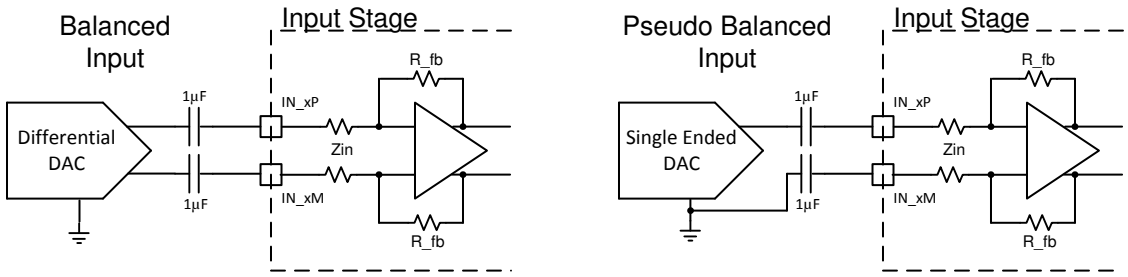

Figure 7-1. Differential Analog Input Connections

7.3.2 Gain Control and AC-Coupling

The gain of the TPA6404-Q1 is configurable in the gain control register through I^2C. There are four gain settings of 10 dB, 16 dB, 22 dB, and 28 dB. 22 dB is the default setting. It is recommended to select the lowest possible gain for the expected PVDD operation and input voltage range to minimize output noise and optimize dynamic range performance.

The combination of input voltage range and supply voltage sets the requirement for the chosen gain setting. Table 7-1 below shows examples:

Table 7-1. Input Voltage Gain Setting

INPUT VOLTAGE	SUPPLY VOLTAGE	GAIN
0.5 Vrms Single ended	14.4V	28dB
1 Vrms Single ended	14.4V	22dB
1 Vrms Differential	14.4V	16dB
2 Vrms Single ended	14.4V	16dB
2 Vrms Differential	14.4V	10dB
1 Vrms Single ended	18V	28dB
1 Vrms Differential	18V	22dB
2 Vrms Single ended	18V	22dB
2 Vrms Differential	18V	16dB

The input impedance is a function of the selected gain, see Table 7-2.

Table 7-2. Input Impedance

GAIN	INPUT IMPEDANCE	INPUT CAPACITOR	HIGH-PASS FILTER
10dB	80kΩ	1µF	2Hz
16dB	40kΩ	1µF	4Hz
22dB	20kΩ	1µF	8Hz
28dB	10kΩ	1µF	16Hz

The inputs need to be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input AC-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

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$$f = \frac{1}{2 \pi R_{in} C_{in}}$$

Figure 7-2. Input High Pass Filter Calculation

If a flat frequency response is required down to 20Hz the recommended cut-off frequency is a tenth of that, 2Hz. Table 7-2 lists the high-pass filter frequency when using a 1µF AC-coupling capacitor. If lower high-pass filter frequencies are needed then larger capacitor values should be used.

It is recommenced to use AC-coupling capacitors with low leakage current, like ceramic-, film- or quality electrolytic-capacitors.

The TPA6404-Q1 has an output DC detection built it to protect the attached speaker in case an input AC-coupling capacitor fails or has too high leakage current.

7.3.3 High-Frequency Pulse-Width Modulator (PWM)

The PWM converts the input audio data into a switched signal of varying duty cycle. The PWM modulator is an advanced design with high bandwidth, low noise, low distortion, and excellent stability.

The output switching rate is selectable via I^2C, register 0x02, and is synchronous to sync-clock input in target mode. In controller mode the sync-clock is an output.

When the device is operated in target mode, the sync pin is used to control the output stage switching frequency while in either MUTE or PLAY mode. The external clock must be applied before Hi-Z mode is exited and remain present until Hi-Z mode is entered again. During Hi-Z mode, the external clock signal is optional.

The four channels can be set to switch with 4 different phase to each other: 0, 30, 45 and 60 degree. The 45 degree setting is default and should be used unless a different phase setting is needed. With 30, 45 and 60 degree the supply ripple current will be minimum. This enables the use of smaller and lower cost external filtering components due to lower power supply ripple.

7.3.4 Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high-current, full-bridge, power-FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

The gate driver power supply voltage, GVDD, is internally generated and a decoupling capacitor must be connected at pin 6 and pin 7.

7.3.5 Power FETs

The BTL output for each channel comprises four N-channel 90 mΩ FETs for high efficiency and maximum power transfer to the load. These FETs are designed to handle large voltage transients during load dump.

7.3.6 Load Diagnostics

The device incorporates both DC- and AC-load diagnostics which are used to determine the status of the load. The DC-diagnostics are turned on by default. However, if a fast startup without diagnostics is required, the diagnostics can be bypassed through I^2C. The DC-diagnostics run when any channel is directed to leave the Hi-Z state and enter the MUTE or PLAY state. The diagnostics can also be enabled manually to run on any or all channels even if the other channels are playing audio. Diagnostics can be started from any operating condition, but if the channel is in PLAY state then the time to complete the diagnostic is longer because the device must go to the Hi-Z state. The diagnostics are available as soon as the device supplies are within the recommended operating range. The diagnostics do not rely on the audio input signals or sync frequency to be available to function since the internal oscillator is used for the diagnostic block. Diagnostic results are reported for each channel separately through the I^2C registers.

7.3.6.1 DC Load Diagnostics

The DC load diagnostics are used to verify the load is connected properly. The DC diagnostics consists of four tests: short-to-power (S2P), short-to-ground (S2G), open-load (OL), and shorted-load (SL). The S2P and S2G

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tests trigger if the impedance to ground or the impedance to power is below that specified in the *Section 5* section. The diagnostic also detects a short to vehicle battery when the supply is boosted. The SL test has an I²C-configurable threshold depending on the expected load to be connected. Because the speakers and cable impedance connected to each channel might be different, each channel can be assigned a unique threshold value. The OL test reports if the selected channel has a load impedance greater than the limits in the *Section 5* section.

The duration of DC load diagnostics can be as short as 250ms and as long as 600ms depending on any fault conditions. The time extension is due to retesting the fault conditions to reduce false positives. Additional time will be added by changing the buffer time or settling time parameters in register 0x09. Buffer time is a delay before the test starts. This is added before the S2G and S2P tests and also added before the SL and the OL tests. The Ramp time is the time that the output is ramped up and down for the SL and OL tests. The settling time is the duration of the SL and OL test.

7.3.6.1.1 Automatic DC Load Diagnostics

The DC load diagnostic is run automatically when the $\overline{\text{STANDBY}}$ pin is pulled high. This assumes that the 3.3Vdc (DVDD) for the device has already been applied. The DC diagnostics will be run on all four channels. If there is a fault on a channel or channels this test will be run again after approximately one second. It will repeat indefinitely until the fault is eliminated, the $\overline{\text{STANDBY}}$ pin is pulled low, or the diagnostics function is turned off by I²C control. This function will also be run after a channel fault.

7.3.6.1.2 I²C Controlled DC Load Diagnostics

Automatic DC load diagnostics may not be a desired function at power up, therefore, it can be bypassed by writing a one to bit 0 in register 0x09. This register must be written before the **STANDBY** pin is pulled high.

DC diagnostics can be used as follows to test all four channels:

1. For DC diagnostics, the output must be placed in Hi-Z mode by writing a 0x55 to register 0x04. This will place all four channels in Hi-Z mode
2. Write any control parameters for DC load diagnostics in Register 0x09
3. Write 0xFF to Register 0x04 to place all channels into load diagnostics mode
4. Monitor (read) register 0x0F continuously until the it changes from 0xFF to 0x55 to indicate that load diagnostics is finished
5. The load diagnostic results are stored in registers 0x0C and 0x0D

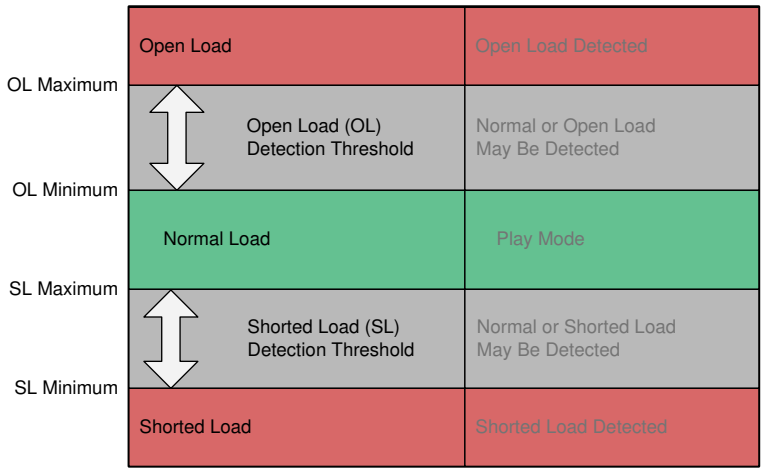

Figure 7-3. DC Load Diagnostic Reporting Thresholds

7.3.6.2 Line Output Diagnostics

The device also includes an optional test to detect a line output load. A line output load is a high-impedance load that is above the open-load (OL) threshold such that the DC-load diagnostics report an OL condition. If the line output detection bit is set to 1, when an OL condition is detected during the DC Diagnostic test, the system also

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checks if a line output load is present. This test may not be pop free, so if an external amplifier is connected it should be muted.

7.3.6.3 AC Load Diagnostics

The AC load diagnostic is used to determine the proper connection of a capacitive coupled speaker or tweeter when used with a passive crossover. The AC load diagnostic is controlled through I^2C. The TPA6404-Q1 provides a required signal source to determine the AC impedance and reports the approximate load impedance and phase to I^2C registers. The I^2C selected test frequency should create current flow through the desired speaker for proper detection. If multiple channels are to be tested, the diagnostics must be run in each channel separately as the results share the same I^2C reporting register. When testing a channel multiple times, it is required to wait at least 200ms before rerunning AC load diagnostics on the same channel.

Note

If an Undervoltage, Overvoltage or Overtemperature fault occurs during AC diagnostics, the AC diagnostics is stopped. AC Diagnostics will not be allowed to be performed again until the DC Diagnostics are performed. This is to ensure the fault is not potentially a hazard during AC diagnostics.

For load-impedance detection, there are three separate groups of processes that must be performed.

- Impedance phase reference measurement
- Impedance phase measurement of the load and calculation
- Impedance magnitude measurement and calculation

7.3.6.3.1 Impedance Phase Reference Measurement

The first stage is to utilize the built-in loopback mode to determine the reference value for the phase measurement. This reference will nullify any phase offset in the device and measure only the phase of the load. This is measured for channels 1 and 3 only. Channel 2 will use the results of channel 1 for the calculations. Channel 4 will use the results of channel 3 for the calculations. Measure channel 1 and channel 3 sequentially, they cannot be measured at the same time.

For loopback delay detection, use the following test procedure:

BTL Mode

1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to 1 to enable loopback mode
2. Set the appropriate test frequency in register 0x2A, the default is set for 18.75kHz
3. For channel 1 set bit 3 in register 0x15 to 1. For channel 3 set bit 1 in register 0x15 to 1
4. Read back the hexadecimal, AC_LDG_PHASE1 value. Register 0x1B holds the MSB and register 0x1C holds the LSB
5. For channel 1 set bit 3 in register 0x15 to 0. For channel 3 set bit 1 in register 0x15 to 0

PBTL Mode

1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to 1 to enable AC loopback mode
2. Set the PBTL CH12 and PBTL CH34 bits (bits 5 and 4 in register 0x00) to 0. This must be performed while the device is in the STANDBY state to enter BTL mode only for load diagnostics
3. Set the appropriate test frequency in register 0x2A, the default is set for 18.75kHz
4. For channel 1 set bit 3 in register 0x15 to 1. For channel 3 set bit 1 in register 0x15 to 1
5. Read back the hexadecimal, AC_LDG_PHASE1 value. Register 0x1B hold the MSB and register 0x1C holds the LSB
6. Set the PBTL CH12 and PBTL CH34 bits (bits 5 and 4 in register 0x00) to 1 to go back to PBTL mode for load diagnostics
7. For channel 1 set bit 3 in register 0x15 to 0. For channel 3 set bit 1 in register 0x15 to 0

When the test is complete, the channel reporting register (0x0F) indicates the status change from the AC diagnostic mode to the Hi-Z state. The detected reference phase is stored in the appropriate I^2C register when the device transitions to the Hi-Z state.

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7.3.6.3.2 Impedance Phase Measurement

After performing the phase reference measurements, measure the phase of the speaker load. This is performed in the same manner as the reference measurements, except the loopback is disabled in bit 7 register 0x16. Previously, the phase reference is measured on channel 1 and channel 3 and in this test stage; all four channels will be measured. Measure the channels sequentially as they cannot be measured at the same time.

1. Set the channel to be tested into the Hi-Z state
2. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to 0
3. Set the appropriate test frequency in register 0x2A, the default is set for 18.75kHz
4. Set the device into the AC diagnostic mode (set bit 3 through bit 0 as needed in register 0x15 to 1 for CH1 to CH4. (For PBTL mode, test channel 1 for PBTL12 and channel 3 for PBTL34))
5. Read back the 16bit hexadecimal, AC_LDG_PHASE value. Register 0x1B holds the MSB and register 0x1C holds the LSB
6. Read back the hexadecimal stimulus value, STI. Register 0x1D holds the MSB and register 0x1E holds the LSB
7. Disable the AC diagnostic mode (set bit 3 through bit 0 as needed in register 0x15 to 0 for CH1 to CH4. (For PBTL mode, disable channel 1 for PBTL12 and channel 3 for PBTL34))

When the test is complete the channel reporting register indicates the status change from the AC diagnostic mode to the Hi-Z state. The detected phase is stored in the appropriate I2C register when the device transitions to the Hi-Z state.

The AC phase in degrees is calculated with the following equation:

$$Phase\_CHx = 360(\frac{Phase\_CHx(LBK) - Phase\_CHx(LDM)}{STI\_CHx(LDM)})$$

Figure 7-4. AC Phase Calculation

Where:

Phase_CHx(LBK) is the reference phase measurement

Phase_CHx(LDM) is the phase measure of the load

STI_CHx(LDM) is the stimulus value

7.3.6.3.3 Impedance Magnitude Measurement

The impedance magnitude value was measured during the second stage or phase measurement stage. These values are stored in register 0x17 through 0x1A, one register per channel. The hexadecimal value must be converted to decimal and used to calculate the impedance magnitude using the following equation:

$$Channelx\ Impedance = \frac{Impedance\_CHx \times 2.371mV}{(Gain)(I\ mA)}\ (Ohms)$$

Figure 7-5. AC Magnitude Calculation

Where:

Gain is the value chosen in register 0x15

I is the current chosen in register 0x16

An alternative is to use the values in Table 7-3 to determine the magnitude of the impedance using the ohms / code value. Change the code to decimal for this calculation.

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Table 7-3. AC Impedance Code to Magnitude

Setting	Gain at 18.75kHz Ohm / Code (decimal)	I (mA)	Impedance Range	Ohm / Code (decimal)
Reg 0x15 bit 7, 5 = 1 Reg 0x16 bit 2 = 1	4	20	0 to 6Ohms	0.029643
Reg 0x15 bit 7, 5 = 1 Reg 0x16 bit 2 = 0	4	10	0 to 12Ohms	0.059287
Reg 0x15 bit 7, 5 = 0 Reg 0x16 bit 2 = 1	1	20	0 to 24Ohms	0.11857
Reg 0x15 bit 7, 5 = 0 Reg 0x16 bit 2 = 0	1	10	0 to 48Ohms	0.23714

7.3.7 Protection and Monitoring

7.3.7.1 Over current Limit (I_{LIMIT})

The over current limit terminates each PWM pulse to limit the output current flow when the current limit (I_{LIMIT}) is exceeded. Power is limited but operation continues without disruption and prevents undesired shutdown for transient music events.

If the current is limited for 45% of the PWM cycles in a 200ms window, I_{LIMIT_WARN} is reported. If the current limit warning is triggered for 400ms, I_{LIMIT_FAULT} is reported and the channel is set in Hi-Z.

Each channel is independently monitored and limited. There are two programmable levels that can be set by the miscellaneous control 1 register, 0x01 bit 4. The current limit values can be seen in Section 5.5.

7.3.7.2 Over current Shutdown (I_{SD})

If the output load current reaches I_{SD}, such as an output short to GND or power supply, then a peak current limit occurs which shuts down the channel. The time to shutdown the channel varies depending on the severity of the short condition. The affected channel is placed into the Hi-Z state, the fault is reported to the register, and the $\overline{FAULT}$ pin is asserted. The device will remain in this state until the CLEAR FAULT bit is set in Miscellaneous Control 3 Register, 0x21 bit 7. After clearing this bit and if the diagnostics are enabled, the device will automatically start diagnostics on the channel and, if no load failure is found, the device will restart. If a load fault is found the device continues to rerun the diagnostics once per second. Because this hiccup mode is using the diagnostics, no high current is created. If the diagnostics are disabled the device sets the state for that channel to Hi-Z and requires the MCU to take the appropriate action, setting the CLEAR FAULT bit after the fault got removed, in order to return to Play state.

There are two programmable levels that can be set by the miscellaneous control 1 register, 0x01 bit 4.

7.3.7.3 DC Detect

This circuit detects a DC offset continuously during normal operation in PLAY mode at the output of the amplifier. If the DC offset exceeds the threshold, that channel is placed in the Hi-Z state, the fault is reported to the I^2C register, and the $\overline{FAULT}$ pin is asserted. A register bit can be used to mask reporting to the $\overline{FAULT}$ pin if needed.

7.3.7.4 Clip Detect

The clip detect reporting level can be set to 1%, 2%, 5% or 10%; and the reporting can be programmed over I^2C. If any channel is in clipping, it is reported to the internal I^2C channel register and the register reporting is latched. By default all channels also report to the $\overline{WARN}$ pin. It can be split into two sections: channel 1 and 2 on the $\overline{WARN}$ pin, and channels 3 and 4 on $\overline{FAULT}$ pin. All pin reporting can be set to latched or non-latched. It is also possible to mask the clip reporting to the pin through I^2C.

As an example, a sine wave signal that is clipped with a THD at the reporting level would provide a pulse at each part of the waveform that is clipped. The duty cycle of the pulse will be between 2% and 6% when the THD is at the reporting level. This assumes the Clip Reporting Latch is disabled by setting register 0x27, bit 0 to 0.

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7.3.7.5 Global Over Temperature Warning (OTW), Over Temperature Shutdown (OTSD) and Thermal Foldback (TFB)

Four over temperature warning levels are available in the device that can be selected (see the *Section 8.1* section for thresholds). When the junction temperature exceeds the warning level, the $\overline{\text{WARN}}$ pin is asserted unless the mask bit has been set to disable reporting. The device functions until OTSD value is reached at which point all channels are placed in the Hi-Z state and the $\overline{\text{FAULT}}$ pin is asserted. When the junction temperature returns to normal levels, the device automatically recovers and places all channels into the state indicated by value in the Channel State Control Register (address = 0x04). The tolerance of the warning levels and OTSD temperatures track each other.

When Thermal Foldback (TFB) is enabled, register 0x28 bit 5, the device automatic reduces the gain and thereby output power when either the global thermal warning, OTW, or the channel thermal warning, OTW(i) signals an over temperature. The attack and release time of the TFB can be programmed from by the register 0x28. The gain is stepped in 1 dB steps with a max attenuation of 12 dB.

7.3.7.6 Channel Over Temperature Warning [OTW(i)] and Shutdown [OTSD(i)]

In addition to the global OTW, each channel also has an individual over temperature warning and shutdown. If a channel exceeds the OTW(i) threshold, the warning register bit is set as the $\overline{\text{WARN}}$ pin is asserted unless the mask bit has been set to disable reporting. If the channel temperature exceeds the OTSD(i) threshold, then that channel goes to the Hi-Z state until the temperature drops below the OTW(i) threshold at which point the channel changes state as indicated by the state control register.

7.3.7.7 Thermal Foldback

The thermal foldback (TFB) circuitry is designed to protect the TPA6404-Q1 from excessive die temperature. This can be caused by being operated beyond the recommended operating temperature or with a weaker thermal system than recommended. The TFB reduces the on die power dissipation by reducing the closed loop gain in steps of 1.0dB, when the temperature exceeds the TFB temperature specification. The gain will increase as the temperature is reduced by the same gain step. The rate of gain reduction (attack) is controlled in register 0x28 bits 2 and 3. The rate of gain increase or recovery (release) is controlled in register 0x28 bits 0 and 1. Pop free gain changes are control by enabling a zero crossing detector, which is enabled by default in register 0x28 bit 4. The zero crossing has a wait time before the gain can change. The default is 20µs and can be increased in register 0x28 bits 7 and 8. The TFB is enabled by default and can be disabled in register 0x28 bit 5.

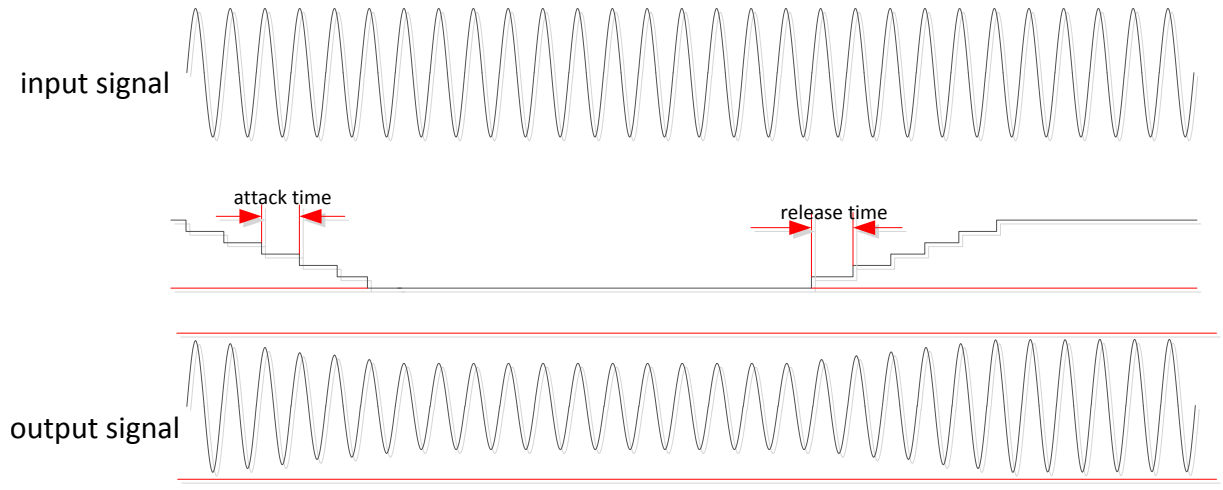

Figure 7-6. Thermal Foldback Attack and Release

7.3.7.8 Undervoltage (UV) and Power-On-Reset (POR)

The undervoltage (UV) protection detects low voltages on the PVDD and VBAT pins. In the event of an undervoltage condition, the $\overline{\text{FAULT}}$ pin is asserted and the I^2C register is updated. A POR on the DVDD pin causes the I^2C to go into a high-impedance (Hi-Z) state and all registers are reset to default values. At power-on or after a POR event, the POR warning bit and $\overline{\text{WARN}}$ pin are asserted.

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7.3.7.9 Over Voltage (OV) and Load Dump

The OV protection detects high voltages on the PVDD pin. If the PVDD pin reaches the over voltage threshold, the $\overline{\text{FAULT}}$ pin is asserted and the I^2C register is updated. The device can withstand 40V load-dump voltage spikes.

7.3.8 Power Supply

The device has three power supply inputs: DVDD, PVDD, and VBAT, which are described as follows:

- DVDD – This pin is a 3.3V supply pin that provides power to the digital circuitry
- VBAT – This pin is a higher voltage supply that can be connected to the vehicle battery or the regulated voltage rail in a boosted system within the recommended limits. For best performance, this rail should be 10V or higher. See the Section 5.3 table for the maximum supply voltage. This supply rail is used for higher voltage analog circuits but not the output FETs
- PVDD – This pin is a high-voltage supply that can either be connected to the vehicle battery or to another voltage rail in a boosted system. The PVDD pin supplies the power to the output FETs and can be within the recommended operating limits, even if that is below the VBAT supply, to allow for dynamic voltage systems

On-chip regulators are included, generating the GVDD_X voltages necessary for the gate drive circuitry. The GVDD supply pins are provided only for bypass capacitors to filter the supply and should not be used to power other circuits.

The device can withstand fortuitous open ground and power conditions within the Section 5.1 ratings for the device. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs.

7.3.8.1 Power-Supply Sequence

No special power supply sequence is required.

7.3.9 Hardware Control Pins

The device has two control pins: $\overline{\text{MUTE}}$ and $\overline{\text{STANDBY}}$, and two status pins: $\overline{\text{WARN}}$ and $\overline{\text{FAULT}}$.

7.3.9.1 $\overline{\text{FAULT}}$

The $\overline{\text{FAULT}}$ pin reports faults and is active low under any of the following conditions:

- Any channel faults (over current or DC detection)
- Over temperature shutdown
- Over voltage or undervoltage conditions on the VBAT or PVDD pins
- Clock errors
- Clip Detection indicators can also be routed to the $\overline{\text{FAULT}}$ pin. This indicator can be configured as latching or non-latching.

The $\overline{\text{FAULT}}$ pin is latching, and can be cleared by writing to register 0x21 bit 7.

Register bits are available to mask fault categories from reporting to the $\overline{\text{FAULT}}$ pin. These bits only mask the setting of the pin and do not affect the register reporting or protection of the device. By default all faults are reported to the pin. See the *Section 8.1* section for a description of the mask settings.

The $\overline{\text{FAULT}}$ pin can also be programmed to show clip detect for channel 3 and 4.

This pin is an open-drain output with an internal 100kΩ pull-up resistor to DVDD.

7.3.9.2 $\overline{\text{WARN}}$

This active low output pin reports audio clipping, over temperature warnings and POR events.

- Clip Detect is reported if any channel is above the programmed THD threshold
- Over temperature warning (OTW) is reported if the general temperature or any of the channel temperature warnings are set. The warning temperature can be set in register 0x01 bit 5-6
- Register bits are available to mask either Clip Detect or OTW reporting to the pin. These bits only mask the setting of the pin and do not affect the register reporting. By default both Clip Detect and OTW are reported
- This pin is an open-drain output with an internal 100kΩ pull-up resistor to DVDD

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7.3.9.3 $\overline{\text{MUTE}}$

This active low input pin is used for hardware control of the mute and un-mute function for all channels. When the $\overline{\text{Mute}}$ pin is set low, all channels stop switching and are set to Hi-Z mode. All internal analog circuitry is biased and enabled, and the input AC-coupling capacitors are charged.

The hardware $\overline{\text{Mute}}$ function is ORed with the I^2C $\overline{\text{Mute}}$ functioned. If either function is set, the $\overline{\text{Mute}}$ function is asserted.

This pin has a 100kΩ internal pull-down resistor.

7.3.9.4 $\overline{\text{STANDBY}}$

The $\overline{\text{STANDBY}}$ pin is active low. The device is in a low current mode on the PVDD and VBAT pins while the output pins are placed into a Hi-Z state. All internal analog bias is disabled. In $\overline{\text{STANDBY}}$ and while DVDD is present, the I^2C bus is active and the internal registers are active.

This pin has a 1MΩ internal pull-down resistor.

7.4 Device Functional Modes

7.4.1 Operating Modes and Faults

The operating modes and faults are listed in Table 7-4, Table 7-5, and Table 7-6.

Table 7-4. Operating Modes

STATE NAME	OUTPUT FETS	OSCILLATOR	I^2C
STANDBY	Hi-Z	Stopped	Active
Hi-Z	Hi-Z	Active	Active
MUTE	Hi-Z	Active	Active
PLAY	Switching with audio	Active	Active

Table 7-5. Global Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION RESULT
POR	Voltage fault	All	I^2C + $\overline{\text{WARN}}$ pin	Standby
VBAT UV		Hi-Z, MUTE, PLAY	I^2C + $\overline{\text{FAULT}}$ pin	Hi-Z
PVDD UV				
VBAT or PVDD OV				
OTW	Thermal warning	Hi-Z, MUTE, PLAY	I^2C + $\overline{\text{WARN}}$ pin	None
OTSD	Thermal shutdown	Hi-Z, MUTE, PLAY	I^2C + $\overline{\text{FAULT}}$ pin	Hi-Z
INVALID CLOCK(1)	Sync Clock Fault	MUTE and PLAY	I^2C + $\overline{\text{FAULT}}$ pin	Hi-Z

(1) Monitored only when the device is configured in TARGET mode

Table 7-6. Channel Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE
Clipping	Warning (can be latched or unlatched)	MUTE and PLAY	$\overline{\text{WARN}}$ pin + $\overline{\text{FAULT}}$ pin	None
Overcurrent limiting	Protection		$\overline{\text{WARN}}$ pin	Current limit
Overcurrent fault	Output channel fault		I^2C + $\overline{\text{FAULT}}$ pin	Hi-Z
DC detect				

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7.5 Programming

7.5.1 I²C Serial Communication Bus

The device communicates with the system processor via the I²C serial communication bus as an I²C target-only device. The processor can poll the device via I²C to determine the operating status, configure settings, or run diagnostics. For a complete list and description of all I²C controls, see the *Section 8.1* section.

The device includes two I²C address pins, so up to four devices can be used together in a system with no additional bus switching hardware. The I²C ADDRx pins set the target address of the device as listed in Table 7-7.

Table 7-7. I²C Addresses

DESCRIPTION	I²C ADDR1	I²C ADDR0	I²C Write	I²C Read
Device 0	0	0	0x54	0x55
Device 1	0	1	0x56	0x57
Device 2	1	0	0x58	0x59
Device 3	1	1	0x5A	0x5B

7.5.2 I²C Bus Protocol

The device has a bidirectional serial control interface that is compatible with the Inter IC (I²C) bus protocol and supports 100 and 400-kbps data transfer rates for random and sequential write and read operations. This is a target-only device that does not support a multicontroller bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I²C bus uses two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the controller device driving a start condition on the bus and ends with the controller device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. The controller generates the 7-bit target address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The device holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the controller transmits the next byte of the sequence. Each device is addressed by a unique 7-bit target address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the controller generates a stop condition to release the bus.

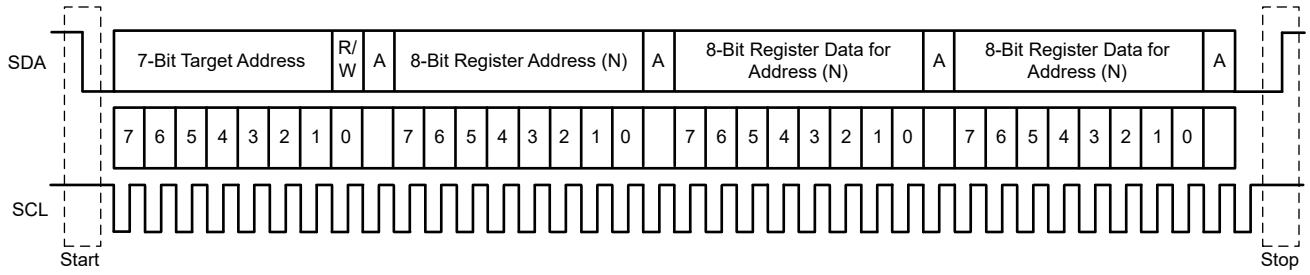

Figure 7-7. Typical I²C Sequence

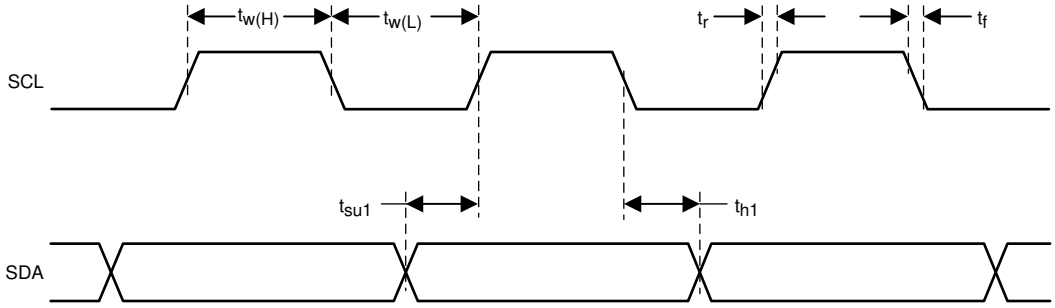

Figure 7-8. SCL and SDA Timing

Use the I²C ADDRx pins to program the device target address. Read and write data can be transmitted using single-byte or multiple-byte data transfers.

7.5.3 Random Write

As shown in Figure 7-9, a single-byte data-write transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the controller transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the controller device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the controller device transmits a stop condition to complete the single-byte data-write transfer.

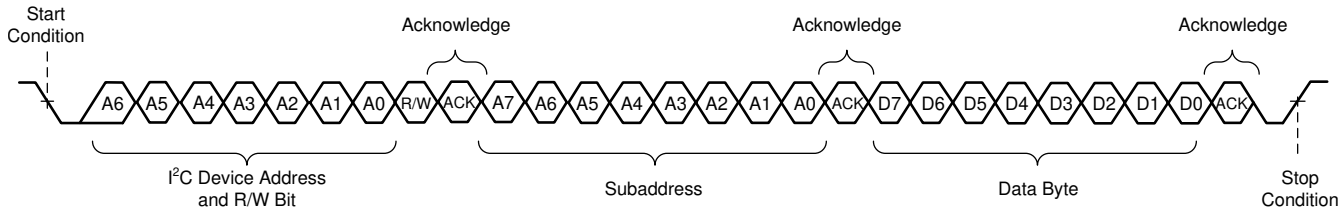

Figure 7-9. Random Write Transfer

7.5.4 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the controller to the device as shown in Figure 7-10. After receiving each data byte, the device responds with an acknowledge bit and the I²C subaddress is automatically incremented by one.

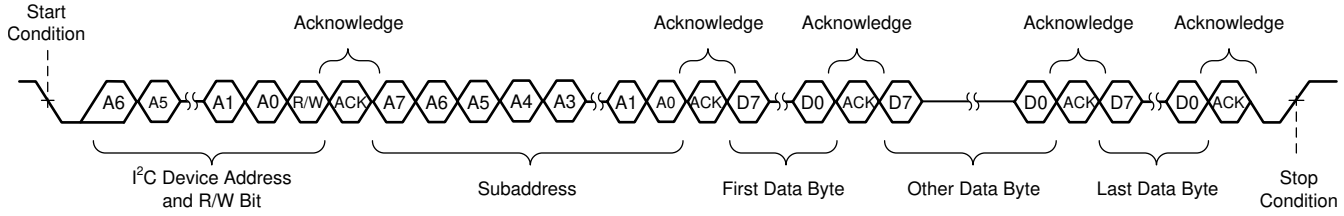

Figure 7-10. Sequential Write Transfer

7.5.5 Random Read

As shown in Figure 7-11, a single-byte data-read transfer begins with the controller device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write

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bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the controller device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

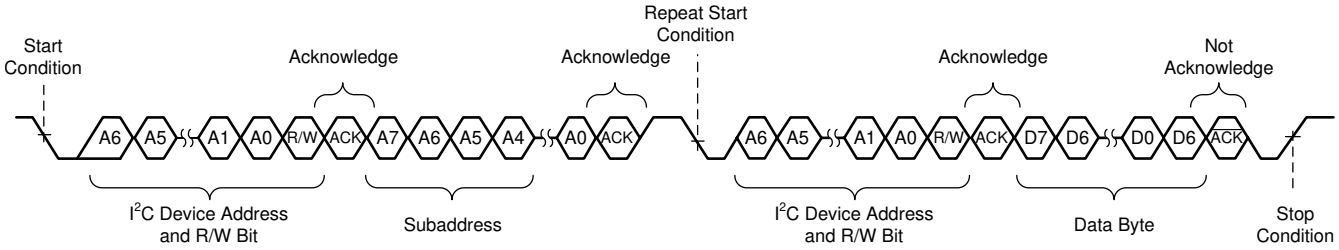

Figure 7-11. Random Read Transfer

7.5.6 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the controller device as shown in Figure 7-12. Except for the last data byte, the controller device responds with an acknowledge bit after receiving each data byte and automatically increments the I²C subaddress by one. After receiving the last data byte, the controller device transmits a not-acknowledge followed by a stop condition to complete the transfer.

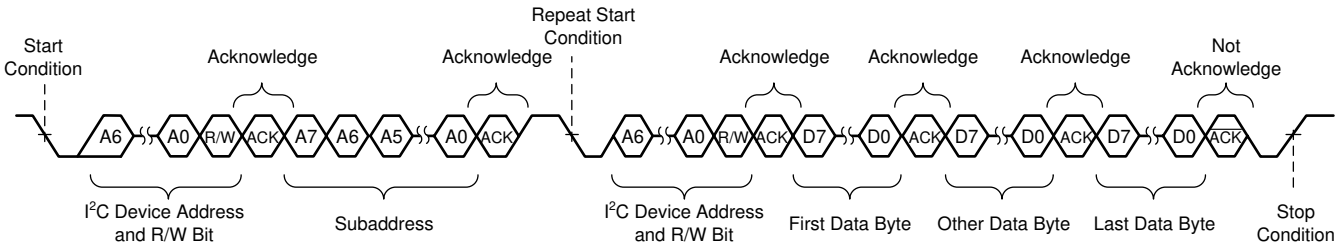

Figure 7-12. Sequential Read Transfer

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8 Registers

8.1 Register Maps

Table 8-1. I²C Address Register Definitions

Address	Type	Register Description	Section
0x00	R/W	Mode control	Mode control
0x01	R/W	Miscellaneous control 1	Misc control 1
0x02	R/W	Miscellaneous control 2	Misc control 2
0x03	R	RESERVED	
0x04	R/W	Channel state control	Ch state control
0x05	R	RESERVED	
0x06	R	RESERVED	
0x07	R	RESERVED	
0x08	R	RESERVED	
0x09	R/W	DC diagnostic control 1	DC diag control 1
0x0A	R/W	DC diagnostic control 2	DC diag control 2
0x0B	R/W	DC diagnostic control 3	DC diag control 3
0x0D	R	DC load diagnostic report channels 3 and 4	DC diag rprt Ch 3,4
0x0E	R	DC load diagnostic report: line output	DC diag rprt LO
0x0F	R	Channel state reporting	Ch state rprt
0x10	R	Channel faults (over current, DC detection)	Ch faults
0x11	R	Global faults 1	Global faults 1
0x12	R	Global faults 2	Global faults 2
0x13	R	Warnings	Warnings
0x14	R/W	Pin control	Pin Control
0x15	R/W	AC load diagnostic control 1	AC diag control 1
0x16	R/W	AC load diagnostic control 2	AC diag control 2
0x17	R	AC load diagnostic report channel 1	AC diag reprt Ch1
0x18	R	AC load diagnostic report channel 2	AC diag reprt Ch2
0x19	R	AC load diagnostic report channel 3	AC diag reprt Ch3
0x1A	R	AC load diagnostic report channel 4	AC diag reprt Ch4
0x1B	R	AC load diagnostic Phase High	AC diag Phase Hi
0x1C	R	AC load diagnostic Phase Low	AC diag phase lo
0x1D	R	AC load diagnostic STI High	AC diag STI hi
0x1E	R	AC load diagnostic STI Low	AC diag STI lo
0x1F	R	RESERVED	
0x20	R	RESERVED	
0x21	R/W	Miscellaneous control 3	Misc control 3
0x22	R/W	Clip control	Clip control
0x23	R	RESERVED	
0x24	R/W	Clip warning	Clip warn
0x25	R/W	Current Limit Status	I-Limit status
0x26	R	RESERVED	
0x27	R/W	Fault and Warning Pin Control	Fault/Warn pin control
0x28	R/W	Thermal Foldback Control	Therm Fb control
0x29	R	RESERVED	
0x2A	R/W	AC Diagnostic Frequency Control	AC diag freq control

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Table 8-1. I²C Address Register Definitions (continued)

Address	Type	Register Description	Section
0x2B	R/W	SYNC PIN CONTROL	Sync pin control

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8.1.1 Mode Control Register (address = 0x00) [default = 0x00]

The Mode Control register is shown in Figure 8-1 and described in Table 8-2.

Figure 8-1. Mode Control Register

7	6	5	4	3	2	1	0
RESET	RESERVED	PBTL_34	PBTL_12	CH1 LO MODE	CH2 LO MODE	CH3 LO MODE	CH4 LO MODE
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-2. Mode Control Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0	**0: Normal operation** 1: Resets the device
6	RESERVED	R	0	
5	PBTL_34	R/W	0	**0: BTL mode** 1: PBTL mode
4	PBTL_12	R/W	0	**0: BTL mode** 1: PBTL mode
3	CH1 LO MODE	R/W	0	**0: Channel 1 is in normal/speaker mode** 1: Channel 1 is in line output mode
2	CH2 LO MODE	R/W	0	**0: Channel 2 is in normal/speaker mode** 1: Channel 2 is in line output mode
1	CH3 LO MODE	R/W	0	**0: Channel 3 is in normal/speaker mode** 1: Channel 3 is in line output mode
0	CH4 LO MODE	R/W	0	**0: Channel 4 is in normal/speaker mode** 1: Channel 4 is in line output mode

8.1.2 Miscellaneous Control 1 Register (address = 0x01) [default = 0x32]

The Miscellaneous Control 1 register is shown in Figure 8-2 and described in Table 8-3.

Figure 8-2. Miscellaneous Control 1 Register

7	6	5	4	3	2	1	0
PI_EN	OTW CONTROL		OC CONTROL	RESERVED		GAIN	
R/W	R/W	R/W	R/W	R	R	R/W	R/W

Table 8-3. Misc Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	PI_EN	R/W	0	**0: Pulse Injector disabled** 1: Pulse Injector enabled
6–5	OTW CONTROL	R/W	01	00: Global over temperature warning set to 140°C **01: Global over temperature warning set to 130C** 10: Global over temperature warning set to 120°C 11: Global over temperature warning set to 110°C
4	OC CONTROL	R/W	1	0: Over current is level 1 **1: Over current is level 2**
3–2	RESERVED		00	
1–0	GAIN	R/W	10	00: 10dB 01: 16dB **10: 22dB** 11: 28dB

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8.1.3 Miscellaneous Control 2 Register (address = 0x02) [default = 0x62]

The Miscellaneous Control 2 register is shown in Figure 8-3 and described in Table 8-4.

Figure 8-3. Miscellaneous Control 2 Register

7	6	5	4	3	2	1	0
RESERVED	PWM FREQUENCY			RAMP_SYNC_PHASE_SEL		OUTPUT PHASE	
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-4. Misc Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	
6–4	PWM FREQUENCY	R/W	110	000: RESERVED 001: RESERVED 010: RESERVED 011: RESERVED 100: RESERVED 101: 1.8 MHz **110: 2.1 MHz** 111: 2.3 MHz
3-2	Ramp Sync Phase Select in Controller Mode (Ramp phase is referenced to selected channel)	R/W	00	**00: CH 4** 01: CH 3 10: CH 2 11: CH 1
1–0	PWM OUTPUT PHASE	R/W	10	00: 0 degrees output-phase switching offset 01: 30 degrees output-phase switching offset **10: 45 degrees output-phase switching offset** 11: 60 degrees output-phase switching offset

8.1.4 Channel State Control Register (address = 0x04) [default = 0x55]

The Channel State Control register is shown in Figure 8-4 and described in Table 8-5.

Figure 8-4. Channel State Control Register

7	6	5	4	3	2	1	0
CH1 STATE CONTROL		CH2 STATE CONTROL		CH3 STATE CONTROL		CH4 STATE CONTROL	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-5. Channel State Control Field Descriptions

Bit	Field	Type	Reset	Description
7–6	CH1 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
5–4	CH2 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
3–2	CH3 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics

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Table 8-5. Channel State Control Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1–0	CH4 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics

8.1.5 DC Load Diagnostic Control 1 Register (address = 0x09) [default = 0x00]

The DC Diagnostic Control 1 register is shown in Figure 8-5 and described in Table 8-6.

Figure 8-5. DC Load Diagnostic Control 1 Register

7	6	5	4	3	2	1	0
DC LDG ABORT	RAMP	SETTLE	BUFF		REPORT	LDG LO ENABLE	LDG BYPASS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-6. DC Load Diagnostics Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	DC LDG ABORT	R/W	0	**0: Default state, clear after abort** 1: Aborts the load diagnostics in progress
6	RAMP TIME - DC DIAG	R/W	0	**0: Default ramp time = 10ms** 1: Half ramp time = 5ms
5	SETTLING TIME - DC DIAG	R/W	0	**0: Default Settle time = 15ms** 1: Double settling time = 30ms
4–3	BUFFER TIME - DC DIAG	R/W	00	**00: 1ms** 01: 10ms 10: 5ms
2	REPORT	R/W	0	**0: Do not report DC diagnostic fault on fault pin** 1: Report DC diagnostic fault on fault pin
1	LDG LO ENABLE	R/W	0	**0: Line output diagnostics are disabled** 1: Line output diagnostics are enabled
0	LDG BYPASS	R/W	0	**0: Automatic diagnostics when leaving Hi-Z and after channel fault** 1: Diagnostics are not run automatically

8.1.6 DC Load Diagnostic Control 2 Register (address = 0x0A) [default = 0x11]

The DC Diagnostic Control 2 register is shown in Figure 8-6 and described in Table 8-7.

Figure 8-6. DC Load Diagnostic Control 2 Register

7	6	5	4	3	2	1	0
CH1 DC LDG SL				CH2 DC LDG SL			
R/W				R/W			

Table 8-7. DC Load Diagnostics Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CH1 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

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Table 8-7. DC Load Diagnostics Control 2 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3–0	CH2 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

8.1.7 DC Load Diagnostic Control 3 Register (address = 0x0B) [default = 0x11]

The DC Diagnostic Control 3 register is shown in Figure 8-7 and described in Table 8-8.

Figure 8-7. DC Load Diagnostic Control 3 Register

7	6	5	4	3	2	1	0
CH3 DC LDG SL				CH4 DC LDG SL			
R/W				R/W			

Table 8-8. DC Load Diagnostics Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CH3 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω
3–0	CH4 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

8.1.8 DC Load Diagnostic Report 1 Register (address = 0x0C) [default = 0x00]

DC Load Diagnostic Report 1 register is shown in Figure 8-8 and described in Table 8-9.

Figure 8-8. DC Load Diagnostic Report 1 Register

7	6	5	4	3	2	1	0
CH1 S2G	CH1 S2P	CH1 OL	CH1 SL	CH2 S2G	CH2 S2P	CH2 OL	CH2 SL
R	R	R	R	R	R	R	R

Table 8-9. DC Load Diagnostics Report 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 S2G	R	0	**0: No short-to-GND detected** 1: Short-To-GND Detected
6	CH1 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
5	CH1 OL	R	0	**0: No open load detected** 1: Open load detected
4	CH1 SL	R	0	**0: No shorted load detected** 1: Shorted load detected

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Table 8-9. DC Load Diagnostics Report 1 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH2 S2G	R	0	**0: No short-to-GND detected** 1: Short-to-GND detected
2	CH2 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
1	CH2 OL	R	0	**0: No open load detected** 1: Open load detected
0	CH2 SL	R	0	**0: No shorted load detected** 1: Shorted load detected

8.1.9 DC Load Diagnostic Report 2 Register (address = 0x0D) [default = 0x00]

The DC Load Diagnostic Report 2 register is shown in Figure 8-9 and described in Table 8-10.

Figure 8-9. DC Load Diagnostic Report 2 Register

7	6	5	4	3	2	1	0
CH3 S2G	CH3 S2P	CH3 OL	CH3 SL	CH4 S2G	CH4 S2P	CH4 OL	CH4 SL
R	R	R	R	R	R	R	R

Table 8-10. DC Load Diagnostics Report 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH3 S2G	R	0	**0: No short-to-GND detected** 1: Short-to-GND detected
6	CH3 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
5	CH3 OL	R	0	**0: No open load detected** 1: Open load detected
4	CH3 SL	R	0	**0: No shorted load detected** 1: Shorted load detected
3	CH4 S2G	R	0	**0: No short-to-GND detected** 1: Short-to-GND detected
2	CH4 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
1	CH4 OL	R	0	**0: No open load detected** 1: Open load detected
0	CH4 SL	R	0	**0: No shorted load detected** 1: Shorted load detected

8.1.10 DC Load Diagnostics Report 3—Line Output—Register (address = 0x0E) [default = 0x00]

The DC Load Diagnostic Report, Line Output, register is shown in Figure 8-10 and described in Table 8-11.

Figure 8-10. DC Load Diagnostics Report 3—Line Output—Register

7	6	5	4	3	2	1	0
RESERVED				CH1 LO LDG	CH2 LO LDG	CH3 LO LDG	CH4 LO LDG
R	R	R	R	R	R	R	R

Table 8-11. DC Load Diagnostics Report 3—Line Output—Field Descriptions

Bit	Field	Type	Reset	Description
7–4	RESERVED	R	0000	

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Table 8-11. DC Load Diagnostics Report 3—Line Output—Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH1 LO LDG	R	0	**0: No line output detected on channel 1** 1: Line output detected on channel 1
2	CH2 LO LDG	R	0	**0: No line output detected on channel 2** 1: Line output detected on channel 2
1	CH3 LO LDG	R	0	**0: No line output detected on channel 3** 1: Line output detected on channel 3
0	CH4 LO LDG	R	0	**0: No line output detected on channel 4** 1: Line output detected on channel 3

8.1.11 Channel State Reporting Register (address = 0x0F) [default = 0x55]

The Channel State Reporting register is shown in Figure 8-11 and described in Table 8-12.

Figure 8-11. Channel State-Reporting Register

7	6	5	4	3	2	1	0
CH1 STATE REPORT		CH2 STATE REPORT		CH3 STATE REPORT		CH4 STATE REPORT	
R	R	R	R	R	R	R	R

Table 8-12. State-Reporting Field Descriptions

Bit	Field	Type	Reset	Description
7–6	CH1 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
5–4	CH2 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
3–2	CH3 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
1–0	CH4 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics

8.1.12 Channel Faults (Over current, DC Detection) Register (address = 0x10) [default = 0x00]

The Channel Faults (overcurrent, DC detection) register is shown in Figure 8-12 and described in Table 8-13.

Figure 8-12. Channel Faults Register

7	6	5	4	3	2	1	0
CH1 OC	CH2 OC	CH3 OC	CH4 OC	CH1 DC	CH2 DC	CH3 DC	CH4 DC
R	R	R	R	R	R	R	R

Table 8-13. Channel Faults Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 OC	R	0	**0: No over current fault detected** 1: Overcurrent fault detected

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Table 8-13. Channel Faults Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CH2 OC	R	0	**0: No over current fault detected** 1: Overcurrent fault detected
5	CH3 OC	R	0	**0: No over current fault detected** 1: Overcurrent fault detected
4	CH4 OC	R	0	**0: No over current fault detected** 1: Overcurrent fault detected
3	CH1 DC	R	0	**0: No DC fault detected** 1: DC fault detected
2	CH2 DC	R	0	**0: No DC fault detected** 1: DC fault detected
1	CH3 DC	R	0	**0: No DC fault detected** 1: DC fault detected
0	CH4 DC	R	0	**0: No DC fault detected** 1: DC fault detected

8.1.13 Global Faults 1 Register (address = 0x11) [default = 0x00]

The Global Faults 1 register is shown in Figure 8-13 and described in Table 8-14.

Figure 8-13. Global Faults 1 Register

7	6	5	4	3	2	1	0
RESERVED			INVALID CLOCK	PVDD OV	VBAT OV	PVDD UV	VBAT UV
R			R	R	R	R	R

Table 8-14. Global Faults 1 Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED		0	**0**
4	INVALID CLOCK	R	0	**0: No sync clock fault detected** 1: Clock fault detected
3	PVDD OV	R	0	**0: No PVDD over voltage fault detected** 1: PVDD overvoltage fault detected
2	VBAT OV	R	0	**0: No VBAT over voltage fault detected** 1: VBAT overvoltage fault detected
1	PVDD UV	R	0	**0: No PVDD undervoltage fault detected** 1: PVDD undervoltage fault detected
0	VBAT UV	R	0	**0: No VBAT undervoltage fault detected** 1: VBAT undervoltage fault detected

8.1.14 Global Faults 2 Register (address = 0x12) [default = 0x00]

The Global Faults 2 register is shown in Figure 8-14 and described in Table 8-15.

Figure 8-14. Global Faults 2 Register

7	6	5	4	3	2	1	0
RESERVED			OTSD	CH1 OTSD	CH2 OTSD	CH3 OTSD	CH4 OTSD
R			R	R	R	R	R

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Table 8-15. Global Faults 2 Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED	R	0	
4	OTSD	R	0	**0: No global over temperature shutdown** 1: Global over temperature shutdown
3	CH1 OTSD	R	0	**0: No over temperature shutdown on Ch1** 1: Over temperature shutdown on Ch1
2	CH2 OTSD	R	0	**0: No over temperature shutdown on Ch2** 1: Over temperature shutdown on Ch2
1	CH3 OTSD	R	0	**0: No over temperature shutdown on Ch4** 1: Over temperature shutdown on Ch3
0	CH4 OTSD	R	0	**0: No over temperature shutdown on Ch4** 1: Over temperature shutdown on Ch4

8.1.15 Warnings Register (address = 0x13) [default = 0x20]

The Warnings register is shown in Figure 8-15 and described in Table 8-16.

Figure 8-15. Warnings Register

7	6	5	4	3	2	1	0
RESERVED		DVDD POR	OTW	OTW CH1	OTW CH2	OTW CH3	OTW CH4
R		R	R	R	R	R	R

Table 8-16. Warnings Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	
5	DVDD POR	R	0	0: No DVDD POR has occurred **1 DVDD POR occurred**
4	OTW	R	0	**0: No global over temperature warning** 1: Global over temperature warning
3	OTW CH1	R	0	**0: No over temperature warning on channel 1** 1: Over temperature warning on channel 1
2	OTW CH2	R	0	**0: No over temperature warning on channel 2** 1: Over temperature warning on channel 2
1	OTW CH3	R	0	**0: No over temperature warning on channel 3** 1: Over temperature warning on channel 3
0	OTW CH4	R	0	**0: No over temperature warning on channel 4** 1: Over temperature warning on channel 4

8.1.16 Pin Control Register (address = 0x14) [default = 0x00]

The Pin Control register is shown in Figure 8-16 and described in Table 8-17.

Figure 8-16. Pin Control Register

7	6	5	4	3	2	1	0
MASK OC	MASK OTSD	MASK UV	MASK OV	MASK DC	MASK I-LIMIT	MASK CLIP	MASK OTW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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Table 8-17. Pin Control Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK OC	R/W	0	**0: Report over current faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report over current faults on the $\overline{\text{FAULT}}$ Pin
6	MASK OTSD	R/W	0	**0: Report over temperature faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report over temperature faults on the $\overline{\text{FAULT}}$ pin
5	MASK UV	R/W	0	**0: Report undervoltage faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report over voltage faults on the $\overline{\text{FAULT}}$ pin
4	MASK OV	R/W	0	**0: Report overvoltage faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report undervoltage faults on the $\overline{\text{FAULT}}$ pin
3	MASK DC	R/W	0	**0: Report DC faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report DC faults on the $\overline{\text{FAULT}}$ pin
2	MASK I-LIMIT	R/W	0	**0: Report I-Limit faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report I-Limit faults on the $\overline{\text{FAULT}}$ pin
1	MASK CLIP DETECT	R/W	0	**0: Report CLIP Detect on the $\overline{\text{WARN}}$ pin** 1: Do not report CLIP Detect on the $\overline{\text{WARN}}$ pin
0	MASK OTW	R/W	0	**0: Report over temperature warnings on the $\overline{\text{WARN}}$ pin** 1: Do not report over temperature warnings on the $\overline{\text{WARN}}$ pin

8.1.17 AC Load Diagnostic Control 1 Register (address = 0x15) [default = 0x00]

The AC Load Diagnostic Control 1 register is shown in Figure 8-17 and described in Table 8-18.

Figure 8-17. AC Load Diagnostic Control 1 Register

7	6	5	4	3	2	1	0
CH1/2 GAIN	RESERVED	CH3/4 GAIN	RESERVED	CH1 ENABLE	CH2 ENABLE	CH3 ENABLE	CH4 ENABLE
R/W	R	R/W	R	R/W	R/W	R/W	R/W

Table 8-18. AC Load Diagnostic Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 and CH2 GAIN	R/W	0	**0: Gain 1** 1: Gain 4
6	RESERVED	R	0	
5	CH3 and CH4 GAIN	R/W	0	**0: Gain 1** 1: Gain 4
4	RESERVED	R	0	
3	CH1 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
2	CH2 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
1	CH3 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
0	CH4 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics

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8.1.18 AC Load Diagnostic Control 2 Register (address = 0x16) [default = 0x00]

The AC Load Diagnostic Control 2 register is shown in Figure 8-17 and described in Table 8-19.

Figure 8-18. AC Load Diagnostic Control 2 Register

7	6	5	4	3	2	1	0
AC DIAGNOSTICS LOOPBACK	RESERVED				DRIVE	RESERVED	
R/W	R				R/W	R	

Table 8-19. AC Load Diagnostic Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	AC DIAGNOSTICS LOOPBACK	R/W	0	**0: Disable LOOPBACK.** . Measure phase delay of load and signal path. 1: Enable LOOPBACK. Measure phase delay of signal path only
6-3	RESERVED	R	0000	
2	DRIVE	R/W	0	**0: 10 mA** 1: 20 mA
1-0	RESERVED	R	00	

8.1.19 AC Load Diagnostic Report Ch1 through CH4 Registers (address = 0x17–0x1A) [default = 0x00]

The AC Load Diagnostic Report Ch1 through CH4 registers are shown in Figure 8-19 and described in Table 8-20.

Figure 8-19. AC Load Diagnostic Report Chx Register

7	6	5	4	3	2	1	0
CHx IMPEDANCE							
R							

Table 8-20. Chx AC LDG Impedance Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	CHx IMPEDANCE	R	00000000	8 bit AC load diagnostic impedance report for each channel. See Table 7-3 for impedance calculation **0x00: 0 Ω** 0x01: 0.059 Ω ... 0xFF: 15.045 Ω

8.1.20 AC Load Diagnostic Report Phase High Register (address = 0x1B) [default = 0x00]

The AC Load Diagnostic Report Ch1 through CH4 registers are shown in Figure 8-19 and described in Table 8-21.

Figure 8-20. AC Load Diagnostic Report Phase High Register

7	6	5	4	3	2	1	0
Phase High							
R							

Table 8-21. AC LDG report Phase High Field Descriptions

Bit	Field	Type	Reset	Description
7–0	Phase High	R	00000000	bit 15:8

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8.1.21 AC Load Diagnostic Report Phase Low Register (address = 0x1C) [default = 0x00]

The AC Load Diagnostic Report Ch1 through CH4 registers are shown in Figure 8-21 and described in Table 8-22.

Figure 8-21. AC Load Diagnostic Report Phase Low Register

7	6	5	4	3	2	1	0
Phase Low							
R							

Table 8-22. AC LDG report Phase Low Field Descriptions

Bit	Field	Type	Reset	Description
7–0	Phase Low	R	00000000	bit 7:0

8.1.22 AC Load Diagnostic Report STI High Register (address = 0x1D) [default = 0x00]

The AC Load Diagnostic Report Ch1 through CH4 registers are shown in Figure 8-22 and described in Table 8-23.

Figure 8-22. AC Load Diagnostic Report STI High Register

7	6	5	4	3	2	1	0
STI High							
R							

Table 8-23. AC LDG report STI High Field Descriptions

Bit	Field	Type	Reset	Description
7–0	STI High	R	00000000	bit 15:8

8.1.23 AC Load Diagnostic Report STI Low Register (address = 0x1E) [default = 0x00]

The AC Load Diagnostic Report Ch1 through CH4 registers are shown in Figure 8-23 and described in Table 8-24.

Figure 8-23. AC Load Diagnostic Report STI Low Register

7	6	5	4	3	2	1	0
STI Low							
R							

Table 8-24. AC LDG report STI Low Field Descriptions

Bit	Field	Type	Reset	Description
7–0	STI Low	R	00000000	bit 7:0

8.1.24 Miscellaneous Control 3 Register (address = 0x21) [default = 0x00]

The Miscellaneous Control 3 register is shown in Figure 8-24 and described in Table 8-25.

Figure 8-24. Miscellaneous Control 3 Register

7	6	5	4	3	2	1	0
CLEAR FAULT	RESERVED	MASK I-LIMIT WARNING	RESERVED	OTSD AUTO RECOVERY	RESERVED		
R/W	R	R/W	R	R/W	R		

Table 8-25. Misc Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	CLEAR FAULT	R/W	0	**0: Normal operation** 1: Clear fault

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Table 8-25. Misc Control 3 Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESERVED	R	0	
5	MASK I-LIMIT WARNING	R/W	0	**0: Report I-LIMIT on the $\overline{\text{WARN}}$ pin** I-LIMIT warning occurs when internal current limiting flags occur at >45% density over a 200 ms window. If the warning window persists for more than four 200 ms windows, the I-LIMIT FAULT is issued and all channels will go Hi-Z 1: Do not report I-LIMIT on the $\overline{\text{WARN}}$ pin
4	RESERVED	R	0	
3	OTSD AUTO RECOVERY	R/W	0	**0: Over temperature faults Latches** 1: Automatic over temperature protection recovery
2–0	RESERVED	R	000	

8.1.25 Clip Control Register (address = 0x22) [default = 0x01]

The Clip Detect register is shown in Figure 8-25 and described in Table 8-26.

Figure 8-25. Clip Control Register

7	6	5	4	3	2	1	0
RESERVED			REPORT	RESERVED	LEVEL		CLIPDET_EN
R			R/W	R	R/W		R/W

Table 8-26. Clip Control Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000	
4	REPORT	R/W	0	**0: CH1-4 Clip Detect Report to $\overline{\text{WARN}}$ pin** 1: CH1-2 Clip Detect Report to $\overline{\text{WARN}}$ pin, CH3-4 Clip Detect Report to $\overline{\text{FAULT}}$ pin
3	RESERVED	R	0	
2-1	LEVEL	R/W	00	**00: 2 % THD** 01: 5 % THD 10: 10 % THD 11: 1 % THD
0	CLIPDET_EN	R/W	1	0: Clip detect disable **1: Clip Detect Enable**

8.1.26 Clip Warning Register (address = 0x24) [default = 0x00]

The Clip Window register is shown in Figure 8-26 and described in Table 8-27.

Figure 8-26. Clip Warning Register

7	6	5	4	3	2	1	0
RESERVED				CH4_CLIP	CH3_CLIP	CH2_CLIP	CH1_CLIP
R				R	R	R	R

Table 8-27. Clip Warning Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED		0	**0**
3	CH4_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect

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Table 8-27. Clip Warning Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	CH3_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect
1	CH2_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect
0	CH1_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect

8.1.27 Current LIMIT Status Register (address = 0x25) [default = 0x00]

The Current Limit Status register is shown in Figure 8-27 and described in Table 8-28.

Figure 8-27. Current Limit Status Register

7	6	5	4	3	2	1	0
CH4 I-LIMIT_FAULT	CH3 I-LIM_FLT	CH2 I-LIM_FLT	CH1 I-LIM_FLT	CH4_I_LIM_WN	CH3_I_LIM_WN	CH2_I_LIM_WN	CH1_I_LIM_WN
R	R	R	R	R	R	R	R

Table 8-28. Current Limit Status Field Descriptions

Bit	Field	Type	Reset	Description
7	CH4_I_LIMIT_FAULT	R	0	**0: No Current Limit Fault** 1: Current Limit Fault
6	CH3_I_LIMIT_FAULT	R	0	**0: No Current Limit Fault** 1: Current Limit Fault
5	CH2_I_LIMIT_FAULT	R	0	**0: No Current Limit Fault** 1: Current Limit Fault
4	CH1_I_LIMIT_FAULT	R	0	**0: Current Limit Fault** 1: Current Limit Fault
3	CH4_I_LIMIT_WARN	R	0	**0: No Current Limit Warning** 1: Current Limit Warning
2	CH3_I_LIMIT_WARN	R	0	**0: No Current Limit Warning** 1: Current Limit Warning
1	CH2_I_LIMIT_WARN	R	0	**0: No Current Limit Warning** 1: Current Limit Warning
0	CH1_I_LIMIT_WARN	R	0	**0: No Current Limit Warning** 1: Current Limit Warning

8.1.28 Fault and Warning Pin Control Register (address = 0x27) [default = 0x7F]

The Warning PIN Control register is shown in Figure 8-28 and described in Table 8-29.

Figure 8-28. Fault and Warning PIN Control Register

7	6	5	4	3	2	1	0
RESERVED	OT_FAULT_LATCH_ENABLE	I_LIMIT_STATUS_LATCH_ENABLE	DVDD_UV_LATCH_ENABLE	POR_LATCH_EN	OTW_LATCH_EN	I_LIMIT_WARNING_LATCH_EN	CLIP_WARNING_LATCH_ENABLE
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-29. Fault and Warning PIN Control Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	

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Table 8-29. Fault and Warning PIN Control Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	OT_FAULT_LATCH_ENABLE	R/W	1	0: Disable Latching of Over Temperature Report on $\overline{\text{FAULT}}$ pin **1: Enable Latching of Over Temperature Report on $\overline{\text{FAULT}}$ pin**
5	I_LIMIT_STATUS_LATCH_ENABLE	R/W	1	0: Disable Latching of Current Limit Fault report on $\overline{\text{FAULT}}$ pin **1: Enable Latching of Current Limit Fault report on $\overline{\text{FAULT}}$ pin**
4	DVDD_UV_LATCH_ENABLE	R/W	1	0: Disable Latching of DVDD Under Voltage Reporting on $\overline{\text{WARN}}$ pin **1: Enable latching of DVDD Under Voltage Report on $\overline{\text{WARN}}$ pin**
3	POR_LATCH_EN	R/W	1	0: Disable Latching of DVDD POR Report on $\overline{\text{WARN}}$ pin **1: Enable Latching of DVDD POR Report on $\overline{\text{WARN}}$ pin**
2	OTW_LATCH_EN	R/W	1	0: Disable Latching of Over Temperature Warning Reporting on $\overline{\text{WARN}}$ pin **1: Enable Latching of Over Temperature Warning Report on $\overline{\text{WARN}}$ pin**
1	I_LIMIT_WARNING_LATCH_EN	R/W	1	0: Disable Latching of Current Limit Warning Reporting on $\overline{\text{WARN}}$ pin **1: Enable Latching of Current Limit Warning Report on $\overline{\text{WARN}}$ pin**
0	CLIP_WARNING_LATCH_ENABLE	R/W	1	0: Disable pin latching of CLIP Reporting **1: Enable pin latching of CLIP Reporting**

8.1.29 Thermal Foldback Control Register (address = 0x28) [default = 0x00]

The Thermal Foldback Control register is shown in Figure 8-29 and described in Table 8-30.

Figure 8-29. Thermal Foldback Control Register

7	6	5	4	3	2	1	0
ZC_WAIT_TIME		BYPASS	ZC_BYPASS	ATTACK		RELEASE	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-30. Thermal Foldback Control Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ZC_WAIT_TIME	R/W	00	**00: 20 µS** System waits this period for Zero Crossing, then changes gain regardless. 01: 80 µS 10: 320 µS 11: 1280 µS
5	BYPASS	R/W	0	**0: Enable Thermal Foldback** 1: Disable Thermal Foldback
4	ZC_BYPASS	R/W	0	**0: Enable Zero Crossing detection** 1: Disable Zero Crossing detection. Gain changes as soon as thermal condition is met without waiting for zero detection.
3-2	ATTACK	R/W	00	**00: 1dB/100 mS** 01: 1dB/ 200 mS 10: 1dB/400 mS 11: 1dB/ 800 mS

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Table 8-30. Thermal Foldback Control Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	RELEASE	R/W	00	**00: 1dB/200 mS** 01: 1dB/400 mS 10:1dB/800 mS 11: 1dB/1600 mS

8.1.30 AC Diagnostic Frequency Control Register (address = 0x2A) [default = 0x32]

The AC Diagnostic Frequency Control register is shown in Figure 8-30 and described in .

Figure 8-30. AC Diagnostic Frequency Control Register

7	6	5	4	3	2	1	0
STIMULUS FREQUENCY							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8-31. AC Diagnostic Frequency Control Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STIMULUS FREQUENCY (375 Hz/ bit)	R/W	00110010	00000000 - 00000010: Reserved 00000011: 1125 Hz .... **00110010: 18.75 kHz** .... 00111100: 22.50 kHz 00111101 - 11111111: Reserved

8.1.31 SYNC PIN Control Register (address = 0x2B) [default = 0x02]

The SYNC PIN Control register is shown in Figure 8-31 and described in Table 8-32.

Figure 8-31. SYNC PIN Control Register

7	6	5	4	3	2	1	0
SYNC ERROR DET BYPASS	RESERVED		SYNC CLOCK ERROR MASK	RESERVED		SYNC CLOCK ERROR LATCH	CONTROLLER/ target
R/W	R	R	R/W	R	R	R/W	R/W

Table 8-32. SYNC PIN Control Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC ERROR DET BYPASS	R/W	0	**0: SYNC Clock Error detection** 1: Bypass SYNC Clock Error detection - this setting may result in abnormal behavior of the device
6-5	RESERVED	R	00	
4	SYNC CLOCK ERROR MASK	R/W	0	**0: Report SYNC Clock Error** 1: Mask SYNC Clock Error
3-2	RESERVED	R	00	
1	SYNC CLOCK ERROR LATCH	R/W	1	0: Non-latch SYNC Clock Error **1: Latch SYNC Clock Error**
0	CONTROLLER/TARGET	R/W	0	**0: Target Mode - external clock into SYNC pin required** 1: Controller Mode

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPA6404-Q1 is a four-channel analog input class-D audio-amplifier design for use in automotive head units and external amplifier modules. The TPA6404-Q1 incorporates the necessary functionality to perform in demanding OEM applications.

9.1.1 AM Radio Avoidance

AM-radio frequency interference is avoided by setting the switching frequency of the device above the AM band. The switching frequency options available are 1.8MHz, 2.1MHz, and 2.3MHz.

9.1.2 Parallel BTL Operation (PBTL)

The device has the capability of placing two channels into a parallel configuration that allows for twice the current drive capability for low impedance loads. BTL and PBTL modes can be me mixed. Channels 1 and 2 can be placed in PBTL, channels 3 and 4 can be placed into PBTL, or both pairs can be placed in PBTL. Follow the Typical application schematic for proper input and output connections for PBTL configuration utilizing both pairs. The speaker output connections must be made on the speaker side of the LC filter. The device can drive more current with paralleling BTL channels on the load side of the LC output filter. The input connections on channel 2 and channel 4 should be connected to ground.

The proper I2C register settings must be made while the STANDBY pin is asserted. Register 0x00, shown in the Mode Control Field Descriptions has two bits, 4 and 5 that needs to be set for PBTL operation. Bit 4 sets channels 1 and 2 to PBTL and bit 5 sets channels 3 and 4 to PBTL.

BTL and PBTL modes can be mixed. CH1/2 in PBTL or CH3/4 in PBTL or both.

Load diagnostics is supported for parallel BTL channels.

9.1.3 Reconstruction Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. An LC reconstruction filter is used to recover the audio signal. The filter attenuates the high-frequency components of the output signals that are out of the audio band. Design of the reconstruction filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N requirements, the selection of the inductors used in the output filter should be carefully considered.

9.1.4 Line Driver Applications

In many automotive audio applications, the same head unit must drive either a speaker (with several Ω of impedance) or an external amplifier input (with several kilo Ω of impedance). The design is capable of supporting both applications and has special line drive gain and diagnostics. Coupled with the high switching frequency the device is well suited for this type of application. Set the desired channel in line driver mode via the mode control I^2C register 0x00, the external connected amplifier need to have a differential impedance between 600Ω and 4.7kΩ for the DC line diagnostic to detect the connected external amplifier. The next figure shows the recommended external amplifier input configuration, balanced capacitor coupled.

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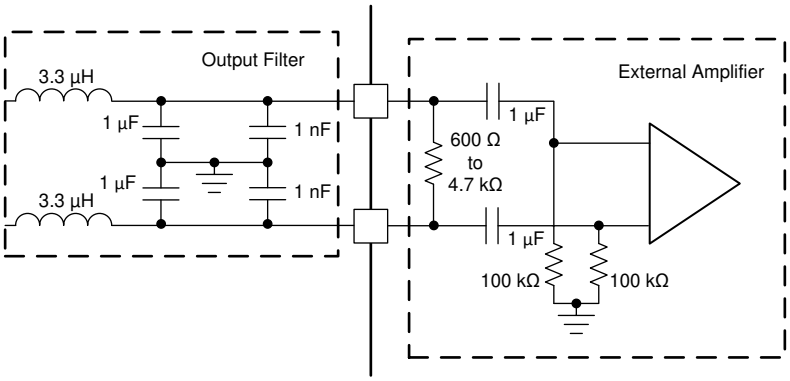

Figure 9-1. Line Driver External Amplifier Input Configuration

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9.2 Typical Applications

9.2.1 BTL Application

Figure 9-2 shows the schematic of a typical 4-channel solution for a head unit application.

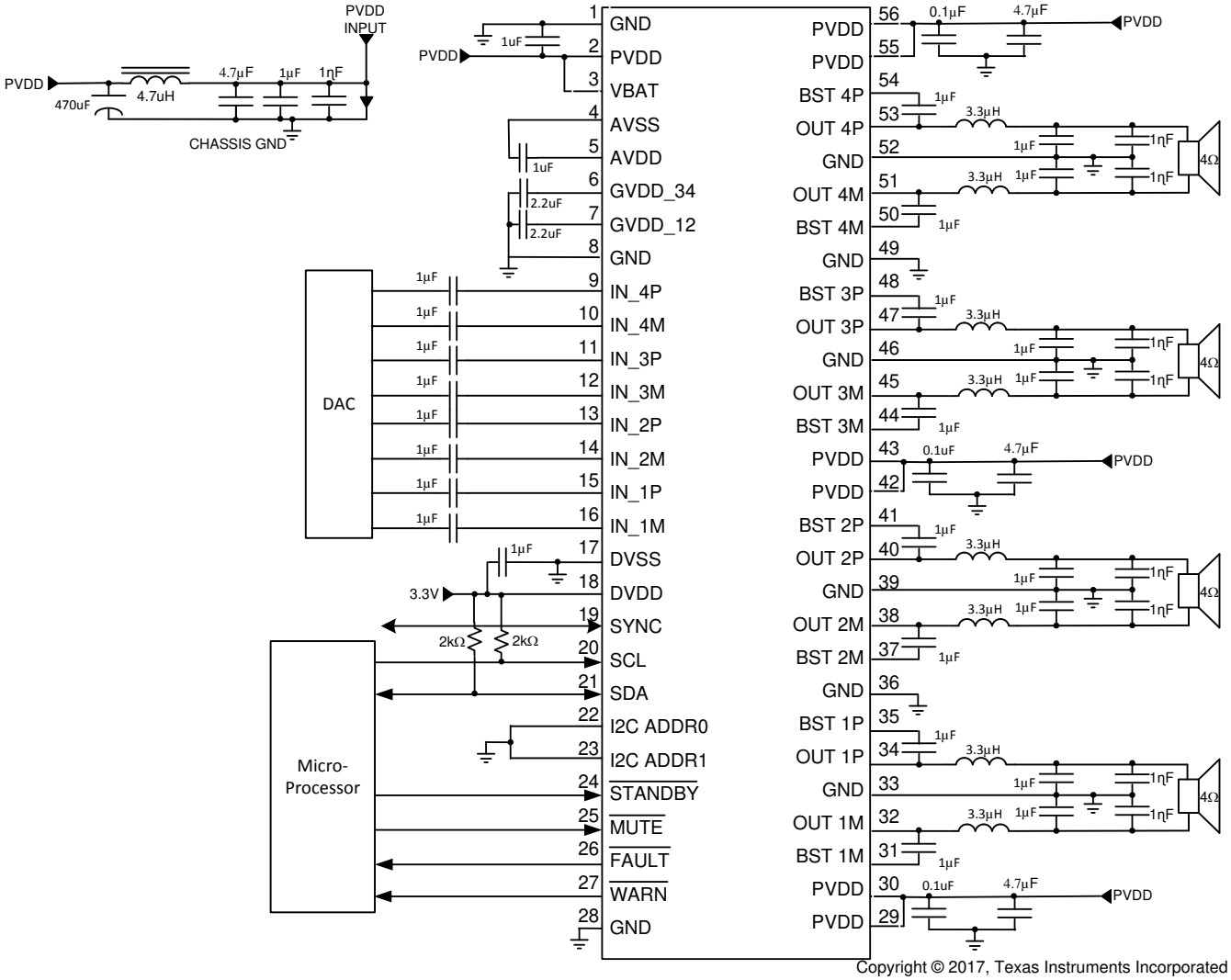

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Figure 9-2. Typical 4-Channel BTL Application Schematic

9.2.1.1 Design Requirements

This head unit example is focused on the smallest solution size for 4 times 25W output power into 4Ω with a battery supply of 14.4V.

The switching frequency is set above the AM-band with a switch frequency of 2.1MHz.

The selection of a 2.1MHz switch frequency enables the use of a small output inductor value of 3.3µH which leads to a very small footprint.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Hardware Design

Use the following procedure for the hardware design:

- Determine the input mode. The input mode can be either balanced or single-ended. The value for the coupling capacitors will be determined by the gain setting to be used and the frequency response required.

- Determine the output power that is required into the load. The output power requirement determines the required power supply voltage and current. The output reconstruction filter components that are required are also driven by the output power.
- With the requirements, adjust the typical application schematic in Figure 9-2.

9.2.1.2.2 Bootstrap Capacitors

The bootstrap capacitors provide the gate-drive voltage of the upper N-channel FET. These capacitors must be sized appropriately for the system specification. For typical applications use 1µF.

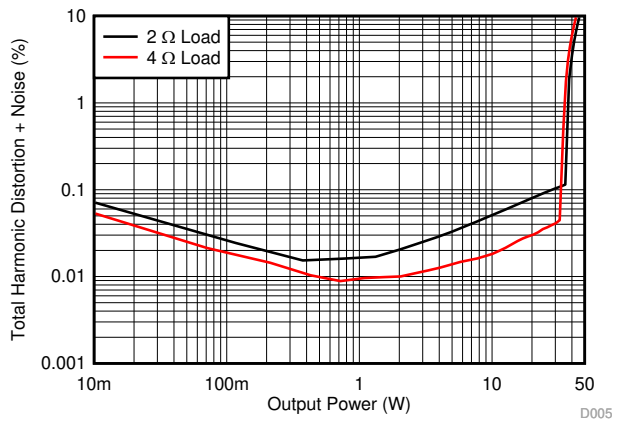
9.2.1.2.3 Output Reconstruction Filter

The output FETs drive the amplifier outputs in an H-Bridge configuration. These transistors are either fully off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. The amplifier outputs require a reconstruction filter that comprises a series inductor and a capacitor to ground on each output, generally called an LC filter. The LC filter attenuates the PWM frequency and reduces electromagnetic emissions, allowing the reconstructed audio signal to pass to the speakers. refer to the Class-D LC Filter Design, *SLAA701A*, application report for a detailed description of proper component description and design of the LC filter based upon the specified load and frequency response.

The recommended low-pass cutoff frequency of the LC filter is dependent on the selected switching frequency. The low-pass cutoff frequency can be as high as 100kHz for a PWM frequency of 2.1MHz.

Certain specifications must be understood for a proper inductor. See the application note TAS6424-Q1 Inductor Selection Guide, *SLOA242*, for information on selection the proper inductor. The inductance value is given at zero current, but the inductors will have current through them as the TPA6404-Q1 drives current into the load. Use the inductance versus current curve for the inductor to made sure the inductance does not drop below 2uH (for f_{sw} = 2.1MHz) at the maximum current for the system design during normal operation. The DCR of the inductor directly affects the output power of the system design. The lower the DCR, the more power is provided to the speakers. The typical inductor DCR for a 4Ω system is 40 to 50mΩ and for a 2Ω system is 15 to 25mΩ.

9.2.1.3 Application Curves



PVDD = 18V

Figure 9-3. THD vs Output Power

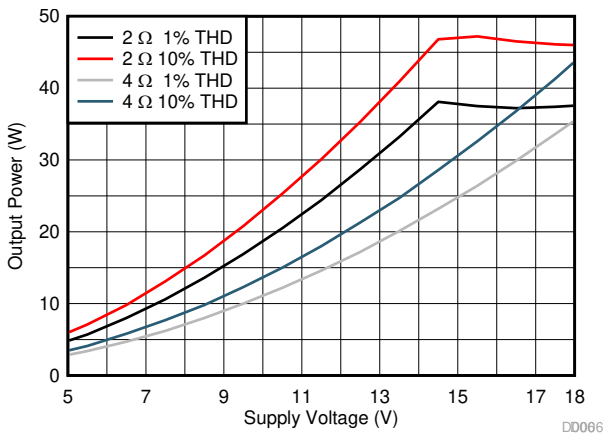


Figure 9-4. Output Power vs Supply Voltage

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9.2.1.4 PBTL Application

Figure 9-5 shows a schematic of a typical 2-channel solution for a head unit or external amplifier application where high power into 2 Ω is required.

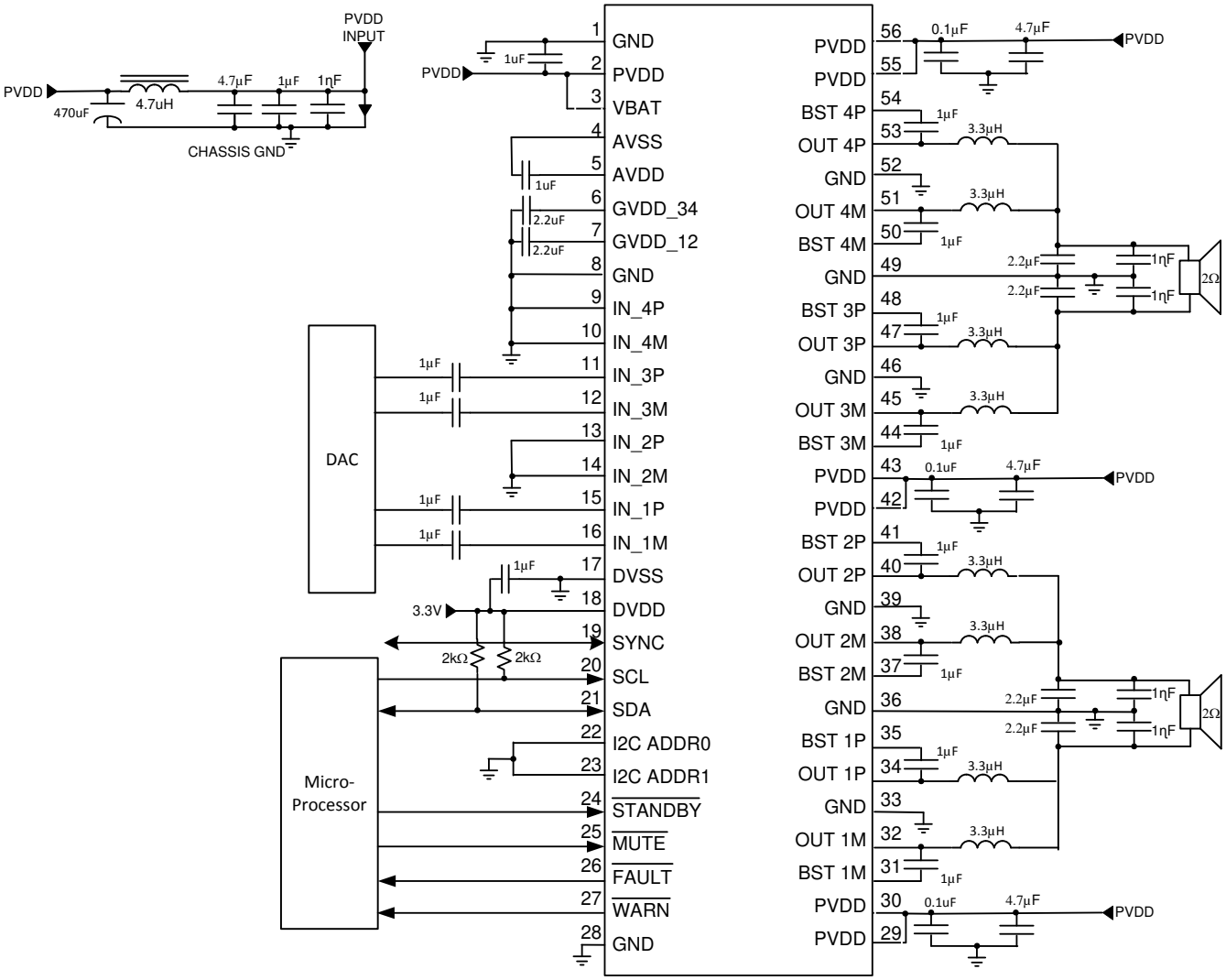

Figure 9-5. 2-Channel PBTL Application Schematic

9.2.1.4.1 Design Requirements

This head unit example is focused on the smallest solution size for 2 times 50W output power into 2Ω with a battery supply of 14.4V.

The switching frequency is set above the AM-band with a switch frequency of 2.1MHz.

The selection of a 2.1MHz switch frequency enables the use of a small output inductor value of 3.3µH which leads to a very small footprint.

9.2.1.4.2 Detailed Design Procedure

9.2.1.4.2.1 Hardware Design

Use the following procedure for the hardware design:

- Determine the input mode. The input mode can be either balanced or single-ended. The value for the coupling capacitors will be determined by the gain setting to be used and the frequency response required.

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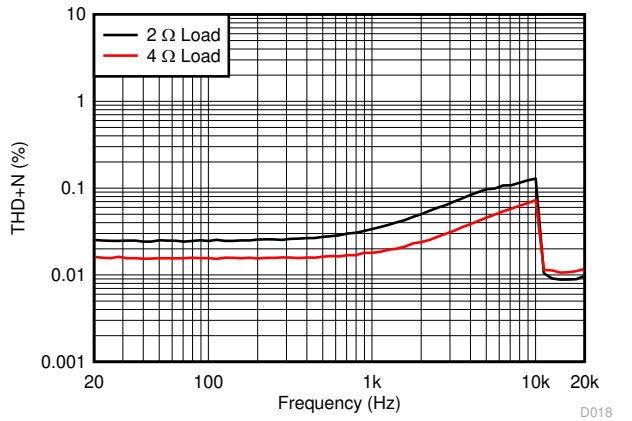
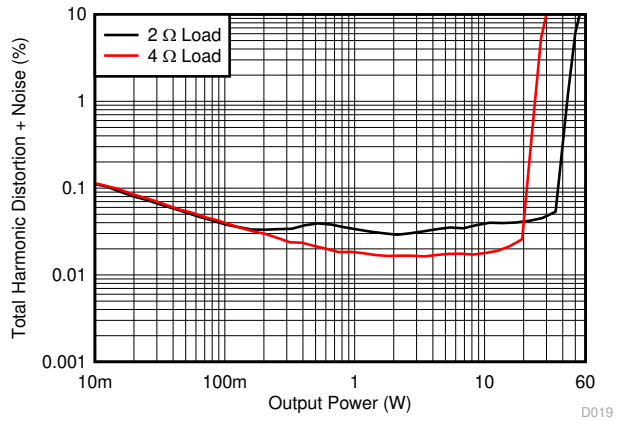
- Determine the output power that is required into the load. The output power requirement determines the required power supply voltage and current. The output reconstruction filter components that are required are also driven by the output power.
- With the requirements, adjust the typical application schematic in Figure 9-5

9.2.1.4.3 Application Curves



PVDD = 14.4V

Figure 9-6. THD vs Frequency



PVDD = 14.4V

Figure 9-7. THD vs Output Power

9.3 Power Supply Recommendations

The TPA6404-Q1 requires two power supply rails. The PVDD supply is the high-current supply in the recommended supply range. The VBAT supply is a lower current that must be in the recommended supply range. The PVDD and VBAT pins can be connected to the same supply if the recommended supply range for VBAT is maintained. The DVDD supply is the 3.3V logic supply and must be maintained in the tolerance as shown in the *Section 5.3* table.

9.4 Layout

9.4.1 Layout Guidelines

The pinout of the TPA6404-Q1 was selected to provide flow through layout with all high-power connections on the right side, and all low-power signals and supply decoupling on left side.

Section 9.4.2 shows the area for the components in the application example (see the *Section 9.2* section). This layout example is taken from the EVM PCB.

The TPA6404-Q1 EVM uses a four-layer PCB. The copper thickness was selected as 70 µm to optimize power loss.

The small value of the output filter provides a small size and, in this case, the low height of the inductor enables double sided mounting

9.4.1.1 Electrical Connection of Thermal pad and Heat Sink

For the DKQ package, the heat sink connected to the thermal pad of the device should be connected to GND. The heat slug must not be connected to any other electrical node.

9.4.1.2 EMI Considerations

Automotive-level EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design. The design has minimal parasitic inductances because of the short leads on the package. This reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The design also incorporates circuitry that optimizes output transitions which cause EMI.

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For optimizing the EMI a solid ground layer plane is recommended, for a PCB design that fulfills the CISPR25 level 5 requirements, see the TPA6404-Q1 EVM layout.

9.4.1.3 General Considerations

The EVM layout is optimized for low noise and EMC performance.

The TPA6404-Q1 has an exposed thermal pad that is up, away from the PCB. The layout must consider an external heat sink.

Refer to Figure 9-8 for the following guidelines:

- A ground plane, A, on the same side as the device pins helps reduce EMI by providing a very-low loop impedance for the high-frequency switching current.
- The decoupling capacitors on PVDD, B, are very close to the device with the ground return close to the ground pins.
- The ground connections for the capacitors in the LC filter, C, have a direct path back to the device and also the ground return for each channel is the shared. This direct path allows for improved common mode EMI rejection.
- The traces from the output pins to the inductors, D, should have the shortest trace possible to allow for the smallest loop of large switching currents.
- Heat-sink mounting screws, E, should be close to the device to keep the loop short from the package to ground.
- Many vias, F, stitching together the ground planes can create a shield to isolate the amplifier and power supply.

9.4.2 Layout Example

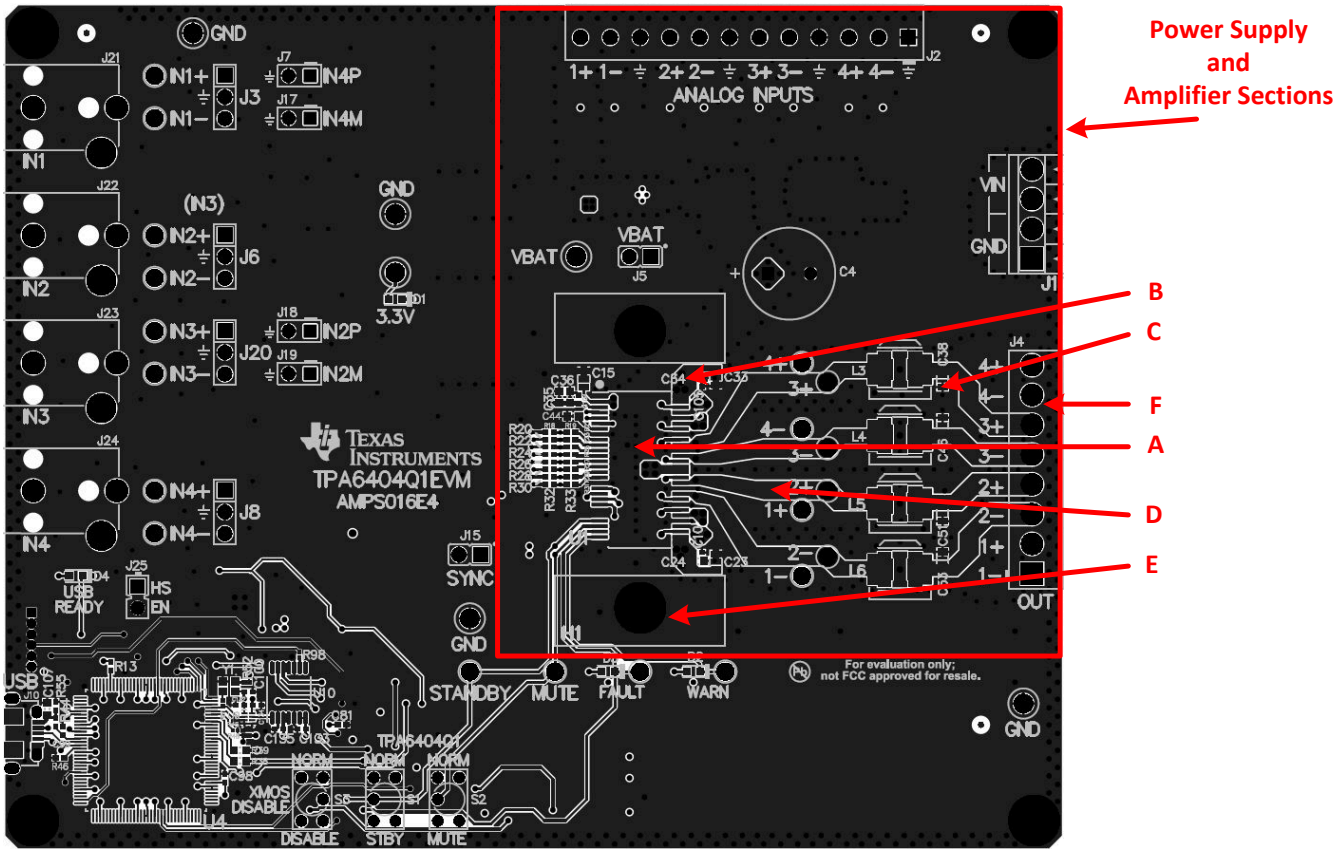

Figure 9-8. Layout Example

9.4.3 Thermal Considerations

The thermally enhanced PowerPAD package has an exposed pad up for connection to a heat sink. The output power of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system such as the ambient operating temperature. The heat sink absorbs heat from the TPA6404-Q1 and transfers it to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. Heat sinks can be smaller than that of classic linear amplifier design because of the excellent efficiency of class-D amplifiers. This device is intended for use with a heat sink, therefore, RθJC will be used as the thermal resistance from junction to the exposed metal package. This resistance will dominate the thermal management, so other thermal transfers will not be considered. The thermal resistance of RθJA (junction to ambient) is required to determine the full thermal solution. The thermal resistance is comprised of the following components:

- RθJC of the TPA6404-Q1
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

The thermal resistance of the thermal interface material can be determined from the manufacturer's value for the area thermal resistance (expressed in °C/mm^{2}W) and the area of the exposed metal package. For example, a typical, white, thermal grease with a 0.0254mm (0.001-inch) thick layer is approximately 4.52°Cmm^2/W. The TPA6404-Q1 in the DKQ package has an exposed area of 47.6mm^2. By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the thermal grease. The thermal resistance of the thermal grease is 0.094°C/W

Table 9-1 lists the modeling parameters for one device on a heat sink. The junction temperature is assumed to be 115°C while delivering and average power of 10 watts per channel into a 4Ω load. The thermal-grease example previously described is used for the thermal interface material. Use Equation 1 to design the thermal system.

$$R_{\theta JA} = R_{\theta JC} + \text{thermal interface resistance} + \text{heat sink resistance} \quad (1)$$

Table 9-1. Thermal Modeling

Description	Value
Ambient Temperature	25°C
Average Power to load	40W (4x 10w)
Power dissipation	8W (4x 2w)
Junction Temperature	115°C
ΔT inside package	5.6°C (0.7°C/W × 8W)
ΔT through thermal interface material	0.75°C (0.094°C/W × 8W)
Required heat sink thermal resistance	10.45°C/W ([115°C – 25°C – 5.6°C – 0.75°C] / 8W)
System thermal resistance to ambient $R_{\theta JA}$	11.24°C/W

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

PurePath™ Console 3 Graphical Development Suite

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10.5 Support Resources

10.6 Trademarks

PurePath™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11 Revision History

Changes from Revision A (February 2018) to Revision B (January 2025)	Page
• First public release of the datasheet	1
• Added disclaimer under Absolute Maximum Ratings	5
• Updated gain values to more accurately reflect device performance	7
• Added minimum value for VBATUV_SET	7
• Added information regarding target mode operation	15
• Updated decoupling capacitor pin connections to the correct value	15
• Changed From: at 250ms To: as 250ms for minimum load diagnostics duration	15
• Added information regarding 200ms wait time requirement	17
• Added clarification of fault types	17
• Added additional step for BTL and PBTL modes	17
• Added information regarding CLEAR FAULT bit	19
• Added clarification that DC detection runs while device is in PLAY mode	19
• Updated internal pull-down resistor value	22
• Updated internal pull-down resistor value	22
• Added bit 7 information	28
• Updated bit 3 description to show correct values	38
• Updated bit 0 description for additional clarification	40
• Updated Packaging Information table	55

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Changes from Revision * (January 2018) to Revision A (February 2018)	Page
• Released data sheet as Production Data	1

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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12.1 Package Option Addendum

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12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TPA6404QDKQRQ1	ACTIVE	HSSOP	DKQ	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA6404

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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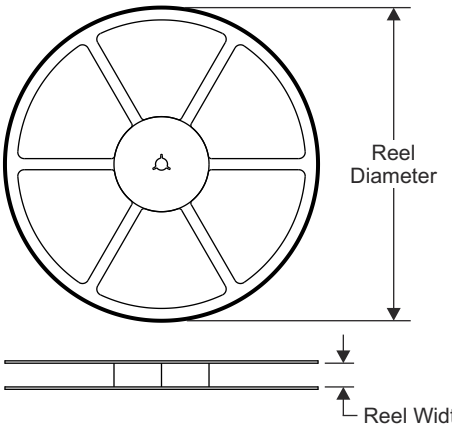
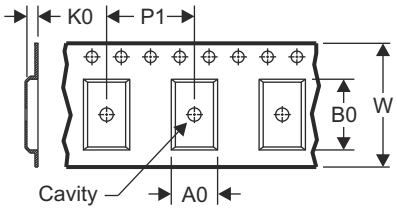
12.1.2 Tape and Reel Information

REEL DIMENSIONS

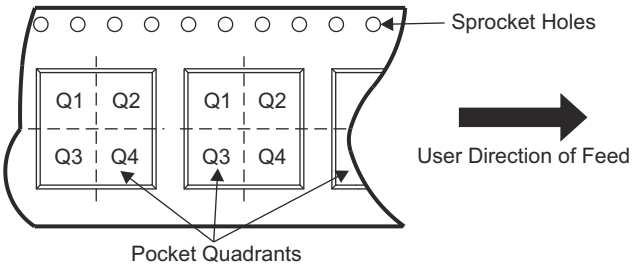


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6404QDKQRQ1	HSSOP	DKQ	56	1000	330.0	32.4	11.35	18.87	3.1	16.0	32.0	Q1

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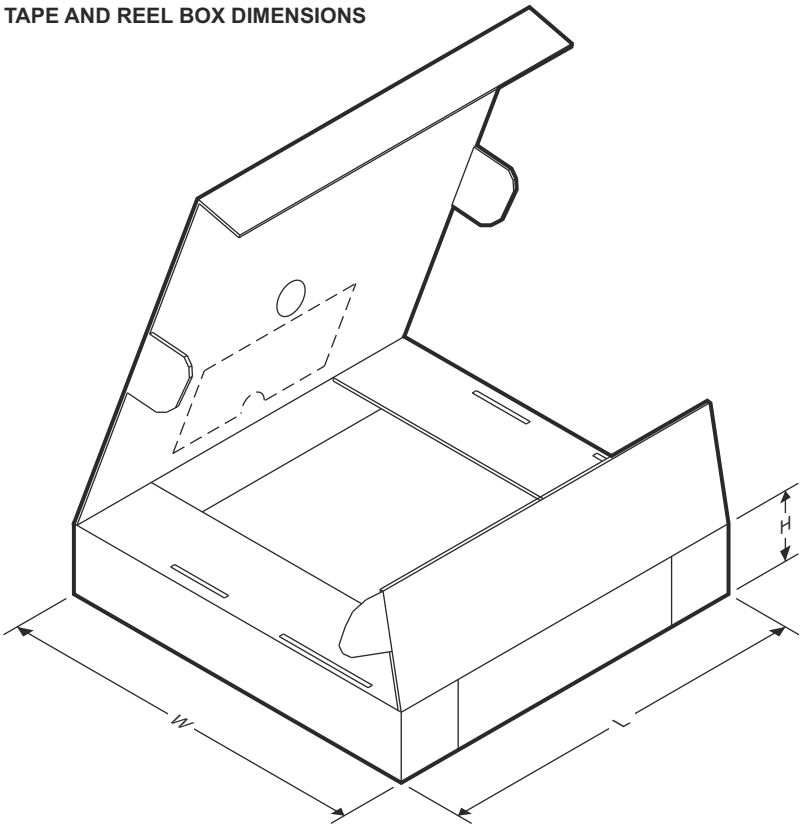
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6404QDKQRQ1	HSSOP	DKQ	56	1000	367.0	367.0	55.0

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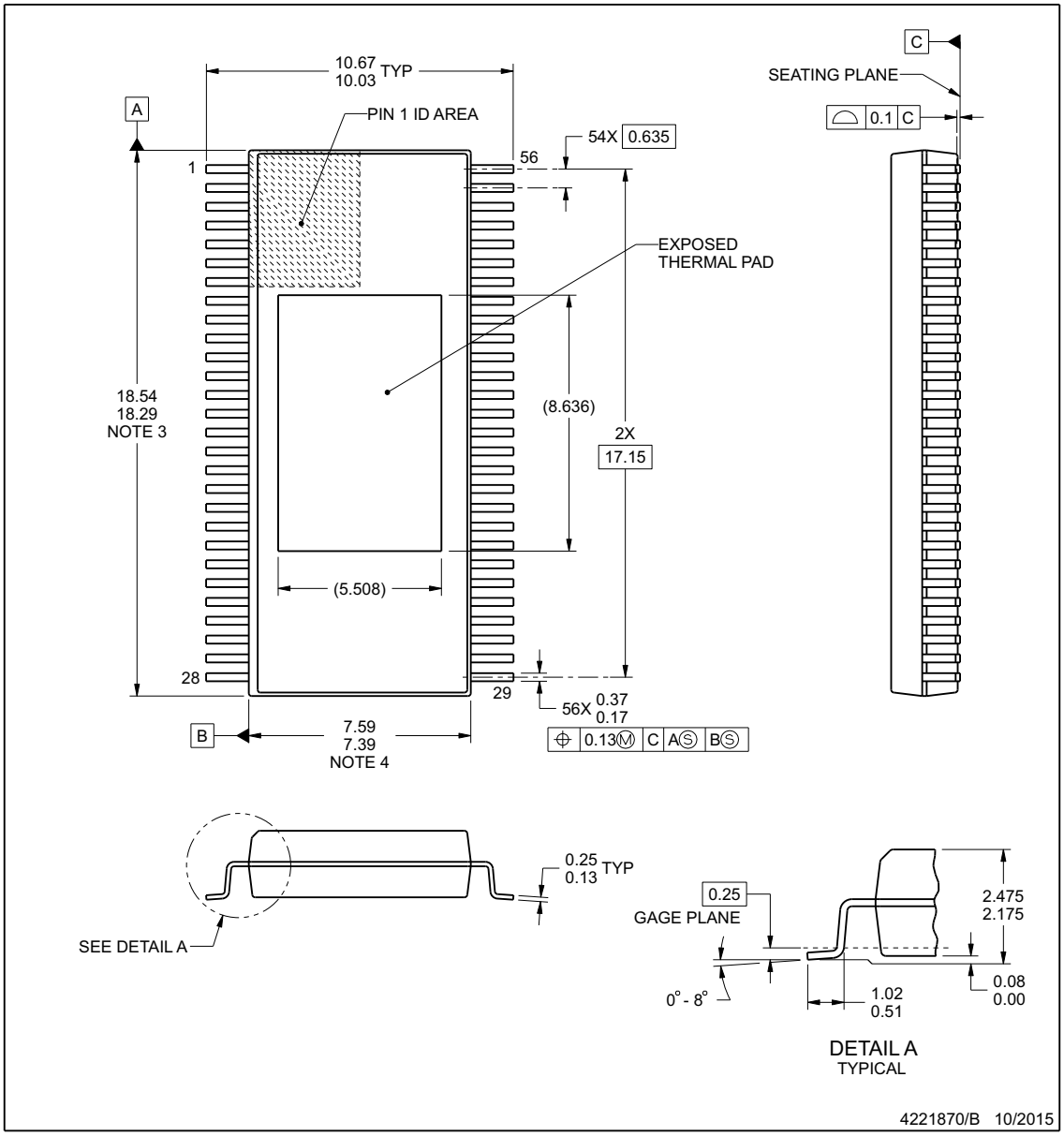
PACKAGE OUTLINE

DKQ0056A

PowerPAD™ SSOP - 2.475 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. The exposed thermal pad is designed to be attached to an external heatsink.

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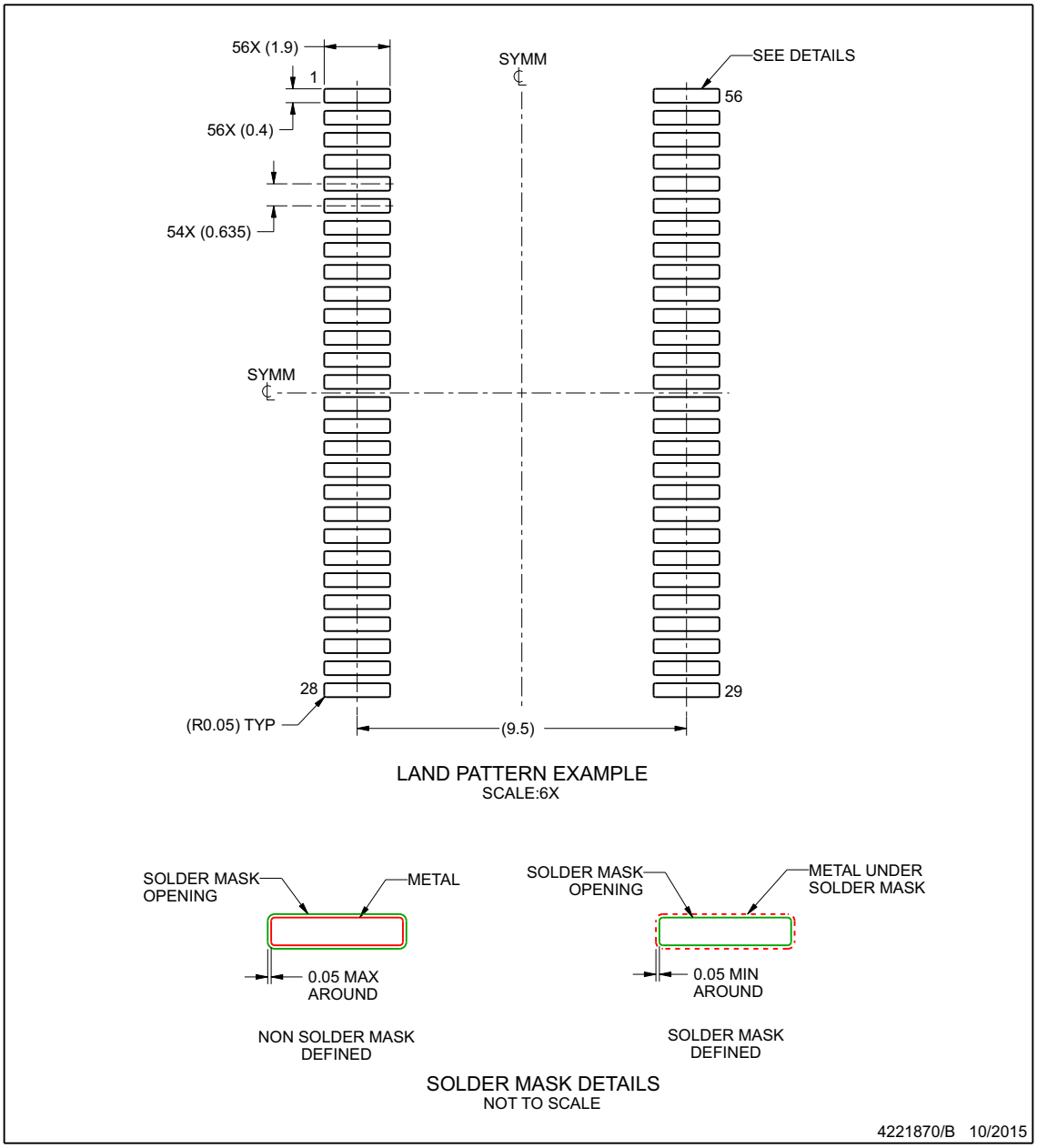
EXAMPLE BOARD LAYOUT

DKQ0056A

PowerPAD™ SSOP - 2.475 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Size of metal pad may vary due to creepage requirement.

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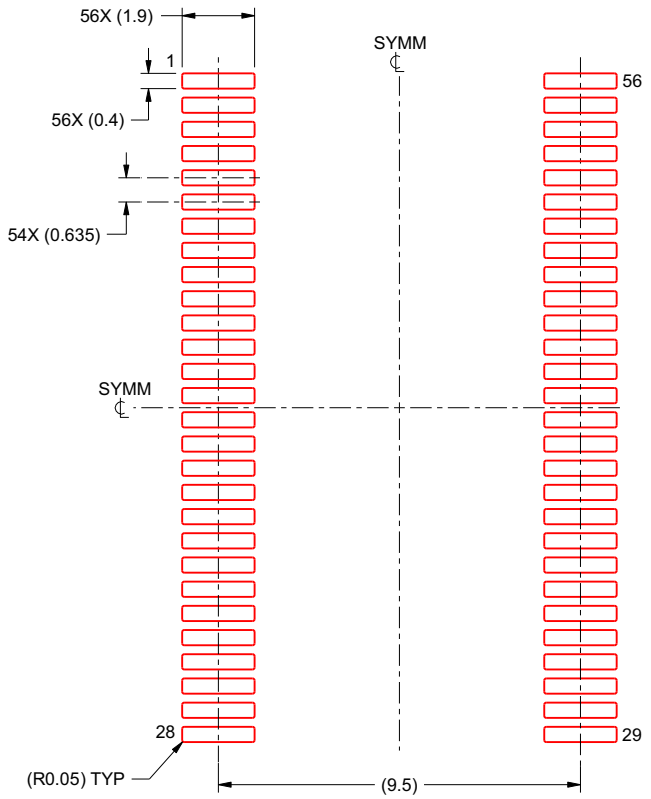
EXAMPLE STENCIL DESIGN

DKQ0056A — **PowerPAD™ SSOP - 2.475 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.127 MM THICK STENCIL
SCALE:6X

4221870/B 10/2015

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6404QDKQQ1.B	Active	Production	HSSOP (DKQ) | 56	20 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA6404
TPA6404QDKQRQ1	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA6404
TPA6404QDKQRQ1.A	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA6404
TPA6404QDKQRQ1.B	Active	Production	HSSOP (DKQ) | 56	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA6404

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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