TMUXHS221F Dual 2:1 USB 2.0 Mux/DeMux With 28V Overvoltage Protection and 1.2V Logic

1 Features

- Supply range: 2.3V to 5.5V
- Differential 2:1 or 1:2 switch/multiplexer or flexible dual single-ended cross switch
- Overvoltage protection (OVP) on common pins - 28V with absolute maximum overvoltage - 30V
- IEC-61000-4-5 Surge Tolerant - +30V
- 1.2V compatible logic inputs: extended 1.2V logic support with 0.77VIH 0.39VIL
- Powered-off protection when VCC = 0V
- Low RON: 9Ω maximum
- BW: 1.5GHz typical
- Low CON: 1.3pF typical
- LowPower Disable mode
- ESD protection exceeds JESD 22 human body model (HBM): 2000V
- Wide temperature range: –40°C to 125°C
- 10-pin small UQFN package - 1.8mm × 1.4mm

2 Applications

- Mobile
- PC, notebook
- Tablet
- Anywhere a USB Type-C® or Micro-B connector is used

3 Description

The TMUXHS221F is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C systems. The device is configured as a dual 2:1 or 1:2 switch. TMUXHS221F is optimized for use with the USB 2.0 D+/- lines in a USB Type-C systems.

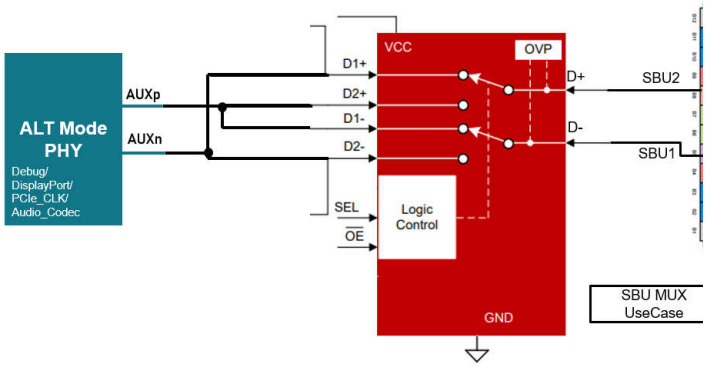
The TMUXHS221F protection on the I/O pins can tolerate up to 30V with automatic shutoff circuitry to protect system components behind the switch.

The TMUXHS221F comes in a small industry standard 10-pin QFN package. TMUXHS221F has an extended temperature range that is an excellent choice for many rugged applications including industrial and high reliability use cases.

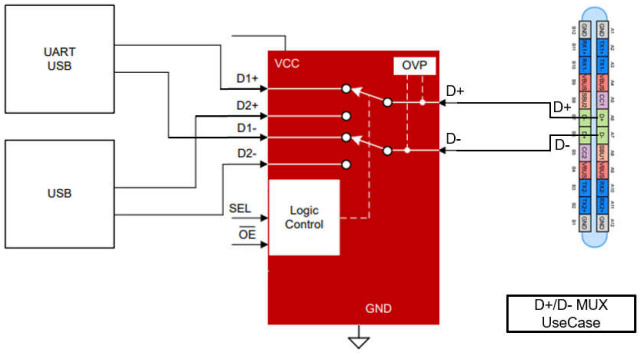
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUXHS221F	RSW (UQFN, 10)	1.8mm × 1.4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



SBU Pins Application Use Case



D+/D- Pins Application Use Case

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4 Pin Configuration and Functions

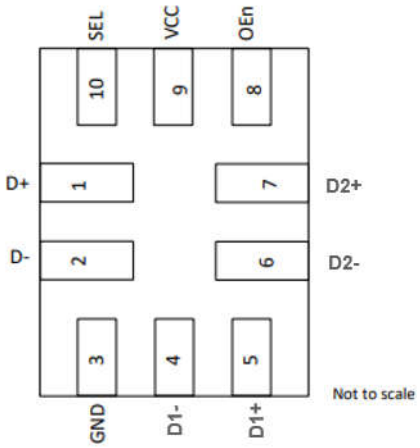

Figure 4-1. RSW Package 10-Pin UQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
D+	1	I/O	Data signals Common Port, positive
D-	2	I/O	Data signals Common Port, negative
D1+	5	I/O	Data signals Port A, positive
D1-	4	I/O	Data signals Port A, negative
D2+	7	I/O	Data signals Port B, positive
D2-	6	I/O	Data signals Port B, negative
SEL	10	IN	Switch control configuration signal as provided in Table 7-1.
OEn	8	IN	
VCC	9	P	Power supply
GND	3	G	Ground

(1) IN = input, I/O = input or output, P = power, G = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	6	V
$V_{I/O}$	Input/Output DC voltage (D±)(2)	–0.5	30	V
$V_{I/O}$	Input/Output DC voltage (D1±, D2±)(2)	–0.5	6	V
V_I	Digital input voltage (SEL, OEn)	–0.5	6	V
I_K	Input-output port diode current (D+, D-, D1+, D1-, D2+, D2-) when $V_{IN} < 0$	–50		mA
I_{IK}	Digital logic input clamp current (SEL, OEn) when $V_I < 0$ (2)	–50		mA
I_{CC}	Continuous current through VCC		100	mA
I_{GND}	Continuous current through GND	–100		mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safemanufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	5.5	V
$V_{I/O}$ (D±)	Analog input/output voltage	0	28	V
$V_{I/O}$ (D1±, D2±)	Analog input/output voltage	0	3.6	V
V_I	Digital input voltage (SEL, OEn)	0	5.5	V
$I_{I/O}$ (D+, D–, D1+, D1–, D2+, D2–)	Analog input/output port continuous current	–50	50	mA
I_{OL}	Digital output current		3	mA
T_A	Operating free-air temperature	–40	125	ºC
T_J	Junction temperature	–40	135	ºC

5.4 Electrical Characteristics

T_A = –40°C to +125°C , V_{CC} = 2.3V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3V, T_A = 25°C, (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power						
$I_{CC-ACTIVE}$	Active supply current	OEn = 0V SEL= 0V, 1.2V or VCC 0V < $V_{I/O}$ < 3.6V		23	62	µA
I_{CC-OVP}	Supply current during OVP condition	OEn = 0V SEL = 0V, 1.2V or V_{CC} $V_{I/O}$ > V_{POS_THLD}		24	50	µA
$I_{CC\_PD\_OVP}$	Standby powered down supply current	OEn = 1.2V, 1.8V, or V_{CC} SEL = 0V, 1.2V, 1.8V, or V_{CC}		5	15	µA
I_{CC_PD}	Standby powered down supply current	OEn = 1.2V, 1.8V, or V_{CC} SEL = 0V, 1.2V, 1.8V, or V_{CC}		2	8	µA
DC Characteristics						
R_{ON}	ON-state resistance	$V_{I/O}$ = 0.4V I_{SINK} = 8mA VCC = 2.3V - 5.5V Refer to Figure 6-1		5.6	13	Ω
ΔR_{ON}	ON-state resistance match between channels	$V_{I/O}$ = 0.4V VCC=2.3V-5.5V I_{SINK} = 8mA Refer to Figure 6-1		0.173	0.349	Ω
$R_{ON\ (FLAT)}$	ON-state resistance flatness	$V_{I/O}$ = 0V to 0.4V VCC=2.3V-5.5V I_{SINK} = 8mA Refer to Figure 6-1		0.055	0.18	Ω
I_{OFF_0V}	I/O pin OFF leakage current when V_{CC} =	OEn = H $V_{D±}$ = 0V or 3.6V V_{CC} = 0V $V_{D1±}$or $V_{D2±}$ = 3.6V or 0V Refer to Figure 6-2	–12.5	0.9	15.5	µA
I_{OFF}	I/O pin OFF leakage current	OEn = H $V_{D±}$ = 0V or 3.6V V_{CC} = 2.3V to 5.5V $V_{D1±}$or $V_{D2±}$ = 3.6V or 0V Refer to Figure 6-2	–2.73	0.1	2.73	µA
$I_{OFF-28V}$	D1±, D2± pin OFF leakage current during OVP scenario on D±	OEn = H $V_{D±}$ = 28V V_{CC} = 2.3V to 5.5V $V_{D1±}$ or $V_{D2±}$ = 0V Refer to Figure 6-2	-0.5		0.5	µA
$I_{OFF-28V-DPN}$	D± pin OFF leakage current during OVP scenario	OEn = H $V_{D±}$ = VOVP_THREDHOLD to 28V V_{CC} = 2.3V to 5.5V $V_{D1±}$ or $V_{D2±}$ = 0V Refer to Figure 6-2	220	626	807	µA
I_{ON}	ON leakage current	$V_{D±}$ = 0V or 3.6V $V_{D1±}$ and $V_{D2±}$ = High-Z Refer to Figure 6-3	–5.5	0.25	7.5	µA
Digital Characteristics						
V_{IH}	Input logic high	SEL, OEn	0.77			V
V_{IL}	Input logic low	SEL, OEn			0.39	V
I_{IH}	Input high leakage current	SEL, OEn = 1.2V, 1.8V, or V_{CC}	–1	0.35	5	µA
I_{IL}	Input low leakage current	SEL, OEn = 0V	–1	±0.002	5	µA
C_I	Digital input capacitance	SEL = 0V, 1.2V, 1.8V, or V_{CC} f = 1MHz			3	pF
Protection						
V_{OVP_TH}	OVP positive threshold (D± rising)		4.8	5.1	5.4	V
V_{OVP_HYST}	OVP threshold hysteresis		125	250	440	mV

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5.4 Electrical Characteristics (continued)

T_A = –40°C to +125°C , V_{CC} = 2.3V to 5.5V, GND = 0V, Typical values are at V_{CC} = 3.3V, T_A = 25°C, (unless otherwise noted) .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CLAMP_V}	Maximum voltage to appear on D1± and D2± pins during OVP scenario	$V_{D±}$ = 0V to 28V VCC=2.3V-5.5V t_{RISE} (10% to 90%) = 100ns R_L = Open OEn= 0V		7.24	7.67	V
		$V_{D±}$ = 0V to 28V t_{RISE} (10% to 90%) = 100ns R_L = 50Ω Switch on or off OEn = 0V		6.8	7.3	V
t_{CLAMP}	Maximum OVP transient duration above 5V	$V_{D±}$ = 0V to 28V VCC=2.3-5.5 t_{RISE} (10% to 90%) = 100ns R_L = Open OEn= 0V		54	84	ns
		$V_{D±}$ = 0V to 28V t_{RISE} (10% to 90%) = 100ns R_L = 50Ω Switch on or off OEn = 0V		39	56	ns

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5.5 Dynamic Characteristics

T_A = –40°C to +125°C , V_{CC} = 2.3V to 5.5V, GND = , Typical values are at V_{CC} = 3.3V, T_A = 25°C, (unless otherwise noted) .

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OFF}	D+, D– off capacitance	$V_{D±}$ = 0 or 3.3V, OEn= V_{CC} f = 240MHz	Switch OFF	1.2	2.7	3.4	pF
	D1+, D1–, D2+, D2– off capacitance	$V_{D±}$ = 0 or 3.3V, OEn = V_{CC} or OEn = 0V with SEL (switch not selected) f = 240MHz	Switch OFF or not selected	1.2	1.6	3.0	pF
C_{ON}	IO pins ON capacitance	$V_{D±}$ = 0 or 3.3V, f = 240MHz	Switch ON	1	1.3	3.9	pF
O_{ISO}	Differential off isolation	R_L = 50Ω C_L = 5pF () f = 100kHz () Refer to Figure 6-6	Switch OFF		–105		dB
		R_L = 50Ω C_L = 5pF () f = 240MHz Refer to Figure 6-6	Switch OFF		–25		dB
X_{TALK}	Channel to Channel crosstalk	R_L = 50Ω C_L = 5pF () f = 240MHz Refer to Figure 6-7	Switch ON		–90		dB
X_{TALK}	Channel to Channel crosstalk	R_L = 50Ω C_L = 5pF () f = 100kHz () Refer to Figure 6-7	Switch ON		-105		dB
BW	–3dB Bandwidth	R_L = 50Ω (Single-ended) Refer to Figure 6-8	Switch ON		1.4		GHz
		R_L = 50Ω (Differential) Refer to Figure 6-8	Switch ON		1.5		GHz
I_{LOSS}	Insertion loss	R_L = 50Ω f = 10 MHz Refer to Figure 6-8	Switch ON		–0.5		dB
I_{LOSS}	Insertion loss	R_L = 50Ω f = 240 MHz Refer to Figure 6-8	Switch ON		–0.8		dB

5.6 Timing Requirements

T_A = –40°C to +125°C , V_{CC} = 2.3V to 5.5V, GND = , Typical values are at V_{CC} = 3.3V, T_A = 25°C, (unless otherwise noted) .

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{SWITCH}	Switching time between channels (SEL to output)	$V_{D±}$ = 0.8V Refer to Figure 6-4	R_L = 50Ω, C_L = 5pF, V_{CC} = 2.3V to 5.5V		0.9	2.8	µs
t_{ON}	Device turn on time (OEn to output)	$V_{D±}$ = 0.8V Refer to Figure 6-5			84	250	µs
t_{OFF}	Device turn off time (OEn to output)	$V_{D±}$ = 0.8V Refer to Figure 6-5			0.75	1	µs
$t_{SK(P)}$	Skew of opposite transitions of same output (between D+ and D–)	$V_{D±}$ = 0.4V Refer to Figure 6-12	R_L = 50Ω, C_L = 5pF, V_{CC} = 2.3V to 5.5V		4	50	ps
t_{PD}	Propagation delay	$V_{D±}$ = 0.4V f = 240MHz Refer to Figure 6-11	R_L = 50Ω, C_L = 5pF, V_{CC} = 2.3V to 5.5V		110	230	ps

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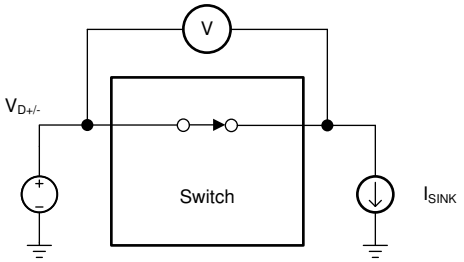
6 Parameter Measurement Information



Channel ON, $R_{ON} = V/I_{SINK}$

Figure 6-1. ON-State Resistance (R_{ON})

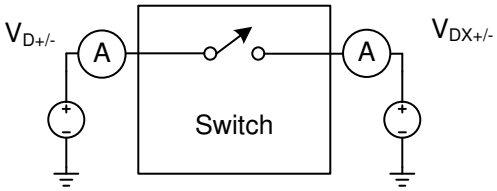


Figure 6-2. Off Leakage

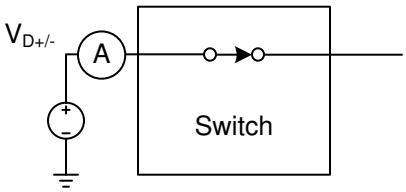
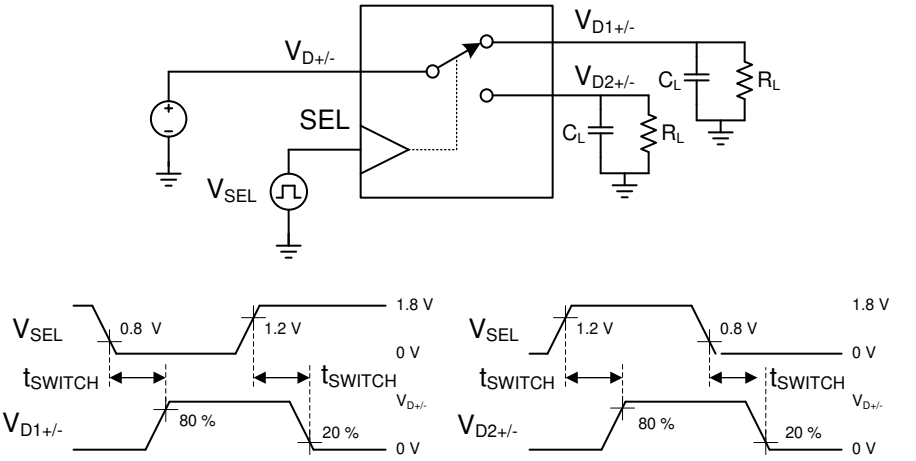
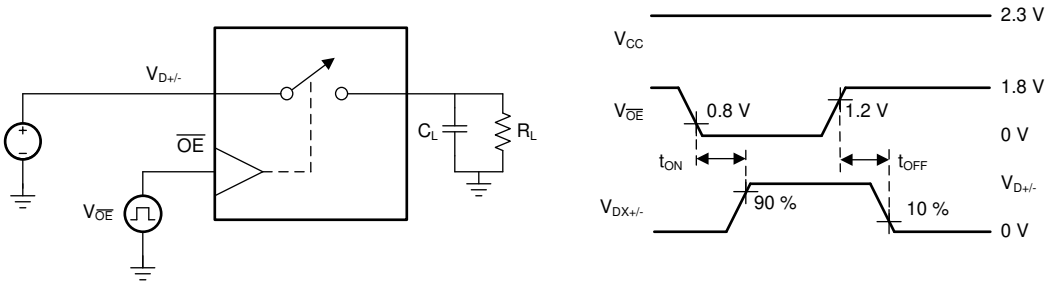


Figure 6-3. On Leakage



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r < 500ps, t_f < 500ps.
B. C_L includes probe and jig capacitance.

Figure 6-4. t_{SWITCH} Timing



A. All input pulses are supplied by generators having the following characteristics: PRR = 10MHz, Z_O = 50Ω, t_r < 500ps, t_f < 500ps.
B. C_L includes probe and jig capacitance.

Figure 6-5. t_{ON}, t_{OFF} for $\overline{OE}$

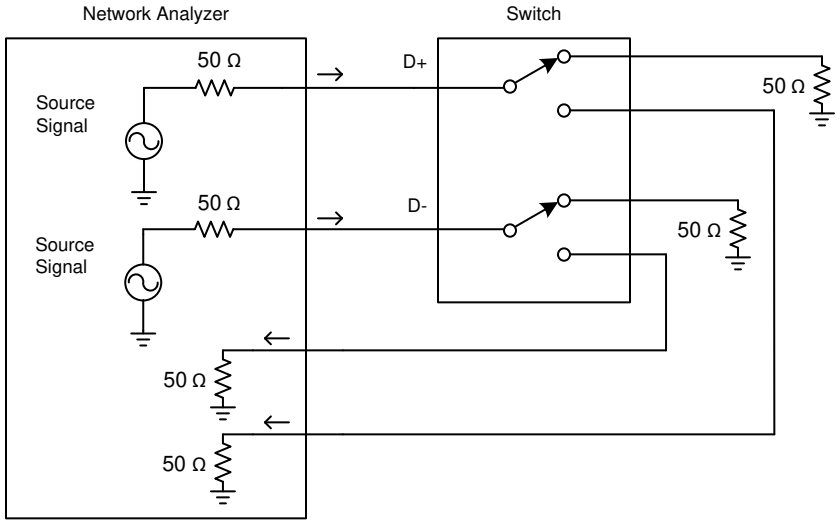


Figure 6-6. Off Isolation

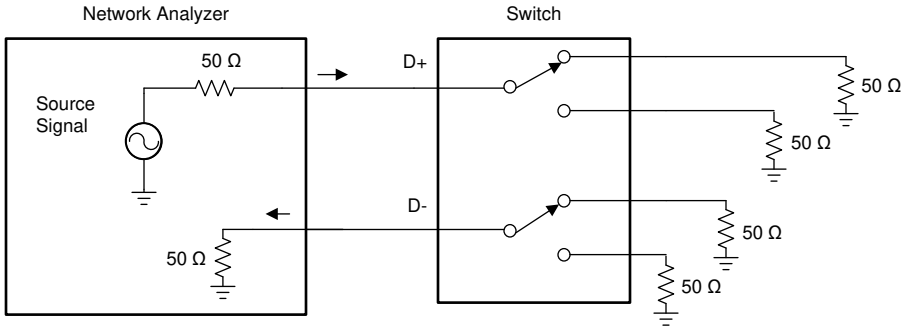


Figure 6-7. Cross Talk

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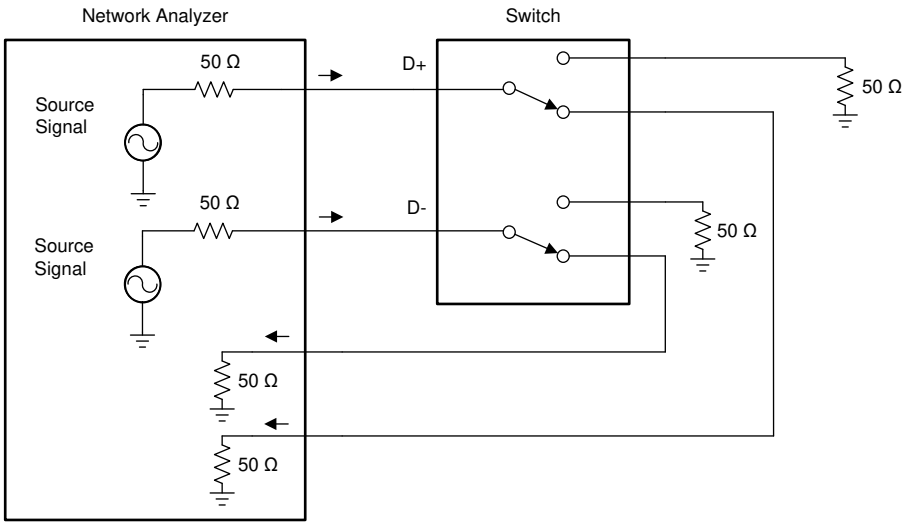


Figure 6-8. BW and Insertion Loss

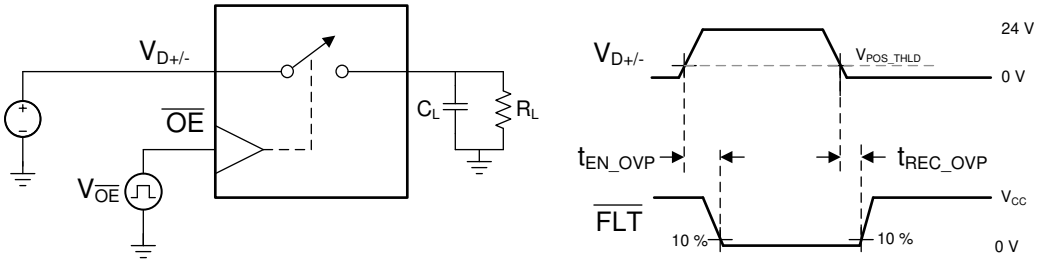


Figure 6-9. t_{EN_OVP} and t_{DIS_OVP} Timing Diagram

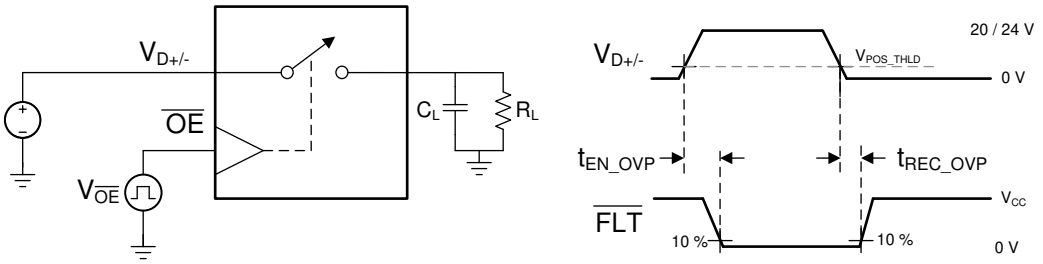
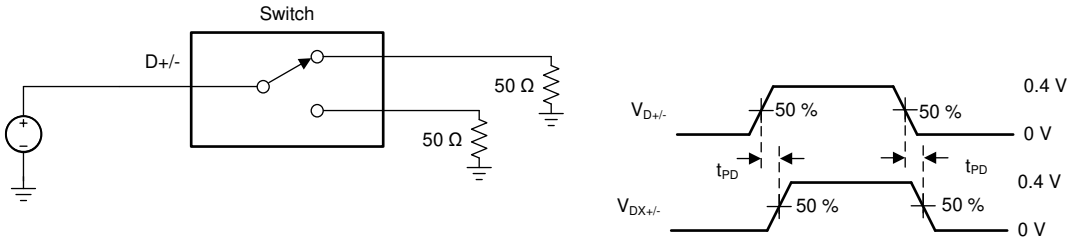
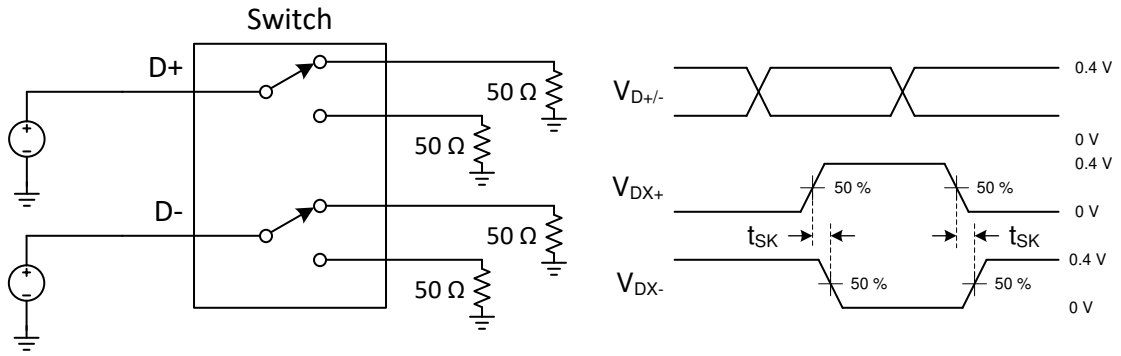


Figure 6-10. t_{EN_OVP} and t_{DIS_OVP} Timing Diagram



A. All input pulses are supplied by generators having the following characteristics: PRR = 240MHz, Z_O = 50Ω, t_r < 500ps, t_f < 500ps.
B. C_L includes probe and jig capacitance.

Figure 6-11. t_{PD}



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, t_r < 500ps, t_f < 500ps.
B. C_L includes probe and jig capacitance.

Figure 6-12. t_{SK}

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7 Detailed Description

7.1 Overview

The TMUXHS221F is a 1.2V Logic Compatible, bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C systems. The device is configured as a dual 2:1 or 1:2 switch. It is optimized for handling the multiplexing solutions for USB 2.0 D+/- lines as well as a cross point switch solution for SBU lines in a USB Type-C system as shown in Figure 7-1.

The TMUXHS221Fis an analog passive mux that can work for any low-speed, high-speed, differential or single-ended signals. The signals must be within the allowable voltage range of −0.3 to 3.6V. The device is optimized for eUSB2 and USB 2.0 LS, FS, and HS signaling. The dynamic characteristics of the device allow high-speed switching with minimal attenuation to the signal eye diagram and little added jitter. While the device is recommended for the interfaces up to 3Gbps, actual data rates where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained, the device can potentially be used for higher data rates.

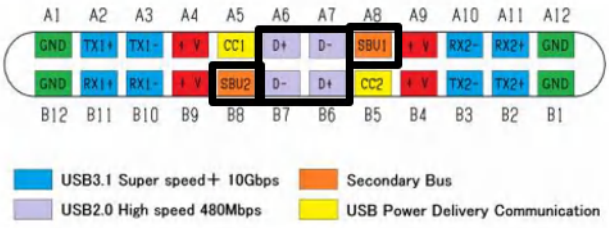
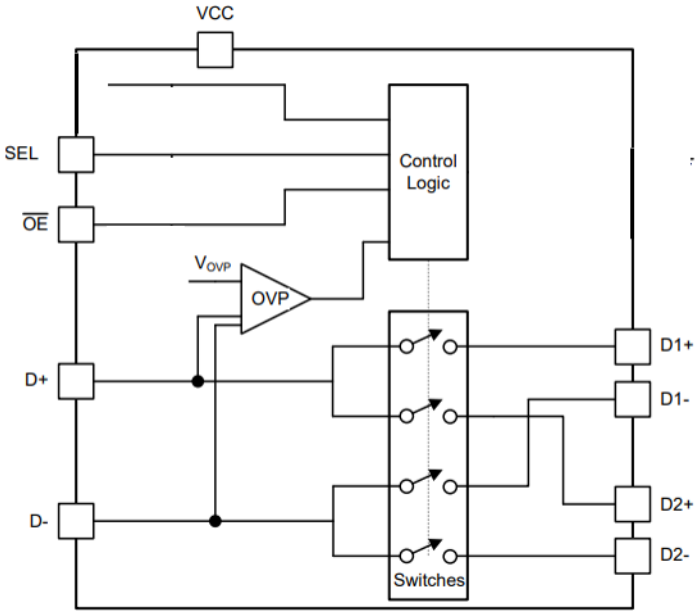


Figure 7-1. USB Type-C Connector Pinout

The TMUXHS221F also works in traditional USB systems that need protection from fault conditions such as automotive and applications that require higher voltage charging. The device maintains excellent signal integrity through the optimization of both R_{ON} and BW while protecting the system with 28V OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive a fault condition where VBUS is shorted to the SBU pins or the D+/D- pins on the connector.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Extended 1.2V Compatibility

TMUXHS221F comes with extended 1.2V control logic not only makes it compatible with latest generation of low nm SoCs but also allows sufficient noise margin for system designers and hence easy usage of TMUXHS221F. The 1.2V logic is non- scalable with supply voltages which gives immense flexibility to power up TMUXHS221F with supplies from 2.3-5.5V and still it stands compatible to 1.2V controlled switches via GPIO/I2C compatible SEL and OE pins.

7.3.2 Overvoltage Protection

The OVP of the TMUXHS221F is designed to protect the system from SBU or D+/- shorts to VBUS at the USB and USB Type-C connector. Figure 7-2 depicts a moisture short that would cause high voltage of 28V to appear on an existing USB solution that could pass through the device and damage components behind the device.

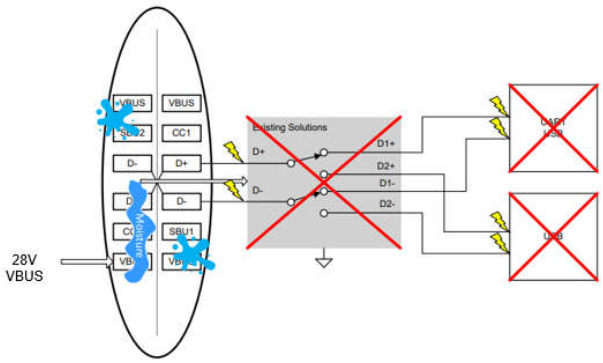


Figure 7-2. Existing Solution Being Damaged by a Short

The TMUXHS221F will open the switches and protect the rest of the system by blocking the 28V as depicted in Figure 7-3.

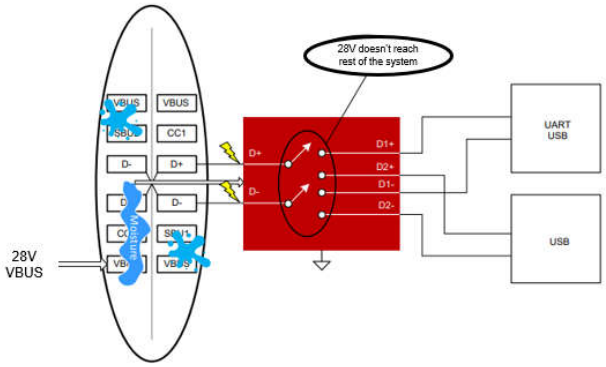


Figure 7-3. Protecting During a 28V Short

7.3.3 Powered-off Protection

When the TMUXHS221F is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the *Electrical Specifications*.

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

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7.4 Device Functional Modes

7.4.1 Pin Functions

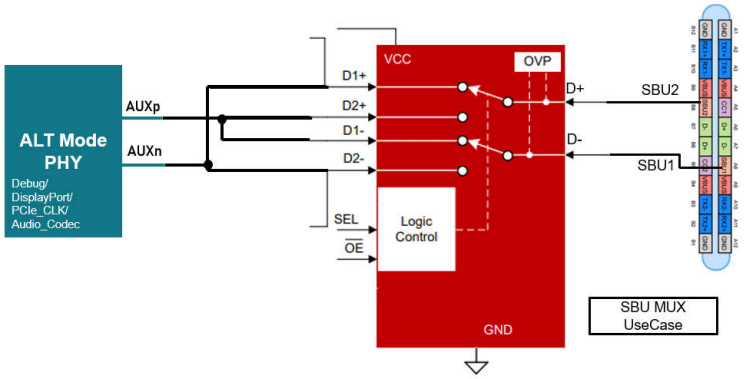

Figure 7-4. SBU Use Case

Table 7-1. SBU Configuration

SEL	OEn	MUX CONFIGURATION
L	L	SBU1 = AUXp SBU2 = AUXn
H	L	SBU2 = AUXp SBU1 = AUXn
X	H	All channels are disabled and Hi-Z

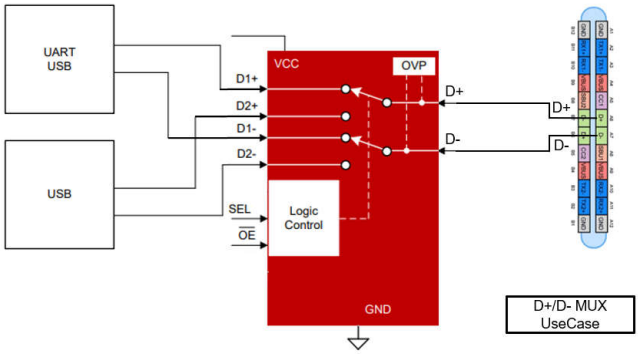

Figure 7-5. D+/D- Use Case

Table 7-2. D+/D- Configuration

SEL	OEn	MUX CONFIGURATION
L	L	D to D1
H	L	D to D2
X	H	All channels are disabled and Hi-Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os or need to route signals from a single USB connector. The TMUXHS221F solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller or route signals from on connector to two different locations.

As systems shiftingaway from using redrivers and SoC directly having high drive capabilities, passive multiplexing solutions like TMUXHS221F help adding capabilties of cross point muxes (SBU switch) or USB2.0 Data multiplexing with Over voltage protection feature so that muxes can directly interface with USB ports avoiding use of port protection ,saving area.

TMUXHS221F comes with extended 1.2V control logic not only makes it compatible with latest generation of low nm SoCs but also allows sufficient noise margin for system designers and hence easy usage of TMUXHS221F.

8.2 Typical Application 1

TMUXHS221F SBU switch. The TMUXHS221F is used as a SBU cross point mux by connecting it in the configuration where the channels are shorted in the way show below. It helps using the SBU (side band usage)pins in the USBC connector for various protocol communication like DisplayPort , Debug , PCIe, and Audio Codec. This allows all protocol support via single USBC connector. SBU mux is used as a cross point mux which helps in determining a consistent +ve and -ve configuration of the SBU1/2 to the Auxn or Auxp pins of the ALT PHY. The TMUXHS221F does not have pull-down/Pull up resistors on SEL and $\overline{OE}$. Hence, they are advised not to be floated to avoid garbage data transfer or high current.

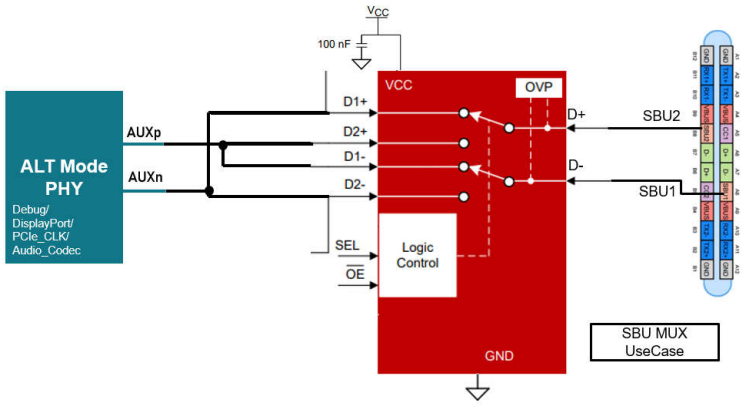

Figure 8-1. Typical TMUXHS221F Application SBU Use case

ADVANCE INFORMATION

8.3 Typical Application 2

TMUXHS221F USB/UART switch. The TMUXHS221F is used to switch signals between the USB path, which goes to the baseband or application processor, or the UART path, which goes to debug port. The TMUXHS221F does not have pull-down/Pull up resistors on SEL and $\overline{OE}$. Hence, they are advised not to be floated to avoid garbage data transfer or high current.

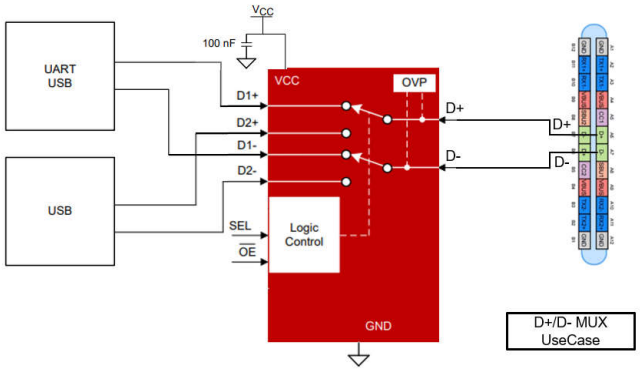

Figure 8-2. Typical TMUXHS221F Application - D+/D- Use case

8.3.1 Design Requirements

Design requirements of USB 1.0,1.1, and 2.0 standards must be followed. The TMUXHS221F does not have pull-down/Pull up resistors on SEL and $\overline{OE}$. Hence, they are advised not to be floated to avoid garbage data transfer or high current.

8.3.2 Detailed Design Procedure

The TMUXHS221F can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50Ω resistor to prevent signal reflections back into the device. TI does recommend a 100nF bypass capacitor placed close to TMUXHS221F VCC pin.

8.4 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a 100nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

8.5 Layout

8.5.1 Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the D± traces.
2. The high-speed D± must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of D+ and D– traces must match the cable characteristic differential impedance for optimal performance.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
6. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200mm.
7. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 8-3.

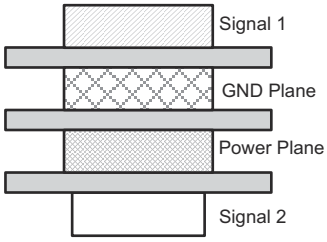

Figure 8-3. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *USB 2.0 Board Design and Layout Guidelines* application note
- Texas Instruments, *High-Speed Layout Guidelines* application note
- Texas Instruments, *High-Speed Interface Layout Guidelines* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
September 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTMUXHS221FRSWR	Active	Preproduction	UQFN (RSW) | 10	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

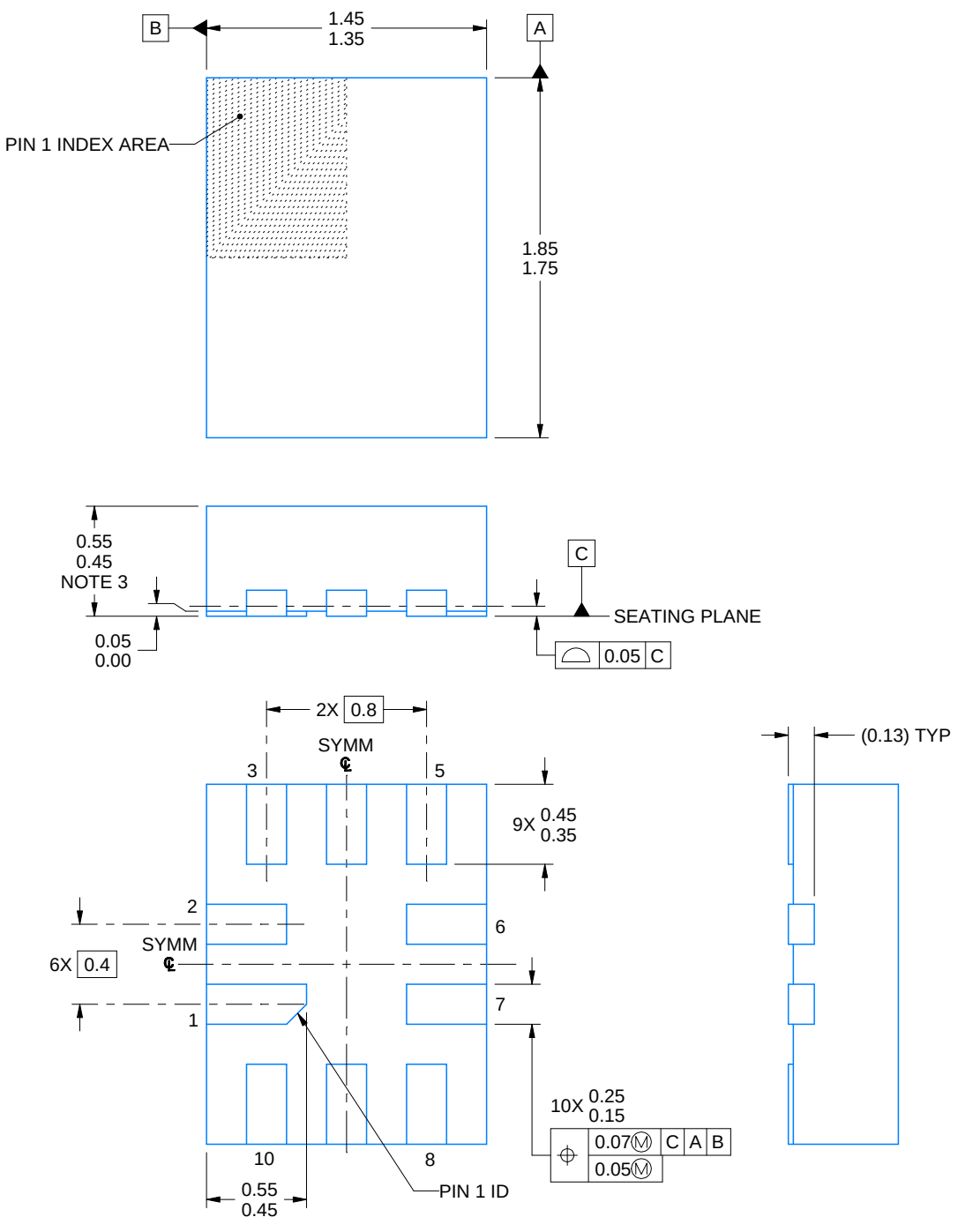
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

RSW0010A

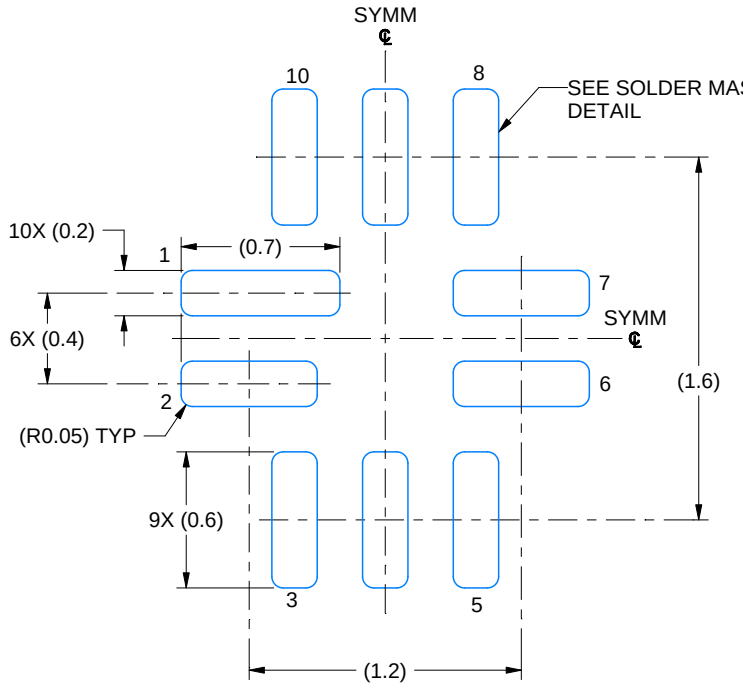
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

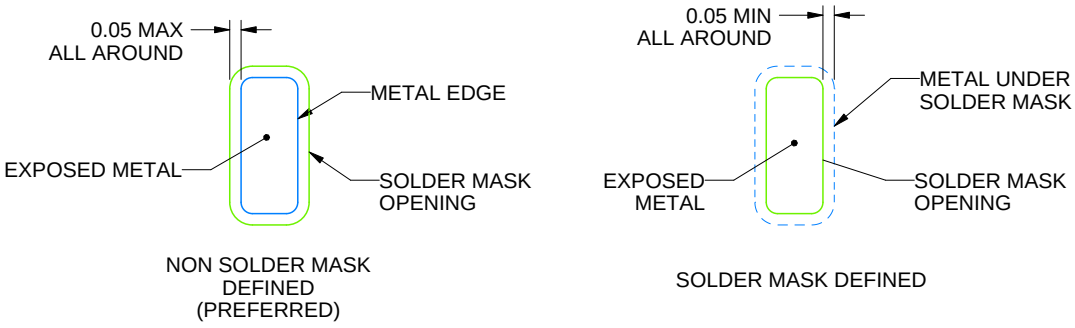


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

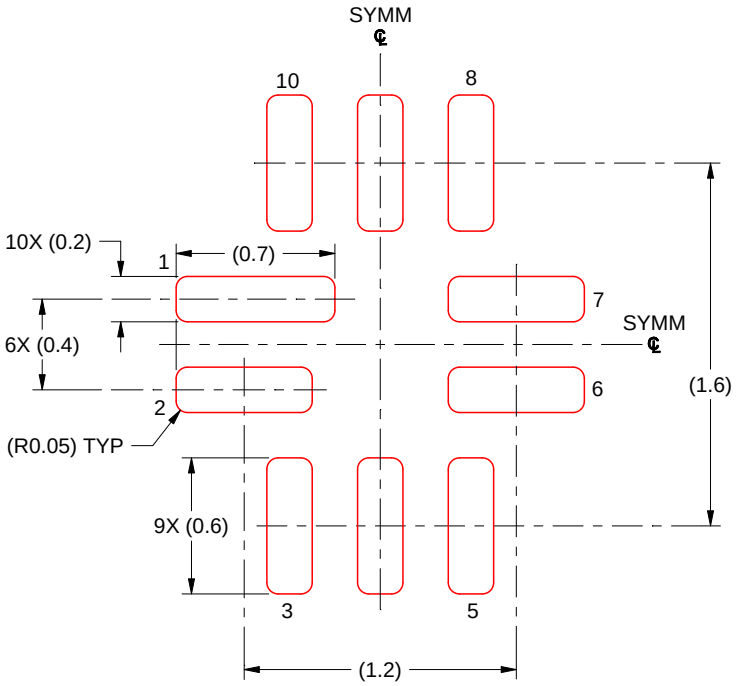


SOLDER MASK DETAILS

4224897/A 03/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4224897/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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