# TMUX9612 220V, Flat Ron, 1:1 (SPST), 4-Channel Switches with Latch-Up Immunity and 1.8V Logic

## 1 Features

- High supply voltage capable:
  - Dual supply: ±10V to ±110V
  - Single supply: 10V to 140V
  - Asymmetric dual supply operation: between +90V / –130V and 140V / -80V
- Consistent parametric across supply voltages
- Latch-up immune
- High continuous current: 200mA
- Low input leakage: 80pA at 25°C
- Low charge injection: –20pC
- Low off isolation & crosstalk: < –100dB
- Low On-Resistance flatness: 0.435Ω
- Low On-Resistance: 14Ω
- Low off-capacitance: 5pF
- Removes need for additional logic rail ($V_L$)
- 1.8-V Logic capable
- Fail-safe logic: up to 48 V independent of supply
- Integrated Pull-Down resistor on logic pins
- Bidirectional signal path
- Wide operating temperature $T_A$: –40°C to 125°C
- Industry-standard, small WQFN package

## 2 Applications

- High voltage bidirectional switching
- Analog and digital signal switching
- Semiconductor test equipment
- LCD test equipment
- Battery test equipment
- Data acquisition systems (DAQ)
- Digital multi-meter (DMM)
- Factory automation and control
- Programmable logic controllers (PLC)
- Analog input modules

## 3 Description

The TMUX9612 is a modern high voltage capable analog switch with Latch-Up immunity. Each device has four independently controllable 1:1, single-pole single-throw (SPST) switch channels. The device works well with dual supplies, a single supply, or asymmetric supplies up to a maximum supply voltage of 220V. The TMUX9612 device provides consistent analog parametric performance across the entire supply voltage range. The device also supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins.

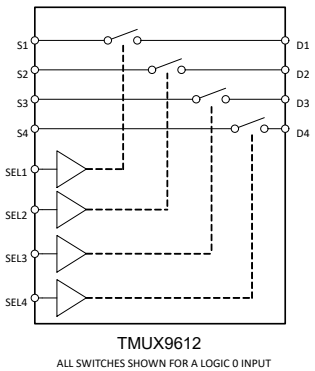
All logic inputs support logic levels of 1.8V, 3.3V, and 5V and can be connected as high as 48V, allowing for system flexibility with control signal voltage. Fail-safe logic circuitry allows voltages on the logic pins to be applied before the supply pin, protecting the device from potential damage.

The device provides Latch-Up immunity, preventing undesirable high current events between parasitic structures within the device. A Latch-Up condition typically continues until the power supply rails are turned off and can lead to device failure. The Latch-Up immunity feature allows this family of multiplexers to be used in harsh environments.

**Package Information**

| PART NUMBER(2) | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| TMUX9612 | RUM (WQFN, 16) | 4.00mm × 4.00mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) See the *Device Comparison Table*.




**Functional Block Diagram**

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## 4 Device Comparison Table

| PRODUCT | DESCRIPTION |
|---|---|
| TMUX9612 | High Voltage, 4-channel, 1:1 (SPST) switches, (Logic High) |

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# 5 Pin Configuration and Functions

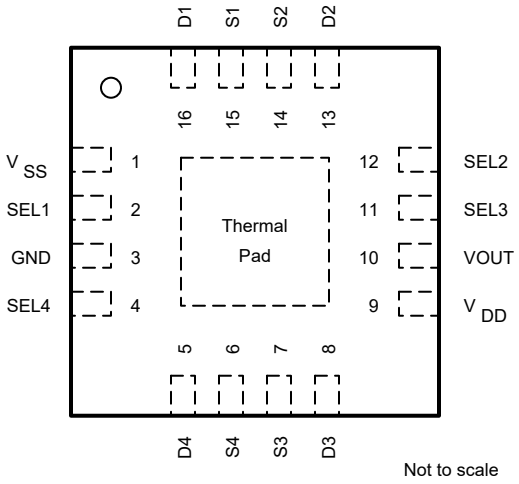


**Figure 5-1. RUM Package, 16-Pin WQFN (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | WQFN | | |
| D1 | 16 | I/O | Drain pin 1. Can be an input or output. |
| D2 | 13 | I/O | Drain pin 2. Can be an input or output. |
| D3 | 8 | I/O | Drain pin 3. Can be an input or output. |
| D4 | 5 | I/O | Drain pin 4. Can be an input or output. |
| GND | 3 | P | Ground (0 V) reference |
| S1 | 15 | I/O | Source pin 1. Can be an input or output. |
| S2 | 14 | I/O | Source pin 2. Can be an input or output. |
| S3 | 7 | I/O | Source pin 3. Can be an input or output. |
| S4 | 6 | I/O | Source pin 4. Can be an input or output. |
| SEL1 | 2 | I | Logic control input 1. |
| SEL2 | 12 | I | Logic control input 2. |
| SEL3 | 11 | I | Logic control input 3. |
| SEL4 | 4 | I | Logic control input 4. |
| VOUT | 10 | P | Internally generated voltage output rail. For reliable operation, connect a decoupling capacitor ranging from 0.01µF to 0.1µF between VOUT and GND on pin 10 or on the thermal pad. Having the decoupling capacitor as close to the thermal pad as possible yeilds the best performance. |
| $V_{DD}$ | 9 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 1µF to 10µF between $V_{DD}$ and GND. |
| $V_{SS}$ | 1 | P | Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 1µF to 10µF between $V_{SS}$ and GND. |
| Thermal Pad (VOUT) | | P | The thermal pad is internally connected to VOUT (same node as pin 10). VOUT is an internally generated voltage output rail. For reliable operation, connect a decoupling capacitor ranging from 0.01µF to 0.1µF between VOUT and GND on pin 10 or on the thermal pad. Having the decoupling capacitor as close to the thermal pad as possible yeilds the best performance. |

(1) I = input, O = output, I/O = input and output, P = power

# 6 Specifications

## 6.1 Absolute Maximum Ratings: TMUX961x Devices

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$–$V_{SS}$ | Supply voltage | | 240 | V |
| $V_{DD}$ | | –0.5 | 240 | V |
| $V_{SS}$ | | –135 | 0.5 | V |
| $V_{SELx}$ | Logic control input pin voltage (SELx) | –0.5 | 50 | V |
| $I_{SELx}$ | Logic control input pin current (SELx) | –30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain voltage (Sx, Dx) | $V_{SS}$–2 | $V_{DD}$+2 | V |
| $I_{DC}$ | Source or drain continuous current (Sx, Dx) | –200 | 200 | mA |
| $I_{IK}$ (2) | Diode clamp current at 85°C | –100 | 100 | mA |
| | Diode clamp current at 125°C | –15 | 15 | mA |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $T_A$ | Ambient temperature | –55 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Signal path pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions: TMUX961x Devices

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ – $V_{SS}$ | Power supply voltage differential | 10 | | 220 | V |
| $V_{DD}$ | Positive power supply voltage | 10 | | 140 | V |
| $V_{SS}$ | Negative power supply voltage | -130 | | 0 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pin) | $V_{SS}$ | | $V_{DD}$ (1) | V |
| $V_{SEL}$ | Logic input pin voltage | 0 | | 48 | V |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | | | $I_{DC}$ (2) | mA |

(1) $R_{ON}$ and $R_{ON\_FLAT}$ will increase when operating $V_S$ or $V_D$ greater than $V_{DD}$ - 5V. Other Electrical Characterisitics specifications may be violated as well.
(2) Refer to *Source or Drain Continuous Current* table for $I_{DC}$ specifications.

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## 6.4 Source and Drain Continuous Current

over operating free-air temperature range (unless otherwise noted)

| | PACKAGE | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DC}$ 1 ch(1) | RUM (WQFN) | Continuous current through switch for 1 channel | $T_A$ = 25°C | | | 200 | mA |
| | | | $T_A$ = 85°C | | | 200 | |
| | | | $T_A$ = 125°C | | | 110 | |
| $I_{DC}$ All ch(2) | RUM (WQFN) | Continuous current through switch on all channels at the same time | $T_A$ = 25°C | | | 150 | mA |
| | | | $T_A$ = 85°C | | | 100 | |
| | | | $T_A$ = 125°C | | | 55 | |

(1) Max continuous current shown for a single channel at a time.
(2) Max continuous current shown for all channels at a time. Refer to max power dissipation ($P_{tot}$) to ensure package limitations are not violated.

## 6.5 Source and Drain Pulse Current

over operating free-air temperature range (unless otherwise noted)

| | PACKAGE | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{DC}$ All ch(1) | RUM (WQFN) | Pulse (2) current through switch on all channels at the same time | $T_A$ = 25°C | | | 250 | mA |
| | | | $T_A$ = 85°C | | | 200 | |
| | | | $T_A$ = 125°C | | | 150 | |

(1) Max pulse current shown for all channels at a time. Refer to max power dissipation ($P_{tot}$) to ensure package limitations are not violated.
(2) Pulsed at 10ms, 10% duty cycle

## 6.6 Electrical Characteristics (Global): TMUX961x Devices

over operating free-air temperature range (unless otherwise noted)
typical at $V_{DD}$ = +110V, $V_{SS}$ = –110V, GND = 0V and $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **LOGIC INPUTS** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 48 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | Logic inputs = 0V, 5V, or 48V | –40°C to +125°C | | 0.4 | 3.8 | µA |
| $I_{IL}$ | Input leakage current | Logic inputs = 0V, 5V, or 48V | –40°C to +125°C | –0.2 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0V, 5V, or 48V | 25°C | | 130 | 175 | µA |
| | | | –40°C to +85°C | | | 190 | µA |
| | | | –40°C to +125°C | | | 210 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | Logic inputs = 0V, 5V, or 48V | 25°C | | 100 | 135 | µA |
| | | | –40°C to +85°C | | | 150 | µA |
| | | | –40°C to +125°C | | | 160 | µA |

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## 6.7 Electrical Characteristics (±110V Dual Supply)

$V_{DD}$ = +110V, $V_{SS}$ = –110V, GND = 0V (unless otherwise noted)
Typical at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = –105V to +105V<br>$I_D$ = –10mA | 25°C | | 14 | 19.6 | Ω |
| | | | –40°C to +50°C | | | 21 | |
| | | | –40°C to +85°C | | | 22.4 | |
| | | | –40°C to +125°C | | | 28 | |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = –105V to +105V<br>$I_D$ = –10mA | 25°C | | 0.28 | 0.84 | Ω |
| | | | –40°C to +50°C | | | 1 | |
| | | | –40°C to +85°C | | | 1.12 | |
| | | | –40°C to +125°C | | | 1.4 | |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = –105V to +105V<br>$I_D$ = –10mA | 25°C | | 0.435 | | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0V, $I_S$ = –10mA | –40°C to +125°C | | 0.08 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 110V, $V_{SS}$ = –110V<br>Switch state is off<br>$V_S$ = +105V / –105V<br>$V_D$ = –105V / +105V | 25°C | | 80 | TBD | pA |
| | | | –40°C to +50°C | TBD | 315 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 110V, $V_{SS}$ = –110V<br>Switch state is off<br>$V_S$ = +105V / –105V<br>$V_D$ = –105V / +105V | 25°C | | 80 | TBD | pA |
| | | | –40°C to +50°C | TBD | 315 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 110V, $V_{SS}$ = –110V<br>Switch state is on<br>$V_S$ = $V_D$ = ±105V | 25°C | | -50 | TBD | pA |
| | | | –40°C to +50°C | TBD | 120 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |

(1) When $V_S$ is positive,$V_D$ is negative. And when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating. And when $V_D$ is at a voltage potential, $V_S$ is floating.

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## 6.8 Electrical Characteristics (±50V Dual Supply)

$V_{DD}$ = +50V, $V_{SS}$ = –50V, GND = 0V (unless otherwise noted)
Typical at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = –45V to 45V<br>$I_D$ = –10mA | 25°C | | 14 | 19.6 | Ω |
| | | | –40°C to +50°C | | | 21 | |
| | | | –40°C to +85°C | | | 22.4 | |
| | | | –40°C to +125°C | | | 28 | |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = –45V to 45V<br>$I_D$ = –10mA | 25°C | | 0.28 | 0.84 | Ω |
| | | | –40°C to +50°C | | | 1 | |
| | | | –40°C to +85°C | | | 1.12 | |
| | | | –40°C to +125°C | | | 1.4 | |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = –45V to 45V<br>$I_D$ = –10mA | 25°C | | 0.4 | | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0V, $I_S$ = –10mA | –40°C to +125°C | | 0.08 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 50V, $V_{SS}$ = –50V<br>Switch state is off<br>$V_S$ = +45V / –45V<br>$V_D$ = –45V / +45V | 25°C | | 30 | TBD | pA |
| | | | –40°C to +50°C | TBD | 130 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 50V, $V_{SS}$ = –50V<br>Switch state is off<br>$V_S$ = +45V / –45V<br>$V_D$ = –45V / +45V | 25°C | | 30 | TBD | pA |
| | | | –40°C to +50°C | TBD | 130 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 50V, $V_{SS}$ = –50V<br>Switch state is on<br>$V_S$ = $V_D$ = ±45V | 25°C | | -35 | TBD | pA |
| | | | –40°C to +50°C | TBD | 25 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |

(1) When $V_S$ is positive, $V_D$ is negative. And when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating. Or when $V_D$ is at a voltage potential, $V_S$ is floating.

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## 6.9 Electrical Characteristics (100V Single Supply)

$V_{DD}$ = +100V, $V_{SS}$ = 0V, GND = 0V (unless otherwise noted)
Typical at $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0V to +95V<br>$I_D$ = –10mA | 25°C | | 14 | 19.6 | Ω |
| | | | –40°C to +50°C | | | 21 | |
| | | | –40°C to +85°C | | | 22.4 | |
| | | | –40°C to +125°C | | | 28 | |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0V to +95V<br>$I_D$ = –10mA | 25°C | | 0.28 | 0.84 | Ω |
| | | | –40°C to +50°C | | | 1 | |
| | | | –40°C to +85°C | | | 1.12 | |
| | | | –40°C to +125°C | | | 1.4 | |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0V to +95V<br>$I_D$ = –10mA | 25°C | | 0.36 | | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 50V, $I_S$ = –10mA | –40°C to +125°C | | 0.08 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 100V, $V_{SS}$ = 0V<br>Switch state is off<br>$V_S$ = +95V / 0V<br>$V_D$ = 0V / +95V | 25°C | | 30 | TBD | pA |
| | | | –40°C to +50°C | TBD | 130 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 100V, $V_{SS}$ = 0V<br>Switch state is off<br>$V_S$ = +95V / 0V<br>$V_D$ = 0V / +95V | 25°C | | 30 | TBD | pA |
| | | | –40°C to +50°C | TBD | 130 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 100V, $V_{SS}$ = 0V<br>Switch state is on<br>$V_S$ = $V_D$ = 0V / +95V | 25°C | | -35 | TBD | pA |
| | | | –40°C to +50°C | TBD | 30 | TBD | |
| | | | –40°C to +85°C | TBD | | TBD | |
| | | | –40°C to +125°C | TBD | | TBD | |

(1) When $V_S$ is positive, $V_D$ is negative. And when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating. Or when $V_D$ is at a voltage potential, $V_S$ is floating.

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## 6.10 Switching Characteristics: TMUX961x Devices

over operating free-air temperature range (unless otherwise noted)
typical at $V_{DD}$ = +110V, $V_{SS}$ = –110V, GND = 0V and $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 10V<br>$R_L$ = 300Ω, $C_L$ = 35pF | 25°C | | 40 | | µs |
| | | | –40°C to +85°C | | | 75 | |
| | | | –40°C to +125°C | | | 75 | |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 10V<br>$R_L$ = 300Ω, $C_L$ = 35pF | 25°C | | 18 | | µs |
| | | | –40°C to +85°C | | | 35 | |
| | | | –40°C to +125°C | | | 35 | |
| $t_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ ramp rate = 20V/µs,<br>$V_S$ = 10V<br>$R_L$ = 300Ω, $C_L$ = 35pF | 25°C | | 45 | | µs |
| $t_{PD}$ | Propagation delay | $R_L$ = 50Ω , $C_L$ = 5pF | 25°C | | 410 | | ps |
| $Q_{INJ}$ | Charge injection | $V_S$ = ($V_{DD}$ + $V_{SS}$) / 2, $C_L$ = 1nF | 25°C | | -20 | | pC |
| $O_{ISO}$ | Off isolation | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = ($V_{DD}$ + $V_{SS}$) / 2, f = 100kHz | 25°C | | –104 | | dB |
| $X_{TALK}$ | Inter-channel crosstalk | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = ($V_{DD}$ + $V_{SS}$) / 2, f = 100kHz | 25°C | | –110 | | dB |
| BW | –3dB bandwidth | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = ($V_{DD}$ + $V_{SS}$) / 2 | 25°C | | 530 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50Ω , $C_L$ = 5pF<br>$V_S$ = ($V_{DD}$ + $V_{SS}$) / 2, f = 1MHz | 25°C | | -1.13 | | dB |
| ACPSRR | AC power supply rejection ratio | $V_{PP}$ = 0.62V on $V_{DD}$ and $V_{SS}$<br>$R_S$ = 5Ω, 0.01µF decoupling cap on VOUT<br>$C_L$ = 50pF<br>f = 1MHz | 25°C | | –70 | | dB |
| THD+N | Total harmonic distortion + Noise | $V_{PP}$ = ($V_{DD}$ - $V_{SS}$)/2V (20V cap),<br>$V_S$ = ($V_{DD}$ + $V_{SS}$) / 2<br>$R_L$ = 1kΩ , $C_L$ = 5pF,<br>f = 20Hz to 20kHz | 25°C | | 0.0015 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = ($V_{DD}$ + $V_{SS}$) / 2V, f = 1MHz | 25°C | | 5 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = ($V_{DD}$ + $V_{SS}$) / 2V, f = 1MHz | 25°C | | 5 | | pF |
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = ($V_{DD}$ + $V_{SS}$) / 2V, f = 1MHz | 25°C | | 15 | | pF |

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## 6.11 Typical Characteristics

at $T_A$ = 25°C, $V_{DD}$ = +110V, and $V_{SS}$ = –110V (unless otherwise noted)

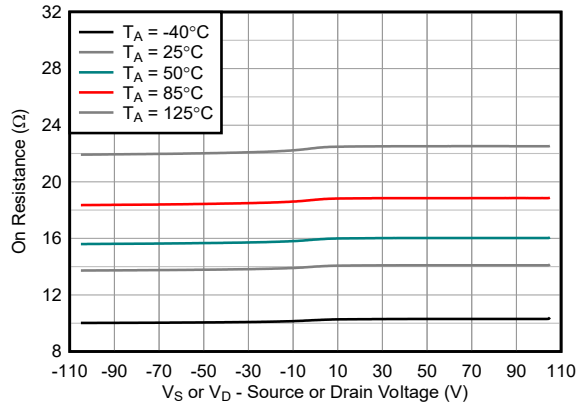


**Figure 6-1. On-Resistance vs Source or Drain Voltage**

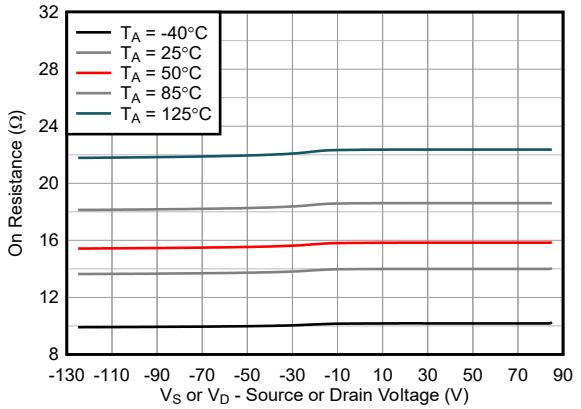


**Figure 6-2. On-Resistance vs Source or Drain Voltage**

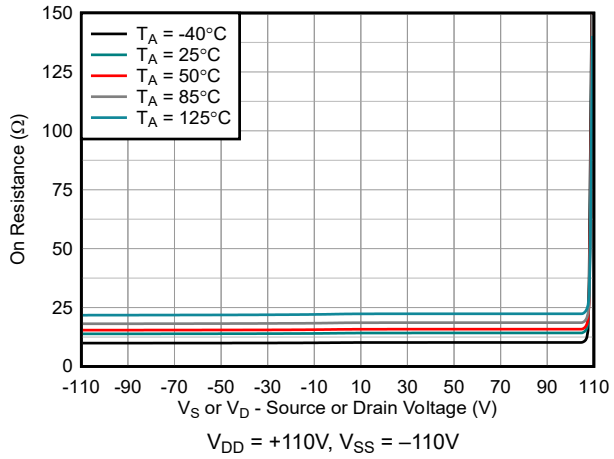


**Figure 6-3. On-Resistance vs Source or Drain Voltage**

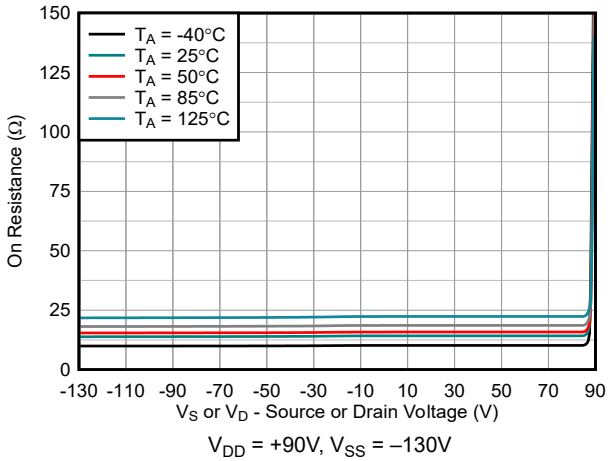


**Figure 6-4. On-Resistance vs Source or Drain Voltage**

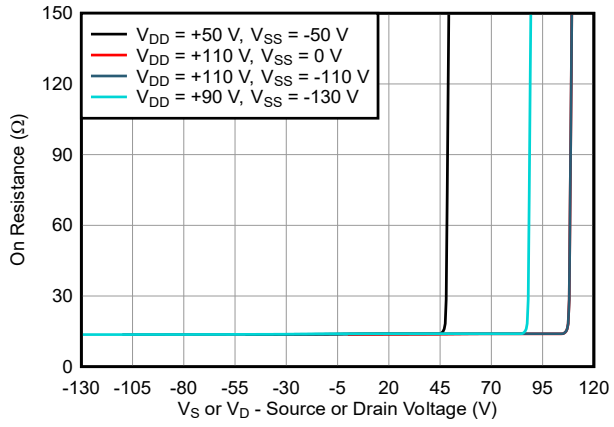


**Figure 6-5. On-Resistance vs Source or Drain Voltage**

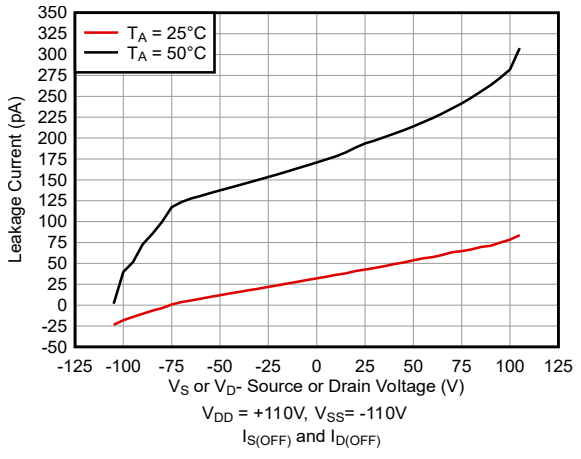


**Figure 6-6. Off-Leakage Current vs Source or Drain Voltage**

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## 6.11 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = +110V, and $V_{SS}$ = –110V (unless otherwise noted)

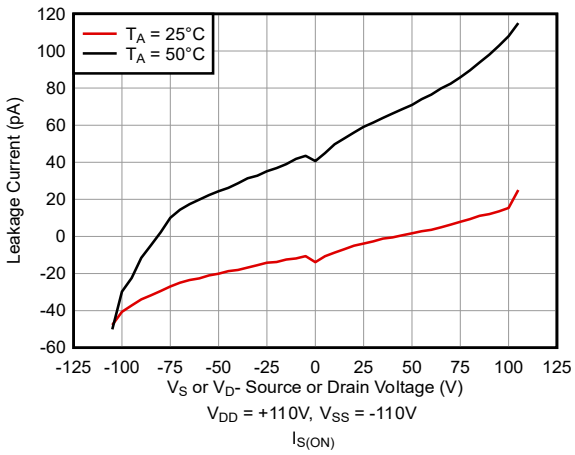


**Figure 6-7. On-Leakage Current vs Source or Drain Voltage**

ADVANCE INFORMATION

# 7 Parameter Measurement Information

## 7.1 On-Resistance

The On-Resistance of the TMUX9612 is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The On-Resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote On-Resistance. Figure 7-1 shows the measurement setup used to measure $R_{ON}$. $\Delta R_{ON}$ represents the difference between the $R_{ON}$ of any two channels, while $R_{ON\_FLAT}$ denotes the flatness that is defined as the difference between the maximum and minimum value of On-Resistance measured over the specified analog signal range.

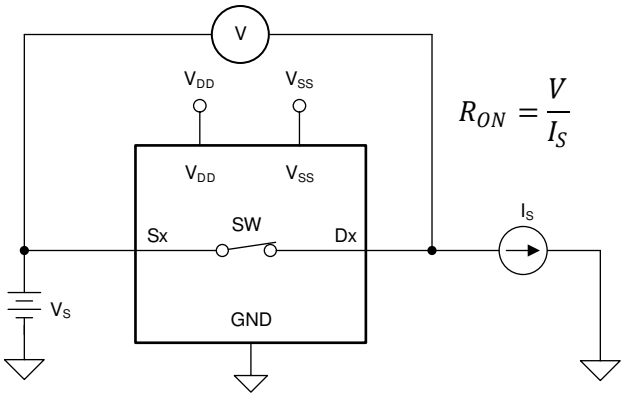


**Figure 7-1. On-Resistance Measurement Setup**

## 7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source Off-Leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain Off-Leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

Figure 7-2 shows the setup used to measure both Off-Leakage currents.

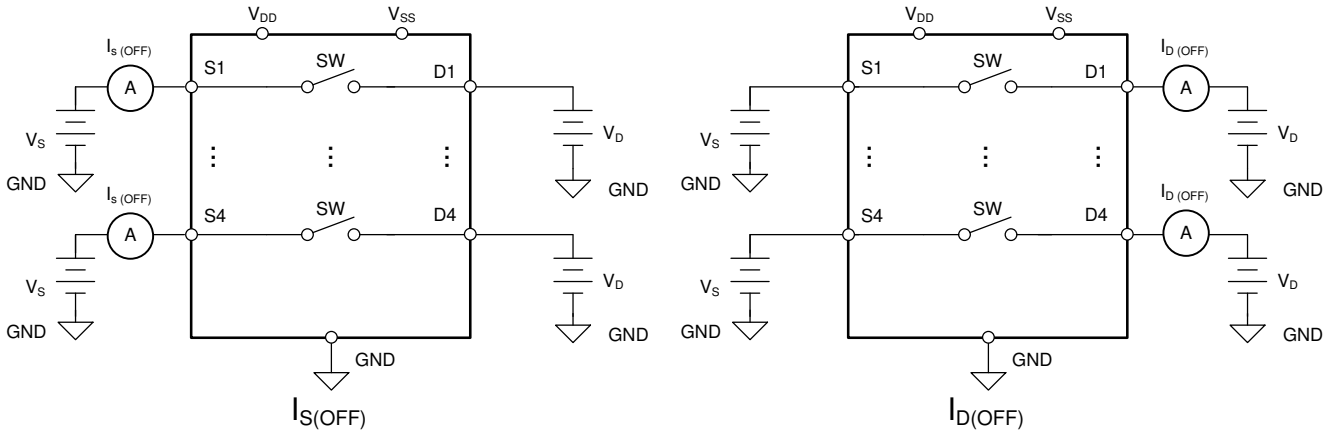


**Figure 7-2. Off-Leakage Measurement Setup**

## 7.3 On-Leakage Current

Source On-Leakage current ($I_{S(ON)}$) and drain On-Leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 7-3 shows the circuit used for measuring the On-Leakage currents.

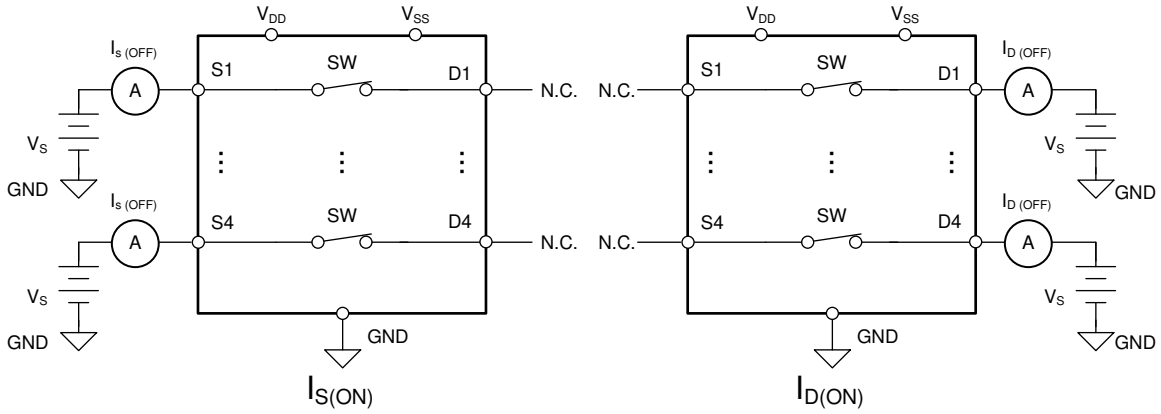


**Figure 7-3. On-Leakage Measurement Setup**

## 7.4 Device Turn-On and Turn-Off Time

Turn-On time ($t_{ON}$) is defined as the time taken by the output of the TMUX9612 to rise to a 90% final value after the SELx signal has risen (for NC switches) or fallen (for NO switches) to a 50% final value. Turn-Off time ($t_{OFF}$) is defined as the time taken by the output of the TMUX9612 to fall to a 10% initial value after the SELx signal has fallen (for NC switches) or risen (for NO switches) to a 50% initial value. Figure 7-4 shows the setup used to measure $t_{ON}$ and $t_{OFF}$.

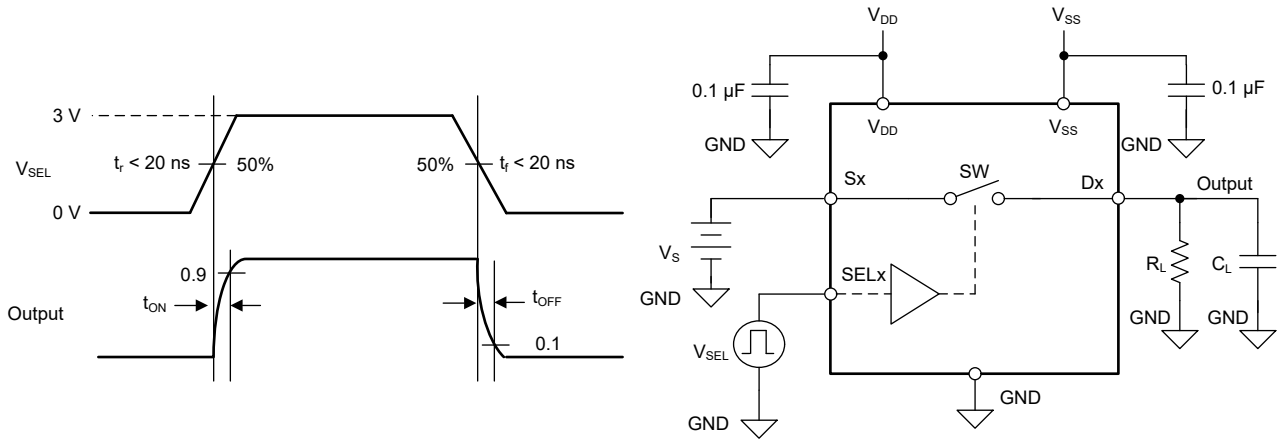


**Figure 7-4. Enable Delay Measurement Setup**

## 7.5 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching, and is denoted by the symbol $Q_{INJ}$. Figure 7-5 shows the setup used to measure charge injection from the source to drain.

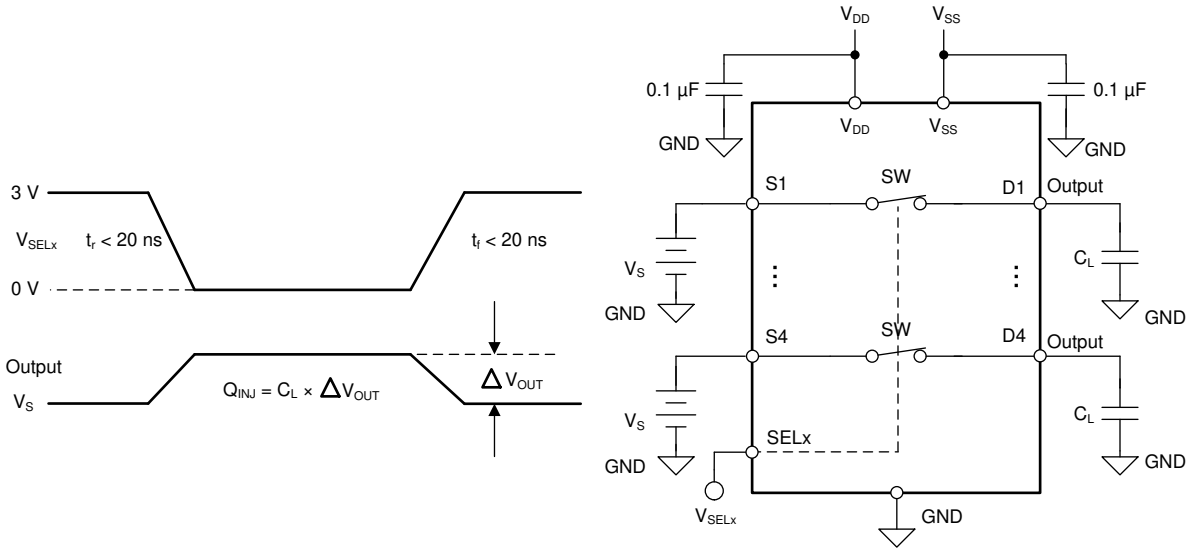


**Figure 7-5. Charge-Injection Measurement Setup**

## 7.6 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, $Z_O$, for the measurement is 50Ω. Figure 7-6 and Equation 1 shows the setup used to measure off isolation.

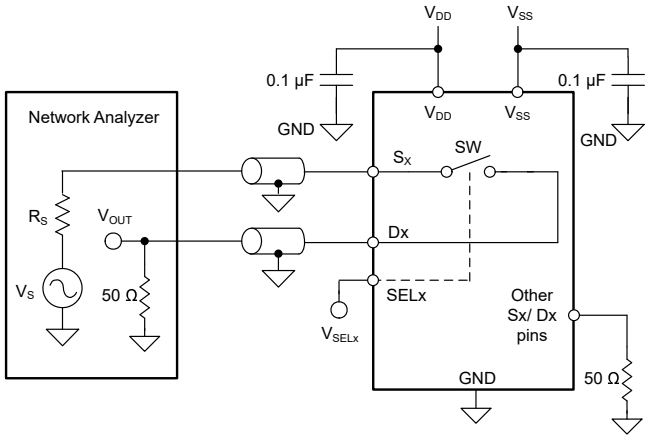


**Figure 7-6. Off Isolation Measurement Setup**

$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S} \quad (1)$$

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## 7.7 Crosstalk

Crosstalk ($X_{TALK}$) is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, $Z_O$, for the measurement is 50Ω, as shown in Figure 7-7 and Equation 2.

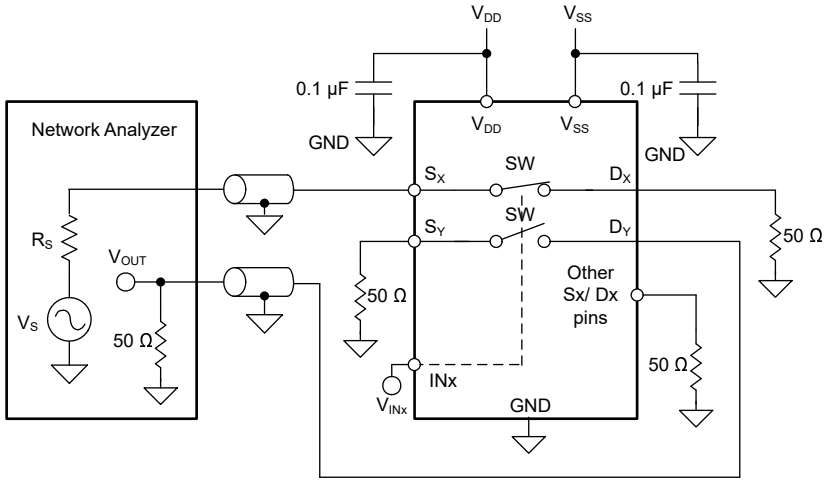


**Figure 7-7. Inter-channel Crosstalk Measurement Setup**

$$Inter-channel\ Crosstalk\ =\ 20\ \times\ Log\ \frac{V_{OUT}}{V_S} \tag{2}$$

## 7.8 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx). Figure 7-8 and Equation 3 shows the setup used to measure bandwidth of the switch.

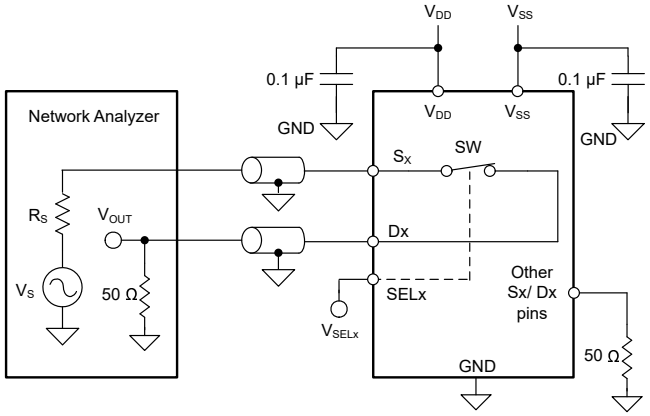


**Figure 7-8. Bandwidth Measurement Setup**

$$Bandwidth\ =\ 20\ \times\ Log\ \frac{V_{OUT}}{V_S} \tag{3}$$

## 7.9 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The On-Resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 7-9 shows the setup used to measure THD+N of the devices.

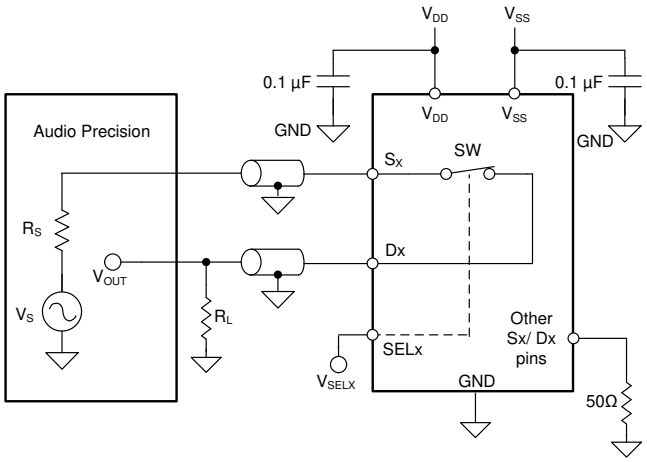


**Figure 7-9. THD+N Measurement Setup**

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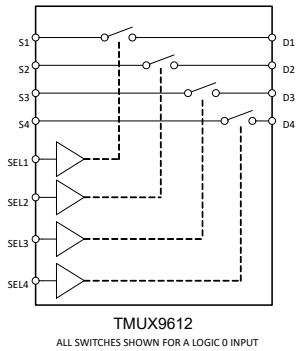
# 8 Detailed Description

## 8.1 Overview

The TMUX9612 is a modern complementary metal-oxide semiconductor (CMOS) analog switches in quad single-pole single-throw configuration. The device works well with dual supplies, a single supply, or asymmetric supplies.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### *8.3.1 Bidirectional Operation*

The devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has similar characteristics in both directions.

### *8.3.2 Flat On-Resistance*

The TMUX9612 devices are designed with a special switch architecture to produce ultra-flat On-Resistance ($R_{ON}$) across most of the switch input operating region. The flat $R_{ON}$ response allows the device to be used in precision sensor applications since the $R_{ON}$ is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

The flattest On-Resistance region extends from $V_{SS}$ to roughly 5V below $V_{DD}$. Once the signal is within 5V of $V_{DD}$ the On-Resistance will exponentially increase and may impact desired signal transmission.

### *8.3.3 Protection Features*

These devices offer a number of protection features to enable robust system implementations.

#### 8.3.3.1 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. Additionally the fail safe logic feature allows the logic inputs of the mux to be interfaced with high voltages, allowing for simplified interfacing if only high voltage control signals are present. The logic inputs are protected against positive faults of up to +48V in powered-off condition, but do not offer protection against negative over-voltage condition.

Fail-safe logic also allows the devices to interface with a voltage greater than $V_{DD}$ on the control pins during normal operation to add maximum flexibility in system design. For example, with a $V_{DD}$ = 15V, the logic control pins could be connected to +24V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 48V.

#### 8.3.3.2 ESD Protection

All pins support HBM ESD protection level up to ±2kV, which helps protect the devices from ESD events during the manufacturing process.

#### 8.3.3.3 Latch-Up Immunity

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or over-voltage), but once activated the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

In the TMUX9612 devices, an insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming. As a result, the devices are Latch-Up immune under all circumstances by device construction.

The TMUX9612 devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to over-voltage or current injections. The Latch-Up immunity feature allows the TMUX9612 to be used in harsh environments. For more information on Latch-Up immunity, refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

### *8.3.4 1.8V Logic Compatible Inputs*

The TMUX9612 devices have 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX9612 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

### *8.3.5 Integrated Pull-Down Resistor on Logic Pins*

The TMUX9612 has internal weak Pull-Down resistors to GND to ensure the logic pins are not left floating. The value of this Pull-Down resistor is approximately 4MΩ, but is clamped to 1µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

## 8.4 Device Functional Modes

### 8.4.1 Normal Mode

In Normal Mode operation, signals of up to $V_{DD}$ and $V_{SS}$ can be passed through the switch from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). The select (SELx) pins determine which switch path to turn on, according to the Truth Table. The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies ($V_{DD}$ – $V_{SS}$) must be greater than or equal to 10V. With a minimum $V_{DD}$ of 10V.
- The input signals on the source (Sx) or the drain (Dx) must be between $V_{DD}$ and $V_{SS}$.
- The logic control (SELx) must have selected the switch.

### 8.4.2 Truth Tables

TMUX9612 Truth Table shows the truth tables for the TMUX9612.

**Table 8-1. TMUX9612 Truth Table**

| SEL #(1) | CHANNEL # |
|---|---|
| 0 | Channel # OFF |
| 1 | Channel # ON |

(1) "#"designates the channel number controlled by SEL pin: "1, 2, 3, or 4"

If unused, then the SELx pins must be tied to GND or Logic High so that the devices do not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND for best performance.

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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The TMUX9612 is a high voltage switch capable of supporting analog and digital signals. The high voltage capability of these multiplexers allow them to be used in systems with high voltage signal swings, or in systems with high common mode voltages.

Additionally, the TMUX9612 provides consistent analog parametric performance across the entire supply voltage range allowing the devices to be powered by the most convenient supply rails in the system while still providing excellent performance.

## 9.2 Typical Application

A common feature of many PMUs (precision measurement units) is the ability to change current ranges. This allows for a system defined current clamp when testing devices and reduces possible damage to the PMU and DUT (device under test). In high voltage PMUs, large relays are often used to enable this switching, but this comes with the trade-off of size. To reduce system size, a multi-channel high voltage switch can be added to facilitate this switching with minimal impact to system size and performance. The TMUX9612 allows for switching between multiple current ranges, and has the added flexibility to use multiple channels in parallel for high current applications.

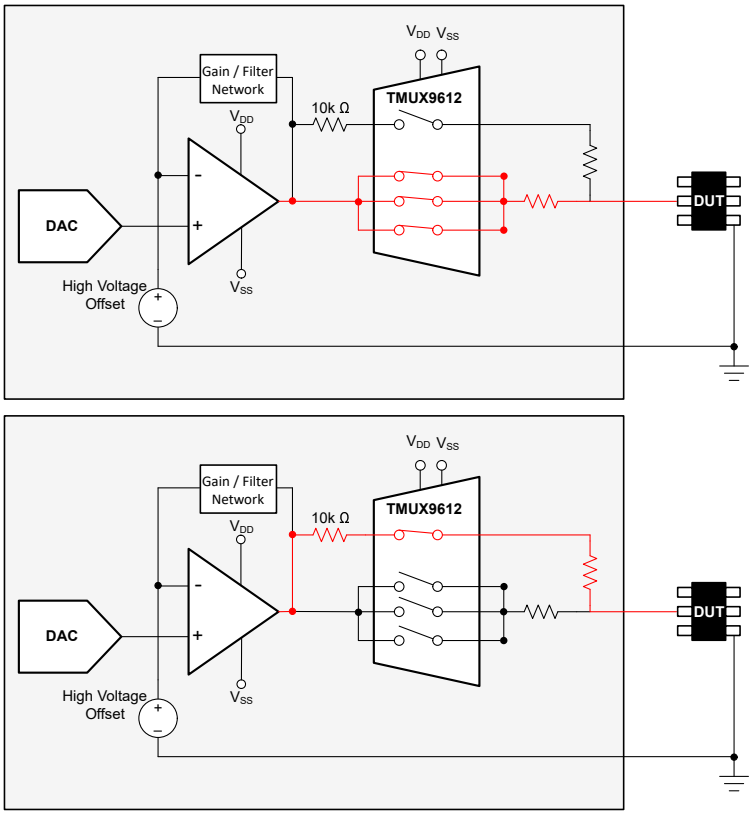


**Figure 9-1. TMUX9612 Application Schematic**

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### 9.2.1 Design Requirements

**Table 9-1. Design Parameters**

| PARAMETERS | VALUES |
|---|---|
| Positive supply ($V_{DD}$) mux and Op Amps | 110V |
| Positive supply ($V_{SS}$) mux and Op Amps | -110V |
| Maximum input or output signals with common mode shift | -110V to 110V |
| Control logic thresholds | 1.8V compatible, up to 48V |
| Temperature range | -40°C to +125°C |

### 9.2.2 Detailed Design Procedure

Multiplexing PMU systems enables a small, flexible solution that can be used over a wide range of current ranges. TI's high voltage multiplexers offer a size advantage over typical relay solutions while still achieving an extremely low level of distortion, noise, and leakage. This high voltage multiplexer can be use in tandem with high voltage operational amplifiers and DACs to create an accurate PMU with excellent signal-to-noise ratio.

In this example application, the TMUX9612 is paired with a high voltage amplifier and a DAC. The DAC generates an arbitrary voltage signal that feeds into the amplifier. An additional high voltage offset is also fed into the amplifier to add any needed common mode shift. This arbitrary signal is then passed through a current limiting resistor before reaching the DUT. To change the current range of the system, different current limiting resistors are added in series with each channel of the multiplexer. In this example, the first channel of the multiplexer uses a 10kΩ resistor for the low current clamp. The maximum output current of the PMU in this range is 5mA because of this design. During the system operation, the PMU is set to this lower current range in the beginning of the test routine. After the DUT is initially checked in this range and is operating normally with no unexpected shorts, the current range can be switched to high current. This way the PMU and DUT will not be unnecessarily damaged from excess current due to a short. In this example, the remaining three channels of the TMUX9612 are connected in parallel, increasing the maximum current through the device and reducing the low On-Resistance. Because of the flexibility of the TMUX9612, this could easily be modified to fit any system need. For example, if less maximum current is needed, then two channels could be connected in parallel instead of three, and the additional single channel could be used to add a third current range option. The additional input channels make this multiplexed application increasingly valuable by greatly reducing solution size.

The TMUX9612 switches have exceptionally flat On-Resistance and low leakage currents across the signal voltage range. The ultra-flat On-Resistance keeps the current clamp constant across the signal voltage range, and the low leakage current reduces the potential noise/offset when measuring on the lowest current range. Additionally, excellent crosstalk and off-isolation performance allows the TMUX9612 device to perform well in multi-channel switching applications without having an unselected channel impact the measurement on selected channels.

### 9.2.3 Application Curves

The example application utilizes the excellent leakage and On-Resistance flatness performance of the TMUX9612 device. Figure 9-2 shows the leakage current for a channel that is ON across a varying source voltage. Figure 9-3 shows the extremely flat On-Resistance across source voltage while operating within the flattest $R_{ON}$ range of the TMUX9612 device. These features make the device an option for applications that require excellent linearity and low distortion.

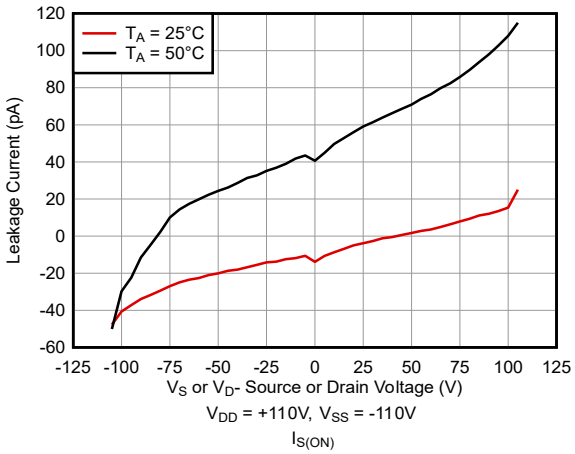


**Figure 9-2. On-Leakage**

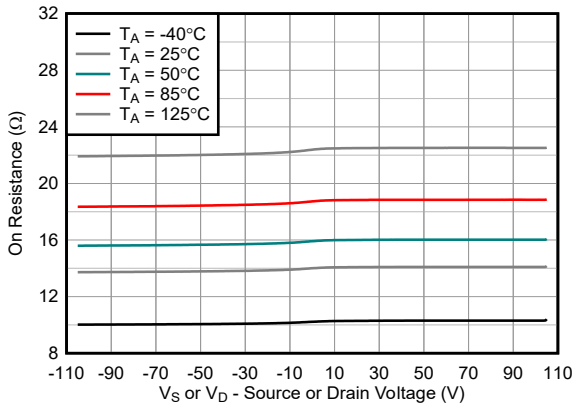


**Figure 9-3. $R_{ON}$ Flatness**

## 9.3 Power Supply Recommendations

The TMUX9612 device operates across a wide supply range of ±10V to ±110V (10V to 140V in single-supply mode). It also performs well with asymmetrical supplies such as $V_{DD}$ = 140V and $V_{SS}$= –80V or $V_{DD}$ = 90V and $V_{SS}$= –130V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1µF to 10µF at both the $V_{DD}$ and $V_{SS}$ pins to ground. An additional 0.1µF capacitor placed closest to the supply pins will provide the best supply decoupling solution. Always ensure the ground (GND) connection is established before supplies are ramped.

VOUT is an internally generated voltage output rail. For reliable operation, connect a decoupling capacitor ranging from 0.01µF to 0.1µF between VOUT and GND on pin 10 or on the thermal pad. Having the decoupling capacitor as close to the thermal pad as possible yeilds the best performance.

## 9.4 Layout

### 9.4.1 Layout Guidelines

The image below illustrates an example of a PCB layout with the TMUX9612 device. Some key considerations are:

- For reliable operation, connect at least one decoupling capacitor ranging from 0.1µF to 10µF between $V_{DD}$ and $V_{SS}$ to GND. We recommend a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- For reliable operation, connect at least one decoupling capacitor ranging from 0.01µF to 0.1µF between VOUT to GND. We recommend a capacitor with sufficient voltage rating, that can keep its capacitance value to at least 0.01µF at 100V.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

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### 9.4.2 Layout Example

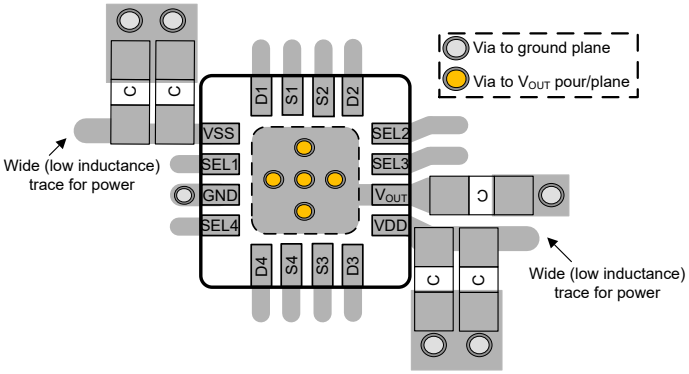



**Figure 9-4. TMUX9612 Layout Example**

ADVANCE INFORMATION

# 10 Device and Documentation Support

## 10.1 Documentation Support

### *10.1.1 Related Documentation*

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 11 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| July 2025 | * | Initial APL Release |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PTMUX9612RUMR | Active | Preproduction | WQFN (RUM) \| 16 | 3000 \| LARGE T&R | - | Call TI | Call TI | - | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

# GENERIC PACKAGE VIEW

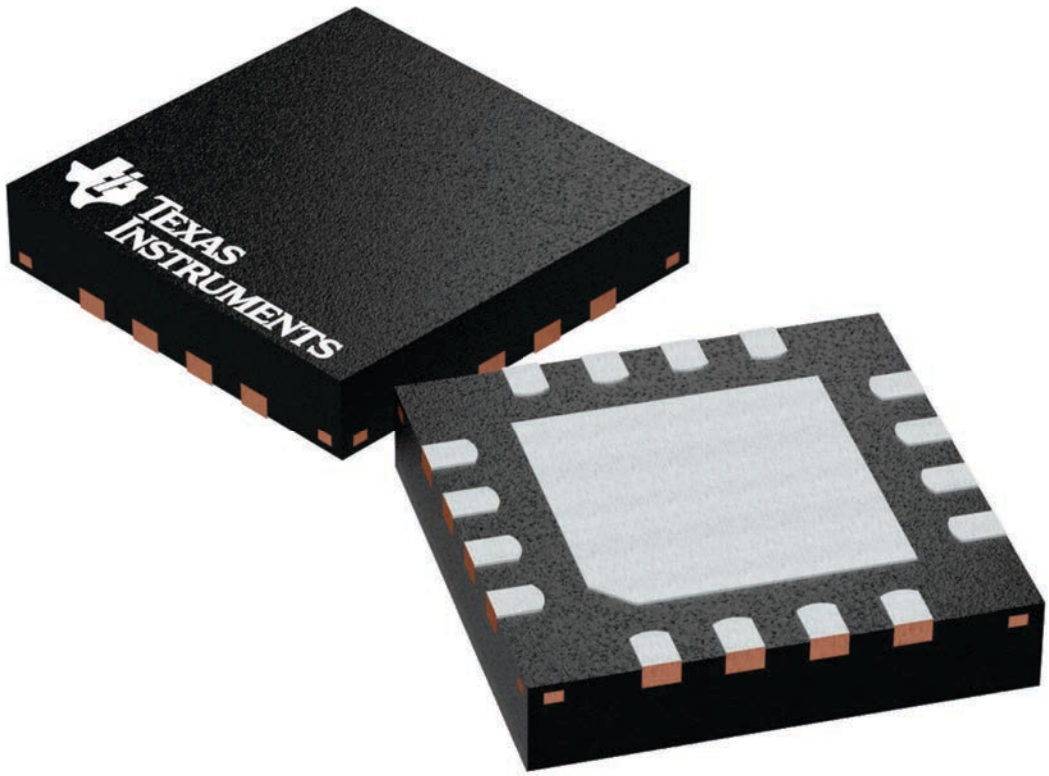
## RUM 16

## WQFN - 0.8 mm max height

**4 x 4, 0.65 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265