![Texas Instruments logo] **TEXAS INSTRUMENTS**

TMUX7211, TMUX7212, TMUX7213
SCDS416D – OCTOBER 2020 – REVISED JULY 2024

TMUX721x 44V, Low-RON, 1:1 (SPST), 4-Channel Precision Switches with Latch-Up Immunity and 1.8-V Logic

1 Features

- Latch-up immune
- Dual supply range: ±4.5V to ±22V
- Single supply range: 4.5V to 44V
- Low on-resistance: 2Ω
- High current support: 220mA (maximum) (TSSOP)
- −40°C to +125°C operating temperature
- Integrated pull-down resistor on logic pins
- 1.8V logic compatible
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional operation

2 Applications

- EV charging station power module
- Advanced driver assistance systems (ADAS)
- Automotive gateway
- Analog and digital multiplexing or demultiplexing
- Automotive head unit
- Telematics control unit
- Emergency call (eCall)
- Infotainment
- Body control modules (BCM)
- Body electronics and lighting
- Battery management systems (BMS)
- HVAC controller module
- ADAS domain controller

3 Description

The TMUX7212 is a complementary metal-oxide semiconductor (CMOS) switch with four independently selectable 1:1, single-pole, single-throw (SPST) switch channels. This device works with a single supply (4.5V to 44V), dual supplies (±4.5V to ±22V), or asymmetric supplies (such as V_{DD} = 12V, V_{SS} = −5V). The TMUX721x supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}.

The switches of the TMUX721x are controlled with appropriate logic control inputs on the SELx pins. The TMUX721x is part of the precision switches and multiplexers family of devices and has very low on and off leakage currents allowing them to be used in high precision measurement applications.

The TMUX721x provides latch-up immunity, preventing undesirable high current events between parasitic structures within the device typically caused by overvoltage events. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows the TMUX721x to be used in harsh environments.

Table 3-1. Device Information

PART NUMBER [1]	ACTIVE LOGIC	PACKAGE [2]
TMUX7211	Logic Low	PW (TSSOP, 16)
TMUX7212	Logic High	RUM (WQFN, 16)
TMUX7213	Logic Low + Logic High	

(1)   See Device Comparison.
(2)   For more information, see Section 12.

TMUX7211
(SELx = Logic 1)

TMUX7212
(SELx = Logic 1)

TMUX7213
(SELx = Logic 1)
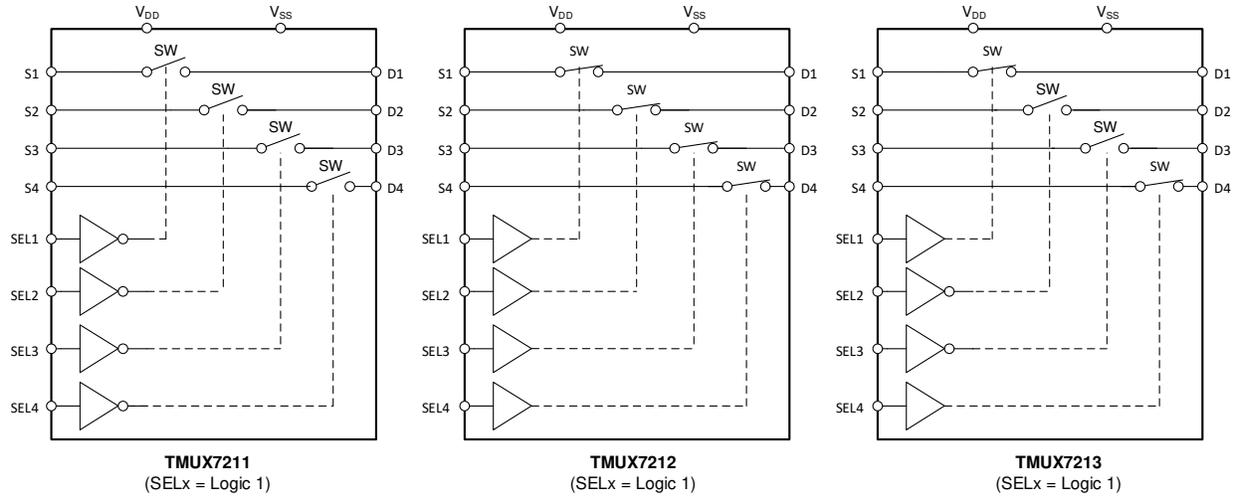
TMUX721x Functional Block Diagram

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4 Device Comparison Table

| PRODUCT	DESCRIPTION
TMUX7211	Low-Leakage-Current, Precision, 4-Channel, 1:1 (SPST) Switches (Logic Low)
TMUX7212	Low-Leakage-Current, Precision, 4-Channel, 1:1 (SPST) Switches (Logic High)
TMUX7213	Low-Leakage-Current, Precision, 4-Channel, 1:1 (SPST) Switches (Logic Low + Logic High)

5 Pin Configuration and Functions
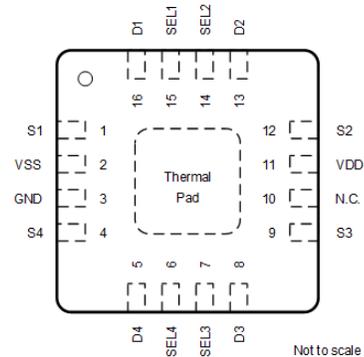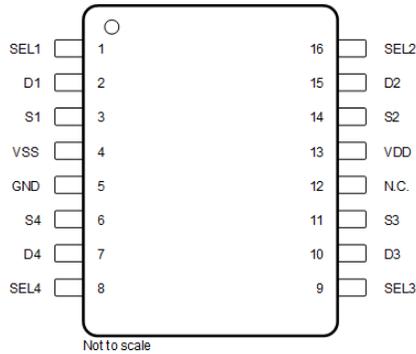
Figure 5-1. PW Package, 16-Pin TSSOP (Top View)

Figure 5-2. RUM Package, 16-Pin WQFN (Top View)

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION [2]
NAME	TSSOP	WQFN		
D1	2	16	I/O	Drain pin 1. Can be an input or output.
D2	15	13	I/O	Drain pin 2. Can be an input or output.
D3	10	8	I/O	Drain pin 3. Can be an input or output.
D4	7	5	I/O	Drain pin 4. Can be an input or output.
GND	5	3	P	Ground (0 V) reference
N.C.	12	10	—	No internal connection. Can be shorted to GND or left floating.
S1	3	1	I/O	Source pin 1. Can be an input or output.
S2	14	12	I/O	Source pin 2. Can be an input or output.
S3	11	9	I/O	Source pin 3. Can be an input or output.
S4	6	4	I/O	Source pin 4. Can be an input or output.
SEL1	1	15	I	Logic control input 1, has internal 4 MΩ pull-down resistor. Controls channel 1 state as shown in Section 8.5.
SEL2	16	14	I	Logic control input 2, has internal 4 MΩ pull-down resistor. Controls channel 2 state as shown in Section 8.5.
SEL3	9	7	I	Logic control input 3, has internal 4 MΩ pull-down resistor. Controls channel 3 state as shown in Section 8.5.
SEL4	8	6	I	Logic control input 4, has internal 4 MΩ pull-down resistor. Controls channel 4 state as shown in Section 8.5.
VDD	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μF to 10 μF between V_{DD} and GND.
VSS	4	2	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 μF to 10 μF between V_{SS} and GND.
Thermal Pad			—	The thermal pad is not connected internally. No requirement to solder this pad, if connected it is recommended that the pad be left floating or tied to GND

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to Section 8.4 for what to do with unused pins.

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$			48	V
V_{DD}	Supply voltage	−0.5	48	V
V_{SS}		−48	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	−0.5	48	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	−30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}−0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current[3]	−30	30	mA
I_S or $I_{D (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %[4]	mA
T_A	Ambient temperature	−55	150	°C
T_{stg}	Storage temperature	−65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (QFN)[5]		1650	mW
	Total power dissipation (TSSOP)[5]		700	mW

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearly above T_A = 70°C by 24.2mW/°C.
For TSSOP package: P_{tot} = 700 mW (max) and derates linearly above T_A = 70°C by 10.7mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
TMUX721x in PW package				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	
TMUX721x in RUM package				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX721x		UNIT
		PW (TSSOP)	RUM (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.5	41.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.5	25.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	16.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.4	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.9	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ [1]	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		44	V
I_S or $I_{D\,(CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ ($V_{DD} - V_{SS}$) ≤ 44 V, and the minimum V_{DD} is met.
(2)   Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC}) [2]		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
PW (TSSOP)	+44 V Dual Supply[1]	220	160	100	mA
	±15 V Dual Supply	220	160	100	mA
	+12 V Single Supply	190	130	90	mA
	±5 V Dual Supply	170	120	80	mA
	+5 V Single Supply	130	90	60	mA
RUM (WQFN)	+44 V Single Supply[1]	330	220	120	mA
	±15 V Dual Supply	330	220	120	mA
	+12 V Single Supply	260	180	110	mA
	±5 V Dual Supply	240	160	100	mA
	+5 V Single Supply	180	120	80	mA

(1)   Specified for nominal supply voltage only.
(2)   Refer to Total power dissipation (P_{tot}) limits in *Absolute Maximum Ratings* table that must be followed with max continuous current specification.

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		2	2.7	Ω
			–40°C to +85°C			3.4	Ω
			–40°C to +125°C			4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–40°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA Refer to On-Resistance	25°C		0.2	0.46	Ω
			–40°C to +85°C			0.65	Ω
			–40°C to +125°C			0.7	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–20		20	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–20		20	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V Refer to On-Leakage Current	25°C	–0.4	0.1	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–3		3	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		35	56	µA
			–40°C to +85°C			65	µA
			–40°C to +125°C			80	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		5	20	µA
			–40°C to +85°C			24	µA
			–40°C to +125°C			35	µA

(1)   When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2)   When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		100	175	ns
			–40°C to +85°C			205	ns
			–40°C to +125°C			225	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		80	205	ns
			–40°C to +85°C			225	ns
			–40°C to +125°C			240	ns
t_{BBM}	Break-before-make time delay (TMUX7213 Only)	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		27		ns
			–40°C to +85°C	5			ns
			–40°C to +125°C	5			ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 μs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–40°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to Propagation Delay	25°C		260		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to Charge Injection	25°C		60		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		56		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–68		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		28		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		45		pF
$C_{S(ON)},$ $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		145		pF

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

6.8 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA Refer to On-Resistance	25°C		1.7	2.5	Ω
			–40°C to +85°C			3	Ω
			–40°C to +125°C			3.6	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			–40°C to +85°C			0.19	Ω
			–40°C to +125°C			0.21	Ω
$R_{ON FLAT}$	On-resistance flatness	V_S = –15 V to +15 V I_S = –10 mA Refer to On-Resistance	25°C		0.3	0.6	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.95	Ω
$R_{ON DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.008		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to Off-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–4.5		4.5	nA
			–40°C to +125°C	–33		33	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V Refer to Off-Leakage Current	25°C	–1	0.1	1	nA
			–40°C to +85°C	–4.5		4.5	nA
			–40°C to +125°C	–33		33	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V Refer to On-Leakage Current	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1.5		1.5	nA
			–40°C to +125°C	–8		8	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		33	65	µA
			–40°C to +85°C			74	µA
			–40°C to +125°C			90	µA
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		7	26	µA
			–40°C to +85°C			30	µA
			–40°C to +125°C			45	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.9 ±20 V Dual Supply: Switching Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		100	185	ns
			–40°C to +85°C			210	ns
			–40°C to +125°C			230	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		90	210	ns
			–40°C to +85°C			225	ns
			–40°C to +125°C			235	ns
t_{BBM}	Break-before-make time delay (TMUX7213 Only)	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF	25°C		28		ns
			–40°C to +85°C	10			ns
			–40°C to +125°C	10			ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 μs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–40°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to Propagation Delay	25°C		260		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to Charge Injection	25°C		92		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω, C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		48		MHz
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.14		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω, C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–68		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20 V, V_{BIAS} = 0 V R_L = 10 kΩ, C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		28		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		45		pF
$C_{S(ON)},$ $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		145		pF

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

6.10 44 V Single Supply: Electrical Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 40 V I_D = −10 mA Refer to On-Resistance	25°C		2	2.4	Ω
			−40°C to +85°C			3.2	Ω
			−40°C to +125°C			3.8	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 40 V I_D = −10 mA Refer to On-Resistance	25°C		0.1	0.18	Ω
			−40°C to +85°C			0.19	Ω
			−40°C to +125°C			0.21	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 40 V I_D = −10 mA Refer to On-Resistance	25°C		0.65	0.8	Ω
			−40°C to +85°C			1.1	Ω
			−40°C to +125°C			1.2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 22 V, I_S = −10 mA Refer to On-Resistance	−40°C to +125°C		0.007		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V Refer to Off-Leakage Current	25°C	−1	0.05	1	nA
			−40°C to +85°C	−7		7	nA
			−40°C to +125°C	−50		50	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 44 V, V_{SS} = 0 V Switch state is off V_S = 40 V / 1 V V_D = 1 V / 40 V Refer to Off-Leakage Current	25°C	−1	0.05	1	nA
			−40°C to +85°C	−7		7	nA
			−40°C to +125°C	−50		50	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 44 V, V_{SS} = 0 V Switch state is on V_S = V_D = 40 V or 1 V Refer to On-Leakage Current	25°C	−1	0.05	1	nA
			−40°C to +85°C	−3.5		3.5	nA
			−40°C to +125°C	−5		5	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		−40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		−40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		−40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		−40°C to +125°C	−0.1	−0.005		µA
C_{IN}	Logic input capacitance		−40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 44 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		44	79	µA
			−40°C to +85°C			88	µA
			−40°C to +125°C			105	µA

(1)   When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2)   When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

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6.11 44 V Single Supply: Switching Characteristics

V_{DD} = +44 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +44 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		80	185	ns
			–40°C to +85°C			205	ns
			–40°C to +125°C			225	ns
t_{OFF}	Turn-off time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		90	205	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			228	ns
t_{BBM}	Break-before-make time delay (TMUX7213 Only)	V_S = 18 V, R_L = 300 Ω, C_L = 35 pF	25°C		27		ns
			–40°C to +85°C	10			ns
			–40°C to +125°C	10			ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 μs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.14		ms
			–40°C to +85°C		0.15		ms
			–40°C to +125°C		0.15		ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to Propagation Delay	25°C		270		ps
Q_{INJ}	Charge injection	V_S = 22 V, C_L = 100 pF Refer to Charge Injection	25°C		104		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		46		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–66		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 22 V, V_{BIAS} = 22 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 22 V, f = 1 MHz	25°C		28		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 22 V, f = 1 MHz	25°C		45		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 22 V, f = 1 MHz	25°C		145		pF

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6.12 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = −10 mA Refer to On-Resistance	25°C		2.8	5.4	Ω
			−40°C to +85°C			6.8	Ω
			−40°C to +125°C			7.4	Ω
$ΔR_{ON}$	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = −10 mA Refer to On-Resistance	25°C		0.13	0.21	Ω
			−40°C to +85°C			0.23	Ω
			−40°C to +125°C			0.25	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = −10 mA Refer to On-Resistance	25°C		1	1.7	Ω
			−40°C to +85°C			1.9	Ω
			−40°C to +125°C			2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = −10 mA Refer to On-Resistance	−40°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C	−0.25	0.01	0.25	nA
			−40°C to +85°C	−2		2	nA
			−40°C to +125°C	−16		16	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C	−0.25	0.05	0.25	nA
			−40°C to +85°C	−2		2	nA
			−40°C to +125°C	−16		16	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to On-Leakage Current	25°C	−0.5	0.05	0.5	nA
			−40°C to +85°C	−1		1	nA
			−40°C to +125°C	−3		3	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		−40°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		−40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		−40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		−40°C to +125°C	−0.1	−0.005		µA
C_{IN}	Logic input capacitance		−40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	44	µA
			−40°C to +85°C			52	µA
			−40°C to +125°C			62	µA

(1)   When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2)   When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.13 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		170	225	ns
			–40°C to +85°C			276	ns
			–40°C to +125°C			315	ns
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		75	248	ns
			–40°C to +85°C			285	ns
			–40°C to +125°C			310	ns
t_{BBM}	Break-before-make time delay (TMUX7213 Only)	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF	25°C		30		ns
			–40°C to +85°C	13			ns
			–40°C to +125°C	13			ns
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.18		ms
			–40°C to +125°C		0.18		ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to Propagation Delay	25°C		270		ps
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF Refer to Charge Injection	25°C		12		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Off Isolation	25°C		–70		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–50		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–112		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–93		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		125		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.25		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–70		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.001		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		35		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		50		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		145		pF

6.14 Typical Characteristics

at T_A = 25°C (unless otherwise noted)
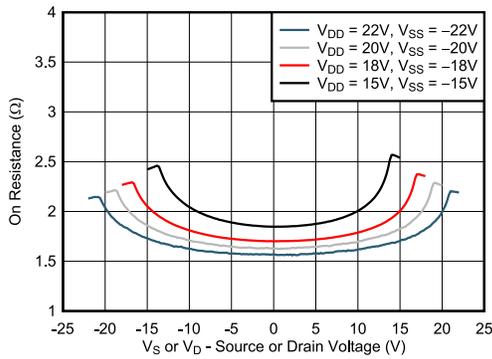
Figure 6-1. On-Resistance vs. Source or Drain Voltage – Dual Supply
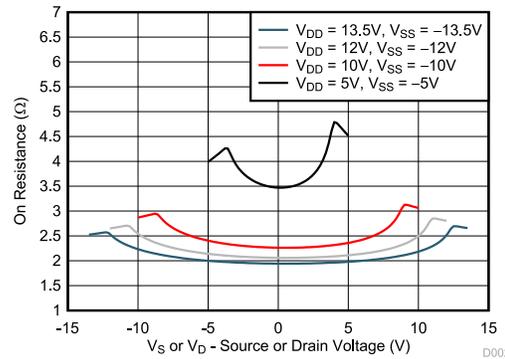
Figure 6-2. On-Resistance vs. Source or Drain Voltage – Dual Supply
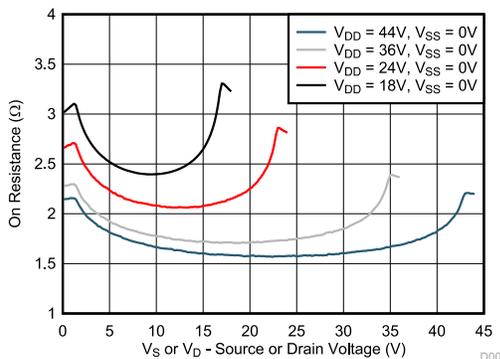
Figure 6-3. On-Resistance vs. Source or Drain Voltage – Single Supply
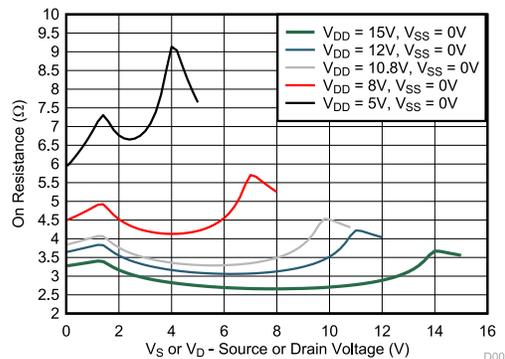
Figure 6-4. On-Resistance vs. Source or Drain Voltage – Single Supply

V_{DD} = 15 V, V_{SS} = -15 V
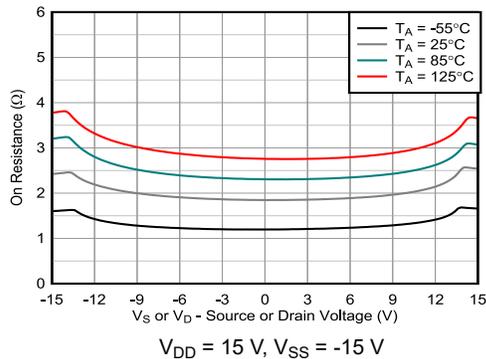
Figure 6-5. On-Resistance vs Temperature

V_{DD} = 20 V, V_{SS} = -20 V
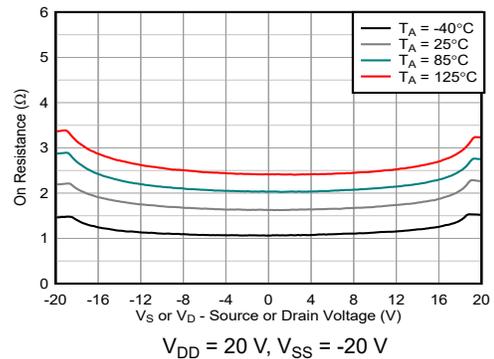
Figure 6-6. On-Resistance vs Temperature

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

V_{DD} = 12 V, V_{SS} = 0V
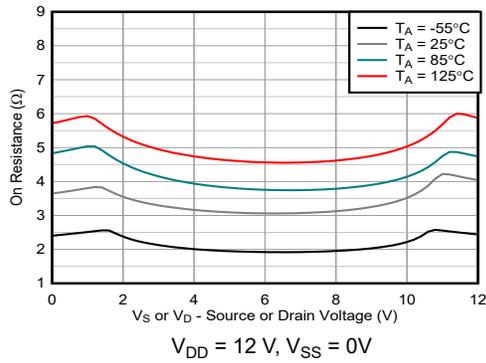
Figure 6-7. On-Resistance vs Temperature

V_{DD} = 36 V, V_{SS} = 0V
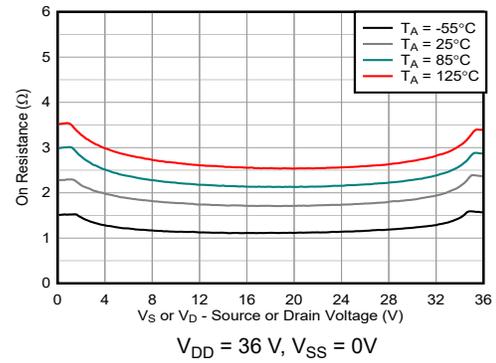
Figure 6-8. On-Resistance vs Temperature

V_{DD} = 20 V, V_{SS} = -20 V
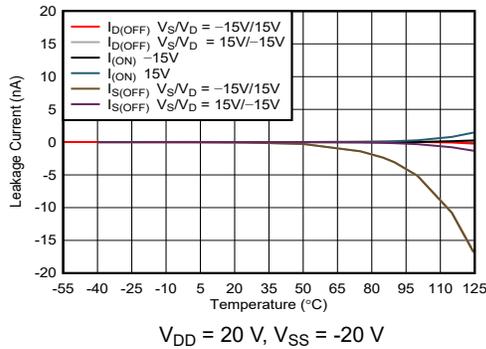
Figure 6-9. Leakage Current vs Temperature

V_{DD} = 15 V, V_{SS} = -15 V
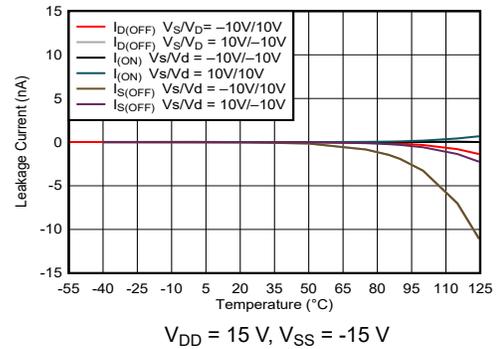
Figure 6-10. Leakage Current vs Temperature

V_{DD} = 36 V, V_{SS} = 0V
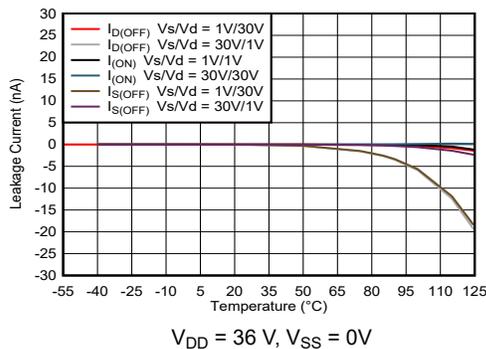
Figure 6-11. Leakage Current vs Temperature

V_{DD} = 12 V, V_{SS} = 0V
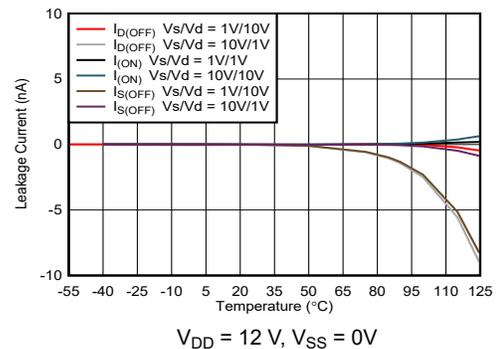
Figure 6-12. Leakage Current vs Temperature
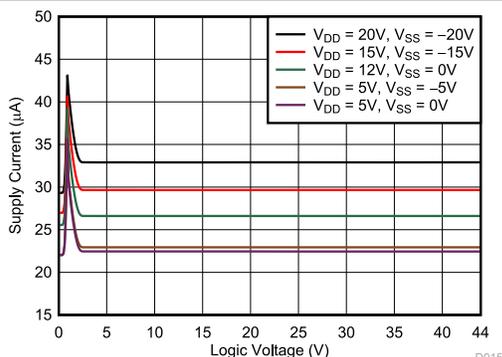
Figure 6-13. Supply Current vs. Logic Voltage
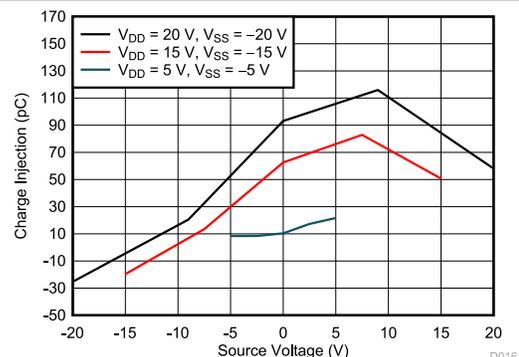
Figure 6-14. Charge Injection vs. Source Voltage – Dual Supply

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6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)
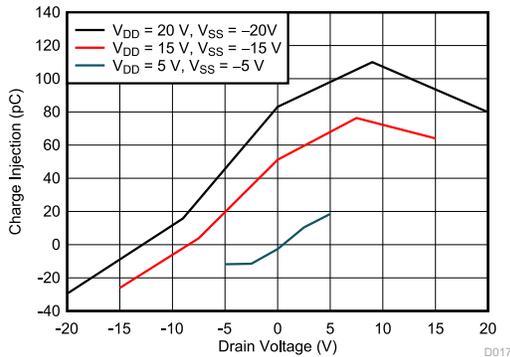
Figure 6-15. Charge Injection vs. Drain Voltage – Dual Supply
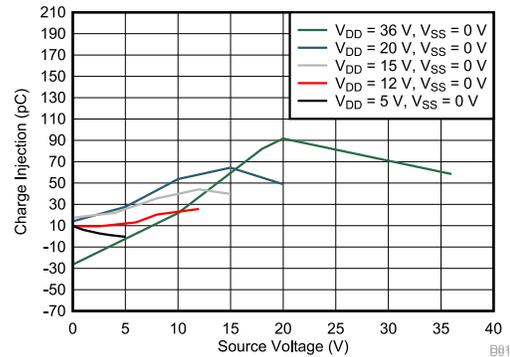
Figure 6-16. Charge Injection vs. Source Voltage – Single Supply
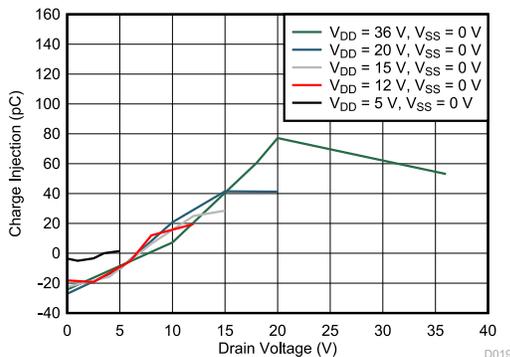
Figure 6-17. Charge Injection vs. Drain Voltage – Single Supply
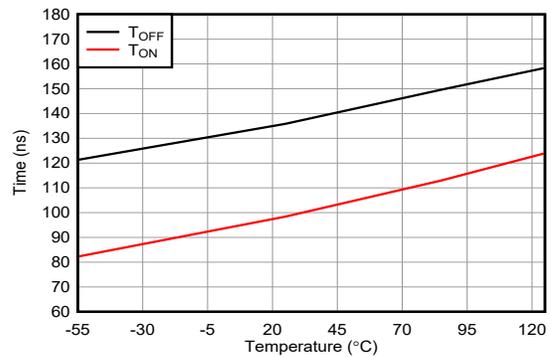
V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-18. T_{ON} and T_{OFF} vs. Temperature

V_{DD} = 36 V, V_{SS} = 0V
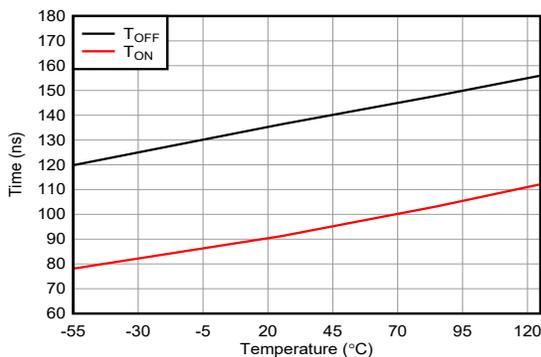
Figure 6-19. T_{ON} and T_{OFF} vs. Temperature
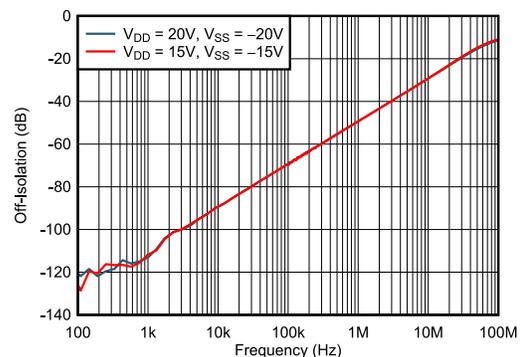
Figure 6-20. Off-Isolation vs Frequency

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)
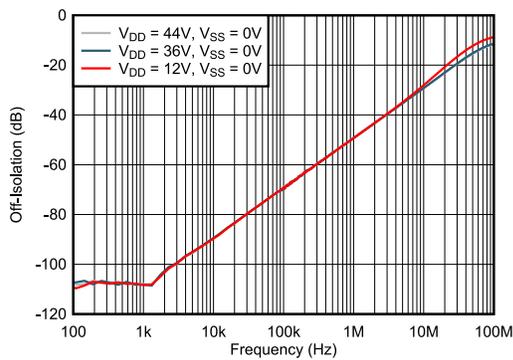
Figure 6-21. Off-Isolation vs Frequency
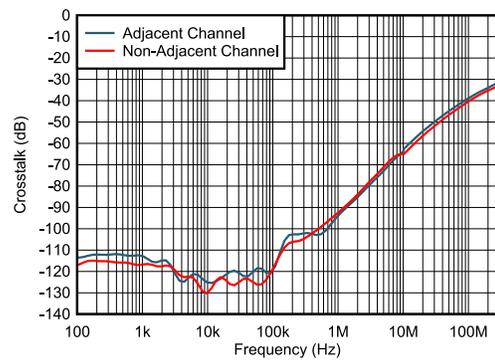
V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-22. Crosstalk vs Frequency
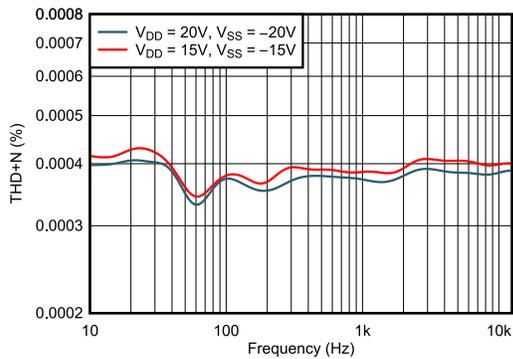
Figure 6-23. THD+N vs. Frequency (Dual Supplies)
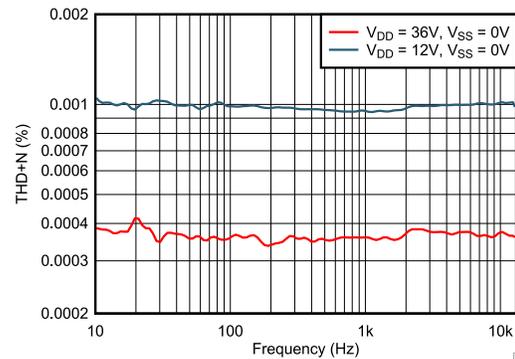
Figure 6-24. THD+N vs. Frequency (Single Supplies)
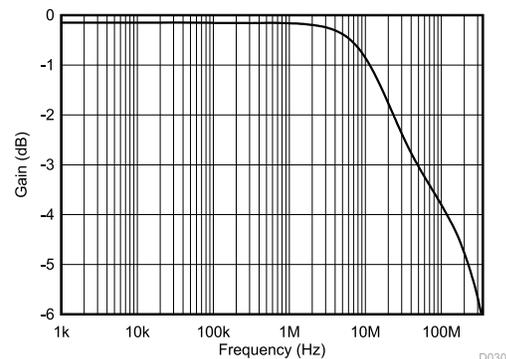
V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-25. On Response vs Frequency
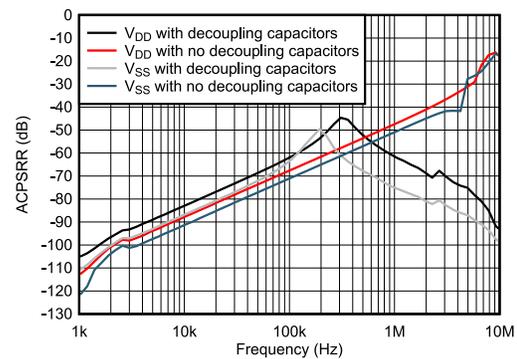
V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-26. ACPSRR vs. Frequency

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6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

V_{DD} = +15 V, V_{SS} = -15 V

Figure 6-27. Capacitance vs. Source Voltage or Drain Voltage

V_{DD} = 12 V, V_{SS} = 0V

Figure 6-28. Capacitance vs. Source Voltage or Drain Voltage
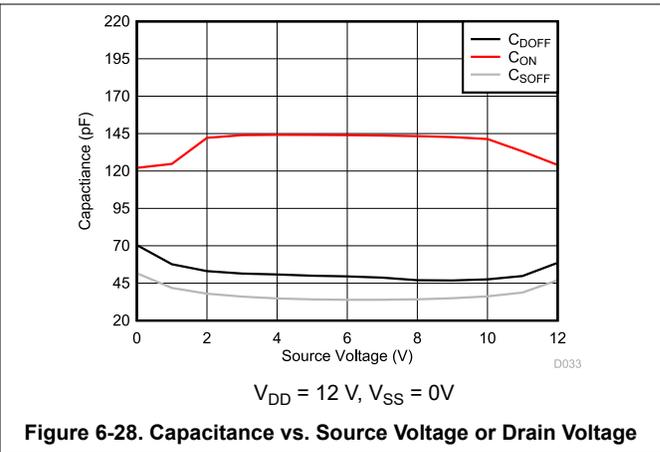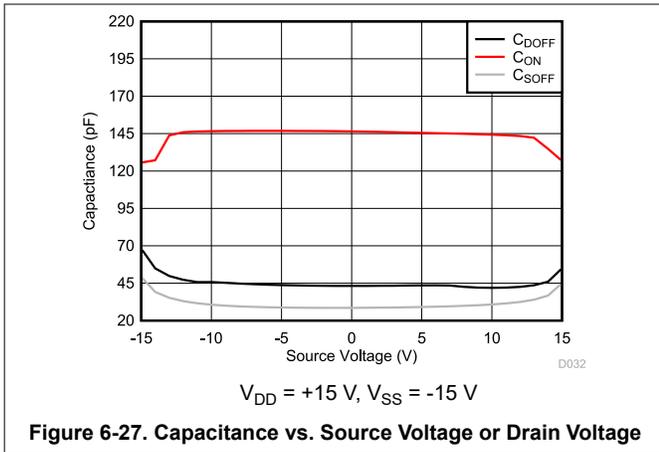
7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 7-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:
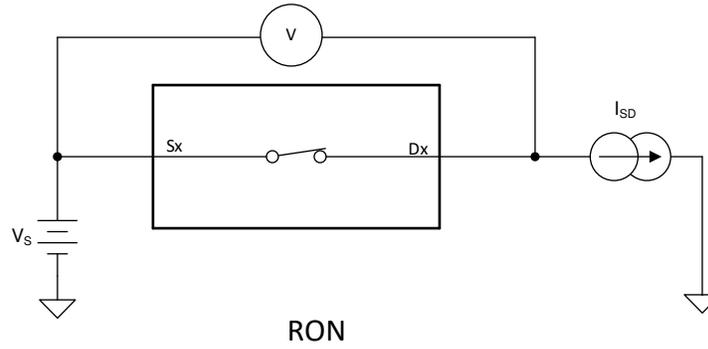
Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 7-2 shows the setup used to measure both off-leakage currents.
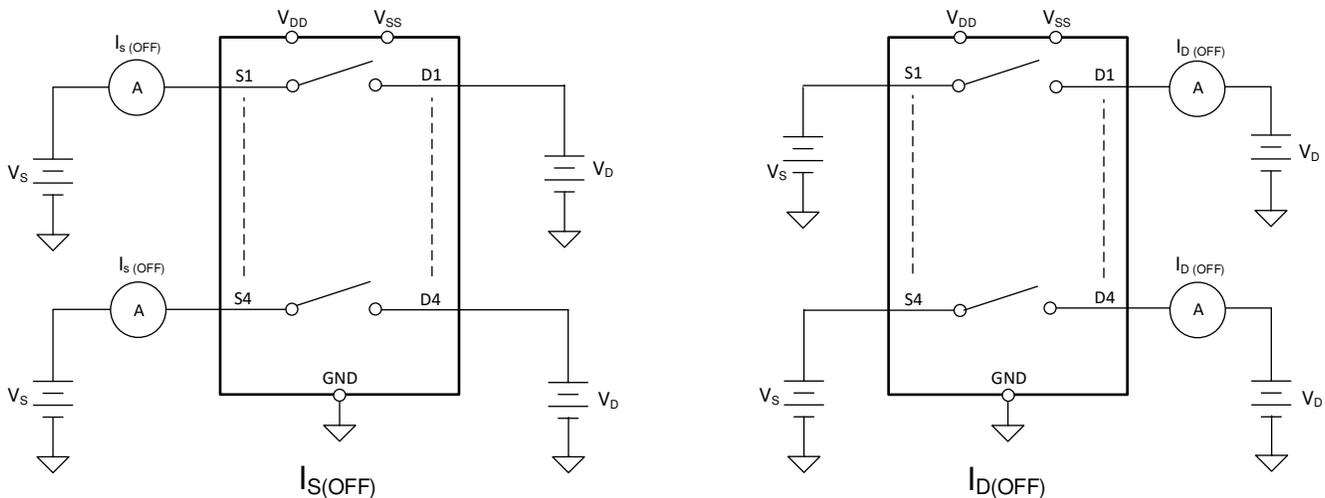
Figure 7-2. Off-Leakage Measurement Setup

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.
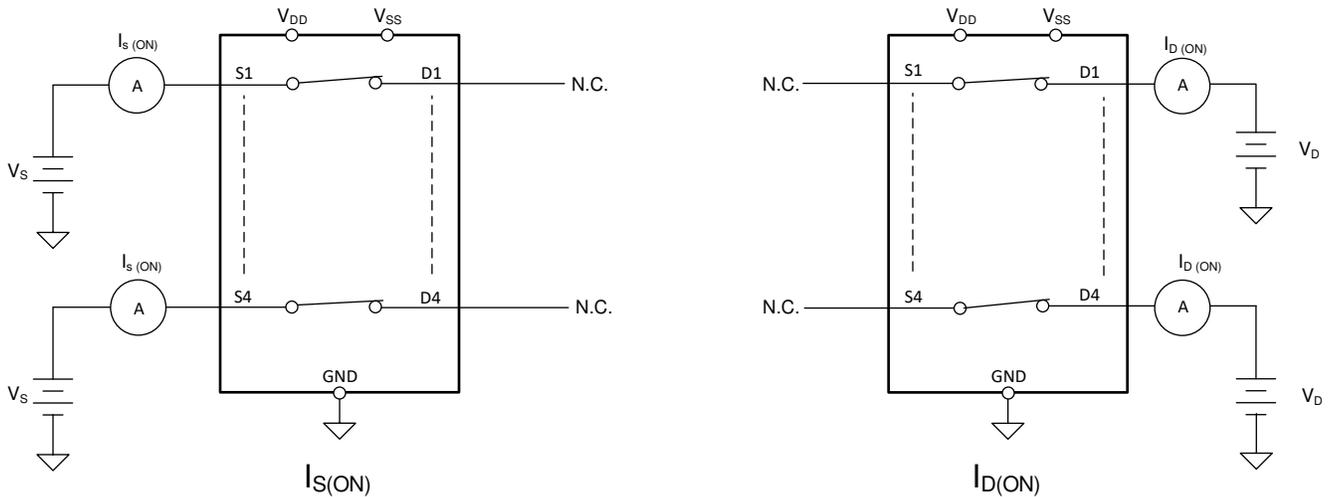
Figure 7-3. On-Leakage Measurement Setup

7.4 t_{ON} and t_{OFF} Time

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure turn-on time, denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF}.
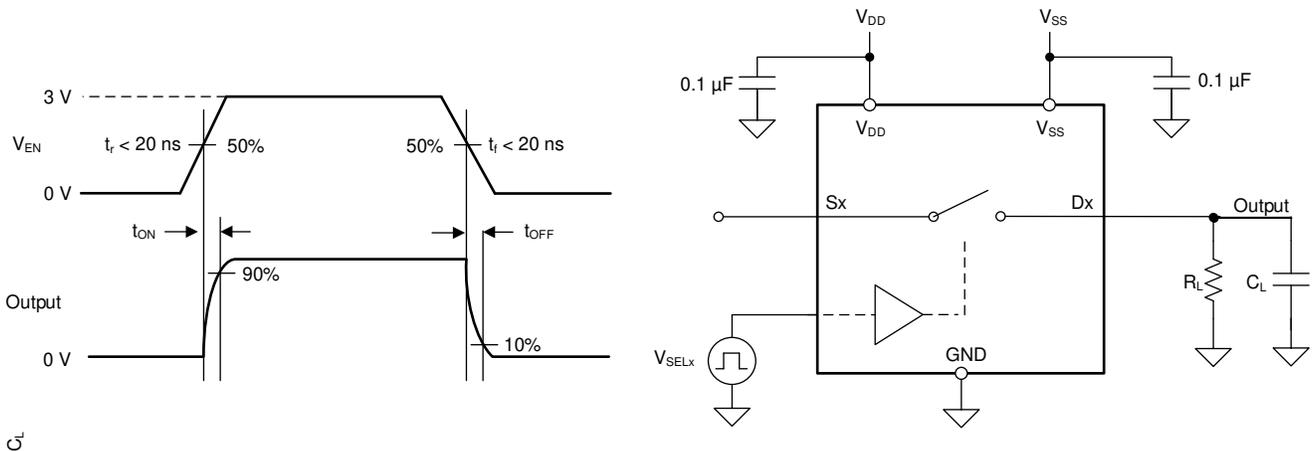
Figure 7-4. Turn-On and Turn-Off Time Measurement Setup

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

7.5 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 7-5 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.
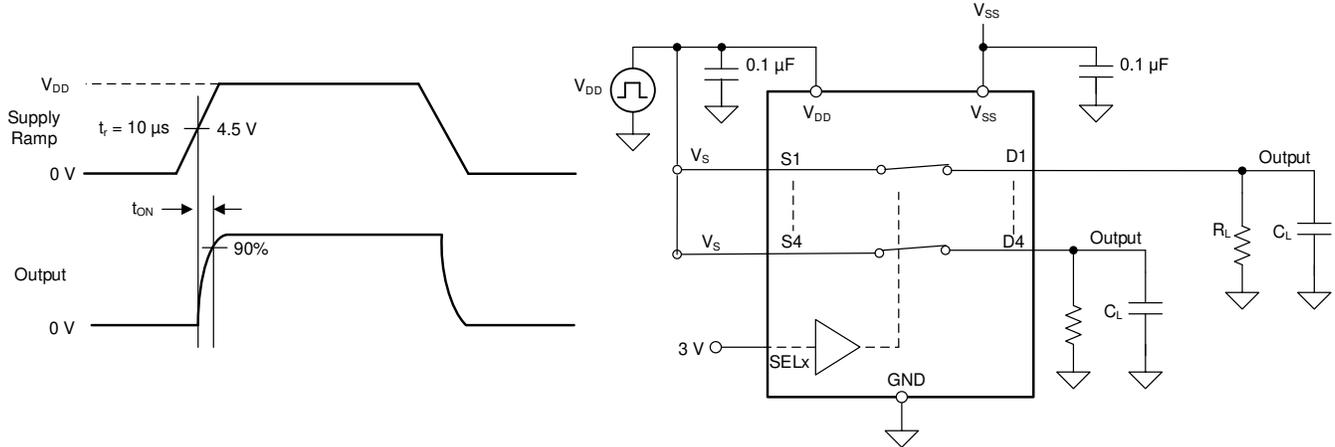

Figure 7-5. $t_{ON\ (VDD)}$ Time Measurement Setup

7.6 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 7-6 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.
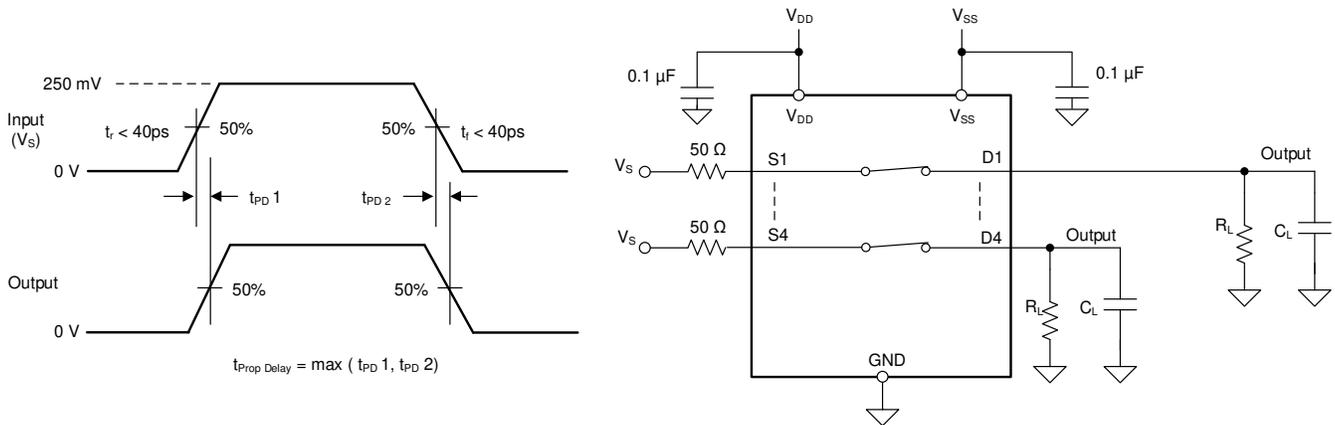

Figure 7-6. Propagation Delay Measurement Setup

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

7.7 Charge Injection

The TMUX721x devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 7-7 shows the setup used to measure charge injection from source (Sx) to drain (Dx).
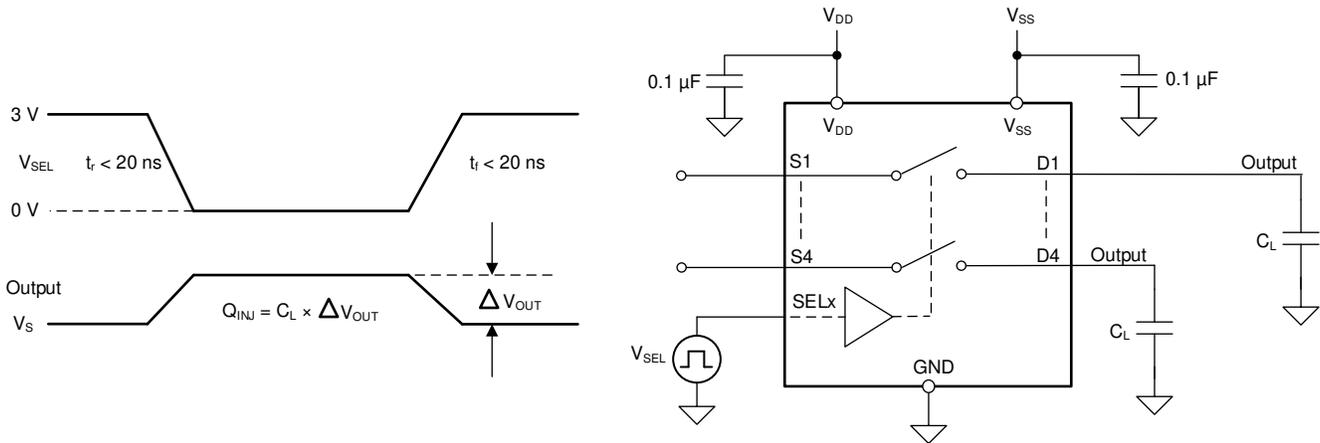

Figure 7-7. Charge-Injection Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 7-8 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.


$$Off\ Isolation = 20 \times Log\frac{V_{OUT}}{V_S}$$
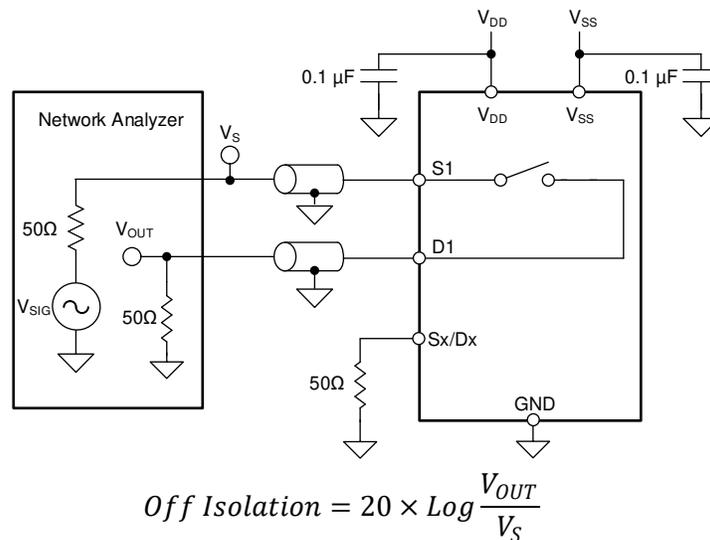
Figure 7-8. Off Isolation Measurement Setup

7.9 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 7-9 shows the setup used to measure, and the equation used to compute crosstalk.


$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$
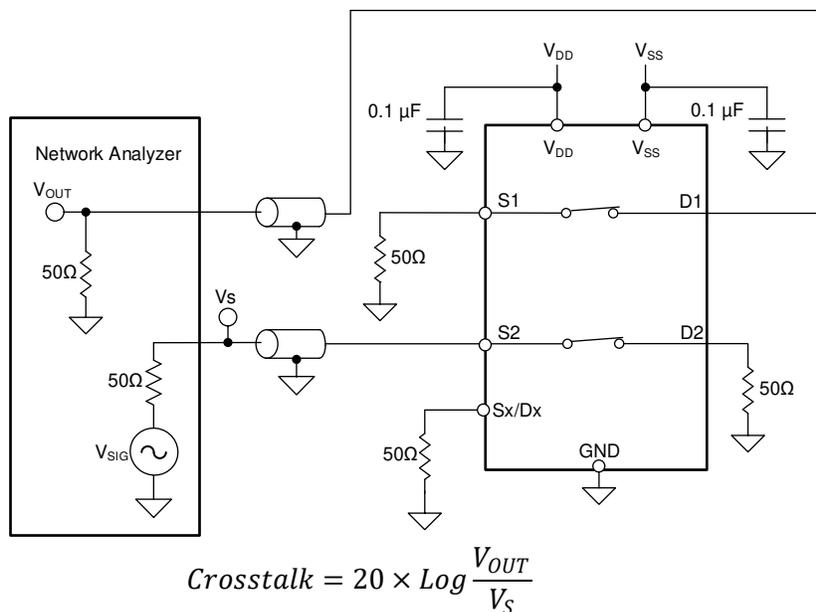
Figure 7-9. Channel-to-Channel Crosstalk Measurement Setup

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 7-10 shows the setup used to measure bandwidth.


$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$
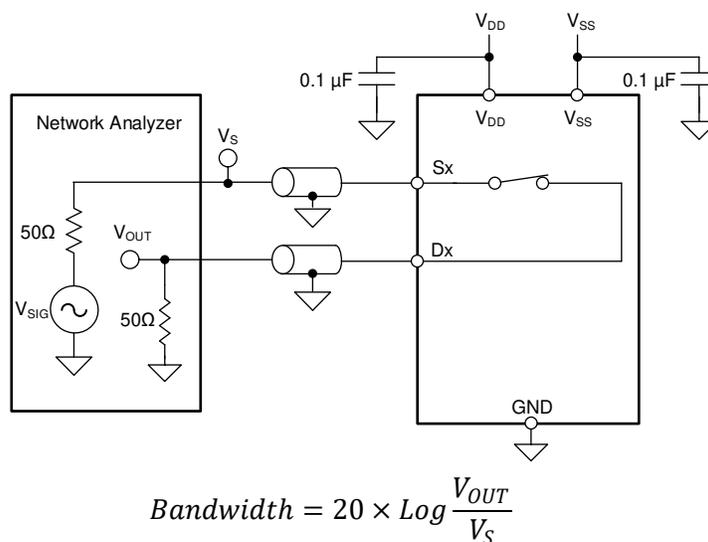
Figure 7-10. Bandwidth Measurement Setup

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

7.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.
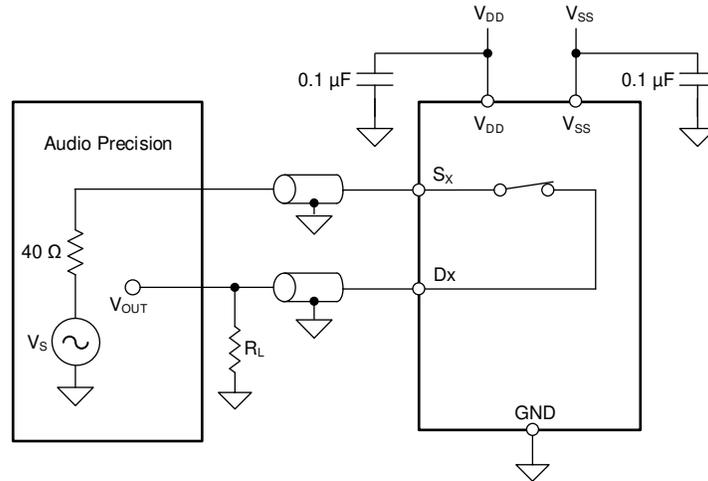

Figure 7-11. THD + N Measurement Setup

7.12 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV$_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.


$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$
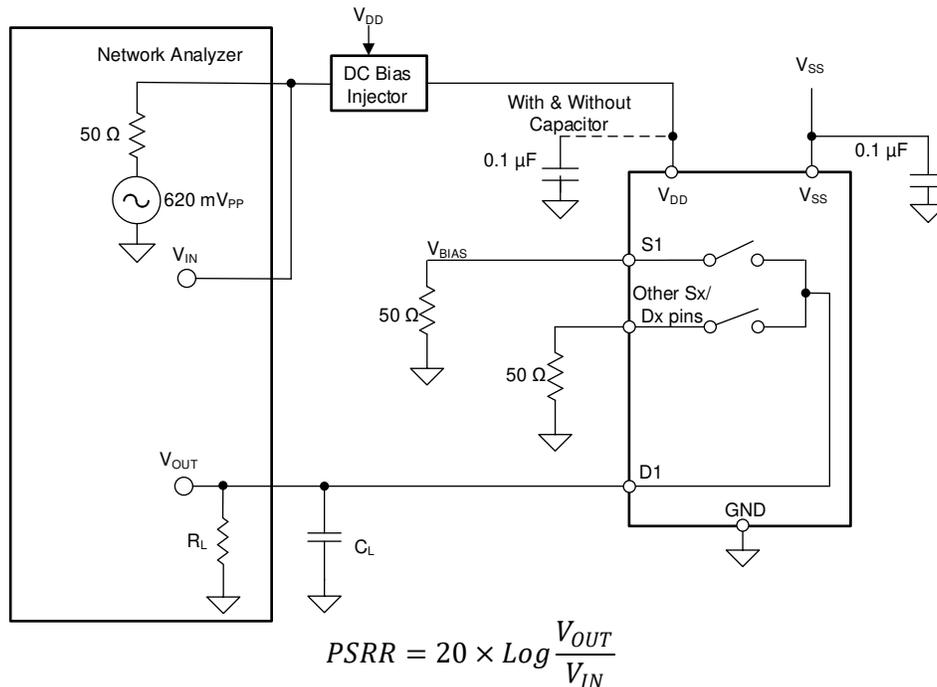
Figure 7-12. AC PSRR Measurement Setup

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

8 Detailed Description

8.1 Overview

The TMUX7212 is a 1:1 (SPST), 4-channel switch. The device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin.

8.2 Functional Block Diagram

TMUX7212M
(SELx = Logic 1)
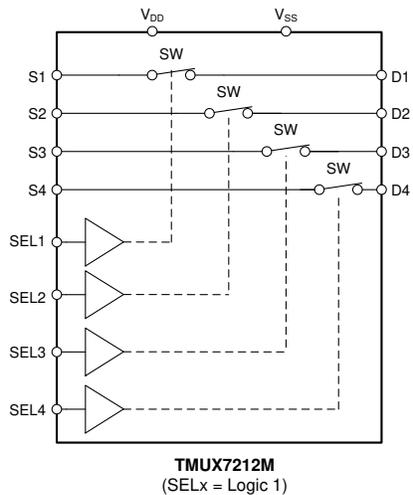
8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX721x conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX721x ranges from V_{SS} to V_{DD}.

8.3.3 1.8V Logic Compatible Inputs

The TMUX721x device has 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX721x to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of material cost. For more information on 1.8V logic implementations refer to *Simplifying Design with 1.8V logic Muxes and Switches*.

8.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX721x has internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.3.5 Fail-Safe Logic

The TMUX721x supports Fail-Safe Logic on the control input pins (SEL1, SEL2, SEL3, and SEL4) allowing for operation up to 44V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX721x to be ramped to 44V while V_{DD} and V_{SS} = 0V. The logic control inputs are protected against positive faults of up to 44V in powered-off condition, but do not offer protection against negative overvoltage conditions.

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

8.3.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX721x family of devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX721x family of switches and multiplexers to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.3.7 Ultra-Low Charge Injection

Figure 8-1 shows how the TMUX721x devices have a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.
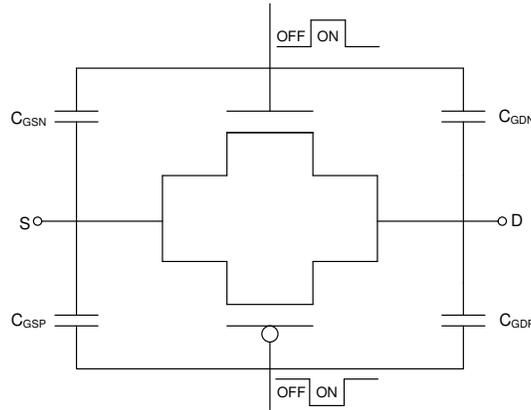

Figure 8-1. Transmission Gate Topology

The TMUX721x contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule, Cp should be 20x larger than the equivalent load capacitance on the Drain (Dx). Figure 8-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX7219M as part of the TMUX72xx family with a 100 pF load capacitance.
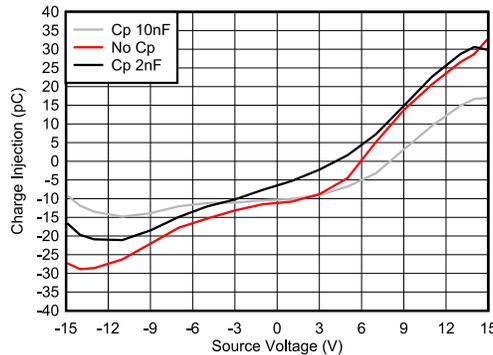

Figure 8-2. Charge Injection Compensation

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

8.4 Device Functional Modes

The TMUX721x device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins can be as high as 44V.

The TMUX721x devices can operate without any external components except for the supply decoupling capacitors. The SELx pins have internal pull-down resistors of 4MΩ. If unused, then the SELx pin must be tied to GND for the device to not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (Sx or Dx) should be connected to GND.

8.5 Truth Tables

Table 8-1 shows the truth tables for the TMUX7212.

Table 8-1. TMUX7212 Truth Table

SEL x [1]	CHANNEL x
0	Channel x OFF
1	Channel x ON

(1)   x denotes 1, 2, 3, or 4 for the corresponding channel.

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMUX721x is part of the precision switches and multiplexers family of devices. These devices operate with dual supplies (±4.5 V to ±22V), a single supply (4.5 V to 44V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V), and offer true rail-to-rail input and output. The TMUX721x offers low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features makes the TMUX721x a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

9.2 Typical Application

One example to take advantage of TMUX721x precision performance is the implementation of parametric measurement unit (PMU) in the semiconductor automatic test equipment (ATE) application.

In Automated Test Equipment (ATE) systems, the Parametric Measurement Unit (PMU) is tasked to measure device (DUT) parametric information in terms of voltage and current. When measuring voltage, current is applied at the DUT pin, and current range adjustment can be done through changing the value of the internal sense resistor. There is sometimes a need, depending on the DUT, to use even higher testing current than natively supported by the system. A 4 channel SPST switch, together with external higher current amplifier and resistor, can be used to achieve the flexibility. The PMU operating voltage is typically in mid voltage (up to 20 V). An appropriate switch like the TMUX721x with low leakage current (0.05 nA typical) works well in these applications to ensure measurement accuracy and low R_{ON} and flat $R_{ON\_FLATNESS}$ allows the current range to be controlled more precisely. Figure 9-1 shows simplified diagram of such implementations in memory and semiconductor test equipment.
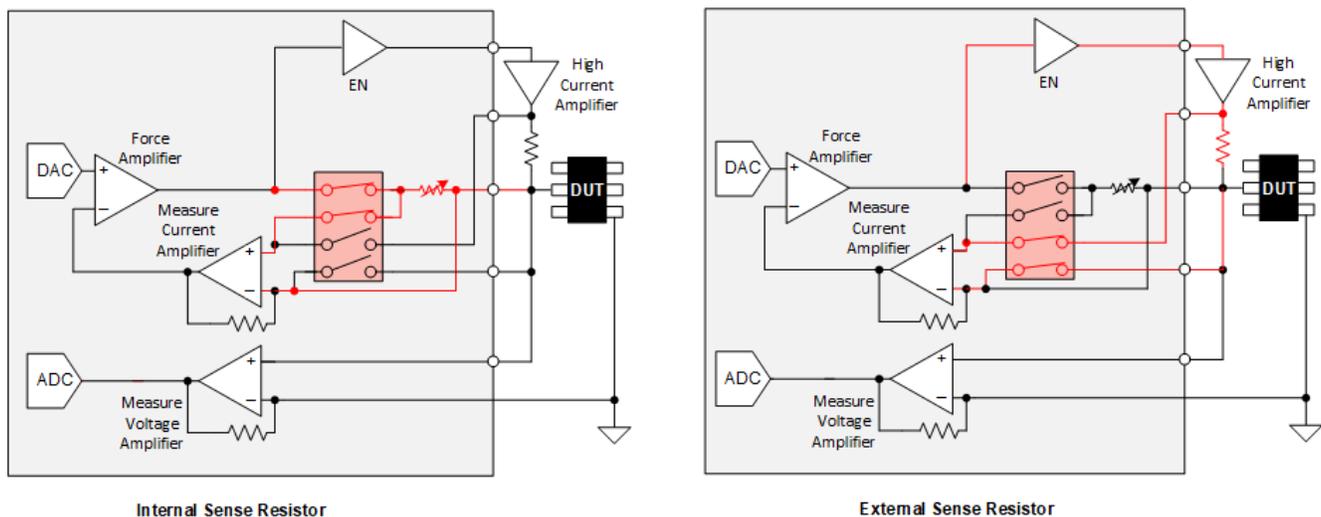

Figure 9-1. High Current Range Selection Using External Resistor

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 9-1.

Table 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	20 V
Supply (V_{SS})	−10 V
Input / Output signal range	−10 V to 20 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatible

9.2.2 Detailed Design Procedure

Figure 10-1 demonstrates how the TMUX721x can be used in semiconductor test equipment for high-precision, high-voltage, multi-channel measurement applications. The TMUX721x can support 1.8 V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX721x can be operated without any external components except for the supply decoupling capacitors. The select pins have an internal pull-down resistor to prevent floating input logic. All inputs to the switch must fall within the recommend operating conditions of the TMUX721x including signal range and continuous current. For this design with a positive supply of 20 V on V_{DD}, and negative supply of -10 V on V_{SS}, the signal range can be 20 V to -10 V. The max continuous current (I_{DC}) can be up to 330 mA as shown in the *Recommended Operating Conditions* table for wide-range current measurement.

9.2.3 Application Curve

The TMUX721x have excellent charge injection performance and ultra-low leakage current, making them ideal choices to minimize sampling error for the sample and hold application.


$T_A = 25°C$
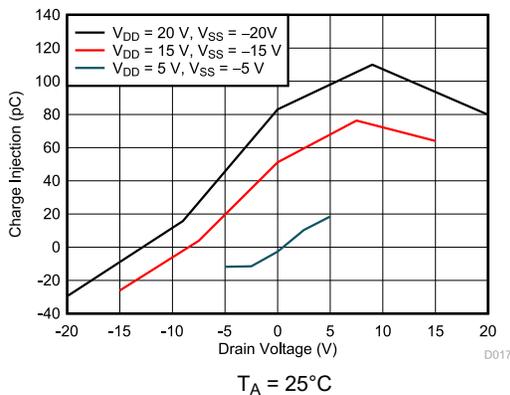
Figure 9-2. Charge Injection vs. Drain Voltage

$V_{DD} = 15 V, V_{DD} = -15 V$
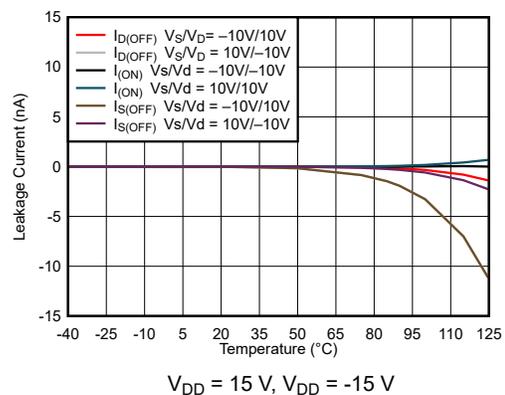
Figure 9-3. On-Leakage vs. Source or Drain Voltage

9.3 Power Supply Recommendations

The TMUX721x device operates across a wide supply range of ±4.5V to ±22V (4.5V to 44V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = −5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias

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in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

9.4 Layout

9.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.
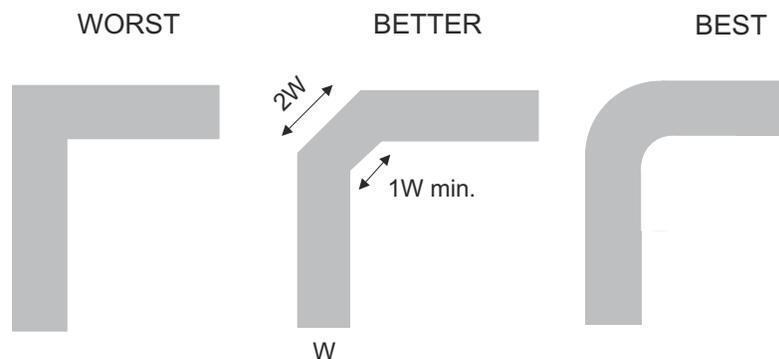
Figure 9-4. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are:

• For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD/VSS and GND. We recommend a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
• Keep the input lines as short as possible.
• Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
• Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
• Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

9.4.2 Layout Example
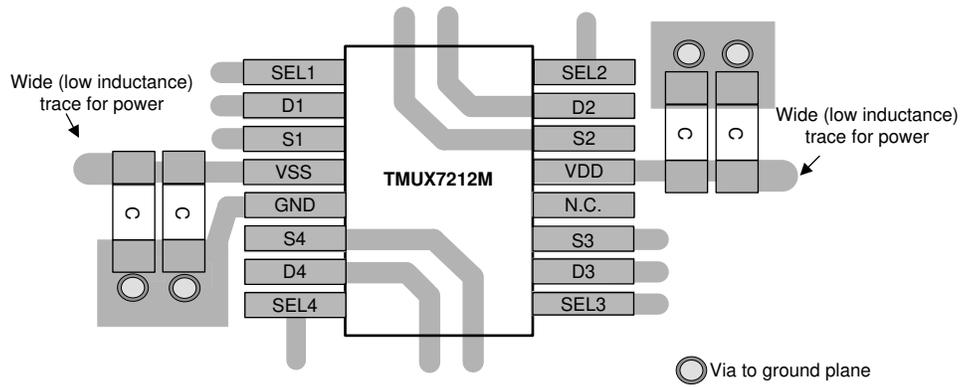
Figure 9-5. TMUX721x Layout Example

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10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability* application note
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* application note
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PW0016A

TSSOP - 1.2 mm max height
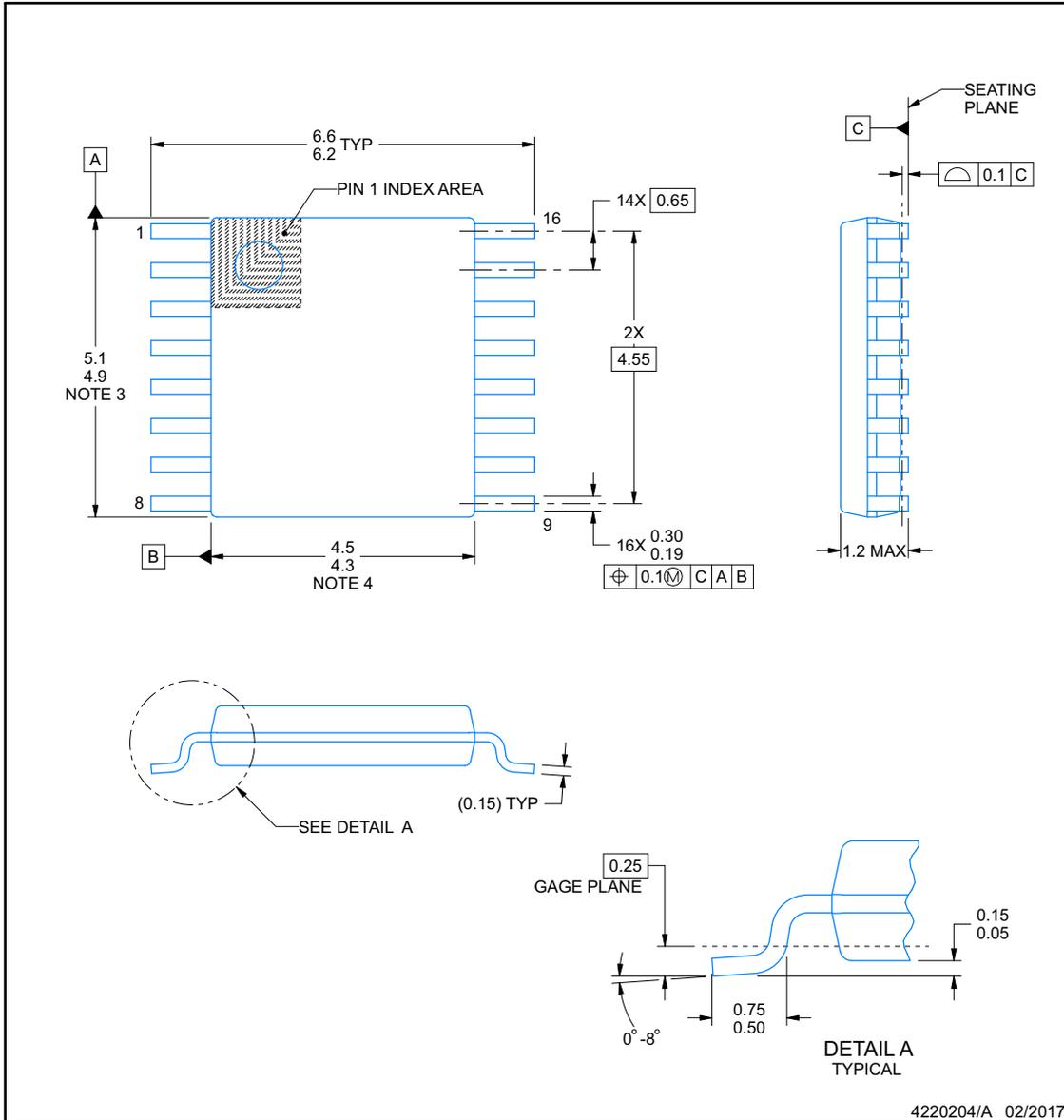
SMALL OUTLINE PACKAGE

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height
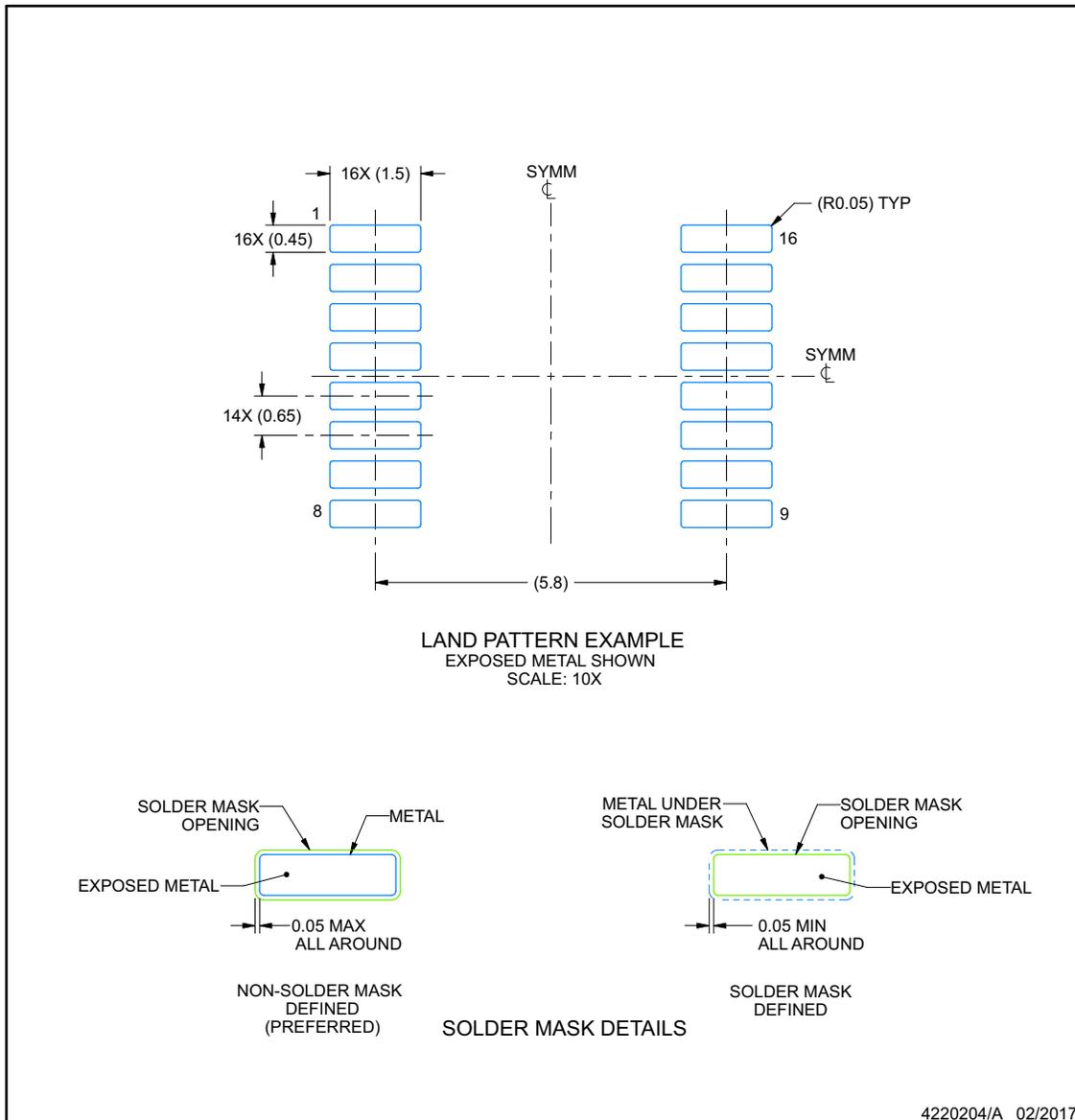
SMALL OUTLINE PACKAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

16X (1.5)

16X (0.45)

14X (0.65)

(5.8)

SYMM

SYMM

(R0.05) TYP

1

16

8

9

SOLDER MASK DETAILS

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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PACKAGE OUTLINE

RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

PIN 1 INDEX AREA

B   4.1 / 3.9   A

4.1 / 3.9

0.8 / 0.7

0.05 / 0.00

C

SEATING PLANE

0.08 C

2X 1.95

SYMM

5   8

EXPOSED
THERMAL PAD

4   9

2X 1.95

SYMM

17

□2.5±0.1

12X 0.65

1   12

PIN 1 ID

16   13

(0.2) TYP

16X 0.35 / 0.25

16X 0.5 / 0.3

0.1 Ⓜ C A B
0.05 Ⓜ

4224815/A   02/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TEXAS
INSTRUMENTS
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Submit Document Feedback

Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

EXAMPLE BOARD LAYOUT

RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK DETAILS

NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

4224815/A 02/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016E

WQFN - 0.8 mm max height
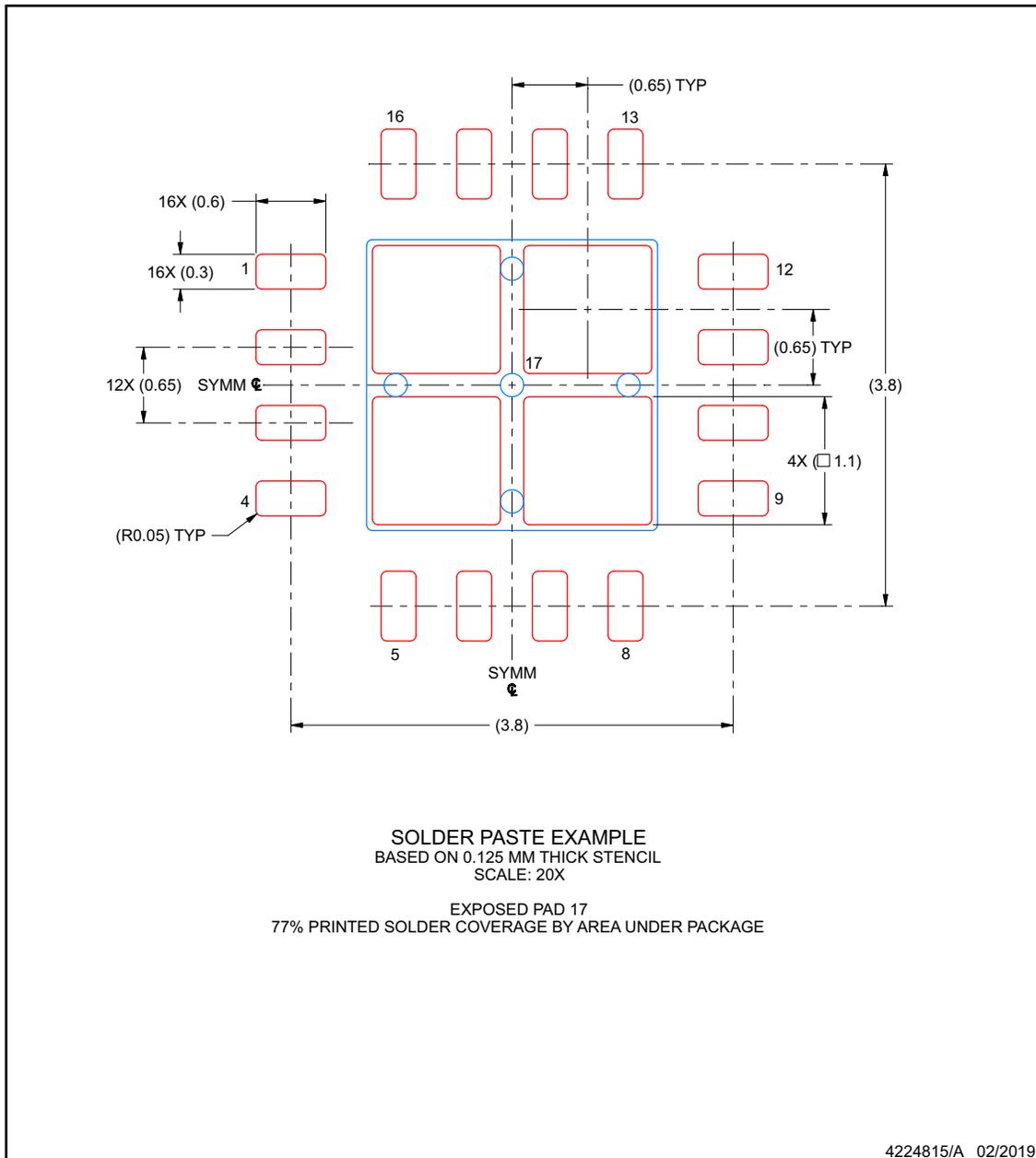
PLASTIC QUAD FLATPACK - NO LEAD

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A   02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

TEXAS INSTRUMENTS
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Product Folder Links: *TMUX7211 TMUX7212 TMUX7213*

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number (1)	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX7211PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X211
TMUX7211PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X211
TMUX7211RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X211
TMUX7211RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X211
TMUX7211RUMRG4	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X211
TMUX7211RUMRG4.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X211
TMUX7212PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X212
TMUX7212PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X212
TMUX7212RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X212
TMUX7212RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X212
TMUX7212RUMRG4	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X212
TMUX7212RUMRG4.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X212
TMUX7213PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X213
TMUX7213PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X213
TMUX7213RUMR	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X213
TMUX7213RUMR.B	Active	Production	WQFN (RUM) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X213

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
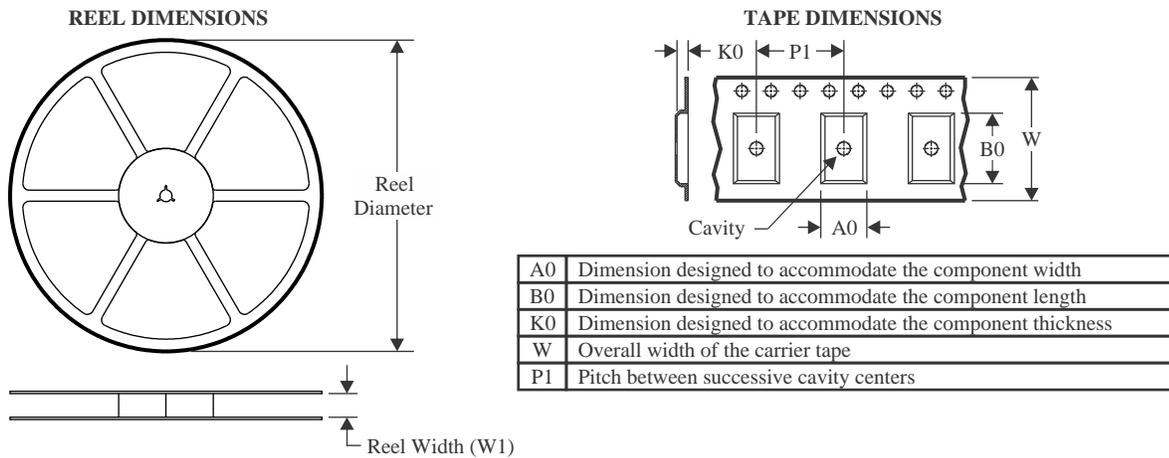
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
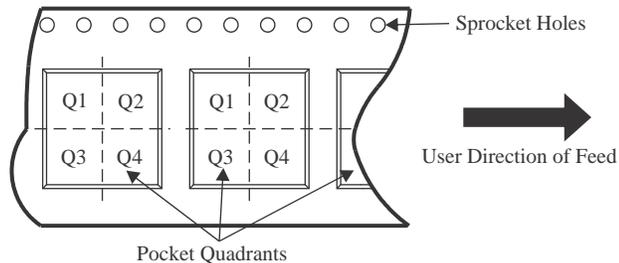
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7211PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX7211RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX7211RUMRG4	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX7212PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX7212RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX7212RUMRG4	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX7213PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX7213RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS
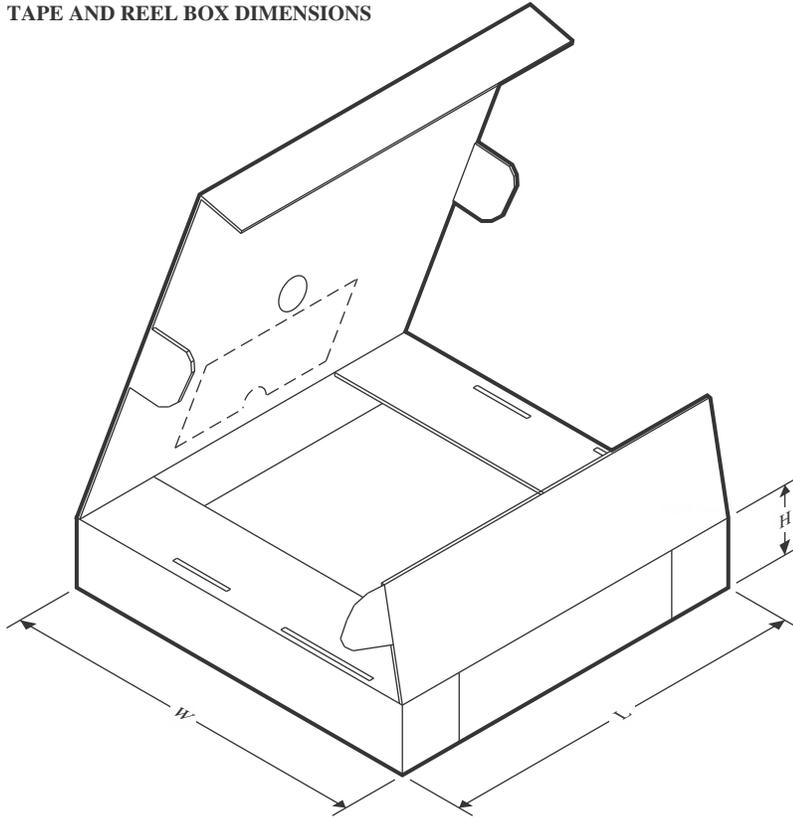
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7211PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX7211RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX7211RUMRG4	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX7212PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX7212RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX7212RUMRG4	WQFN	RUM	16	3000	367.0	367.0	35.0
TMUX7213PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX7213RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0

6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

5.1
4.9
NOTE 3

2X
4.55

1

8

9

16X 0.30
0.17

⊕ 0.1 Ⓜ C A B

B

4.5
4.3
NOTE 4

SEATING
PLANE

C

◯ 0.1 C

4X (0° -12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

GAGE PLANE

0.25

0° -8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL

4220204/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

(R0.05) TYP

1

16X (0.45)

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RUM 16

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224843/A

4224815/A   02/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

($\square$ 2.5)

SYMM

16   13

SEE SOLDER MASK
DETAIL

16X (0.6)

16X (0.3)   1

12

12X (0.65)

17   SYMM

(3.8)

(1)

4

(R0.05) TYP

9

($\varnothing$ 0.2) TYP
VIA

5   8

(1)

(3.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

0.07 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224815/A   02/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
   number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown
   on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A   02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.