TMUX7208M 44V, Latch-Up Immune, 8:1, 1-Channel Precision Multiplexers with 1.8V Logic

1 Features

- Latch-up immune
- Dual supply range: ±4.5V to ±22V
- Single supply range: 4.5V to 44V
- –55°C to +125°C operating temperature
- Low on-resistance: 4Ω
- Low charge injection: 3pC
- High current support: 300mA (maximum)
- 1.8 V logic compatible inputs
- Integrated pull-down resistor on logic pins
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional signal path
- Break-before-make switching

2 Applications

- Avionics flight control unit
- Aircraft cockpit display
- Standalone avionics precision flight control
- Interconnect and distribution box
- Aerospace and defense

3 Description

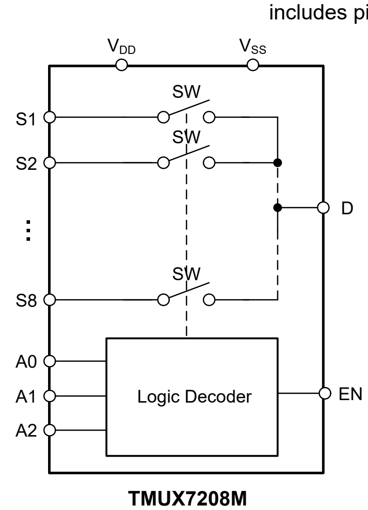
The TMUX7208M is a precision 8:1, single channel multiplexer featuring low on resistance and charge injection. The devices work with a single supply (4.5V to 44V), dual supplies (±4.5V to ±22V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5V). The TMUX7208M support bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from V_{SS} to V_{DD}.

The TMUX7208M is part of the precision switches and multiplexers family of devices and have very low on and off leakage currents allowing them to be used in high precision measurement applications. The TMUX72xx family provides latch-up immunity, preventing undesirable high current events between parasitic structures within the device typically caused by overvoltage events. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments. Additionally, the TMUX7208M is rated for extended temperature use down to –55°C, making it ideal for harsh industrial and aerospace applications.

Package Information

PART NUMBER	PACKAGE(2)	PACKAGE SIZE(3)
TMUX7208M	PW (TSSOP, 16)	5mm × 6.4mm

(1) See Device Comparison
(2) For more information, see Section 12
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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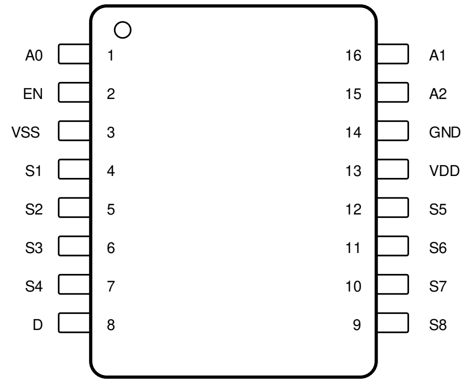
4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX7208M	Low-Leakage-Current, Precision, 8:1, 1-Ch. multiplexer

5 Pin Configuration and Functions



Not to scale

Figure 5-1. TMUX7208M: PW Package, 16-Pin TSSOP (Top View)

Table 5-1. TMUX7208M Pin Functions

PIN			TYPE(1)	DESCRIPTION(2)
NAME	PW	RUM		
A0	1	15	I	Logic control input, has internal 4MΩ pull-down resistor. Controls the switch configuration as shown in Section 8.5.
A1	16	14	I	Logic control input, has internal 4MΩ pull-down resistor. Controls the switch configuration as shown in Section 8.5.
A2	15	13	I	Logic control input, has internal 4MΩ pull-down resistor. Controls the switch configuration as shown in Section 8.5.
D	8	6	I/O	Drain pin. Can be an input or output.
EN	2	16	I	Active high logic enable, has internal 4MΩ pull-down resistor. When this pin is low, all switches are turned off. When this pin is high, the Ax logic input determines which switch is turned on.
GND	14	12	P	Ground (0V) reference.
S1	4	2	I/O	Source pin 1. Can be an input or output.
S2	5	3	I/O	Source pin 2. Can be an input or output.
S3	6	4	I/O	Source pin 3. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
S5	12	10	I/O	Source pin 5. Can be an input or output.
S6	11	9	I/O	Source pin 6. Can be an input or output.
S7	10	8	I/O	Source pin 7. Can be an input or output.
S8	9	7	I/O	Source pin 8. Can be an input or output.
VDD	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
VSS	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{SS} and GND.
Thermal Pad			—	The thermal pad is not connected internally. No requirement to solder this pad, if connected it is recommended that the pad be left floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to Section 8.4 for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		48	V
V_{DD}		–0.5	48	V
V_{SS}		–48	0.5	V
$V_{ADDRESS}$ or V_{EN}	Logic control input pin voltage (EN, A0, A1, A2)	–0.5	48	V
$I_{ADDRESS}$ or I_{EN}	Logic control input pin current (EN, A0, A1, A2)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (TSSOP package)(5)		700	mW

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearly above T_A = 70°C by 24.4mW/°C.
For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 10.8mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
TMUX7208M				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX7208M PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential	4.5		44	V
V_{DD}	Positive power supply voltage	4.5		44	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
$V_{ADDRESS}$ or V_{EN}	Address or enable pin voltage	0		36	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	mA
T_A	Ambient temperature	–55		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5V ≤ (V_{DD} – V_{SS}) ≤ 36V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC})					
PACKAGE	TEST CONDITIONS	T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PW (TSSOP)	±15V Dual Supply	300	190	110	mA
	+36V Single Supply[1]	280	170	100	mA
	+12 V Single Supply	220	150	90	mA
	±5V Dual Supply	210	140	90	mA
	+5V Single Supply	170	110	70	mA

(1) Specified for nominal supply voltage only.

6.6 ±15V Dual Supply: Electrical Characteristics

V_{DD} = +15V ± 10%, V_{SS} = –15V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10V to +10V I_D = –10mA Refer to On-Resistance	25°C		4	5.9	Ω
			–40°C to +85°C			7.4	Ω
			–55°C to +125°C			8.7	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10V to +10V I_D = –10mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–55°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10V to +10V I_S = –10mA Refer to On-Resistance	25°C		0.4	1.5	Ω
			–40°C to +85°C			1.7	Ω
			–55°C to +125°C			1.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.02		Ω/°C
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V Refer to Off-Leakage Current	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–1		1	nA
			–55°C to +125°C	–5		5	nA
$I_{D(OFF)}$	Drain off leakage current[(1)]	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V Refer to Off-Leakage Current	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–6		6	nA
			–55°C to +125°C	–42		42	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[(2)]	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is on V_S = V_D = ±10V Refer to On-Leakage Current	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–5		5	nA
			–55°C to +125°C	–40		40	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.4	1.2	µA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 0V, 5V, or V_{DD}	25°C		35	57	µA
			–40°C to +85°C			60	µA
			–55°C to +125°C			75	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 0V, 5V, or V_{DD}	25°C		3	14	µA
			–40°C to +85°C			15	µA
			–55°C to +125°C			22	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.7 ±15V Dual Supply: Switching Characteristics

V_{DD} = +15V ± 10%, V_{SS} = –15V ± 10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10V R_L = 300Ω, C_L = 35pF Refer to Transition Time	25°C		140	195	ns
			–40°C to +85°C			220	ns
			–55°C to +125°C			240	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		140	195	ns
			–40°C to +85°C			220	ns
			–55°C to +125°C			240	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		200	268	ns
			–40°C to +85°C			285	ns
			–55°C to +125°C			298	ns
t_{BBM}	Break-before-make time delay	V_S = 10V, R_L = 300Ω, C_L = 35pF Refer to Break-Before-Make	25°C		60		ns
			–40°C to +85°C	1			ns
			–55°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17		ms
			–55°C to +125°C		0.17		ms
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF Refer to Propagation Delay	25°C		1.8		ns
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF Refer to Charge Injection	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 0V Refer to Bandwidth	25°C		30		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–74		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15V, V_{BIAS} = 0V R_L = 10kΩ , C_L = 5pF, f = 20 Hz to 20kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0V, f = 1MHz	25°C		15		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0V, f = 1MHz	25°C		135		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0V, f = 1MHz	25°C		185		pF

6.8 ±20V Dual Supply: Electrical Characteristics

V_{DD} = +20V ± 10%, V_{SS} = –20V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +20V, V_{SS} = –20V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15V to +15V I_D = –10mA Refer to On-Resistance	25°C		3.5	5.4	Ω
			–40°C to +85°C			6.7	Ω
			–55°C to +125°C			7.9	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15V to +15V I_D = –10mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–55°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –15V to +15V I_S = –10mA Refer to On-Resistance	25°C		0.4	1.2	Ω
			–40°C to +85°C			1.5	Ω
			–55°C to +125°C			1.9	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.016		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 22V, V_{SS} = –22V Switch state is off V_S = +15V / –15V V_D = –15V / + 15V Refer to Off-Leakage Current	25°C	–1	0.04	1	nA
			–40°C to +85°C	–2		2	nA
			–55°C to +125°C	–10		10	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 22V, V_{SS} = –22V Switch state is off V_S = +15V / –15V V_D = –15V / + 15V Refer to Off-Leakage Current	25°C	–1	0.04	1	nA
			–40°C to +85°C	–11		11	nA
			–55°C to +125°C	–70		70	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 22V, V_{SS} = –22V Switch state is on V_S = V_D = ±15V Refer to On-Leakage Current	25°C	–1	0.04	1	nA
			–40°C to +85°C	–10		10	nA
			–55°C to +125°C	–62		62	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.4	1.2	µA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22V, V_{SS} = –22V Logic inputs = 0V, 5V, or V_{DD}	25°C		40	60	µA
			–40°C to +85°C			70	µA
			–55°C to +125°C			84	µA
I_{SS}	V_{SS} supply current	V_{DD} = 22V, V_{SS} = –22V Logic inputs = 0V, 5V, or V_{DD}	25°C		2	9	µA
			–40°C to +85°C			18	µA
			–55°C to +125°C			24	µA

(1) When V_S is positive, V_D is negative, and vice versa.
(2) When V_S is at a voltage potential, V_D is floating, and vice versa.

6.9 ±20V Dual Supply: Switching Characteristics

V_{DD} = +20V ± 10%, V_{SS} = –20V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +20V, V_{SS} = –20V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10V R_L = 300Ω, C_L = 35pF Refer to Transition Time	25°C		115	208	ns
			–40°C to +85°C			230	ns
			–55°C to +125°C			248	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		115	205	ns
			–40°C to +85°C			228	ns
			–55°C to +125°C			248	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		148	270	ns
			–40°C to +85°C			285	ns
			–55°C to +125°C			290	ns
t_{BBM}	Break-before-make time delay	V_S = 10V, R_L = 300Ω, C_L = 35pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–55°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.15		ms
			–40°C to +85°C		0.16		ms
			–55°C to +125°C		0.16		ms
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF Refer to Propagation Delay	25°C		1.8		ns
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF Refer to Charge Injection	25°C		2		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 100kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX7208)	R_L = 50Ω , C_L = 5pF V_S = 0V Refer to Bandwidth	25°C		30		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz	25°C		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–72		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 20V, V_{BIAS} = 0V R_L = 10kΩ , C_L = 5pF, f = 20 Hz to 20kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0V, f = 1MHz	25°C		14		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX7208)	V_S = 0V, f = 1MHz	25°C		130		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX7208)	V_S = 0V, f = 1MHz	25°C		180		pF

6.10 44V Single Supply: Electrical Characteristics

V_{DD} = +44V, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +44V, V_{SS} = 0V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to 40V I_D = –10mA Refer to On-Resistance	25°C		3.5	5.5	Ω
			–40°C to +85°C			7	Ω
			–55°C to +125°C			8.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0V to 40V I_D = –10mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–55°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to 40V I_D = –10mA Refer to On-Resistance	25°C		0.4	1.85	Ω
			–40°C to +85°C			2.3	Ω
			–55°C to +125°C			2.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 22V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = 44V, V_{SS} = 0V Switch state is off V_S = 40V / 1 V V_D = 1 V / 40V Refer to Off-Leakage Current	25°C	–1	0.04	1	nA
			–40°C to +85°C	–2.5		2.5	nA
			–55°C to +125°C	–14		14	nA
$I_{D(OFF)}$	Drain off leakage current[(1)]	V_{DD} = 44V, V_{SS} = 0V Switch state is off V_S = 40V / 1 V V_D = 1 V / 40V Refer to Off-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–16		16	nA
			–55°C to +125°C	–110		110	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[(2)]	V_{DD} = 44V, V_{SS} = 0V Switch state is on V_S = V_D = 40V or 1 V Refer to On-Leakage Current	25°C	–1	0.05	1	nA
			–40°C to +85°C	–15		15	nA
			–55°C to +125°C	–98		98	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.4	1.2	µA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 44V, V_{SS} = 0V Logic inputs = 0V, 5V, or V_{DD}	25°C		55	85	µA
			–40°C to +85°C			95	µA
			–55°C to +125°C			110	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.11 44V Single Supply: Switching Characteristics

V_{DD} = +44V, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +44V, V_{SS} = 0V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 18 V R_L = 300Ω, C_L = 35pF Refer to Transition Time	25°C		110	205	ns
			–40°C to +85°C			226	ns
			–55°C to +125°C			245	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 18 V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		120	205	ns
			–40°C to +85°C			225	ns
			–55°C to +125°C			245	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 18 V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		280	300	ns
			–40°C to +85°C			310	ns
			–55°C to +125°C			320	ns
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300Ω, C_L = 35pF Refer to Break-Before-Make	25°C		40		ns
			–40°C to +85°C	1			ns
			–55°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.12		ms
			–40°C to +85°C		0.13		ms
			–55°C to +125°C		0.13		ms
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF Refer to Propagation Delay	25°C		2.5		ns
Q_{INJ}	Charge injection	V_S = 22V, C_L = 100pF Refer to Charge Injection	25°C		–5		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 100kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 1MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 100kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–85		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 6 V Refer to Bandwidth	25°C		30		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 1MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–70		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 22V, V_{BIAS} = 22V R_L = 10kΩ , C_L = 5pF, f = 20 Hz to 20kHz Refer to THD + Noise	25°C		0.0002		%
$C_{S(OFF)}$	Source off capacitance	V_S = 22V, f = 1MHz	25°C		15		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 22V, f = 1MHz	25°C		135		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 22V, f = 1MHz	25°C		185		pF

6.12 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to 10V I_D = –10mA Refer to On-Resistance	25°C		7	11.8	Ω
			–40°C to +85°C			14.2	Ω
			–55°C to +125°C			16.5	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0V to 10V I_D = –10mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–55°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0V to 10V I_S = –10mA Refer to On-Resistance	25°C		1.7	3.4	Ω
			–40°C to +85°C			3.8	Ω
			–55°C to +125°C			4.6	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10mA Refer to On-Resistance	–55°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2V, V_{SS} = 0V Switch state is off V_S = 10V / 1 V V_D = 1 V / 10V Refer to Off-Leakage Current	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–1		1	nA
			–55°C to +125°C	–8		8	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2V, V_{SS} = 0V Switch state is off V_S = 10V / 1 V V_D = 1 V / 10V Refer to Off-Leakage Current	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–5		5	nA
			–55°C to +125°C	–30		30	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2V, V_{SS} = 0V Switch state is on V_S = V_D = 10V or 1 V Refer to On-Leakage Current	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–4		4	nA
			–55°C to +125°C	–28		28	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–55°C to +125°C	1.3		44	V
V_{IL}	Logic voltage low		–55°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–55°C to +125°C		0.4	1.2	µA
I_{IL}	Input leakage current		–55°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–55°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2V, V_{SS} = 0V Logic inputs = 0V, 5V, or V_{DD}	25°C		30	48	µA
			–40°C to +85°C			54	µA
			–55°C to +125°C			65	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.13 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300Ω, C_L = 35pF Refer to Transition Time	25°C		180	210	ns
			–40°C to +85°C			245	ns
			–55°C to +125°C			276	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 8 V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		115	202	ns
			–40°C to +85°C			235	ns
			–55°C to +125°C			265	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 8 V R_L = 300Ω, C_L = 35pF Refer to Turn-on and Turn-off Time	25°C		290	318	ns
			–40°C to +85°C			350	ns
			–55°C to +125°C			370	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300Ω, C_L = 35pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–55°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17	1	ms
			–55°C to +125°C		0.17	1	ms
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF Refer to Propagation Delay	25°C		2.5		ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100pF Refer to Charge Injection	25°C		2		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 100kHz	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 1MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 100kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 6 V Refer to Bandwidth	25°C		28		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 6 V, f = 1MHz	25°C		–0.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz Refer to ACPSRR	25°C		–74		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10kΩ , C_L = 5pF, f = 20 Hz to 20kHz Refer to THD + Noise	25°C		0.0007		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1MHz	25°C		17		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1MHz	25°C		155		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1MHz	25°C		200		pF

6.14 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

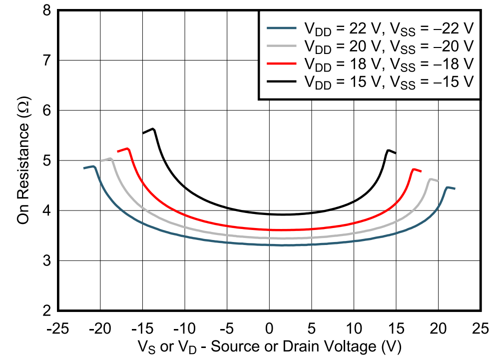


Figure 6-1. On-Resistance vs Source or Drain Voltage – Dual Supply

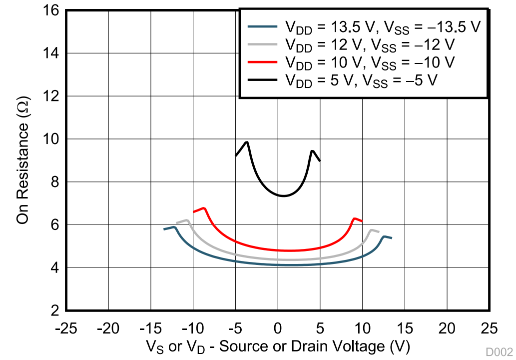


Figure 6-2. On-Resistance vs Source or Drain Voltage – Dual Supply

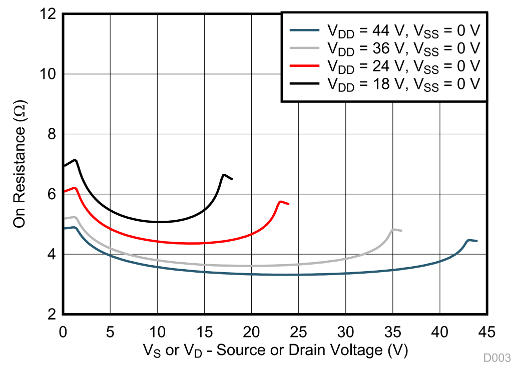


Figure 6-3. On-Resistance vs Source or Drain Voltage – Single Supply

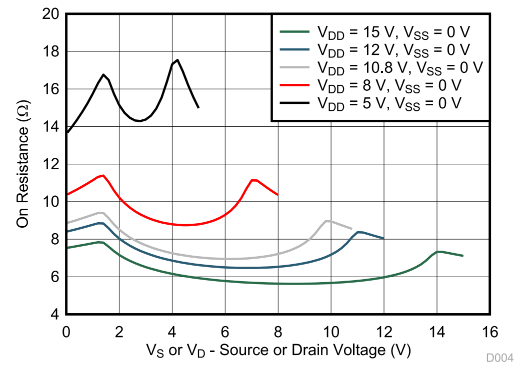
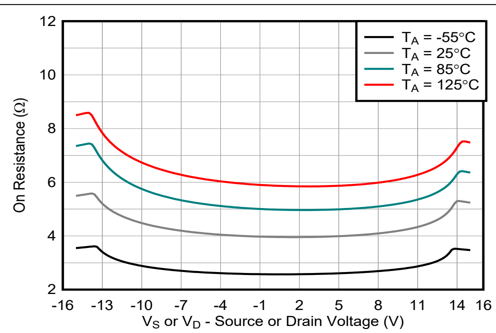
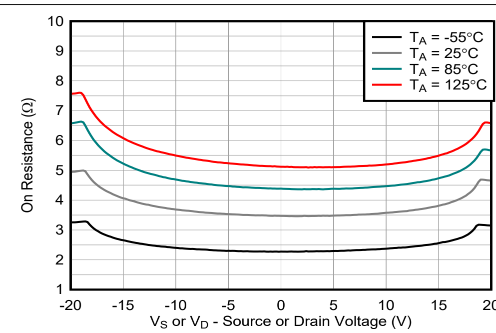


Figure 6-4. On-Resistance vs Source or Drain Voltage – Single Supply



V_{DD} = 15V, V_{SS} = -15V

Figure 6-5. On-Resistance vs Temperature

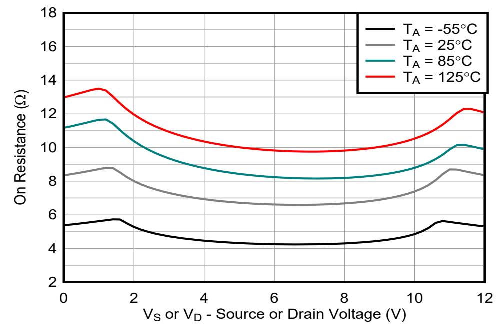


V_{DD} = 20V, V_{SS} = -20V

Figure 6-6. On-Resistance vs Temperature

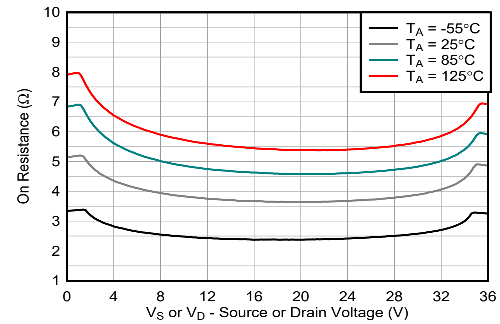
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



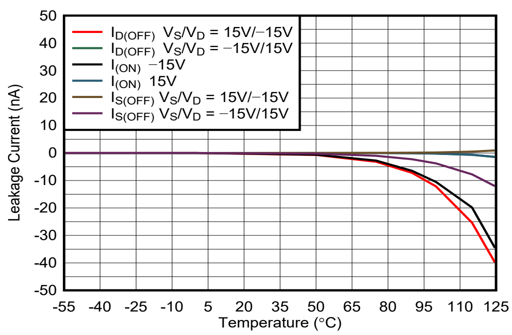
V_{DD} = 12 V, V_{SS} = 0V

Figure 6-7. On-Resistance vs Temperature



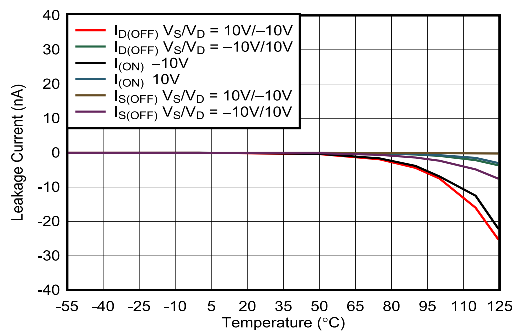
V_{DD} = 36V, V_{SS} = 0V

Figure 6-8. On-Resistance vs Temperature



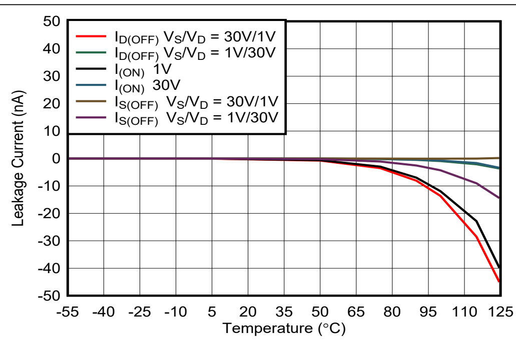
V_{DD} = 20V, V_{SS} = -20V

Figure 6-9. Leakage Current vs Temperature



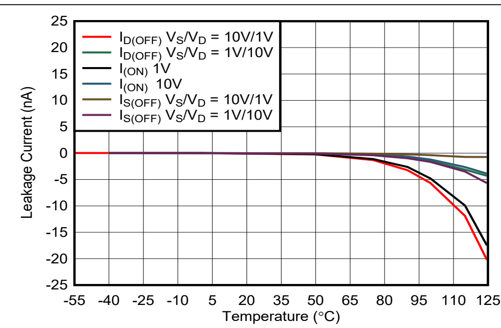
V_{DD} = 15V, V_{SS} = -15V

Figure 6-10. Leakage Current vs Temperature



V_{DD} = 36V, V_{SS} = 0V

Figure 6-11. Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0V

Figure 6-12. Leakage Current vs Temperature

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

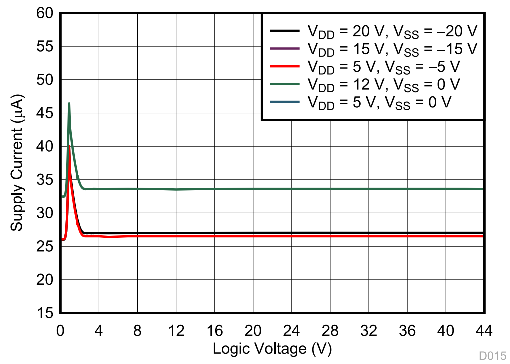


Figure 6-13. Supply Current vs Logic Voltage

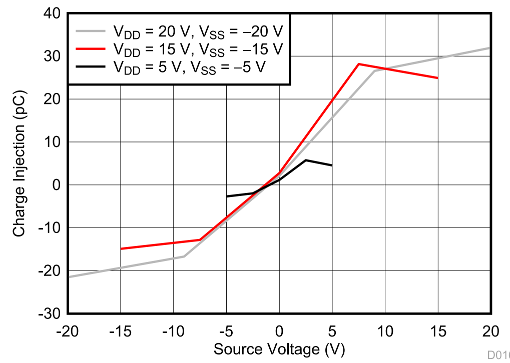


Figure 6-14. Charge Injection vs Source Voltage – Dual Supply

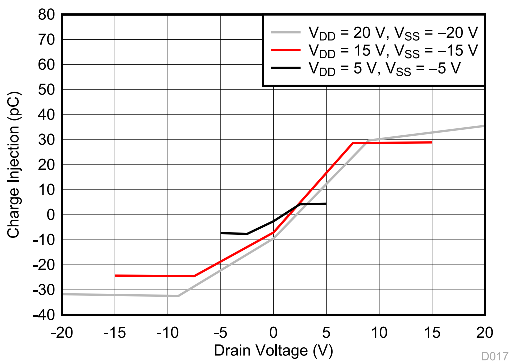


Figure 6-15. Charge Injection vs Drain Voltage – Dual Supply

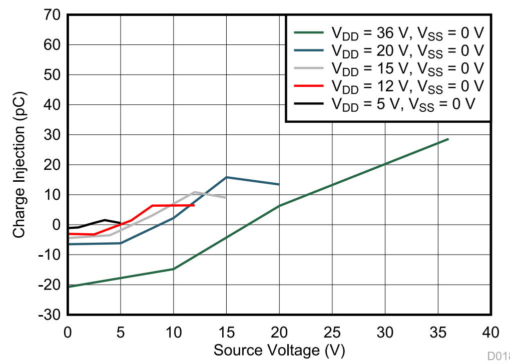


Figure 6-16. Charge Injection vs Source Voltage – Single Supply

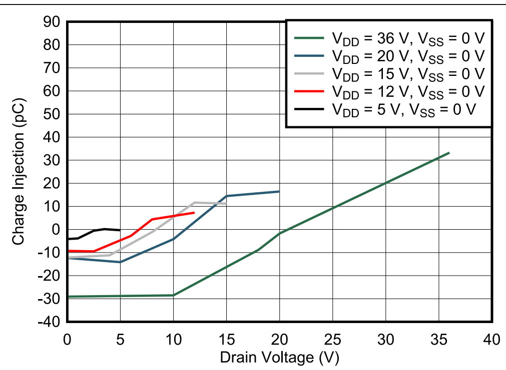


Figure 6-17. Charge Injection vs Drain Voltage – Single Supply

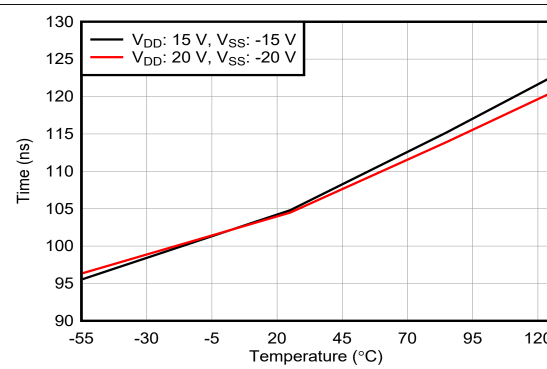


Figure 6-18. $T_{TRANSITION}$ vs Temperature

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

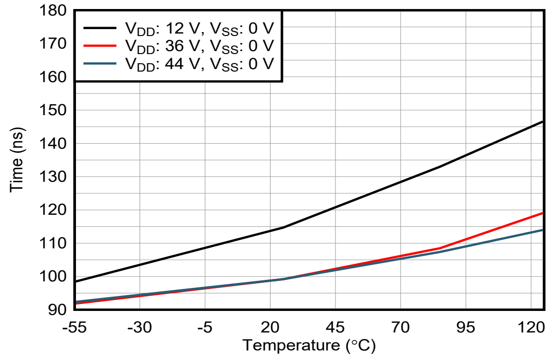
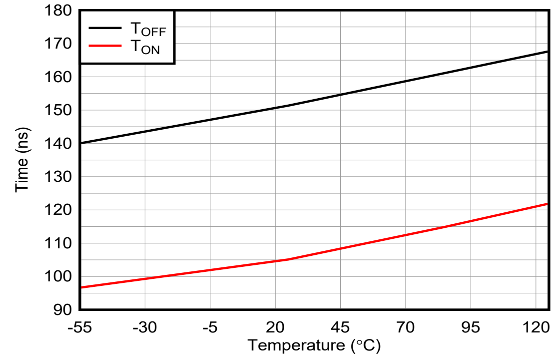
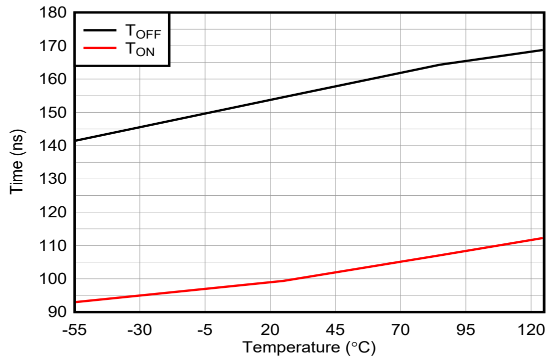


Figure 6-19. $T_{TRANSITION}$ vs Temperature



V_{DD} = 15V, V_{SS} = -15V

Figure 6-20. T_{ON} and T_{OFF} vs Temperature



V_{DD} = 44V, V_{SS} = 0V

Figure 6-21. T_{ON} and T_{OFF} vs Temperature

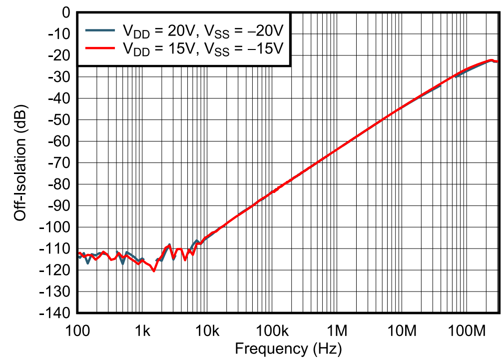


Figure 6-22. Off-Isolation vs Frequency

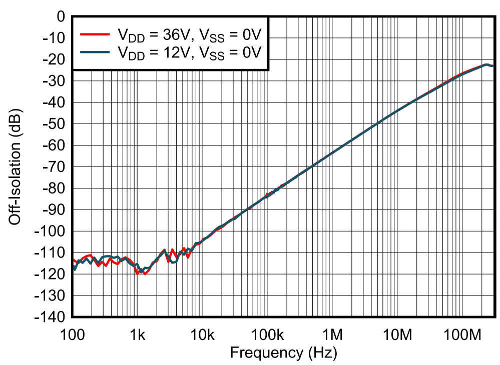
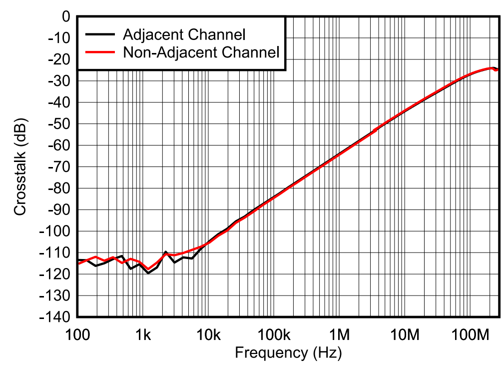


Figure 6-23. Off-Isolation vs Frequency



V_{DD} = 15V, V_{SS} = -15V

Figure 6-24. Crosstalk vs Frequency

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

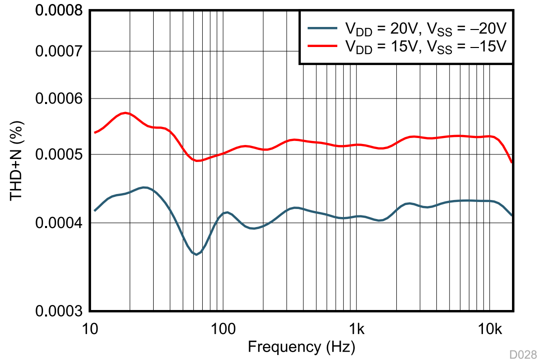


Figure 6-25. THD+N vs Frequency (Dual Supply)

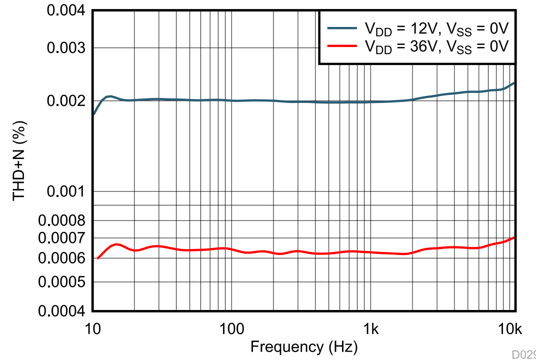
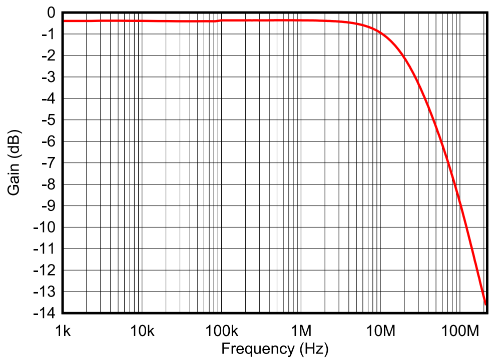
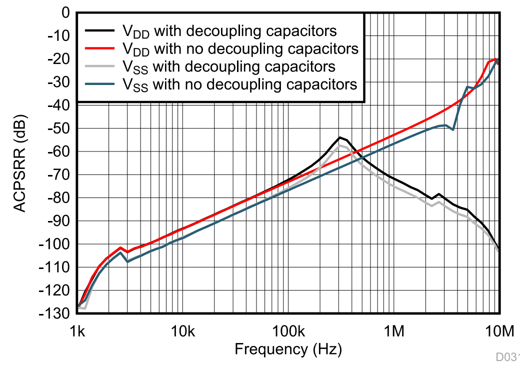


Figure 6-26. THD+N vs Frequency (Single Supply)



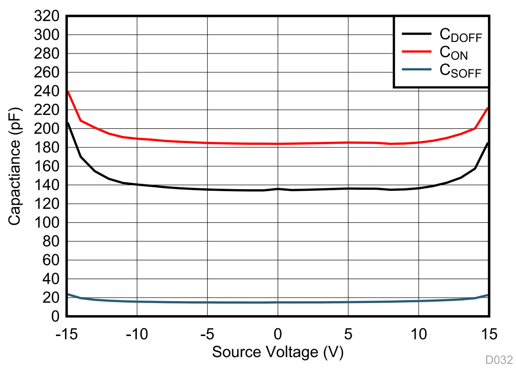
V_{DD} = 15V, V_{SS} = -15V

Figure 6-27. On Response vs Frequency



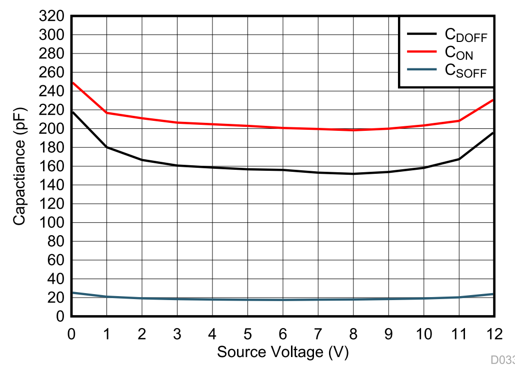
V_{DD} = +15V, V_{SS} = -15V

Figure 6-28. ACPSRR vs Frequency



V_{DD} = +15V, V_{SS} = -15V

Figure 6-29. Capacitance vs Source Voltage or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0V

Figure 6-30. Capacitance vs Source Voltage or Drain Voltage

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 7-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

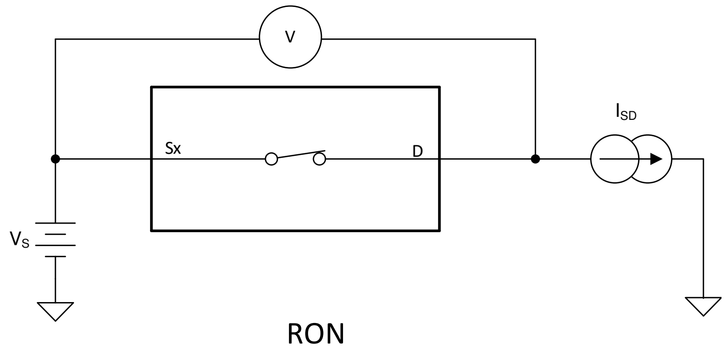


Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 7-2 shows the setup used to measure both off-leakage currents.

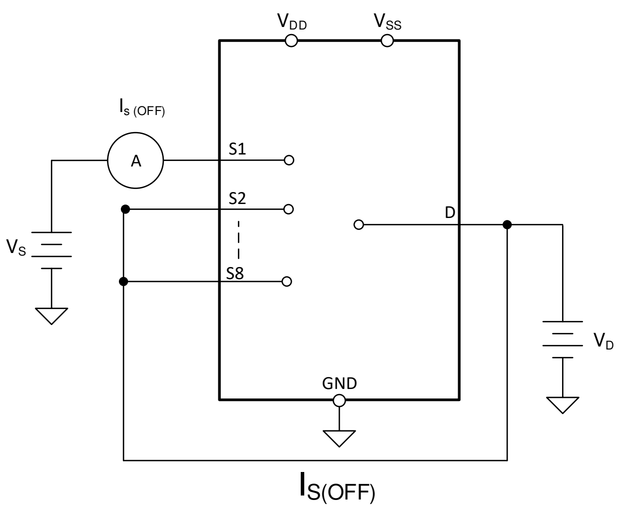


Figure 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

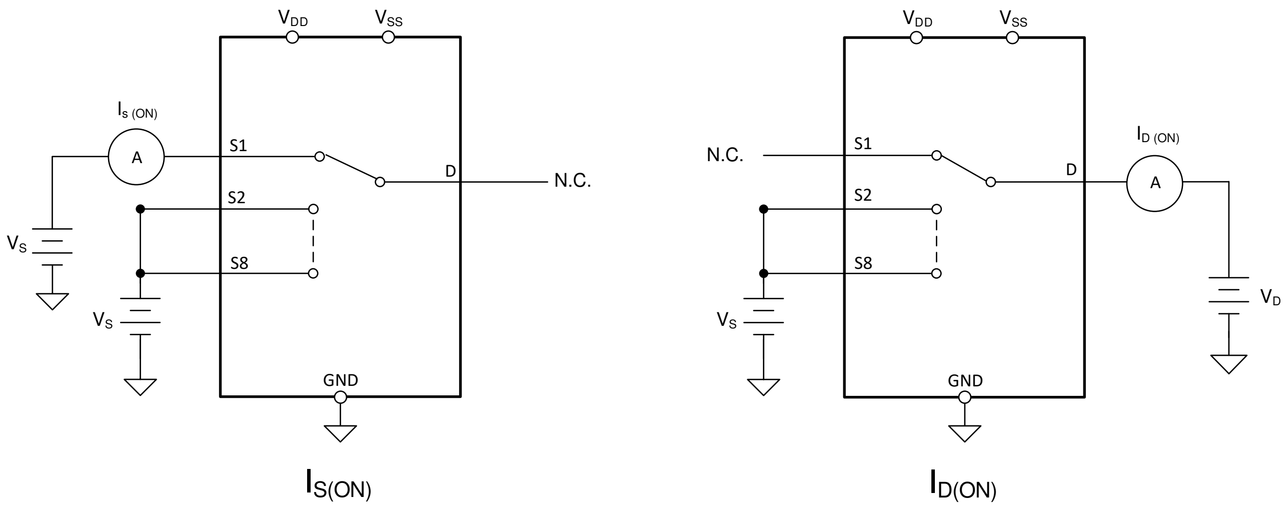


Figure 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

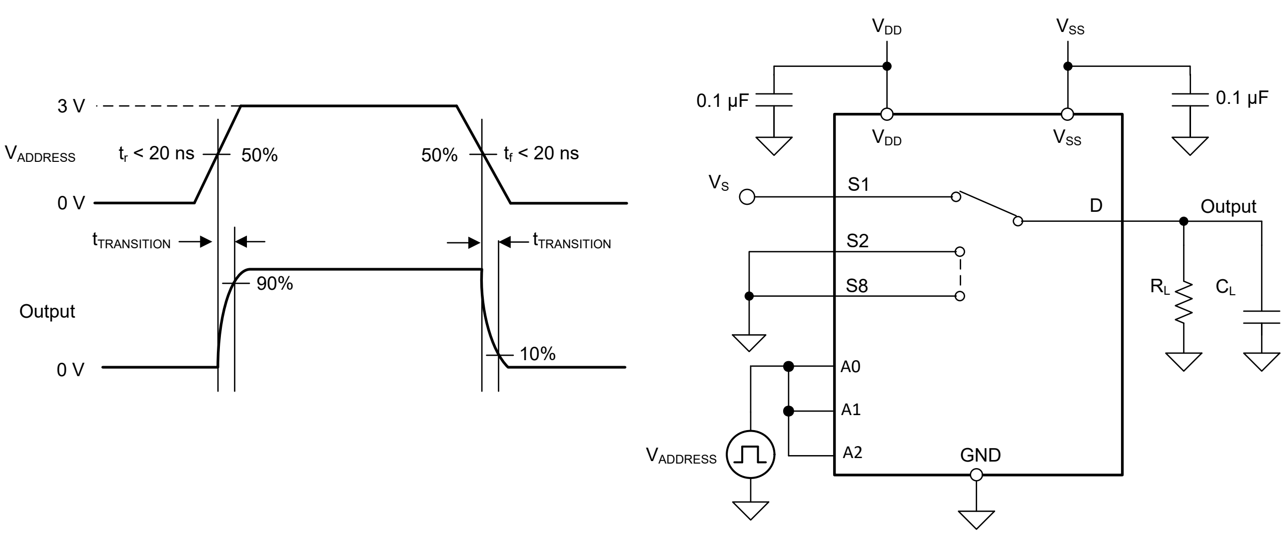


Figure 7-4. Transition-Time Measurement Setup

7.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-7 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 7-7 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

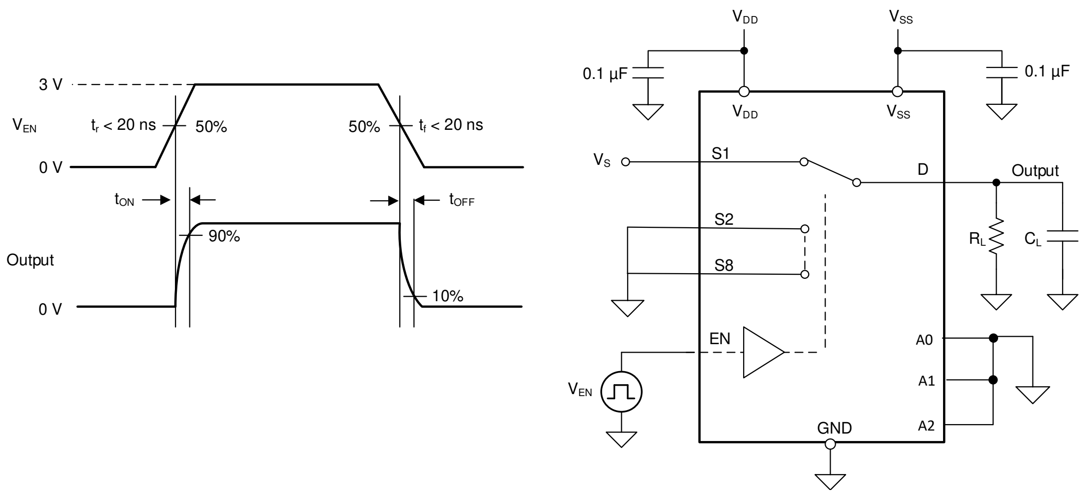


Figure 7-5. Turn-On and Turn-Off Time Measurement Setup

7.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

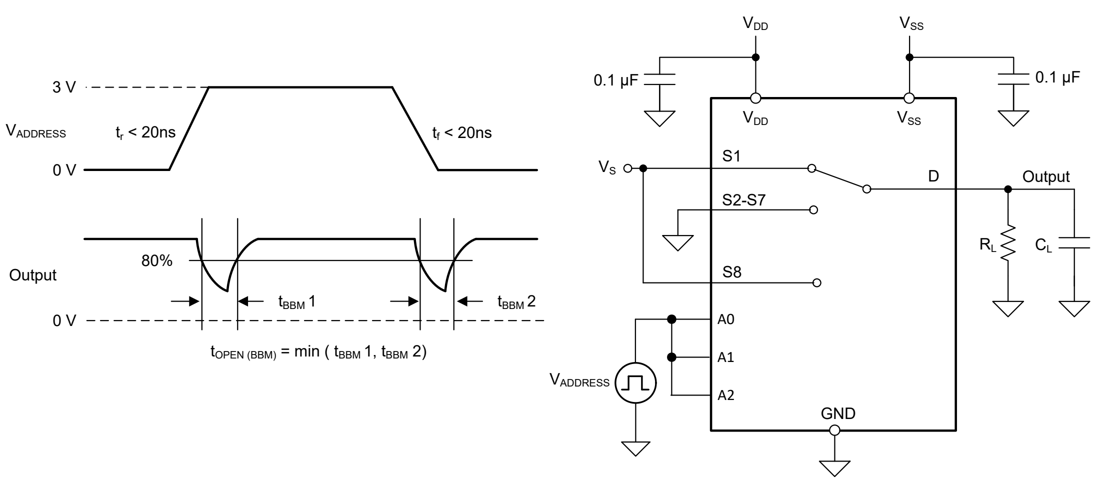


Figure 7-6. Break-Before-Make Delay Measurement Setup

7.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 7-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

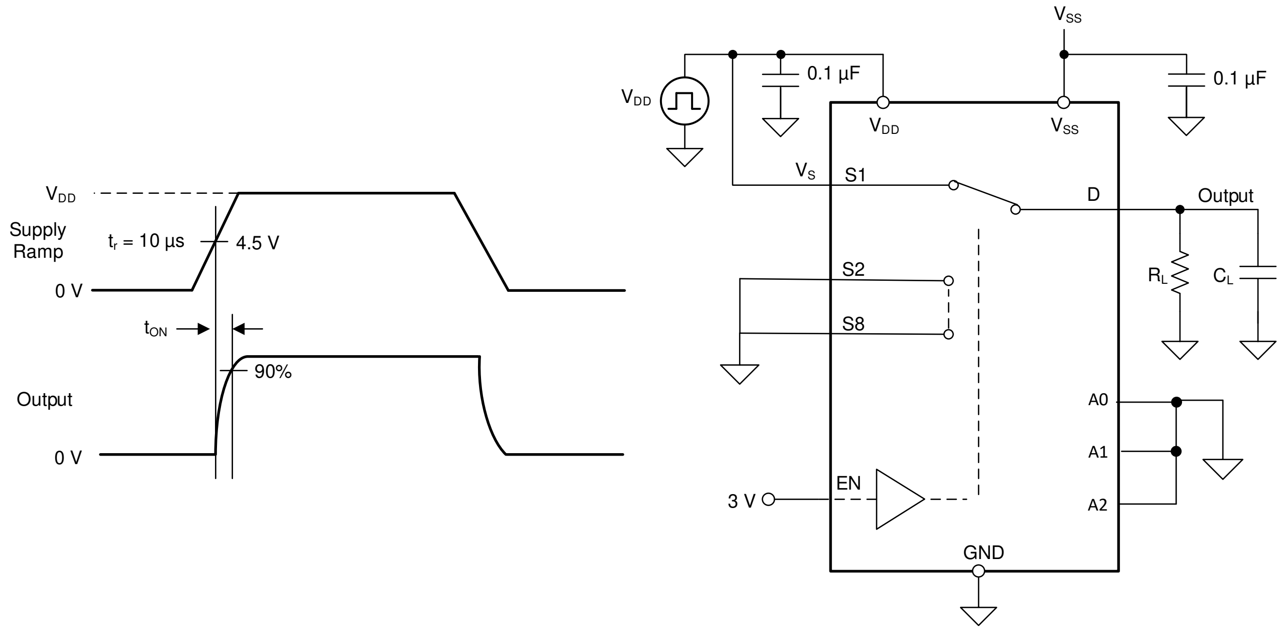


Figure 7-7. $t_{ON\ (VDD)}$ Time Measurement Setup

7.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 7-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

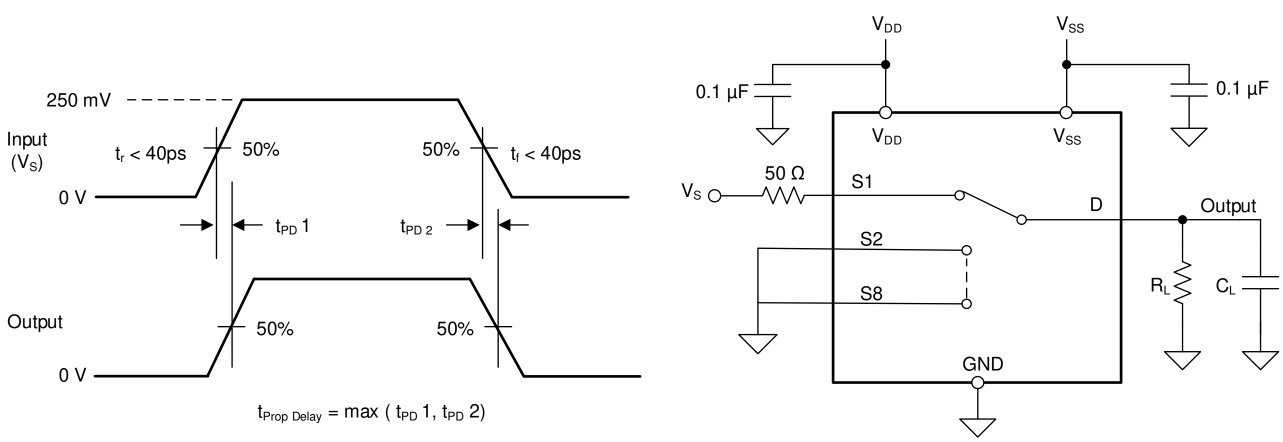


Figure 7-8. Propagation Delay Measurement Setup

7.9 Charge Injection

The TMUX7208M has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 7-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

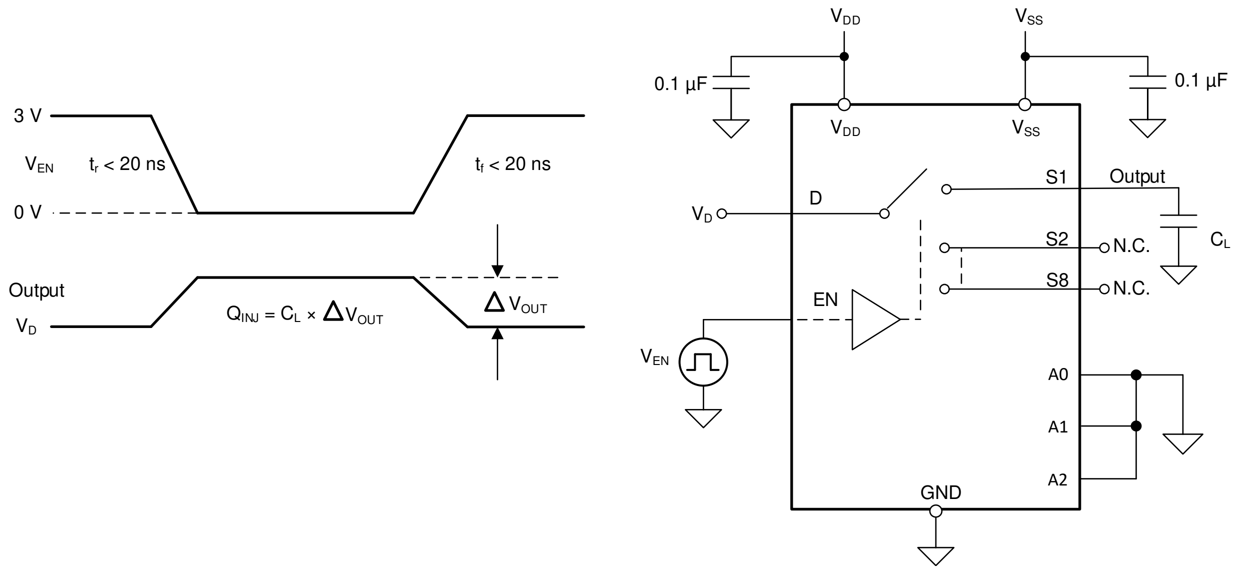
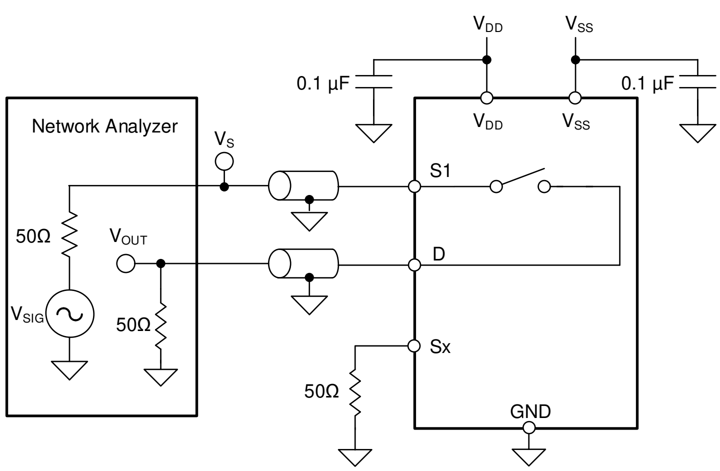


Figure 7-9. Charge-Injection Measurement Setup

7.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-10 shows the setup used to measure, and the equation used to calculate off isolation.

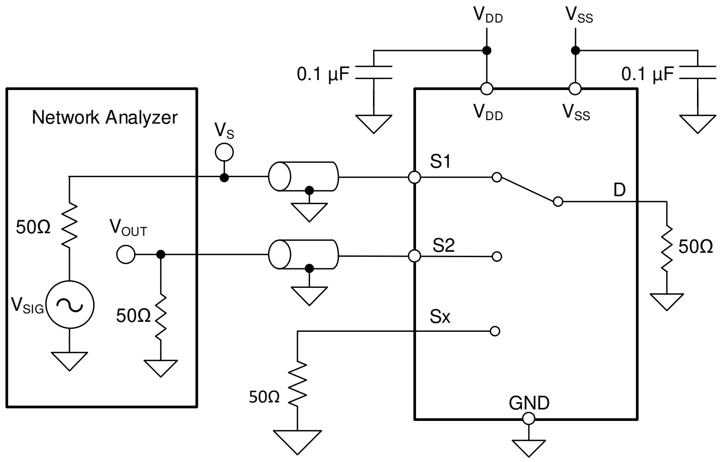


$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-10. Off Isolation Measurement Setup

7.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 7-11 shows the setup used to measure, and the equation used to calculate crosstalk.

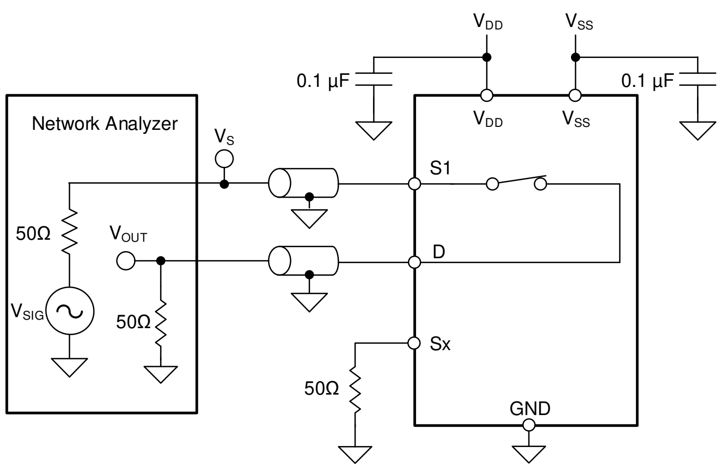


$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-11. Crosstalk Measurement Setup

7.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 7-12 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 7-12. Bandwidth Measurement Setup

7.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N.

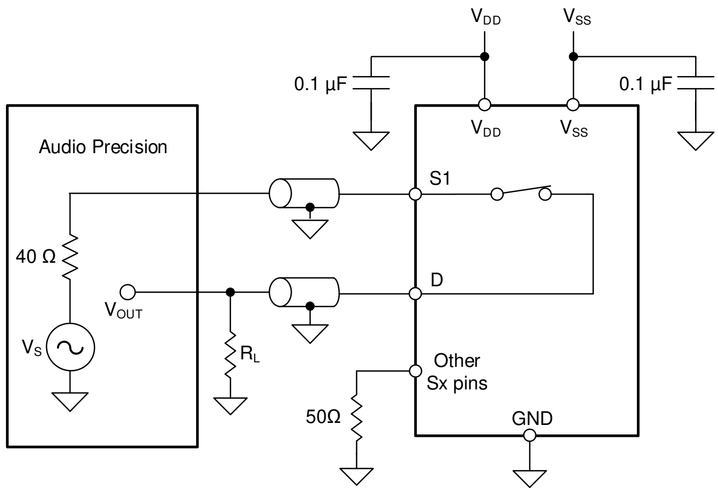
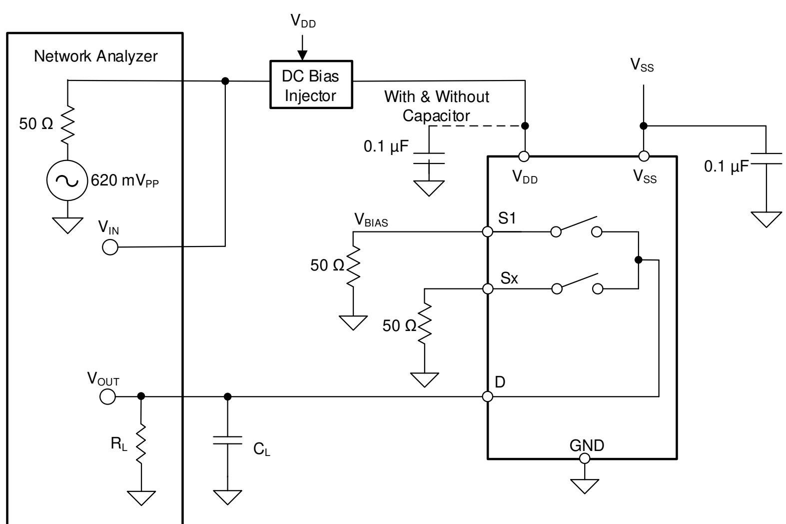


Figure 7-13. THD+N Measurement Setup

7.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

Figure 7-14 shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.



$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

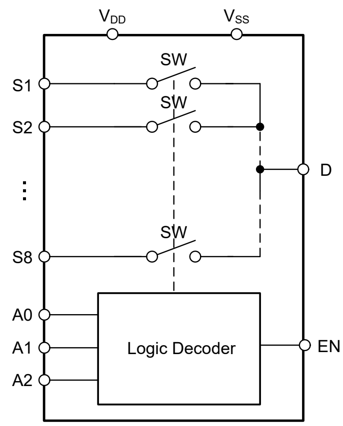
Figure 7-14. ACPSRR Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX7208M is an 8:1, 1-channel multiplexer. Each channel is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX7208M conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input or output voltage for the TMUX7208M ranges from V_{SS} to V_{DD}.

8.3.3 1.8 V Logic Compatible Inputs

TMUX7208M have 1.8V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

8.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX7208M has internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4MΩ, but is clamped to about 1µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.3.5 Fail-Safe Logic

TMUX7208M supports fail-safe logic on the control input pins (EN and Ax) allowing it to operate up to 44V, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-safe logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the fail-safe logic feature allows the TMUX7208M logic input pins to ramp up to +44V while V_{DD} and V_{SS} = 0V. The logic control inputs are protected against positive faults of up to +44V in powered-off condition, but do not offer protection against negative overvoltage conditions.

8.3.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX72xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.3.7 Ultra-Low Charge Injection

The TMUX7208M have a transmission gate topology, as shown in Figure 8-1. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

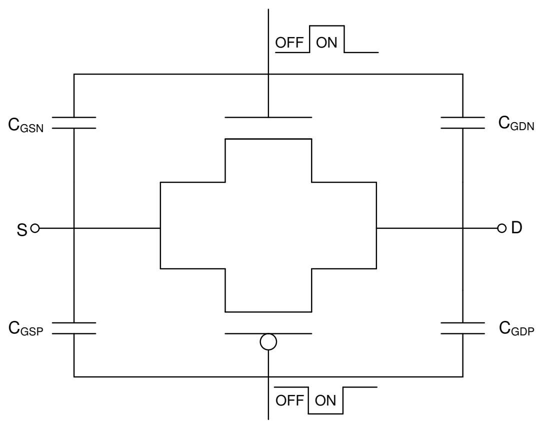


Figure 8-1. Transmission Gate Topology

The TMUX7208M contains specialized architecture to reduce charge injection on the Drain (D). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the Source (Sx) instead of the Drain (D). As a general rule of thumb, Cp should be 20x larger than the equivalent load capacitance on the Drain (D). Figure 8-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX7219M as part of the TMUX72xx family with a 100pF load capacitance.

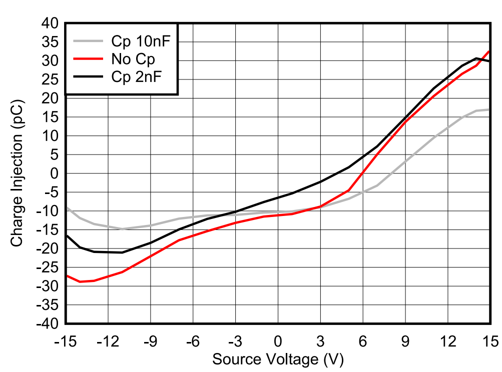


Figure 8-2. Charge Injection Compensation

8.4 Device Functional Modes

When the EN pin of the TMUX7208M is pulled high, one of the switches is closed based on the state of the Ax pin. When the EN pin is pulled low, all of the switches are in an open state regardless of the state of the Ax pin. The control pins can be as high as 44V.

The TMUX7208M can operate without any external components except for the supply decoupling capacitors. The EN and Ax pins have internal pull-down resistors of 4MΩ. If unused, tie Ax and EN pins to GND to prevent the device from consuming additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or D) should be connected to GND.

8.5 Truth Tables

Table 8-1 provides the truth tables for the TMUX7208M.

Table 8-1. TMUX7208M Truth Table

EN	A2	A1	A0	Selected Source Connected To Drain (D) Pin
0	X(1)	X	X	All sources are off (HI-Z)
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) X denotes *do not care*.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMUX7208M is part of the precision switches and multiplexers family of devices. These devices operate with dual supplies (±4.5V to ±22V), a single supply (4.5V to 44V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5V), and offer true rail-to-rail input and output. The TMUX7208M offers low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features makes the TMUX72xx a family of precision, robust, high-performance analog multiplexers for high-voltage, industrial applications.

9.2 Typical Application

One example to take advantage of performance is the implementation of multiplexed data acquisition front end for multiple input sensors. Applications such as analog input modules for programmable logic controllers (PLCs), data acquisition (DAQ), and semiconductor test systems commonly need to monitor multiple signals into a single ADC channel. The multiple inputs can come from different system voltages being monitored, or environmental sensors such as temperature or humidity. Figure 9-1 shows a simplified example of monitoring multiple inputs into a single ADC using a multiplexer.

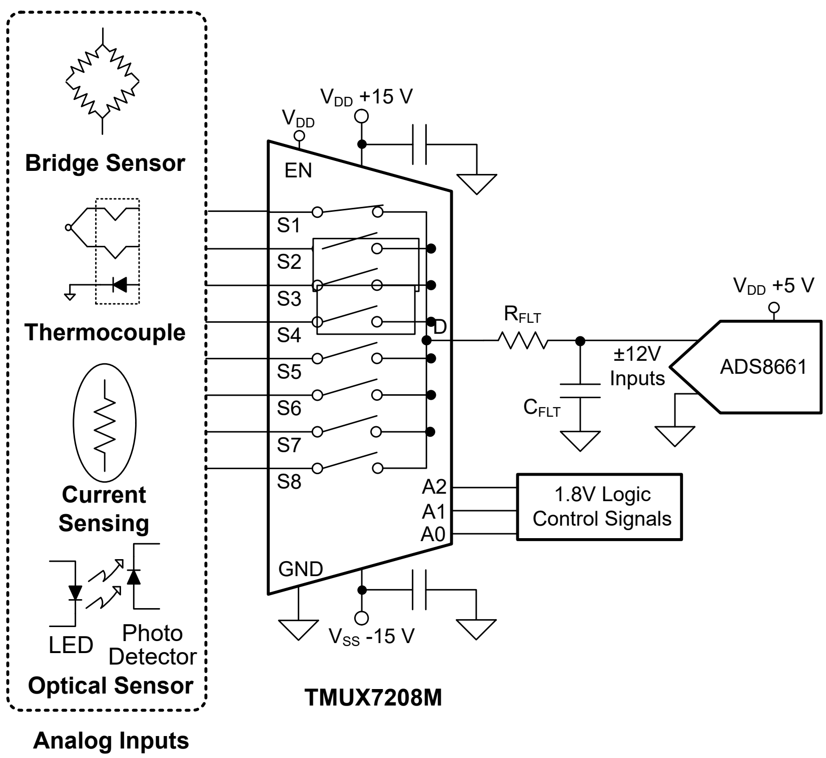


Figure 9-1. Multiplexed Data Acquisition Front End

9.2.1 Design Requirements

Table 9-1. Design Parameters

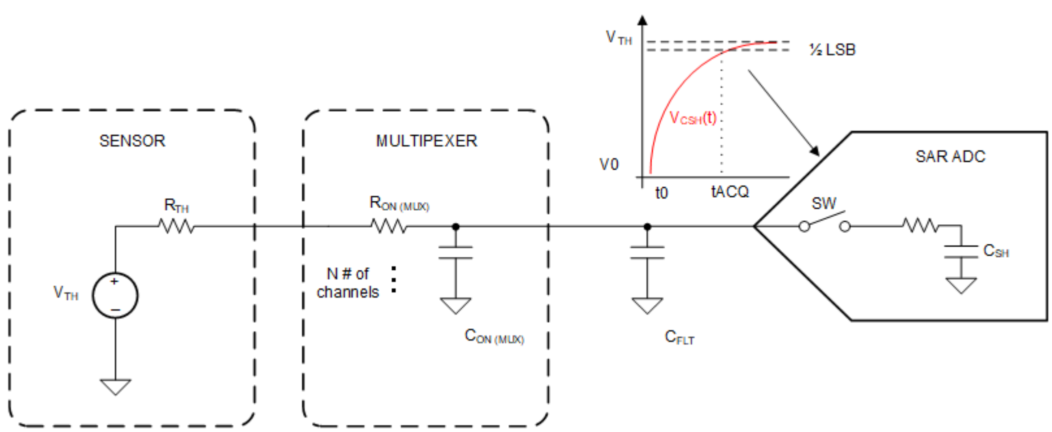
PARAMETER	VALUE
Positive supply (VDD)	+15V
Negative supply (V_{SS})	-15V
Input and output signal range	-12 V to 12 V (limit of ADC)
Control logic thresholds	1.8 V compatible
Temperature range	-55°C to +125°C

9.2.2 Detailed Design Procedure

The application shown in Figure 9-1 demonstrates how a multiplexer can be used to simplify the signal chain and monitor multiple input signals to a single ADC channel. In this example the ADC has software programmable input ranges up to ±12.288 V. The ADC also has overvoltage protection up to ±20V, which allows for the multiplexer to be powered with wider supply voltages than the input signal range to maximize the on resistance performance of the multiplexer, while still maintaining system level overvoltage protection beyond the useable signal range. Both the multiplexer and the ADC are capable of operation in extended industrial temperature range of -55°C to +125°C allowing for use in a wider array of industrial systems.

Many SAR ADCs have an analog input structure that consists of a sampling switch and a sampling capacitor. Many signal chains will have a driver amplifier to help charge the input of the ADC to meet a fast system acquisition time. However, a driver amplifier is not always needed to drive SAR ADCs. Figure 9-2 shows a typical diagram of a sensor driving the SAR ADC input directly after being passed through the multiplexer. A filter capacitor (C_{FLT}) is connected to the input of the ADC to reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitor of the ADC.

The sensor block simplifies the device into a Thevenin equivalent voltage source (V_{TH}) and resistance (R_{TH}) which can be extracted from the device data sheets. Similarly the multiplexer can be thought of as a series resistance ($R_{ON(MUX)}$) and capacitance ($C_{ON(MUX)}$). To ensure maximum precision of the signal chain, the system should be able to settle within 1/2 of an LSB within the acquisition time of the ADC. The time constant can be calculated as shown in Figure 9-2. This equation highlights the importance of selecting a multiplexer with low on-resistance to further reduce the system time constant. Additionally, low charge injection performance of the multiplexer is helpful to reduce conversion errors and improve accuracy of the measurements.



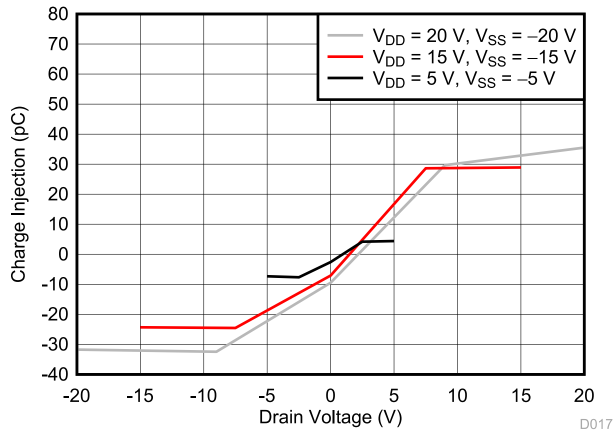
$t_{ACQ} > k \times \tau_{FLT}$

- $\tau_{FLT} = (R_{TH} + R_{ON\ (MUX)})\ X\ (C_{FLT} + C_{ON\ (MUX)})$
- k is single pole time constant for N bit ADC

Figure 9-2. Driving SAR ADC

9.2.3 Application Curve

The low on and off leakage currents of TMUX7208M and ultra-low charge injection performance make this device ideal for implementing high precision industrial systems. The TMUX7208M contains specialized architecture to reduce charge injection on the drain side (D) (see Section 8.3.7 for more details). Figure 9-3 shows the plot for the charge injection versus source voltage for the TMUX7208M.



T_A = 25°C

Figure 9-3. Charge Injection vs Drain Voltage

9.3 Power Supply Recommendations

The TMUX7208M operates across a wide supply range of ±4.5V to ±22V (4.5V to 44V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF at the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

9.4 Layout

9.4.1 Layout Guidelines

A reflection can occur when a PCB trace turns a corner at a 90° angle. A reflection occurs primarily because of the change of width of the trace. The trace width increases to 1.414 times the width at the apex of the turn. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 9-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

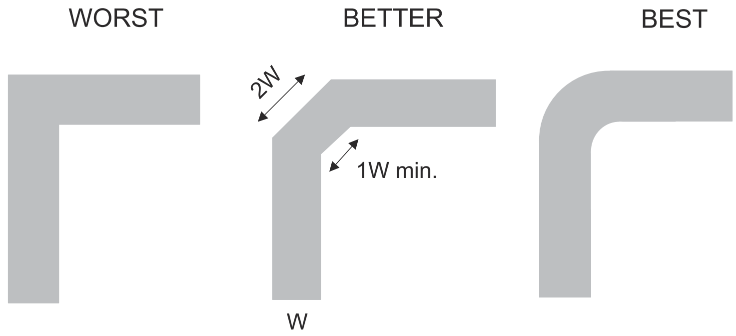


Figure 9-4. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 9-5 shows an example of a PCB layout with the TMUX7208M. Some key considerations are:

- Decouple the supply pins with a 0.1 µF and 1 µF capacitor, placed lowest value capacitor as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

9.4.2 Layout Example

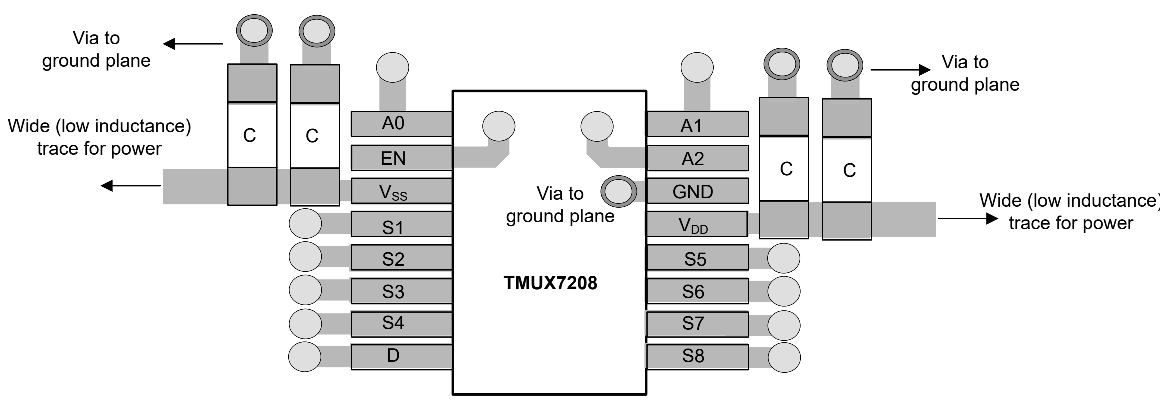


Figure 9-5. TMUX7208M Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability* application note
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

DATE	REVISION	NOTES
January 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX7208MPWR	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	X208
TMUX7208MPWR.B	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	X208

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

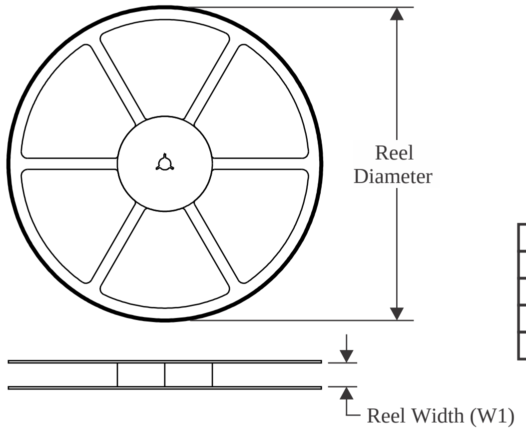
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

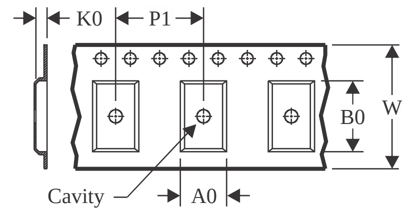
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

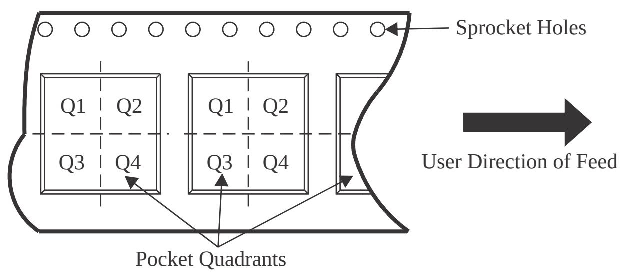


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

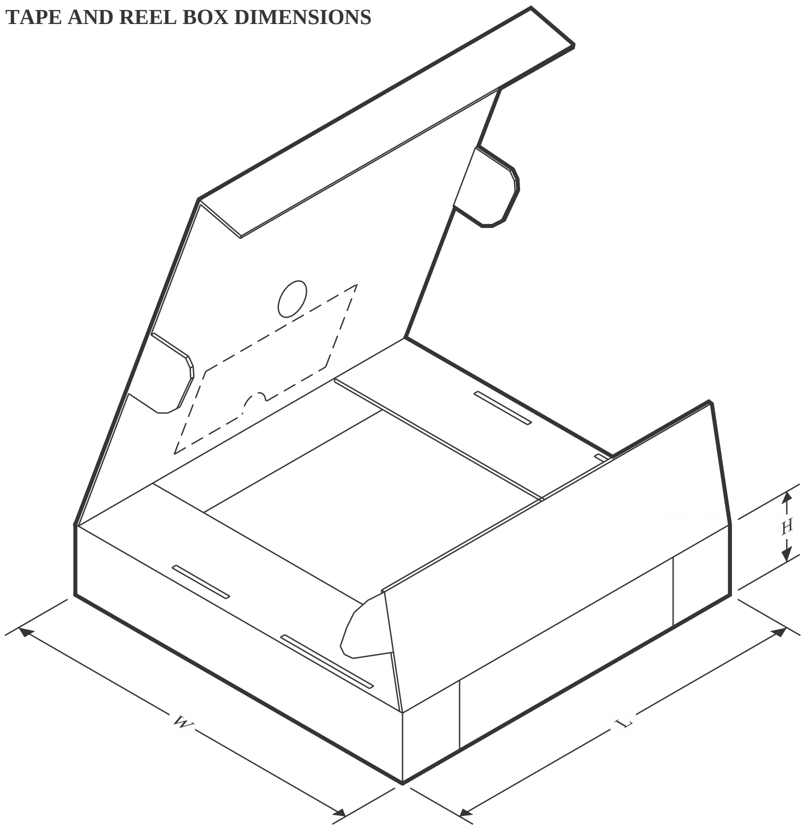
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

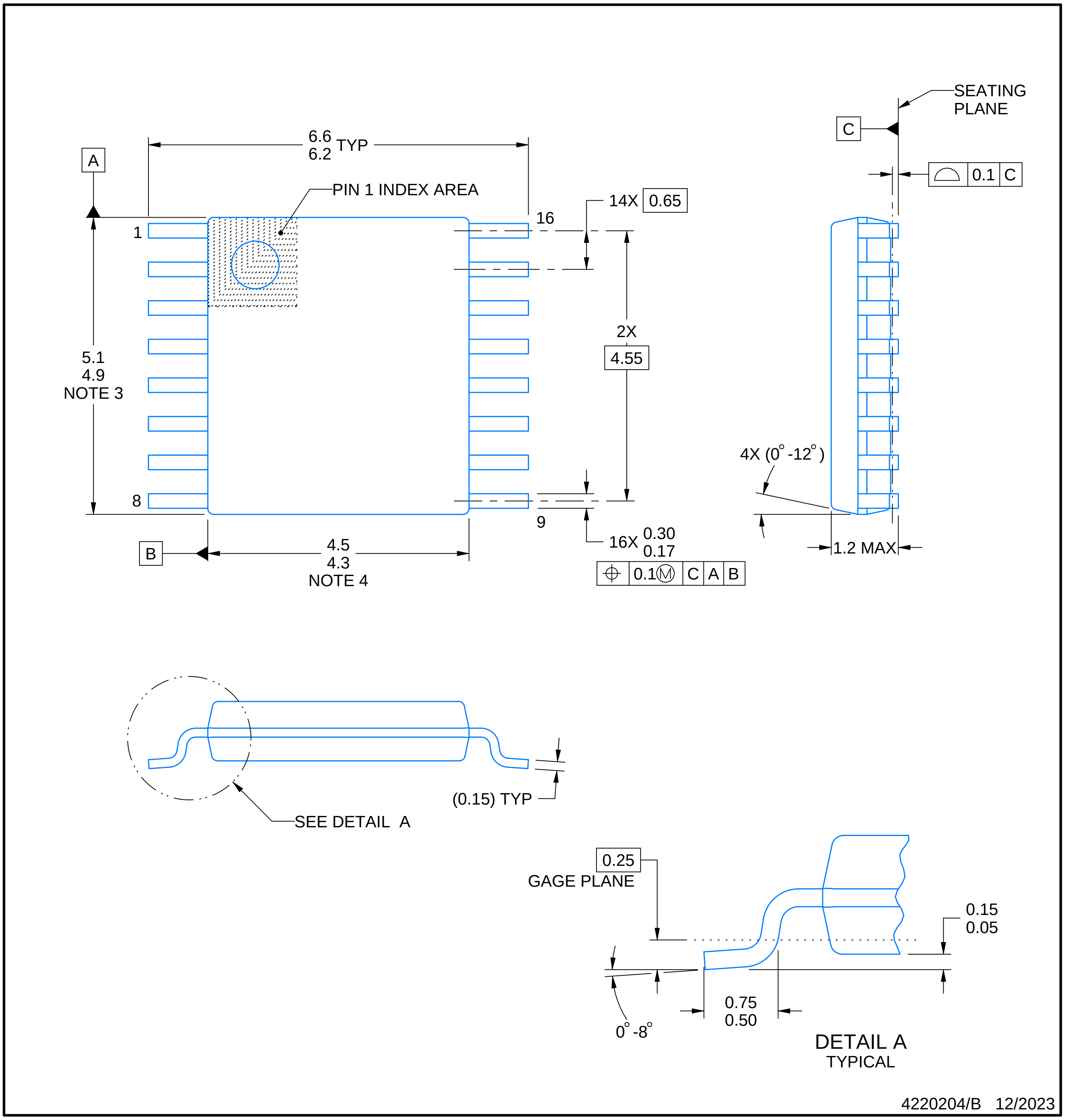
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7208MPWR	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



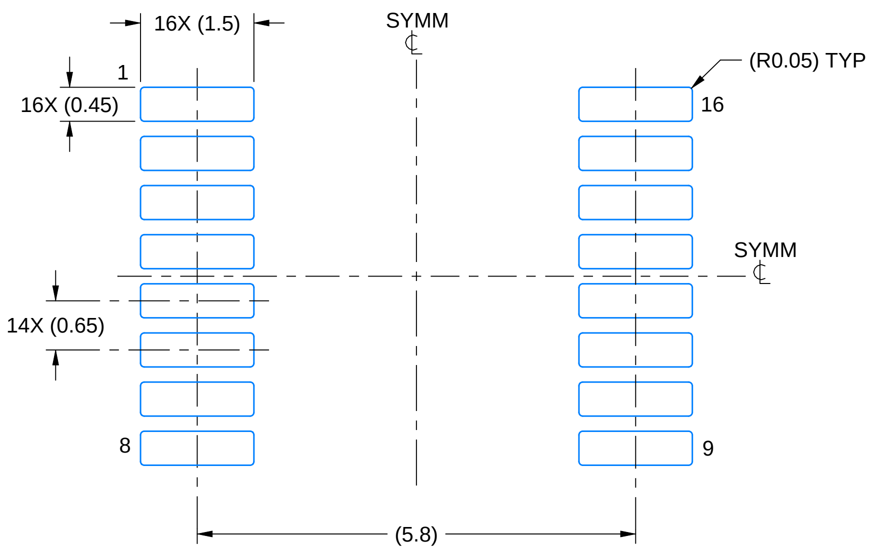
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7208MPWR	TSSOP	PW	16	2500	353.0	353.0	32.0

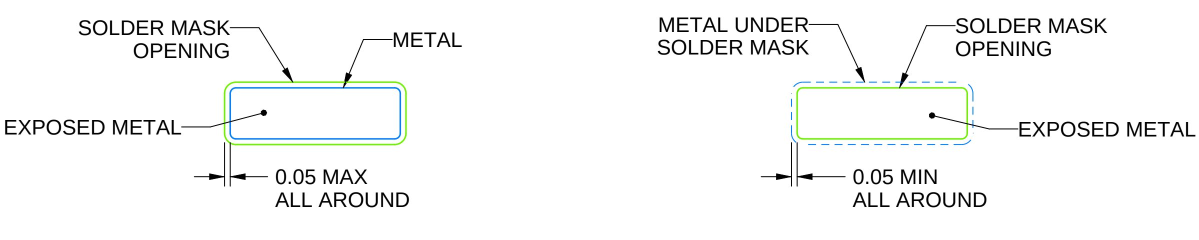


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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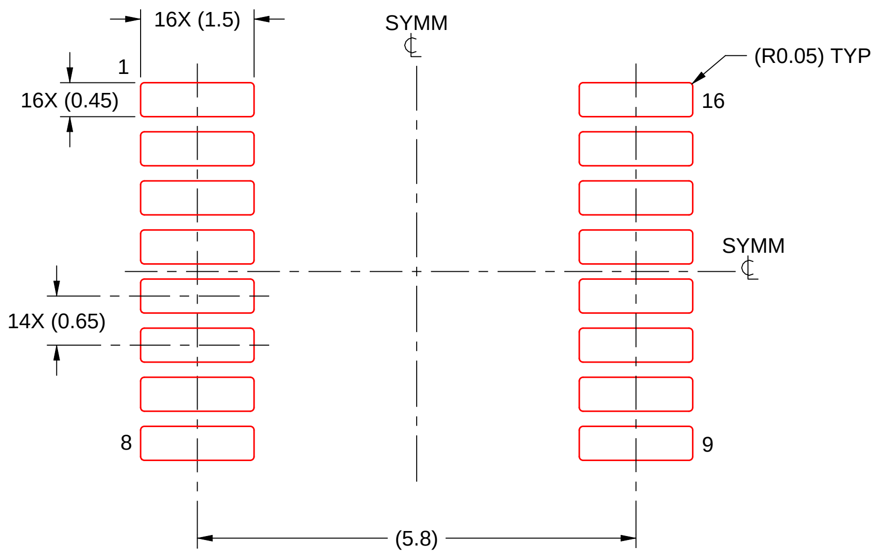
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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