TMUX6612-Q1 Automotive 30V, Low-RON, 1:1 (SPST), 4-Channel Precision Switches with 1.8V Logic

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature
- Functional safety-capable
  - Documentation available to aid functional safety system design
- Dual supply range: ±4.5V to ±20V
- Single supply range: 4.5V to 36V
- Asymmetric dual supply operation (for example, +20V, -10V)
- 1.8V logic compatible
- Precision performance:
  - Low on-resistance: 1.1Ω (typical)
  - Ultra low on-resistance flatness: 0.005Ω (typical)
  - High current support: 470mA (maximum)
  - Ultra low charge injection: 6pC (typical)
- –40°C to +125°C operating temperature
- Rail-to-rail operation
- Bidirectional operation
- Break-before-make switching

2 Applications

- OBDII CAN switching
- On board charging (OBC)
- Advanced driver assistance systems (ADAS)
- ADAS domain controller
- Telematics control unit
- Body control modules (BCM)
- Body electronics and lighting
- Battery management systems
- HVAC controller module

3 Description

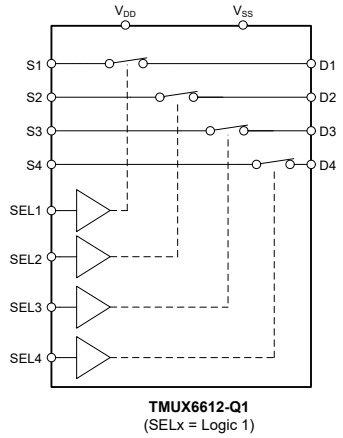
The TMUX6612-Q1 is a complementary metal-oxide semiconductor (CMOS) switch device with four independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device works with a single supply (4.5V to 36V), dual supplies (±4.5V to ±20V), or asymmetric supplies (such as V_{DD} = 20V, V_{SS} = –10V). The TMUX6612-Q1 supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}.

The switches of the TMUX6612-Q1 are controlled with appropriate logic control inputs on the SELx pins. The TMUX6612-Q1 features a special architecture which allows for ultra-low charge injection. This helps prevent unwanted coupling from the control input to the analog output of the device and reduces AC noise and offset errors.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX6612-Q1	PW (TSSOP, 16)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length x width) is a nominal value and includes pins, where applicable.



TMUX6612-Q1 Block Diagram

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4 Pin Configuration and Functions

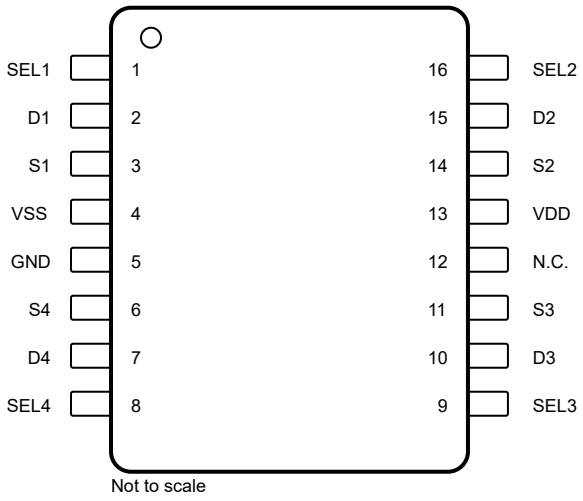


Figure 4-1. PW Package, 16-Pin TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
D1	2	I/O	Drain pin 1. Can be an input or output.
D2	15	I/O	Drain pin 2. Can be an input or output.
D3	10	I/O	Drain pin 3. Can be an input or output.
D4	7	I/O	Drain pin 4. Can be an input or output.
GND	5	P	Ground (0V) reference.
N.C.	12	—	No internal connection. Can be shorted to GND or left floating
S1	3	I/O	Source pin 1. Can be an input or output.
S2	14	I/O	Source pin 2. Can be an input or output.
S3	11	I/O	Source pin 3. Can be an input or output.
S4	6	I/O	Source pin 4. Can be an input or output.
SEL1	1	I	Logic control input 1, has internal pull-down resistor. Controls channel 1 state as provided in Table 17-1.
SEL2	16	I	Logic control input 2, has internal pull-down resistor. Controls channel 2 state as provided in Table 17-1.
SEL3	9	I	Logic control input 3, has internal pull-down resistor. Controls channel 3 state as provided in Table 17-1.
SEL4	8	I	Logic control input 4, has internal pull-down resistor. Controls channel 4 state as provided in Table 17-1.
VDD	13	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND
VSS	4	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VSS and GND. In single-supply applications, this pin should be connected to ground.

(1) I = input, O = output, I/O = input and output, P = power.

5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		42	V
V_{DD}		–0.5	40	V
V_{SS}		–32	0.5	V
V_{SEL}-V_{SS}	Logic Supply Voltage	–0.5	40	V
I_{SEL}	Logic control input pin current (SEL pins)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain current (Sx, Dx)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Current* table for I_{DC} specifications.

6 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7 Thermal Information

THERMAL METRIC(1)		TMUX6612 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8 Source or Drain Current through Switch

Current through the Switch	Test Conditions	T_J = 25°C	T_J = 50°C	T_J = 85°C	T_J = 105°C	T_J = 125°C	T_J = 135°C	T_J = 150°C	UNIT
I_{DC} (1)	V_{SS} to V_{DD} - 2.5V	470	470	470	309	143	100	60	mA
I_{peak} (2)	V_{SS} to V_{DD} - 2.5V	470	470	470	470	470	470	470	mA

(1) See Section 18.5 for more details
(2) Pulse current of 1ms with 10% Duty Cycle

9 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential		4.5		40	V
V_{DD}	Positive power supply voltage		4.5		36	V
V_S or V_D	Single Supply: Signal path input/output voltage (source or drain pin) (Sx, Dx)	Signal path input/ output voltage (source or drain pin) (Sx, D)	0		V_{DD}	V
	Dual Supply: Signal path input/output voltage (source or drain pin) (Sx, Dx)(3)		V_{SS}		V_{DD}	V
$\lvert V_S - V_D \rvert$	Signal voltage across the switch path (source or drain pin) (Sx, Dx)	Signal path input/ output voltage (source or drain pin) (Sx, D)	0		30	V
V_{SEL}-V_{SS}	Logic Supply Voltage	Logic supply voltage	0		36	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)				I_{DC} (2)	mA
T_A	Ambient temperature		–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5V ≤ (V_{DD} – V_{SS}) ≤ 40V, and the minimum and maximum V_{DD} is met.
(2) Refer to Section 8 through Switch table for I_{DC} specifications.
(3) Follow $\lvert V_S - V_D \rvert$ ≤ 30V for nominal operating conditions.

10 Electrical Characteristics (Global)

Typical at V_{DD} = +15V, V_{SS} = –15V, V_L = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.005	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–2	–0.005		µA
T_{SD}	Thermal shutdown				165		°C
T_{SD_HYST}	Thermal shutdown hysteresis				15		°C
C_{IN}	Logic input capacitance		–40°C to +125°C		4		pF

11 Electrical Characteristics (±15V Dual Supply)

V_{DD} = +15V ± 10%, V_{SS} = –15V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10V to +10V I_D = –10mA	25°C		1.1	1.4	Ω
			–40°C to +85°C			1.8	
			–40°C to +125°C			2.2	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10V to +10V I_D = –10mA	25°C		0.005		Ω
			–40°C to +85°C			0.055	
			–40°C to +125°C			0.060	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10V to +10V I_D = –10mA	25°C		0.05		Ω
			–40°C to +85°C			0.055	
			–40°C to +125°C			0.060	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –10mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–6		6	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–6		6	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is on V_S = V_D = ±10V	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–6		6	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels(2)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is on V_S = V_D = ±10V	25°C		10		pA
			–40°C to +85°C		22		
			–40°C to +125°C		32		
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 16.5V, V_{SS} = –16.5V All switches OFF	25°C		35	45	µA
			–40°C to +85°C			55	
			–40°C to +125°C			65	
I_{DD}	V_{DD} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V All switches ON	25°C		435	480	µA
			–40°C to +85°C			520	
			–40°C to +125°C			545	
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 16.5V, V_{SS} = –16.5V All switches OFF	25°C		15	20	µA
			–40°C to +85°C			25	
			–40°C to +125°C			40	
I_{SS}	V_{SS} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V All switches ON	25°C		340	380	µA
			–40°C to +85°C			410	
			–40°C to +125°C			425	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

12 Switching Characteristics (±15V Dual Supply)

V_{DD} = +15V ± 10%, V_{SS} = –15V ±10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10V R_L = 300Ω, C_L = 35pF	25°C		2.0	2.5	µs
			–40°C to +85°C			2.75	µs
			–40°C to +125°C			3	µs
t_{OFF}	Turn-off time from control input	V_S = 10V R_L = 300Ω, C_L = 35pF	25°C		1.7	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 10V, R_L = 300Ω, C_L = 35pF	25°C		310		ns
			–40°C to +85°C	125			ns
			–40°C to +125°C	125			ns
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF	25°C		-6		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 100kHz	25°C		–105		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 1MHz	25°C		–74		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 100kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS} = 0V	25°C		180		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, V_{BIAS} = 0V, f = 1MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz	25°C		–80		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15V, V_{BIAS} = 0V R_L = 110Ω , C_L = 5pF, f = 20Hz to 20kHz	25°C		0.001		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 0V, f = 1MHz	25°C		27		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 0V, f = 1MHz	25°C		27		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 0V, f = 1MHz	25°C		22		pF

13 Electrical Characteristics (12V Single Supply)

V_{DD} = +12V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +12V, V_{SS} = 0V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 3V to 9V I_D = –10mA	25°C		1.15	1.6	Ω
			–40°C to +85°C			2	
			–40°C to +125°C			2.3	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 3V to 9V I_D = –10mA	25°C		0.005		Ω
			–40°C to +85°C			0.05	
			–40°C to +125°C			0.05	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 3V to 9V I_D = –10mA	25°C		0.084		Ω
			–40°C to +85°C			0.15	
			–40°C to +125°C			0.16	
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –10mA	–40°C to +125°C		0.006		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 12V, V_{SS} = 0V Switch state is off V_S = 1V / 10V V_D = 10V / 1V	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–6		6	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 12V, V_{SS} = 0V Switch state is off V_S = 1V / 10V V_D = 10V / 1V	25°C	–0.25	0.05	0.25	nA
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–6		6	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 12V, V_{SS} = 0V Switch state is on V_S = V_D = 1V or 10V	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–0.75		0.75	
			–40°C to +125°C	–6		6	
POWER SUPPLY							
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 12V, V_{SS} = 0V All switches OFF	25°C		30	40	µA
			–40°C to +85°C			45	
			–40°C to +125°C			55	
I_{DD}	V_{DD} supply current	V_{DD} = 12V, V_{SS} = 0V All switches ON	25°C		385	440	µA
			–40°C to +85°C			470	
			–40°C to +125°C			480	

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

14 Switching Characteristics (12V Single Supply)

V_{DD} = +12V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +12V, V_{SS} = 0V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8V R_L = 300Ω, C_L = 35pF	25°C		2	2.5	µs
			–40°C to +85°C			3	µs
			–40°C to +125°C			3.5	µs
t_{OFF}	Turn-off time from control input	V_S = 8V R_L = 300Ω, C_L = 35pF	25°C		1.7	2.2	µs
			–40°C to +85°C			2.5	µs
			–40°C to +125°C			3	µs
t_{BBM}	Break-before-make time delay	V_S = 8V, R_L = 300Ω, C_L = 35pF	25°C		320		ns
			–40°C to +85°C	160			ns
			–40°C to +125°C	160			ns
Q_{INJ}	Charge injection	V_S = 6V, C_L = 100pF	25°C		4		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, VBIAS = 6V, f = 100kHz	25°C		–100		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, VBIAS = 6V, f = 1MHz	25°C		–70		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, VBIAS = 6V, f = 100kHz	25°C		–114		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, VBIAS = 6V, f = 1MHz	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, VBIAS = 6V	25°C		165		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 200mV_{RMS}, VBIAS = 6V, f = 1MHz	25°C		–0.095		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz	25°C		–78		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6V, V_{BIAS} = 6V R_L = 110Ω , C_L = 5pF, f = 20Hz to 20kHz	25°C		0.01		%
$C_{S(OFF)}$	Source off capacitance to ground	V_S = 6V, f = 1MHz	25°C		37		pF
$C_{D(OFF)}$	Drain off capacitance to ground	V_S = 6V, f = 1MHz	25°C		37		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance to ground	V_S = 6V, f = 1MHz	25°C		27		pF

15 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

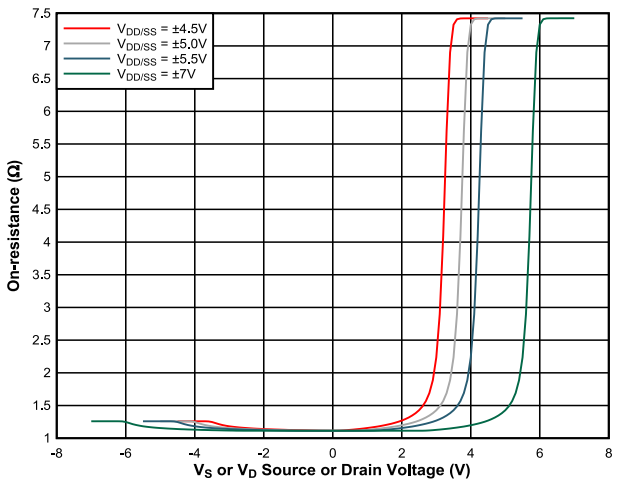


Figure 15-1. On-Resistance vs Source or Drain Voltage

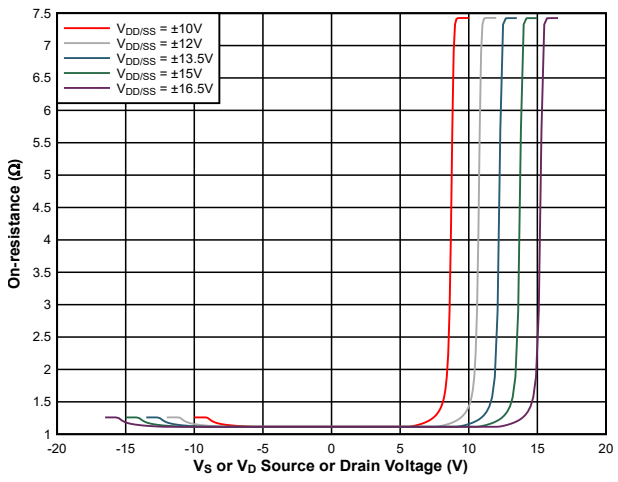


Figure 15-2. On-Resistance vs Source or Drain Voltage

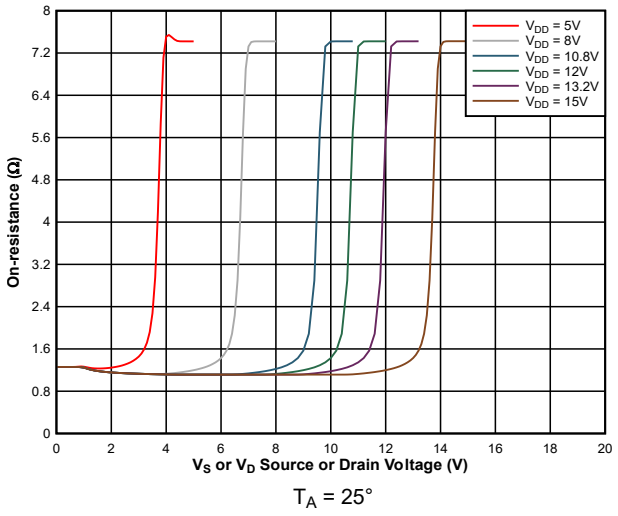


Figure 15-3. On-Resistance vs Source or Drain Voltage

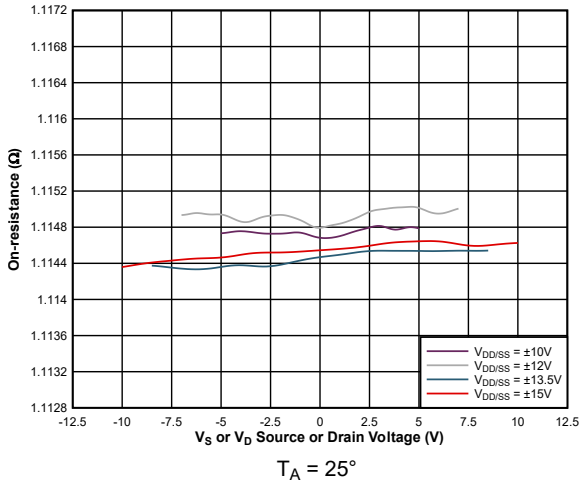
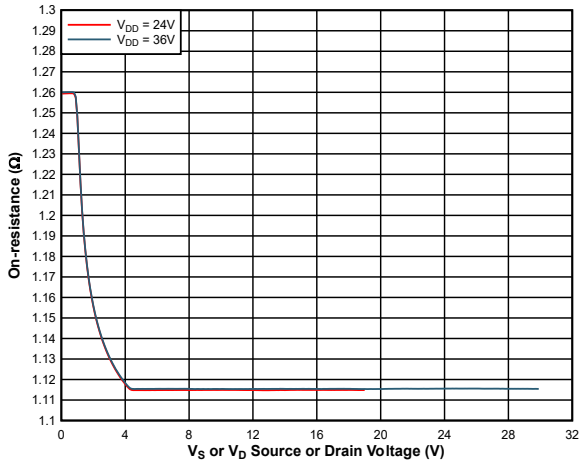


Figure 15-4. On-Resistance vs Source or Drain Voltage

15 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



T_A = 25°

Figure 15-5. On-Resistance vs Source or Drain Voltage

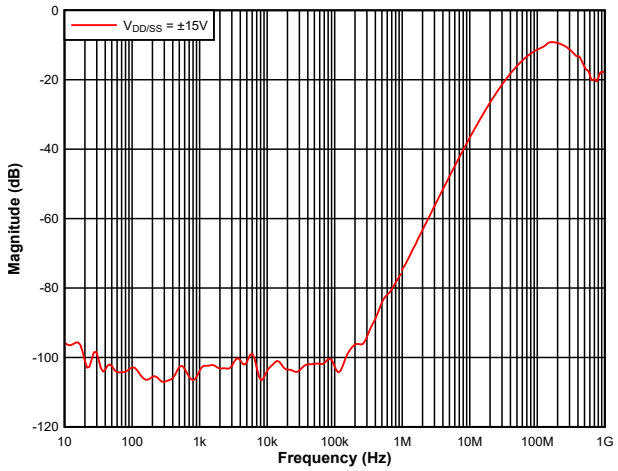


Figure 15-6. Off-Isolation vs Frequency

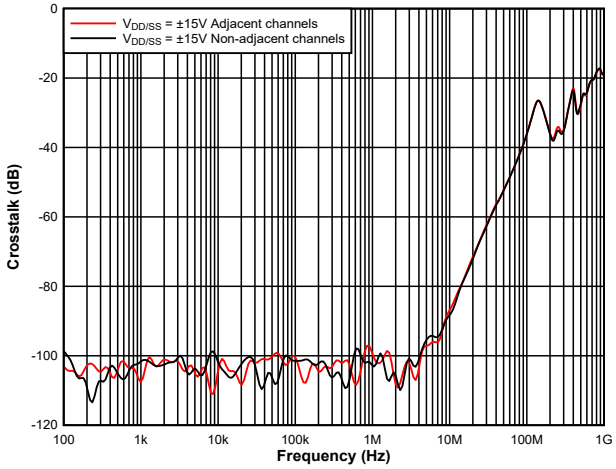


Figure 15-7. Crosstalk vs Frequency

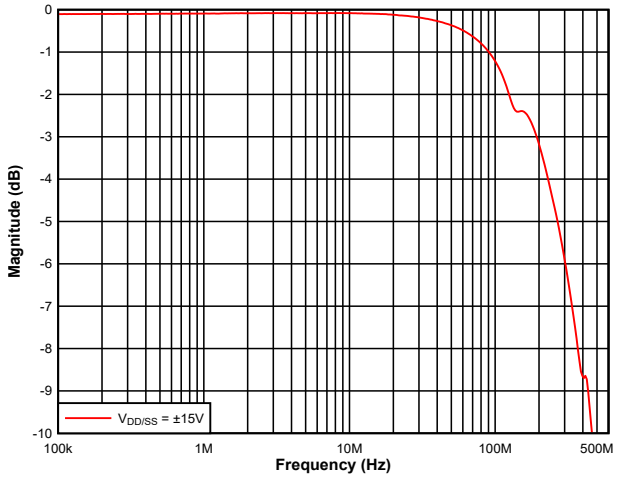


Figure 15-8. Bandwidth vs Frequency

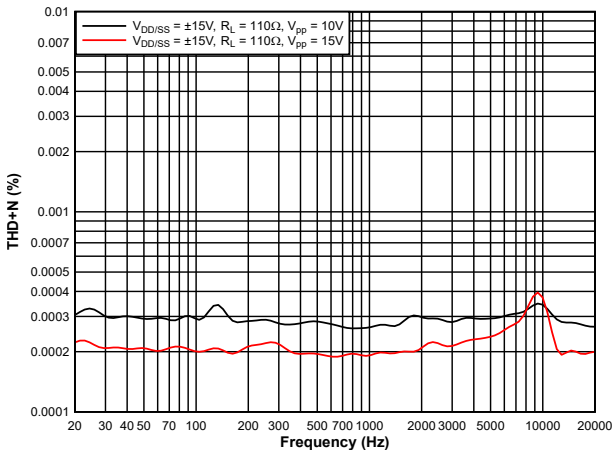


Figure 15-9. THD+N vs Frequency

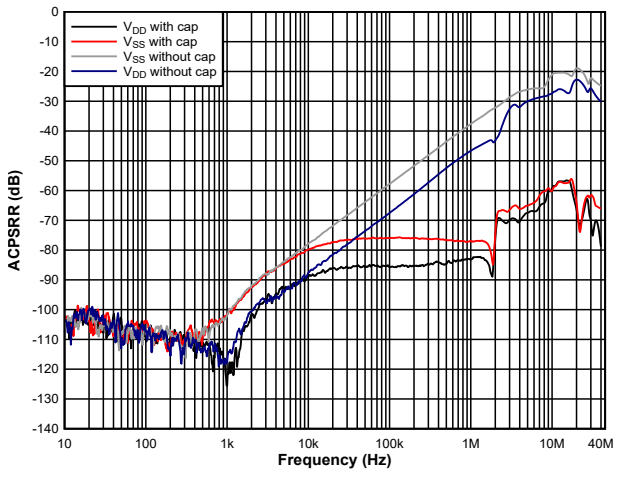


Figure 15-10. ACPSRR vs Frequency

15 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

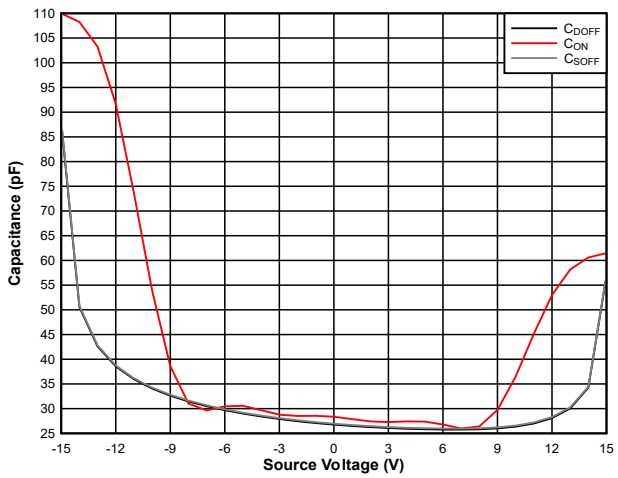


Figure 15-11. Capacitance vs Source or Drain Voltage

16 Parameter Measurement Information

16.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 16-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

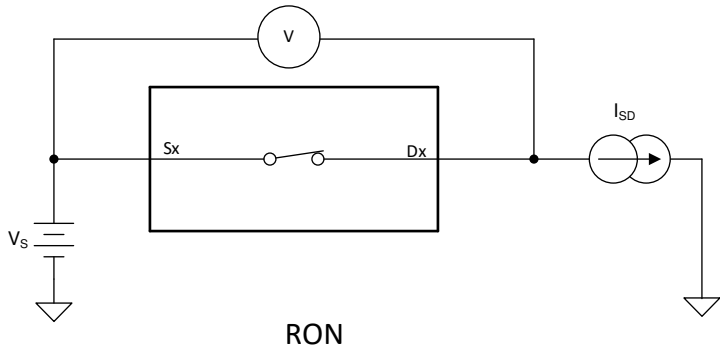


Figure 16-1. On-Resistance Measurement Setup

16.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 16-2 shows the setup used to measure both off-leakage currents.

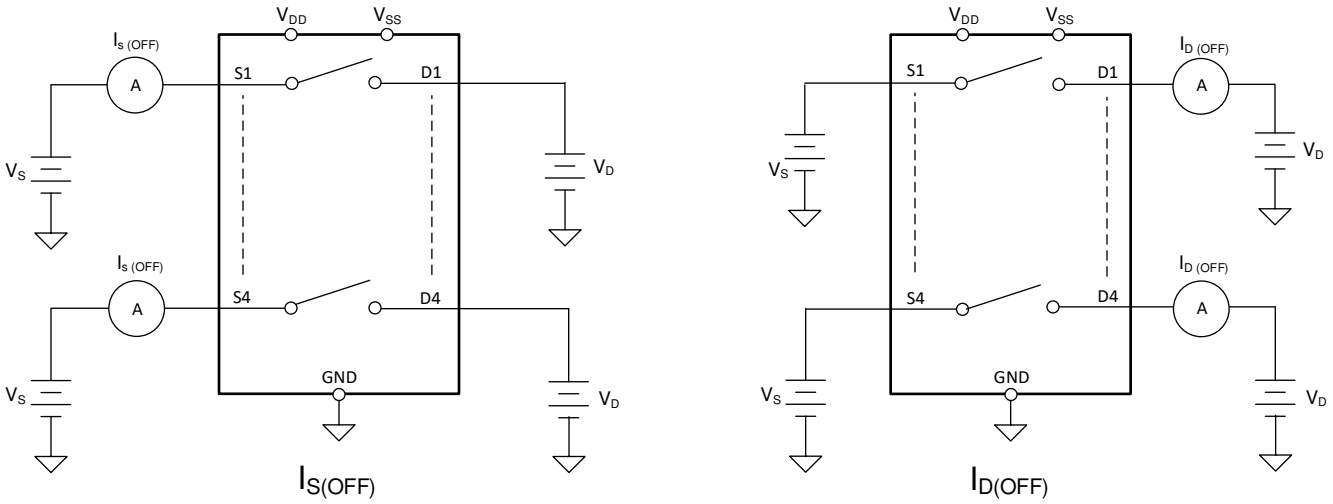


Figure 16-2. Off-Leakage Measurement Setup

16.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 16-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

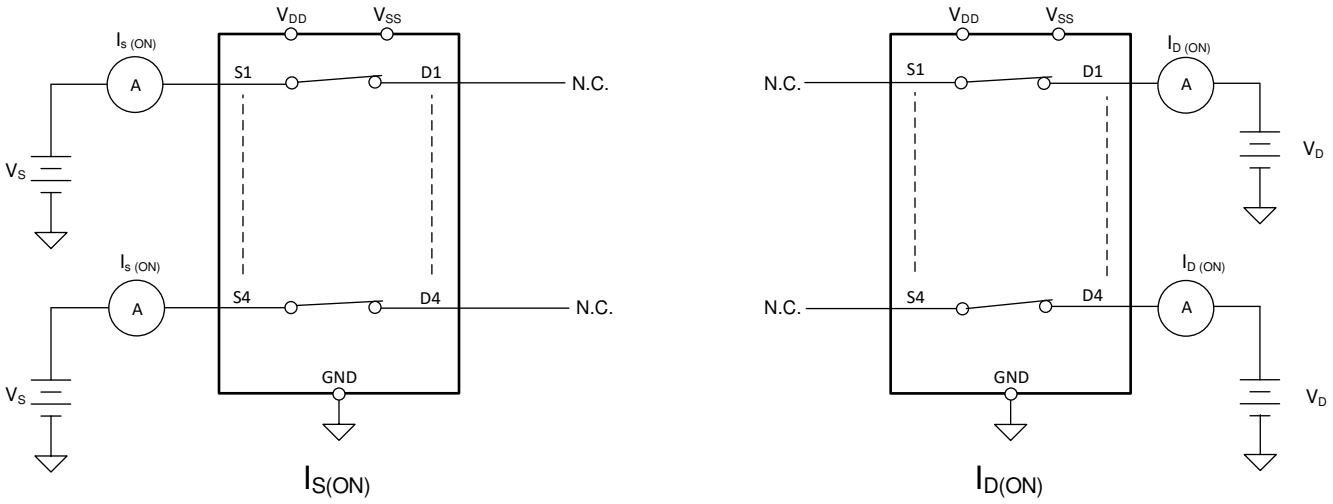


Figure 16-3. On-Leakage Measurement Setup

16.4 t_{ON} and t_{OFF} Time

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 16-4 shows the setup used to measure turn-on time, denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 16-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF}.

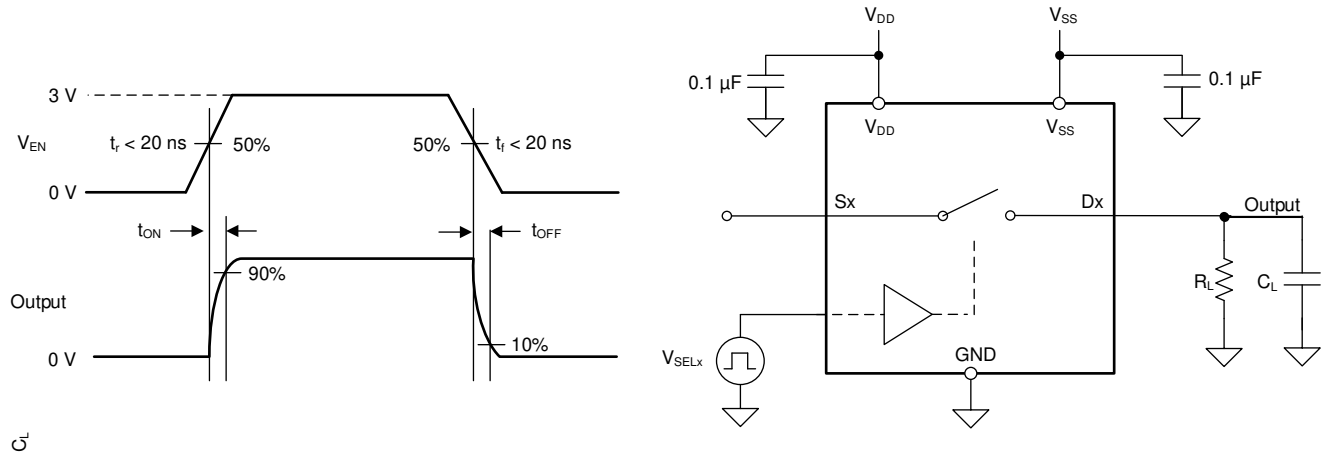


Figure 16-4. Turn-On and Turn-Off Time Measurement Setup

16.5 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 16-5 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

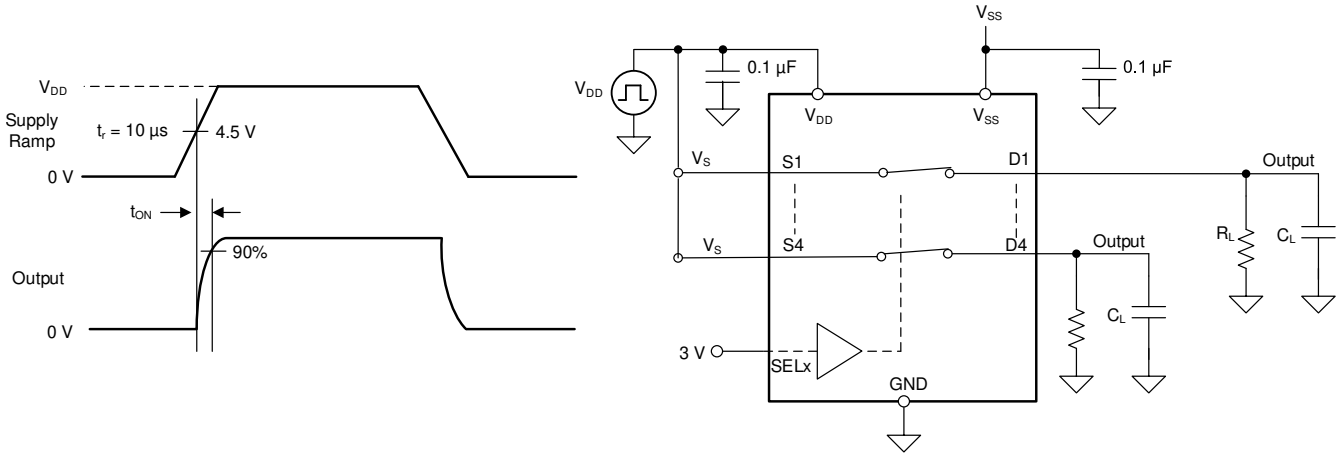


Figure 16-5. $t_{ON\ (VDD)}$ Time Measurement Setup

16.6 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 16-6 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

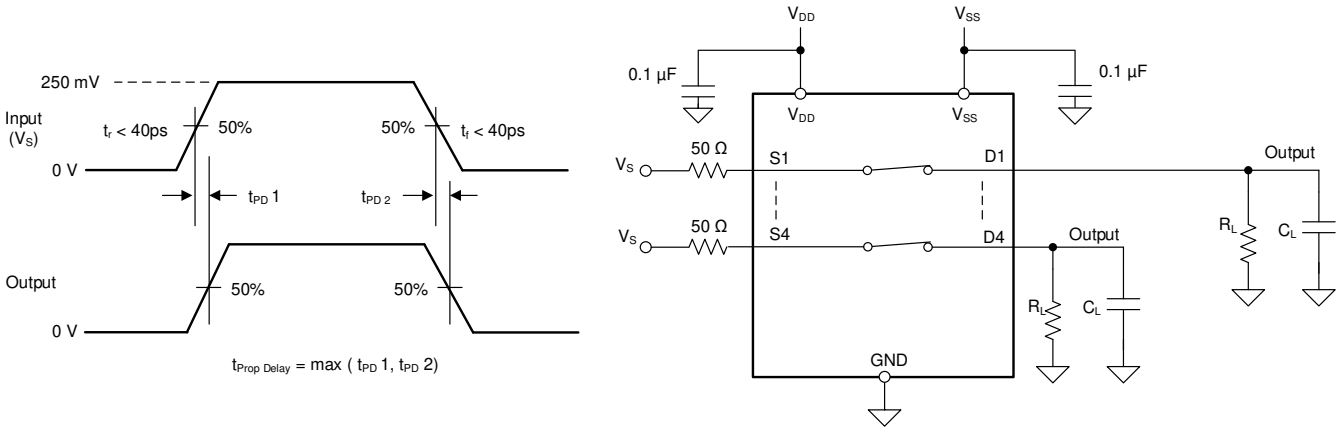


Figure 16-6. Propagation Delay Measurement Setup

16.7 Charge Injection

The TMUX6612-Q1 devices have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 16-7 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

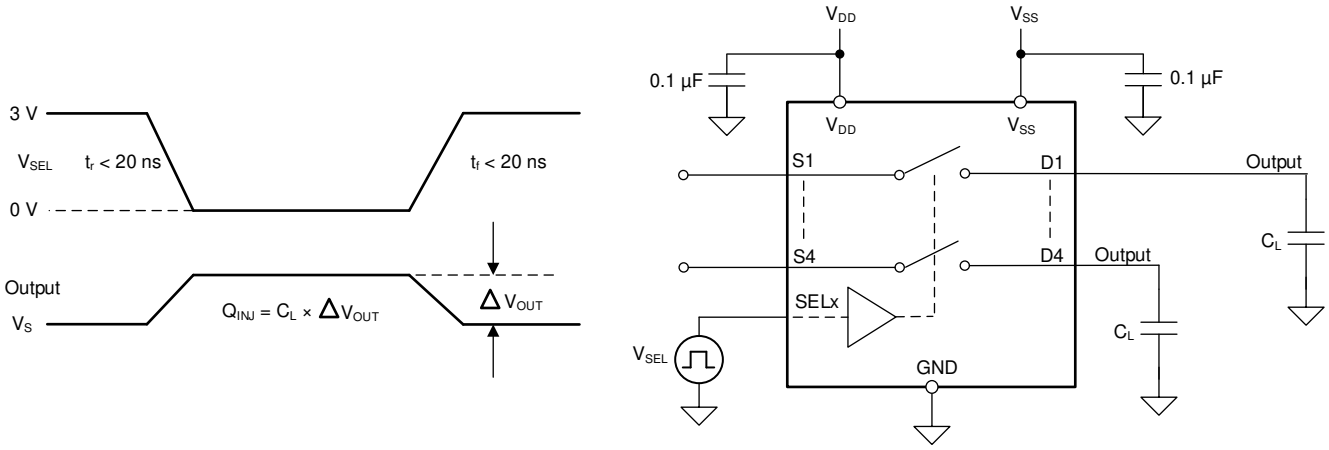
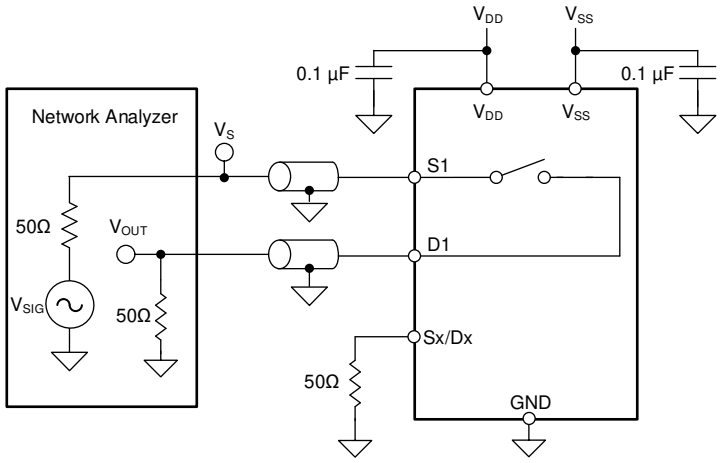


Figure 16-7. Charge-Injection Measurement Setup

16.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 16-8 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

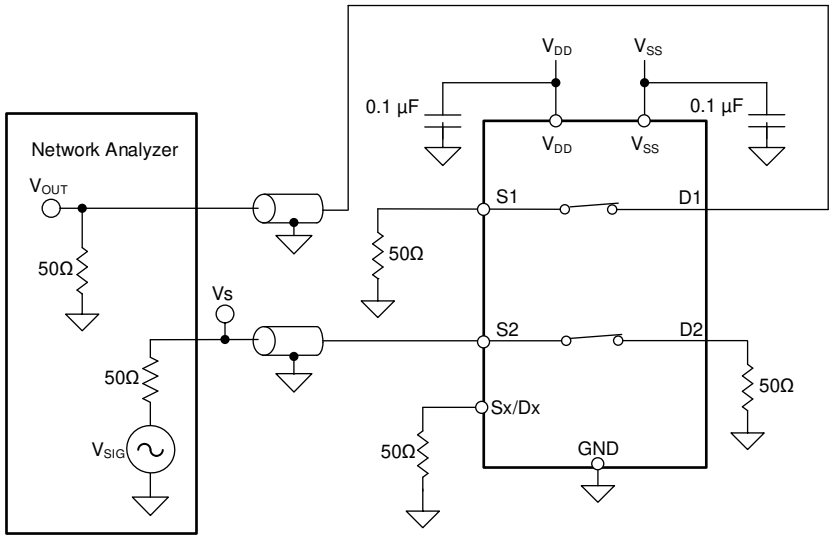


$$Off\ Isolation = 20 \times Log\frac{V_{OUT}}{V_S}$$

Figure 16-8. Off Isolation Measurement Setup

16.9 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 16-9 shows the setup used to measure, and the equation used to compute crosstalk.

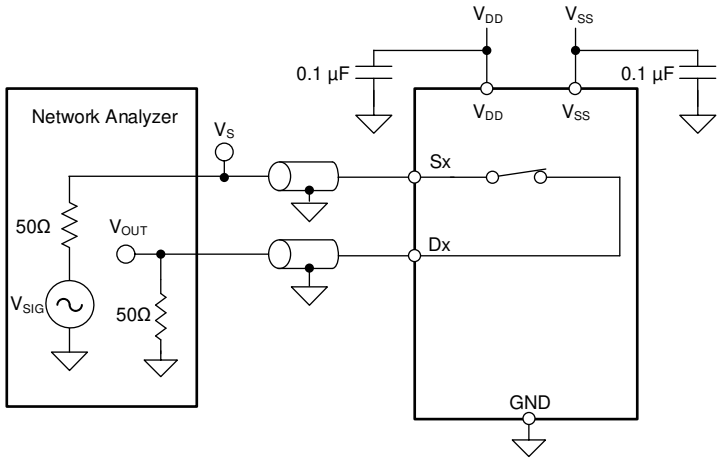


$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 16-9. Channel-to-Channel Crosstalk Measurement Setup

16.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 16-10 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 16-10. Bandwidth Measurement Setup

16.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

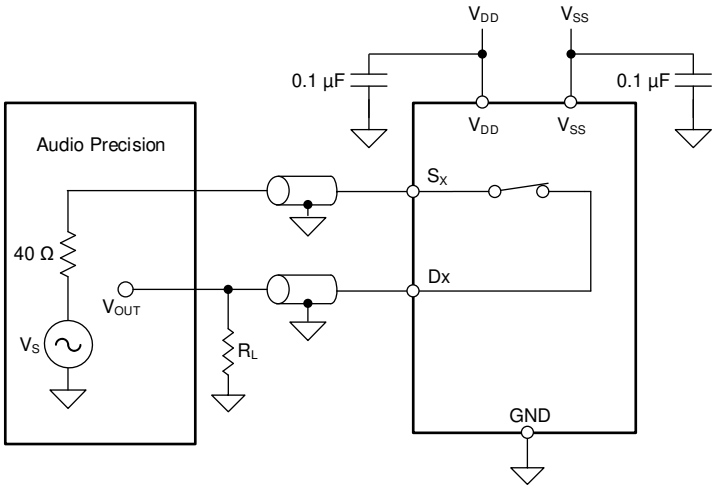
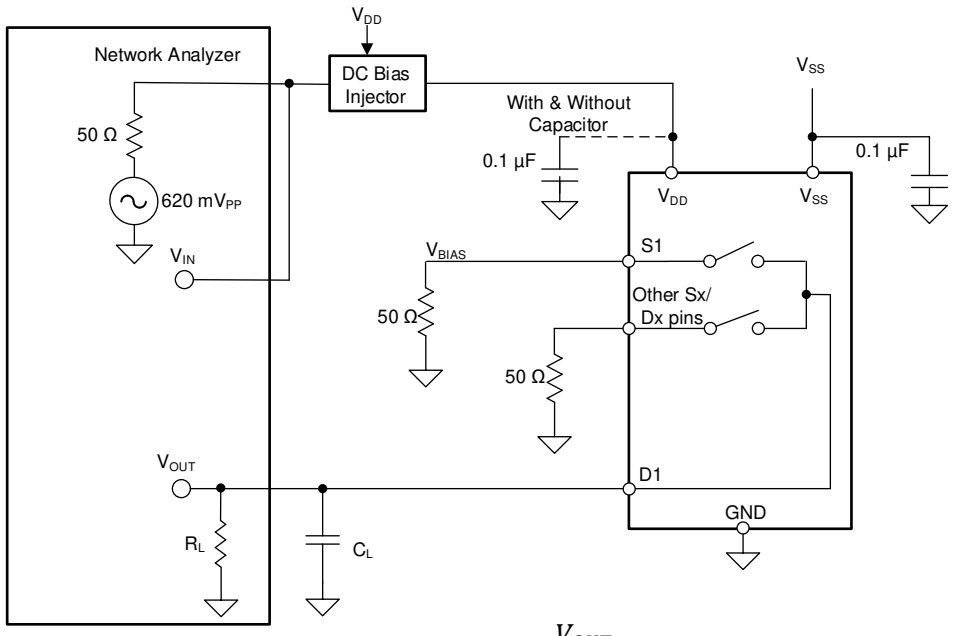


Figure 16-11. THD + N Measurement Setup

16.12 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100mV$_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.



$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

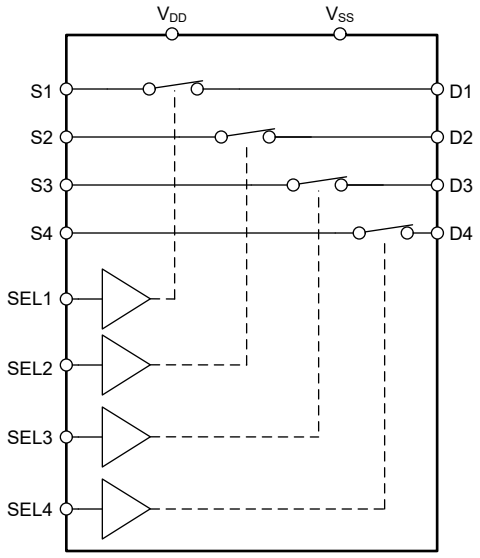
Figure 16-12. AC PSRR Measurement Setup

17 Detailed Description

17.1 Overview

TMUX6612-Q1 is a 1:1 (SPST), 4-channel switch. This device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. This device works well with dual supplies, a single supply, or asymmetric supplies such as V_{DD} = 20V, V_{SS} = –10V.

17.2 Functional Block Diagram



TMUX6612-Q1
(SELx = Logic 1)

17.3 Feature Description

17.3.1 Bidirectional Operation

The TMUX6612-Q1 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

17.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX6612-Q1 ranges from 0V to 30V.

17.3.3 1.8V Logic Compatible Inputs

The TMUX6612-Q1 has 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX6612-Q1 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

17.3.4 Flat On-Resistance

The TMUX6612-Q1 is designed with a special switch architecture to produce ultra-flat on-resistance (RON) across most of the switch input operating region. The flat RON response allows the device to be used in precision applications since the RON is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so unwanted noise is not produced from the device to affect sampling accuracy.

This architecture also keeps RON the same regardless of the supply voltage. The flattest on-resistance region extends roughly from 5V above VSS to 5V below VDD. As long as this headroom is maintained, the TMUX6612-Q1 exhibits an extremely linear response.

17.3.5 Power-Up Sequence Free

The TMUX6612-Q1 supports any power up sequencing. With the supply rails (VDD and VSS), any rail can be powered on first. Similarly, when powering down the supply rails can be powered down in any order.

17.4 Device Functional Modes

The TMUX6612-Q1 has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins operate down to 1.8V logic and can be as high as 36V.

The TMUX6612-Q1 devices can be operated without any external components except for the supply decoupling capacitors. The SELx pins have internal pull-down resistors.

17.4.1 Truth Tables

Table 17-1 provides the truth table for TMUX6612-Q1.

Table 17-1. TMUX6612-Q1 Truth Table

SEL x (1)	CHANNEL x
0	Channel x OFF
1	Channel x ON

(1) x denotes 1, 2, 3, or 4 for the corresponding channel.

18 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

18.1 Application Information

The TMUX6612-Q1 is a part of the precision switches and multiplexers family of devices. The device operates with dual supplies (±4.5V to ±20V), a single supply (4.5V to 36V), or asymmetric supplies (such as V_{DD} = 20V, V_{SS} = –10V), and offers output signal ranges up to 30V. The TMUX6612-Q1 offers a low R_{ON}, low on and off leakage currents and ultra-low charge injection performance. These features make the TMUX6612-Q1 a great option for high-performance and high-voltage automotive applications.

18.2 Design Requirements

For this design example, use the parameters listed in Table 18-1.

Table 18-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	15V
Supply (V_{SS})	- 15V
Input / Output signal range	-12V to 12V
Control logic thresholds	1.8V compatible

18.3 Detailed Design Procedure

TMUX6612-Q1 can be used to expand the functionality of an EV Charging station to an additional connector or outlet that follows the same communication and hardware protocols (such as NACS and CCS1). The input signal is a ±12V differential, and requires the switch to have low R_{ON} and handle the full voltage range with minimal changes in resistance on a ±15V supply. For this application the 4 channel 1:1 switch is reconfigured into a 2 channel 2:1 by connecting D1 and D3 to outlet 1 then D2 and D4 to outlet 2. Then S1:S2 is shorted for differential Plus while S3:S4 is shorted for differential Minus. Shorting Sel1:Sel3 and Sel2:Sel4 allows for the device to be controlled with only two GPIOs. Sel1:Sel3 selects outlet 1 and Sel2:Sel4 selects outlet 2. This device can support 1.8V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX6612-Q1 can be operated without any external components except for the supply decoupling capacitors. The select pins have an internal pull-down resistor to prevent floating input logic. The TMUX6612-Q1 supports asymmetric supply rails within a 40V differential, and down to 4.5V on the positive supply. For this design, the signal range must stay within the supply rails of the device and at or below 30V V_{DS}.

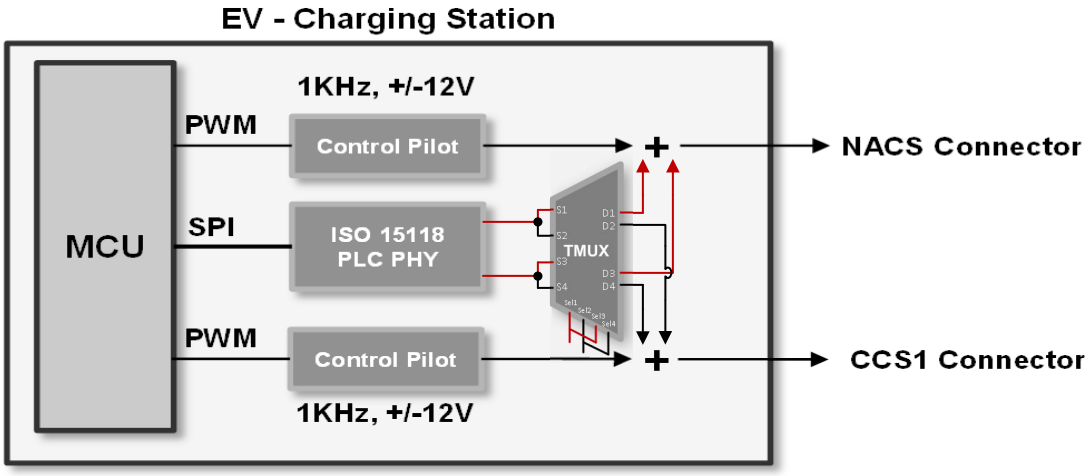


Figure 18-1. EV Charging Station Application

18.4 Application Curve

TMUX6612-Q1 has excellent flatness across the signal range; however, entering within 5V of either supply rail results in a slightly increased on-resistance. Figure 18-2 shows an example of what the on-resistance looks like across a +/-12V signal range using +/-15V supply rails. For this application, the small increase within the headroom is still acceptable.

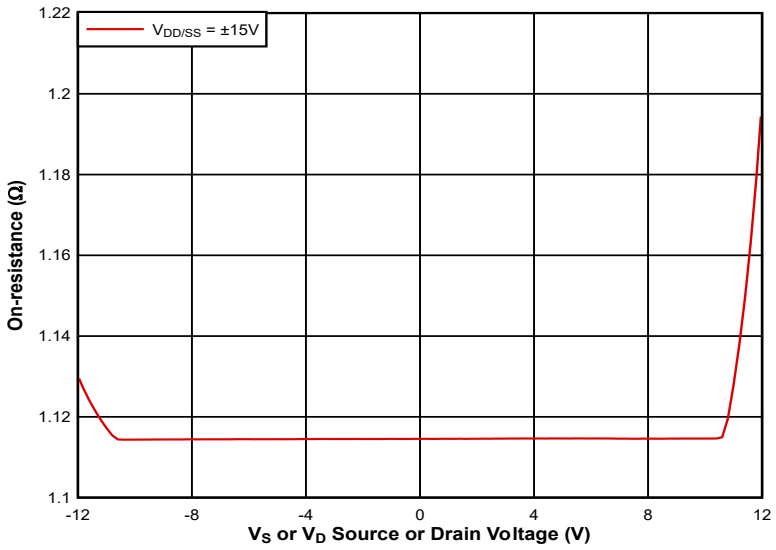


Figure 18-2. Ron Profile

18.5 Thermal Considerations

For analog switches in many applications, several 100mA of current needs to be supported through the switch (from source to drain, or NO/NC to COM). Many devices already have a maximum current specified based on ambient temperature, but if a device specifies with junction temperature or to calculate for a specific use case (temperature, supply voltage, channels in parallel), use the following equations and scheme.

There are 2 main limitations to this maximum current:

1. Inherent metal limitations of the device
2. Thermal self-heating limitations

The following information is needed to calcualate maximum current for a specific setup:

- T_A = maximum ambient temperature
- $R_{\Theta JA}$ = package thermal coefficients
- R_{ON} = on resistance
- n = number of channels in parallel
- Limitations on maximum current based on junction temperature from the data sheet

Below is an example using TMUX6612-Q1 specifications:

Device maximum T_J=150°C

$R_{\Theta JA}$=99.3 °C/W

While operating with 4 channels in parallel at ±15V, assume R_{ON} = 1.8Ω by taking the maximum specified value at T_A = 105°C. Use T_J = 125°C. Using the following equation, calculate the maximum thermal limitation.

$$I = \sqrt{\frac{T_J - T_A}{R_{\theta JA} \times R_{ON} \times n}} \quad (1)$$

The current calculated from this example is 0.167A, so only a maximum of 0.167A can pass through each of the 4 channels in parallel. If only running with one channel then the equation outputs 0.334A, but due to the inherent metal limitation take the lower of the value calculated and the value provided in the maximum current table based on T_J in the data sheet, which is 0.143A.

Similarly, calculate the T_J and total power dissipated in these examples with the following equations. Note there is some small power dissipated from the supply current consumption of the device, which is ignored here.

$$T_J = R_{\theta JA} \times I^2 \times R_{ON} \times n + T_A \quad (2)$$

$$P_{total} = \frac{T_J - T_A}{R_{\theta JA}} \quad (3)$$

Pulse current can be calculated the same way, but using the duty cycle, d. Typically, pulse current is specified at a 10% duty cycle; however, do not exceed the maximum current provided in the pulse current table even with a shorter duty cycle.

$$I = \frac{1}{d}\sqrt{\frac{T_J - T_A}{R_{\theta JA} \times R_{ON} \times n}} \quad (4)$$

$$T_J = R_{\theta JA} \times (d \times I)^2 \times R_{ON} \times n + T_A \quad (5)$$

18.6 Power Supply Recommendations

The TMUX6612-Q1 device operates across a wide supply range of ±4.5V to ±20V (4.5V to 36V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 20V and V_{SS} = –10V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer improved noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always make sure a solid ground (GND) connection is established before supplies are ramped.

18.7 Layout

18.7.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 18-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

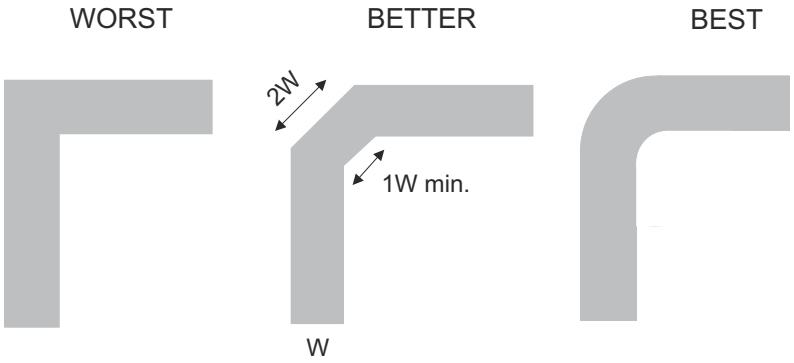


Figure 18-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 18-4 shows an example of a PCB layout with the TMUX6612-Q1.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD/VSS and GND. We recommend a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

18.7.2 Layout Example

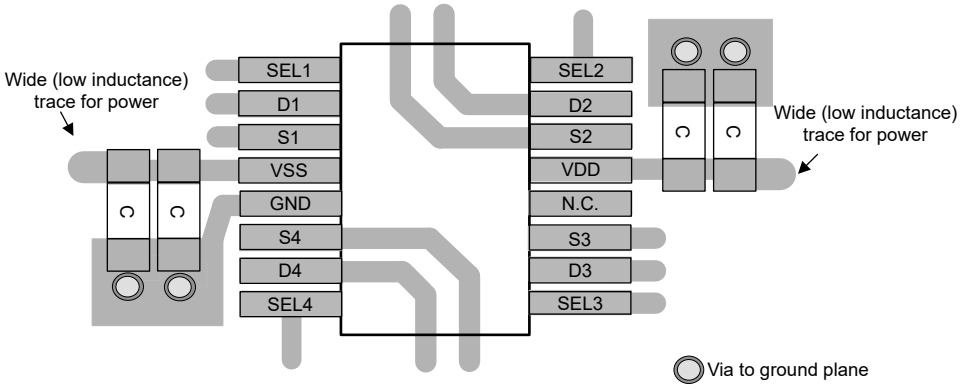


Figure 18-4. TMUX6612-Q1 Layout Example

19 Device and Documentation Support

19.1 Documentation Support

19.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *When to Replace a Relay with a Multiplexer* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

19.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

19.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

19.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

19.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

19.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

20 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial Release

21 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX6612PWRQ1	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6612Q
TMUX6612PWRQ1.A	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6612Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

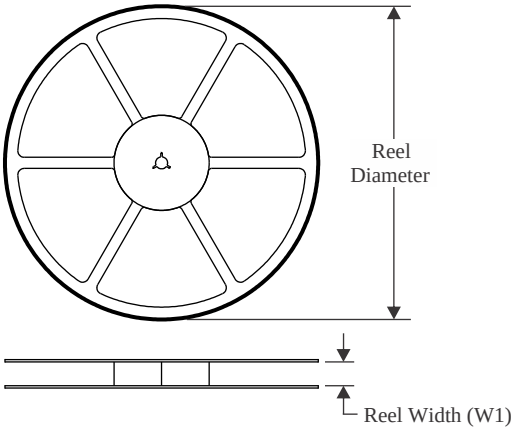
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

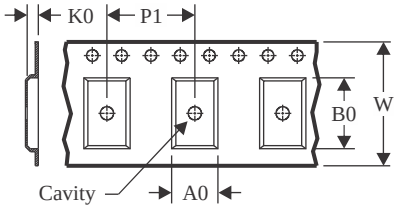
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

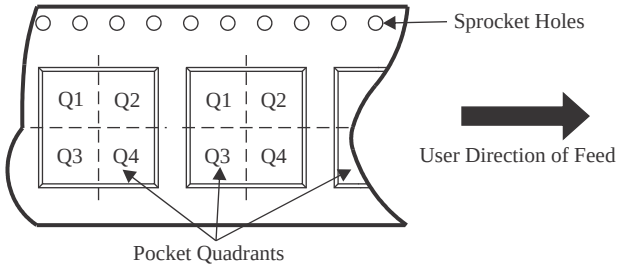


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

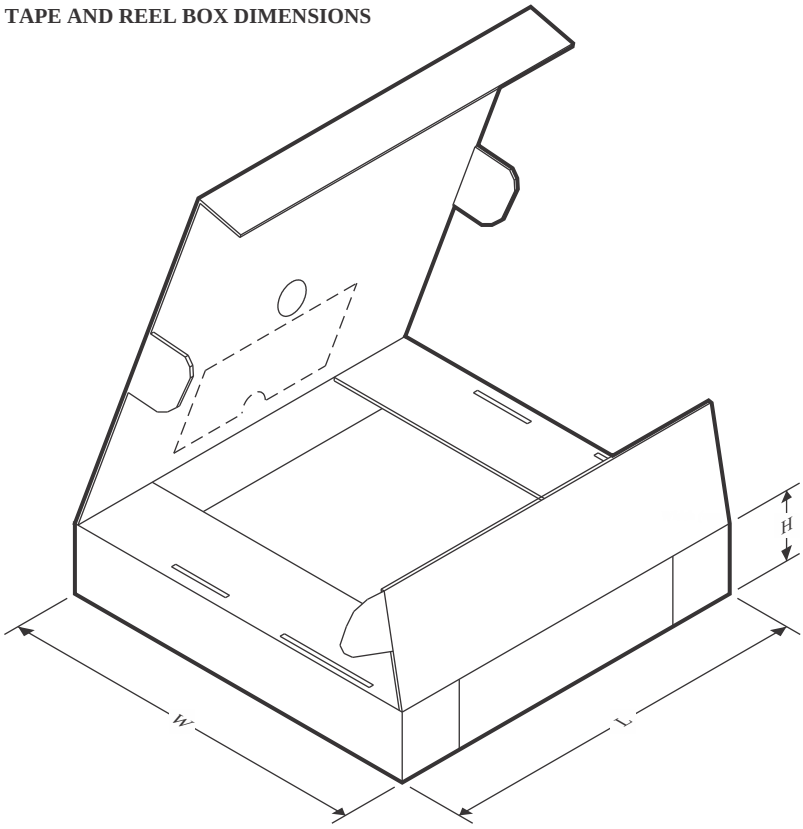
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6612PWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

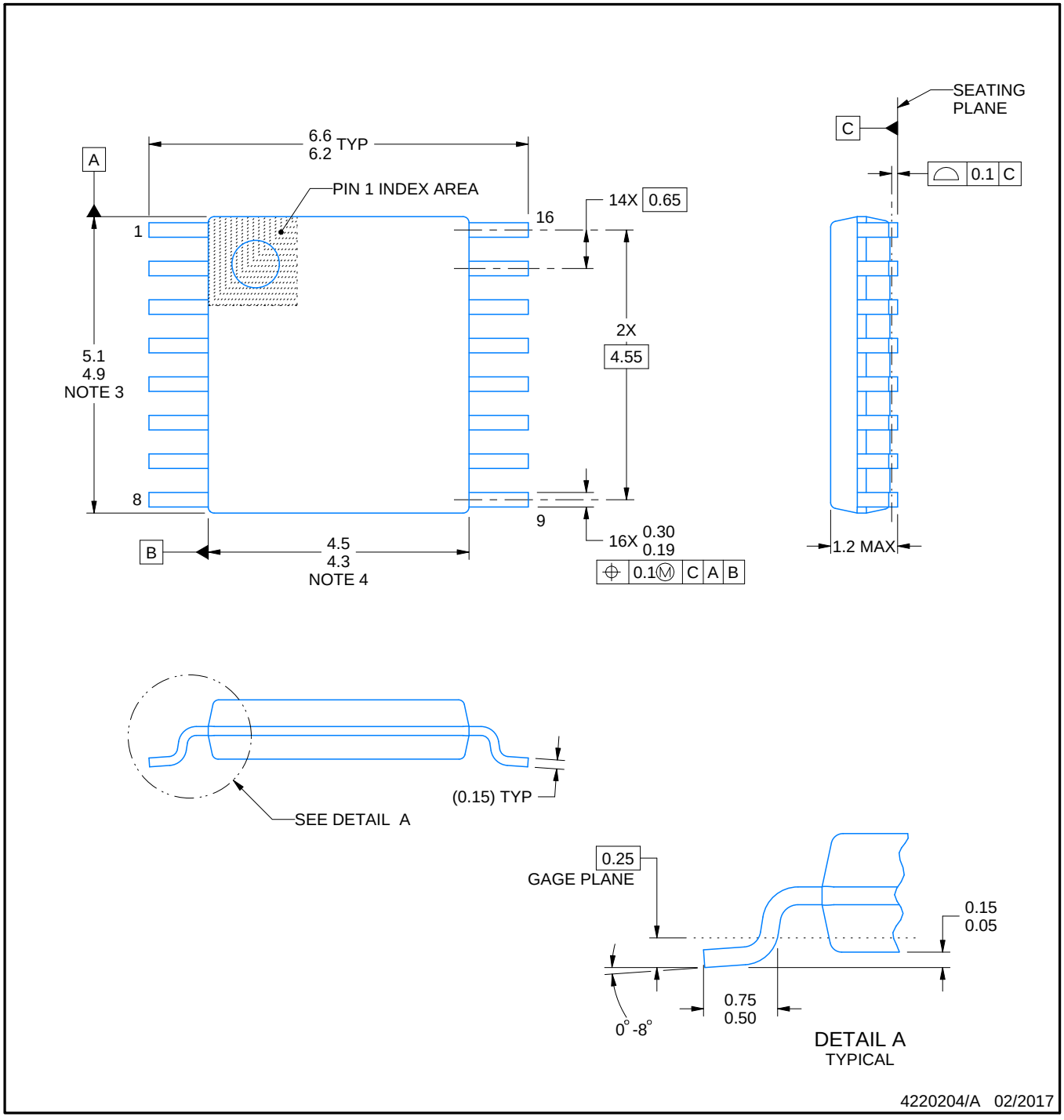
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6612PWRQ1	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

PW0016A

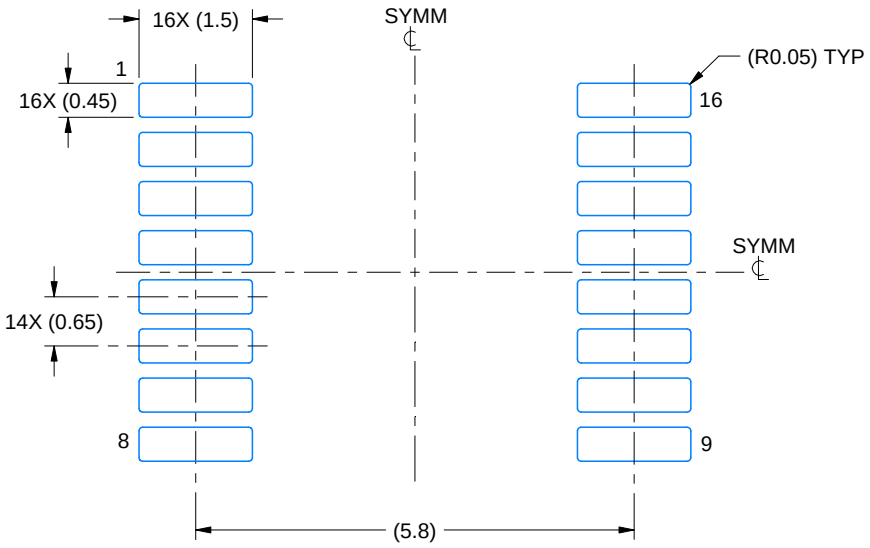
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

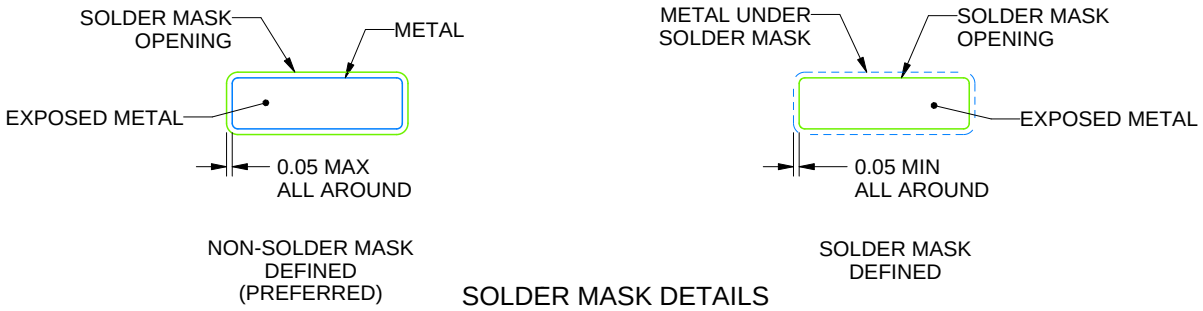


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

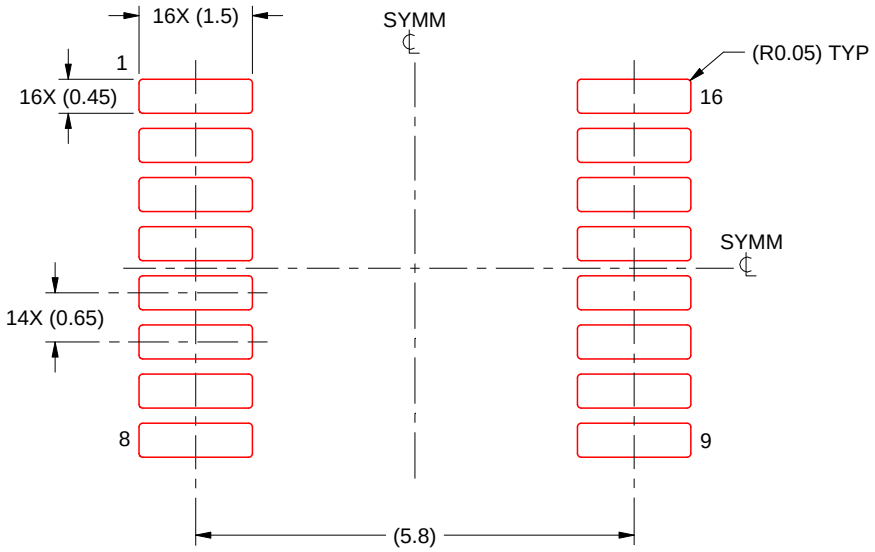


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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