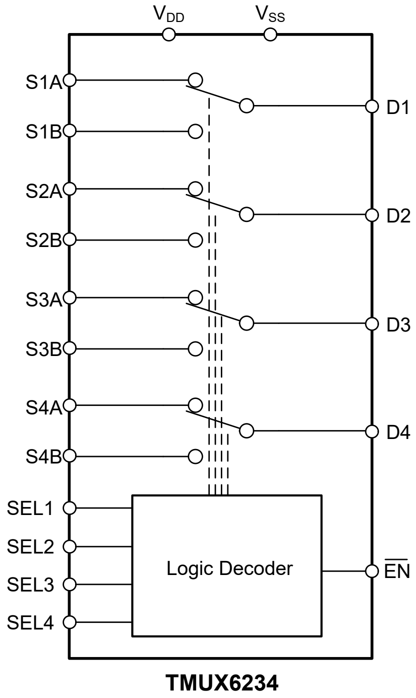
TMUX6234 36V, Low Ron, 2:1, 4 Channel Precision Switches with 1.8V Logic

1 Features

- Dual supply range: ±4.5V to ±18V
- Single supply range: 4.5V to 36V
- Low on-resistance: 3.6Ω
- Low crosstalk: –105dB
- Low propagation delay: 450ps
- High current support: 400mA (maximum)
- –40°C to +125°C operating temperature
- 1.8V logic compatible inputs
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional signal path
- Break-before-make switching

2 Applications

- Remote radio units (RRU)
- Active antenna system mMIMO (AAS)
- Programmable logic controllers (PLC)
- Analog input modules
- Semiconductor test equipment
- Battery test equipment
- Data acquisition systems (DAQ)
- Ultrasound scanners
- Patient monitoring and diagnostics
- Optical networking
- Optical test equipment
- Wired networking



Simplified Diagram

3 Description

The TMUX6234 is a multi-channel CMOS switch with low on-resistance. The TMUX6234 contains four independently controlled SPDT switches with an $\overline{\text{EN}}$ pin to enable or disable all four channels. The device supports single supply (4.5V to 36V), dual supplies (±4.5V to ±18V), or asymmetric supplies (such as V_{DD} = 18V and V_{SS} = –5V). The TMUX6234 supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from V_{SS} to V_{DD}.

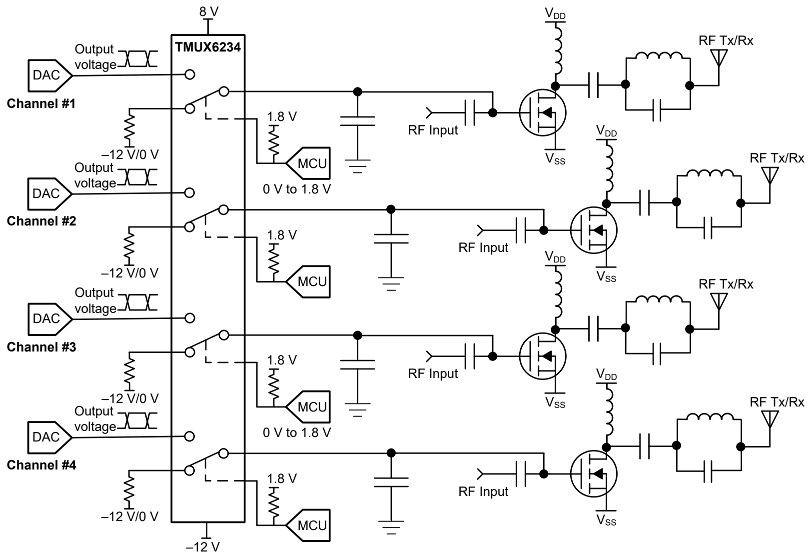
All logic control input pins support logic levels from 1.8V to V_{DD}, ensuring logic compatibility when operating with a wide range of logic voltages. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

The TMUX6234 is part of the precision switches and multiplexers family of devices. These devices have very low on and off leakage currents and low charge injection, allowing them to be used in high precision measurement applications.

Package Information

PART NUMBER	PACKAGE[1]	BODY SIZE (NOM)
TMUX6234	PW (TSSOP, 20)	6.50 mm × 4.40 mm
	RRQ (WQFN, 20)	4.00 mm × 4.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



Typical Application

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4 Pin Configuration and Functions

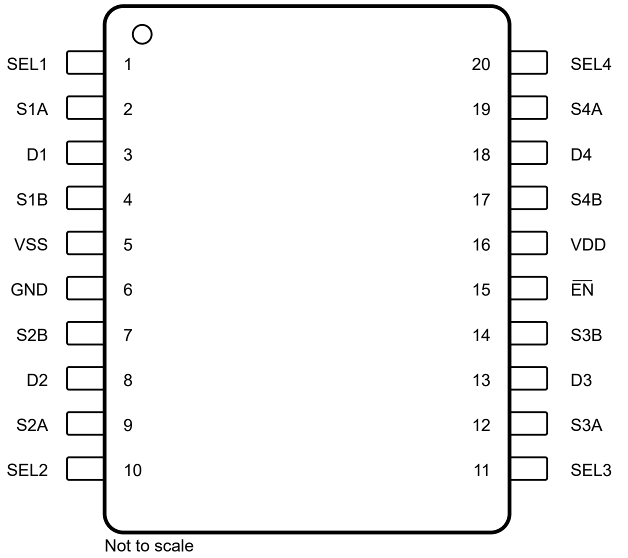


Figure 4-1. TMUX6234 PW Package, 20-Pin TSSOP (Top View)

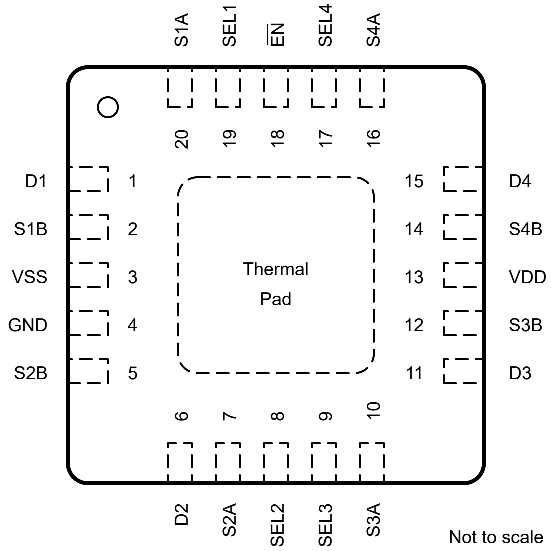


Figure 4-2. TMUX6234 RRQ Package, 20-Pin WQFN (Top View)

Table 4-1. Pin Functions TMUX6234

PIN			TYPE[(1)]	DESCRIPTION [(2)]
NAME	PW NO.	RRQ NO.		
D1	3	1	I/O	Drain pin 1. Can be an input or output.
D2	8	6	I/O	Drain pin 2. Can be an input or output.
D3	13	11	I/O	Drain pin 3. Can be an input or output.
D4	18	15	I/O	Drain pin 4. Can be input or output
$\overline{\text{EN}}$	15	18	I	Active low logic enable; has internal pull-down resistor. The SELx logic inputs determine switch connections when this pin is low (see Section 7.5).
GND	6	4	P	Ground (0 V) reference.
S1A	2	20	I/O	Source pin 1A. Can be an input or output.
S1B	4	2	I/O	Source pin 1B. Can be an input or output.
S2A	9	7	I/O	Source pin 2A. Can be an input or output.
S2B	7	5	I/O	Source pin 2B. Can be an input or output.
S3A	12	10	I/O	Source pin 3A. Can be an input or output.
S3B	14	12	I/O	Source pin 3B. Can be an input or output.
S4A	19	16	I/O	Source pin 4A. Can be an input or output.
S4B	17	14	I/O	Source pin 4B. Can be an input or output.
SEL1	1	19	I	Logic control input 1; has internal pull-down resistor. Controls switch 1 (see Section 7.5).
SEL2	10	8	I	Logic control input 2; has internal pull-down resistor. Controls switch 2 (see Section 7.5).
SEL3	11	9	I	Logic control input 3; has internal pull-down resistor. Controls switch 3 (see Section 7.5).
SEL4	20	17	I	Logic control input 4, has internal pull-down resistor. Controls switch 4 (see Section 7.5).
VDD	16	13	P	Positive power supply. This pin has the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND.
VSS	5	3	P	Negative power supply. This pin has the most negative power-supply potential. This pin can be connected to ground in single supply applications. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VSS and GND for reliable operation.
Thermal Pad			—	The thermal pad is not connected internally. There is no requirement to solder this pad. If connected, it is recommended to leave the pad floating or tied to GND.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to Section 7.4 for what to do with unused pins.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
V_{DD}–V_{SS}	Supply voltage		38	V
V_{DD}		–0.5	38	V
V_{SS}		–38	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx, $\overline{EN}$)	–0.5	38	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx, $\overline{EN}$)	–30	30	mA
V_S or V_D	Source or drain voltage (SxA, SxB, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current[3]	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (SxA, SxB, Dx)		I_{DC} ± 10 %[4]	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (QFN package)[5]		1680	mW

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearily above T_A = 70°C by 24.8mW/°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		TMUX6234		UNIT
		PW (TSSOP)	RRQ (WQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.7	40.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	19.9	24.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.3	16.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.7	16.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ (1)	Power supply voltage differential	4.5		36	V
V_{DD}	Positive power supply voltage	4.5		36	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (SxA, SxB, Dx)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		36	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (SxA, SxB, Dx)			I_{DC} (2)	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ ($V_{DD} - V_{SS}$) ≤ 36 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	TEST CONDITIONS				
PW (TSSOP)	±15 V Dual Supply(1)	360	235	130	mA
	+36 V Single Supply	345	225	128	mA
	+12 V Single Supply	260	177	108	mA
	±5 V Dual Supply	255	175	105	mA
	+5 V Single Supply	170	129	80	mA
RRQ (WQFN)	±15 V Dual Supply(1)	400	230	120	mA
	+36 V Single Supply	300	190	110	mA
	+12 V Single Supply	300	180	100	mA
	±5 V Dual Supply	300	180	100	mA
	+5 V Single Supply	240	150	85	mA

(1) Specified for nominal supply voltage only.

5.6 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		3.6	6.2	Ω
			–40°C to +85°C			7.9	Ω
			–40°C to +125°C			9.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 30 V I_S = –10 mA Refer to On-Resistance	25°C		1.6	1.8	Ω
			–40°C to +85°C			2.5	Ω
			–40°C to +125°C			3.1	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 18 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to Section 6.2	25°C	–0.4	0.02	0.4	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–15		15	nA
$I_{D(OFF)}$	Drain off leakage current[1]	Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to Section 6.2	25°C	–0.5	0.04	0.5	nA
			–40°C to +85°C	–8		8	nA
			–40°C to +125°C	–30		30	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	Switch state is on V_S = V_D = 30 V or 1 V Refer to Section 6.3	25°C	–0.5	0.04	0.5	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–30		30	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 36 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		65	100	µA
			–40°C to +85°C			110	µA
			–40°C to +125°C			130	µA

(1) When V_S is 30 V, V_D is 1 V. Or when V_S is 1 V, V_D is 30 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

5.7 36 V Single Supply: Switching Characteristics

V_{DD} = +36 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		90	170	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			200	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		95	180	ns
			–40°C to +85°C			200	ns
			–40°C to +125°C			210	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		85	150	ns
			–40°C to +85°C			160	ns
			–40°C to +125°C			170	ns
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		40		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1μs R_L = 300 Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.15		ms
			–40°C to +85°C		0.15		ms
			–40°C to +125°C		0.15		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 6.8	25°C		560		ps
Q_{INJ}	Charge injection	V_D = 18 V, C_L = 100 pF Refer to Section 6.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		95		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to Section 6.14	25°C		–46		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} =18 V, V_{BIAS} = 18 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to Section 6.13	25°C		0.0006		%
$C_{S(OFF)}$	Source off capacitance	V_S = 18 V, f = 1 MHz	25°C		17		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 18 V, f = 1 MHz	25°C		28		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 18 V, f = 1 MHz	25°C		77		pF

5.8 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		3.6	5.5	Ω
			–40°C to +85°C			7.1	Ω
			–40°C to +125°C			8.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.3	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA Refer to On-Resistance	25°C		0.4	1.5	Ω
			–40°C to +85°C			1.7	Ω
			–40°C to +125°C			1.9	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Section 6.2	25°C	–0.6	0.01	0.6	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–10		10	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Section 6.2	25°C	–0.8	0.02	0.8	nA
			–40°C to +85°C	–6		6	nA
			–40°C to +125°C	–30		30	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V Refer to Section 6.3	25°C	–0.8	0.02	0.8	nA
			–40°C to +85°C	–6		6	nA
			–40°C to +125°C	–30		30	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		42	70	µA
			–40°C to +85°C			80	µA
			–40°C to +125°C			95	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		8	25	µA
			–40°C to +85°C			30	µA
			–40°C to +125°C			40	µA

(1) When V_S is positive, V_D is negative. Or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

5.9 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		105	190	ns
			–40°C to +85°C			200	ns
			–40°C to +125°C			210	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		105	190	ns
			–40°C to +85°C			200	ns
			–40°C to +125°C			210	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		80	150	ns
			–40°C to +85°C			160	ns
			–40°C to +125°C			170	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1μs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.16		ms
			–40°C to +125°C		0.16		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 6.8	25°C		450		ps
Q_{INJ}	Charge injection	V_D = 0 V, C_L = 100 pF Refer to Section 6.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		100		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to Section 6.14	25°C		–48		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to Section 6.13	25°C		0.0004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		16		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		28		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		77		pF

5.10 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		6.2	12	Ω
			–40°C to +85°C			15	Ω
			–40°C to +125°C			18	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.3	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			1	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA Refer to On-Resistance	25°C		2.4	3.6	Ω
			–40°C to +85°C			3.9	Ω
			–40°C to +125°C			4.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.025		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Section 6.2	25°C	–0.4	0.01	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–8		8	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Section 6.2	25°C	–0.5	0.02	0.5	nA
			–40°C to +85°C	–6		6	nA
			–40°C to +125°C	–30		30	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to Section 6.3	25°C	–0.5	0.02	0.5	nA
			–40°C to +85°C	–6		6	nA
			–40°C to +125°C	–30		30	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		33	60	µA
			–40°C to +85°C			70	µA
			–40°C to +125°C			80	µA

(1) When V_S is 10 V, V_D is 1 V. Or when V_S is 1 V, V_D is 10 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

5.11 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		105	210	ns
			–40°C to +85°C			230	ns
			–40°C to +125°C			260	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		110	210	ns
			–40°C to +85°C			230	ns
			–40°C to +125°C			260	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		105	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			250	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		60		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.16		ms
			–40°C to +125°C		0.16		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 6.8	25°C		500		ps
Q_{INJ}	Charge injection	V_D = 6 V, C_L = 100 pF Refer to Section 6.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		130		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.5		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to Section 6.14	25°C		–48		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to Section 6.13	25°C		0.0016		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		19		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		33		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		78		pF

5.12 ±5 V Dual Supply: Electrical Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –4.5 V to +4.5 V I_D = –10 mA Refer to On-Resistance	25°C		7	13.5	Ω
			–40°C to +85°C			16.2	Ω
			–40°C to +125°C			18.5	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –4.5 V to +4.5 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –4.5 V to +4.5 V I_D = –10 mA Refer to On-Resistance	25°C		2.6	3.8	Ω
			–40°C to +85°C			4.2	Ω
			–40°C to +125°C			4.9	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is off V_S = +4.5 V / –4.5 V V_D = –4.5 V / + 4.5 V Refer to Section 6.2	25°C	–0.5	0.01	0.5	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–5		5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is off V_S = +4.5 V / –4.5 V V_D = –4.5 V / + 4.5 V Refer to Section 6.2	25°C	–0.5	0.01	0.5	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–8		8	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is on V_S = V_D = ±4.5 V Refer to Section 6.3	25°C	–0.5	0.01	0.5	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–8		8	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.6	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = +5.5 V, V_{SS} = –5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		28	45	µA
			–40°C to +85°C			55	µA
			–40°C to +125°C			85	µA
I_{SS}	V_{SS} supply current	V_{DD} = +5.5 V, V_{SS} = –5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		4	10	µA
			–40°C to +85°C			15	µA
			–40°C to +125°C			25	µA

(1) When V_S is positive, V_D is negative. Or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

5.13 ±5 V Dual Supply: Switching Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		120	210	ns
			–40°C to +85°C			230	ns
			–40°C to +125°C			250	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		130	220	ns
			–40°C to +85°C			240	ns
			–40°C to +125°C			260	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Section 6.5	25°C		120	210	ns
			–40°C to +85°C			230	ns
			–40°C to +125°C			250	ns
t_{BBM}	Break-before-make time delay	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		65		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1μs R_L = 300 Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.16		ms
			–40°C to +125°C		0.16		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Section 6.8	25°C		400		ps
Q_{INJ}	Charge injection	V_D = 0 V, C_L = 100 pF Refer to Section 6.9	25°C		1		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–105		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		130		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 10 MΩ , C_L = 5 pF, f = 1 MHz Refer to Section 6.14	25°C		–53		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 5 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to Section 6.13	25°C		0.002		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		20		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		34		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		80		pF

5.14 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

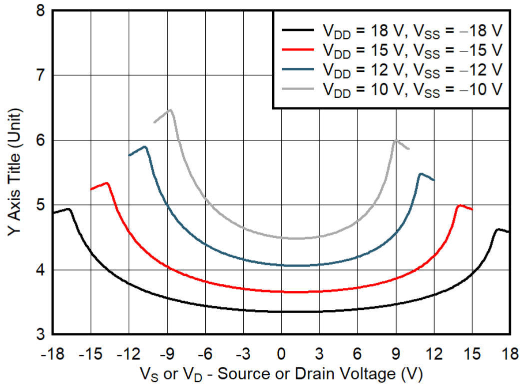


Figure 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply

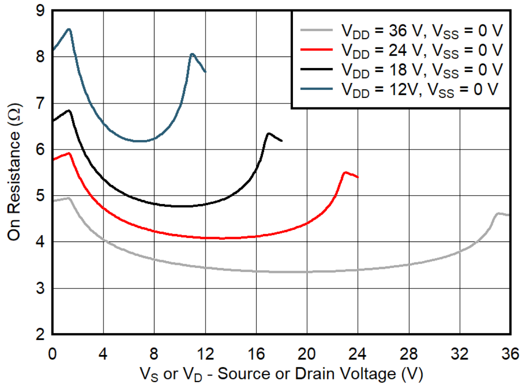
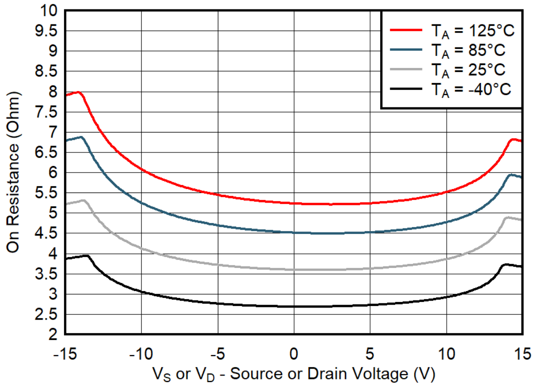
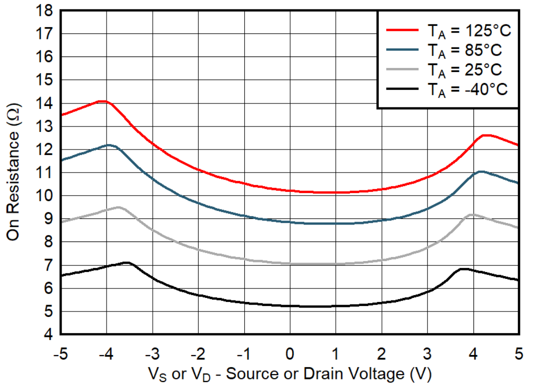


Figure 5-2. On-Resistance vs Source or Drain Voltage – Single Supply



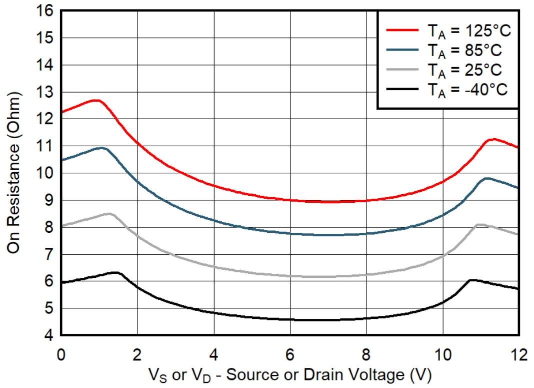
V_{DD} = 15 V, V_{SS} = -15 V

Figure 5-3. On-Resistance vs Temperature



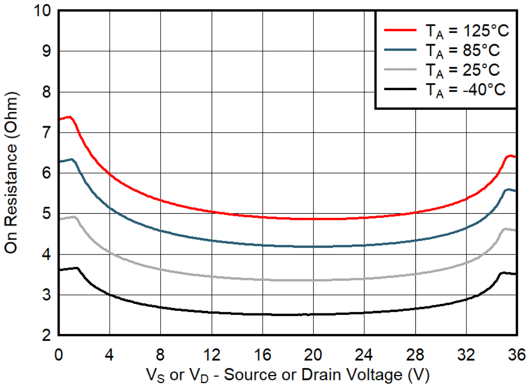
V_{DD} = 5 V, V_{SS} = -5 V

Figure 5-4. On-Resistance vs Temperature



V_{DD} = 12 V, V_{SS} = 0 V

Figure 5-5. On-Resistance vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-6. On-Resistance vs Temperature

5.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

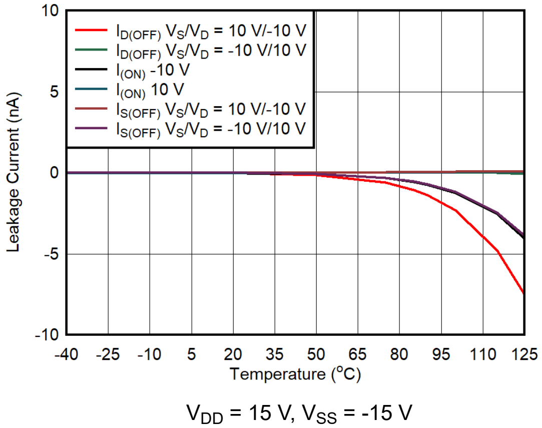


Figure 5-7. Leakage Current vs Temperature

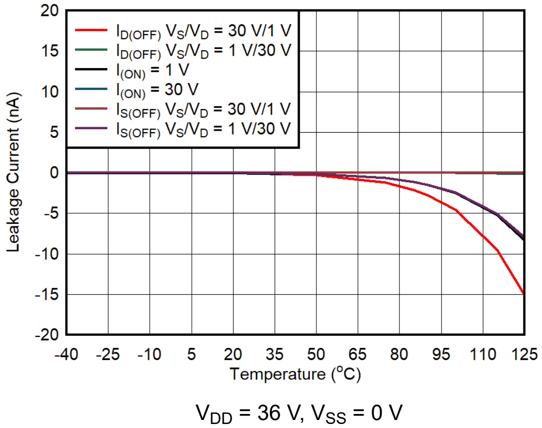


Figure 5-8. Leakage Current vs Temperature

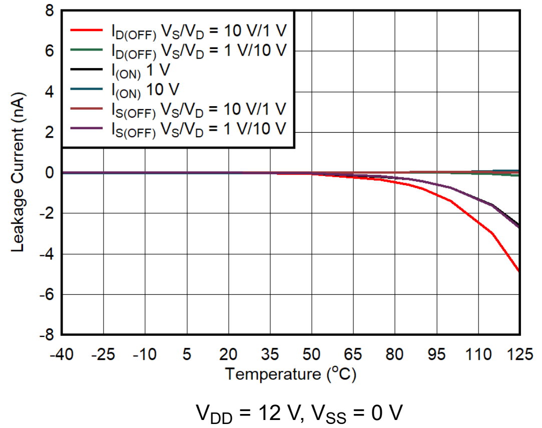


Figure 5-9. Leakage Current vs Temperature

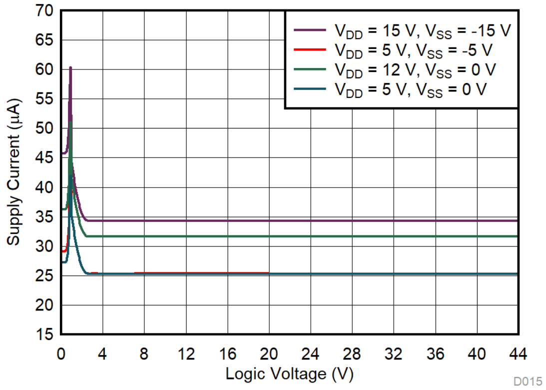


Figure 5-10. Supply Current vs Logic Voltage

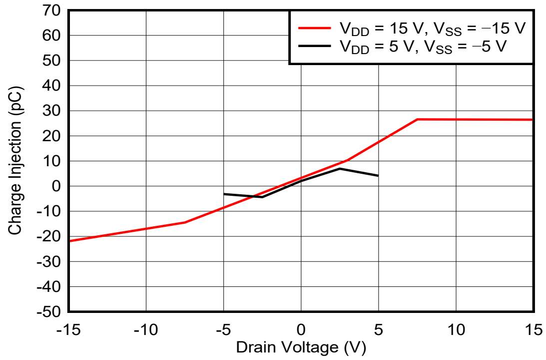


Figure 5-11. Charge Injection vs Source Voltage – Dual Supply

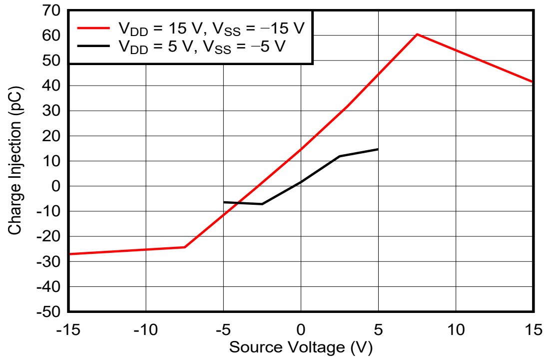


Figure 5-12. Charge Injection vs Drain Voltage – Dual Supply

5.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

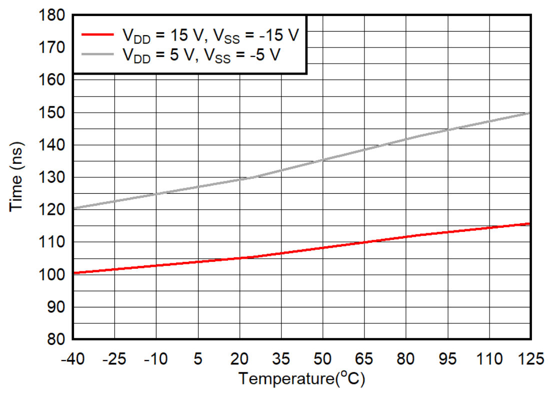
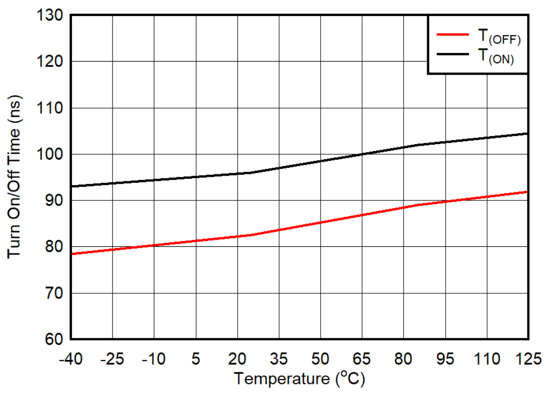
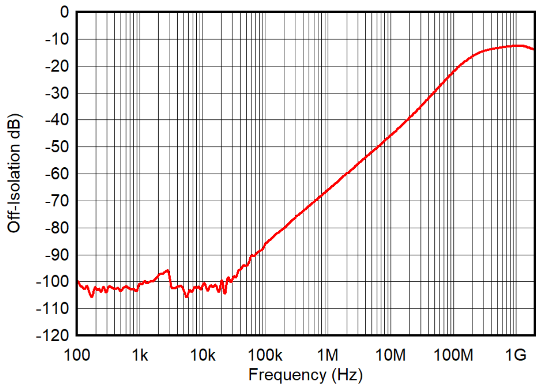


Figure 5-13. $T_{TRANSITION}$ vs Temperature



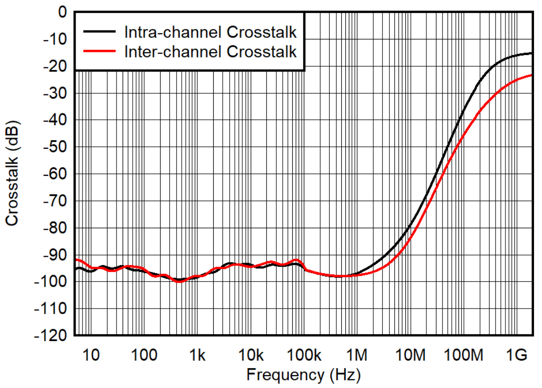
V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-14. T_{ON} and T_{OFF} vs Temperature



V_{DD} = 15 V, V_{SS} = -15 V, T_A = 25°C

Figure 5-15. Off-Isolation vs Frequency



V_{DD} = 15 V, V_{SS} = -15 V

Figure 5-16. Crosstalk vs Frequency

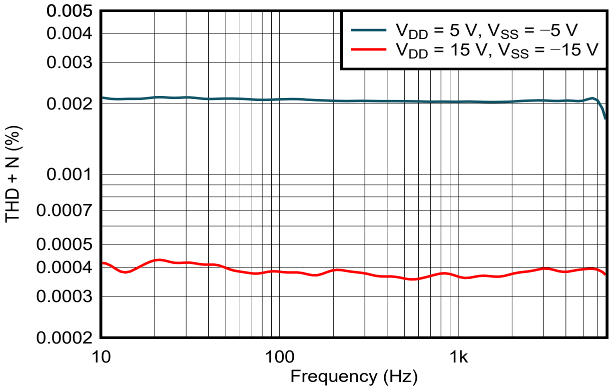


Figure 5-17. THD+N vs Frequency (Dual Supply)

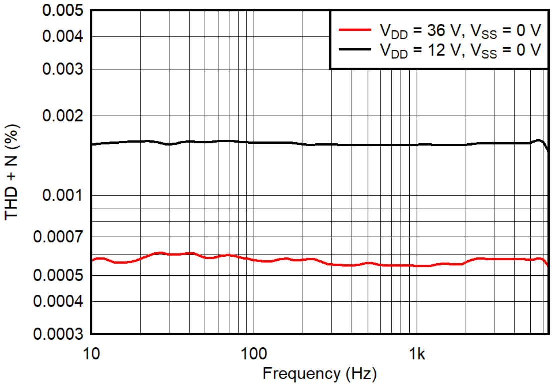
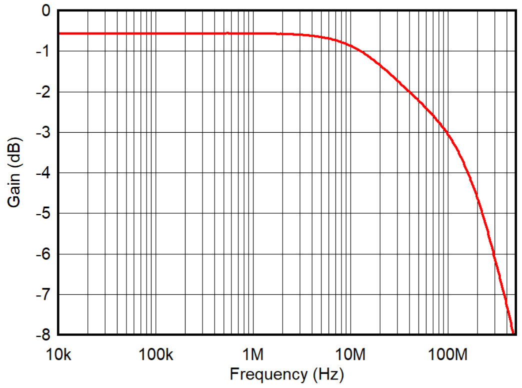


Figure 5-18. THD+N vs Frequency (Single Supply)

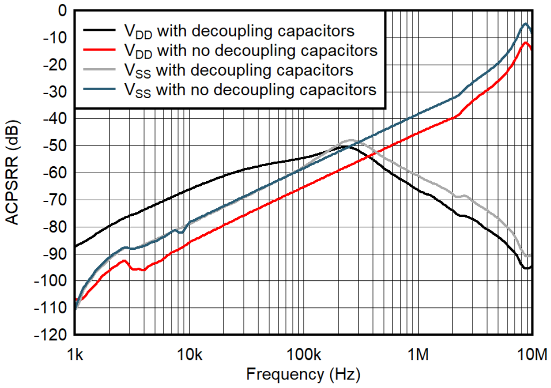
5.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



V_{DD} = 15 V, V_{SS} = -15 V

Figure 5-19. On Response vs Frequency



V_{DD} = +15 V, V_{SS} = -15 V

Figure 5-20. ACPSRR vs Frequency

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

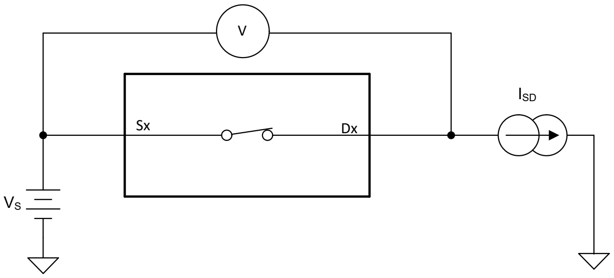


Figure 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

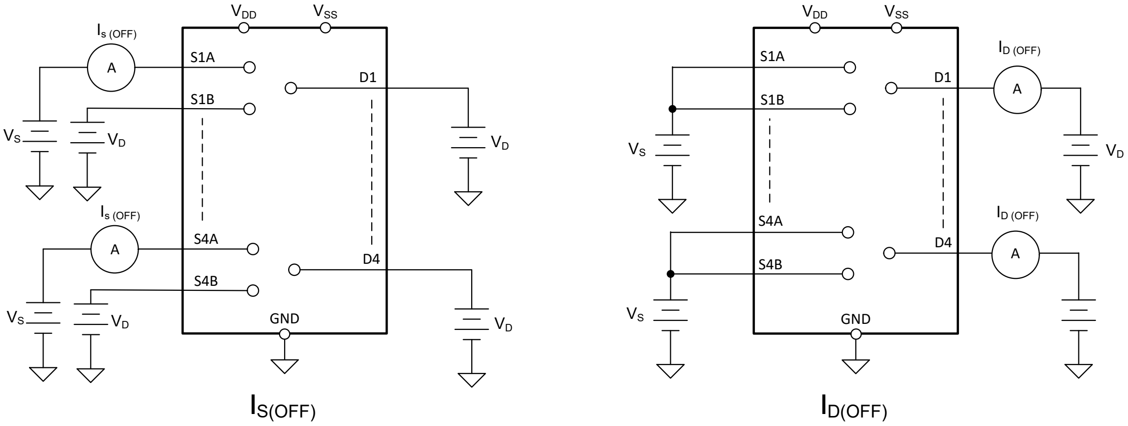


Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

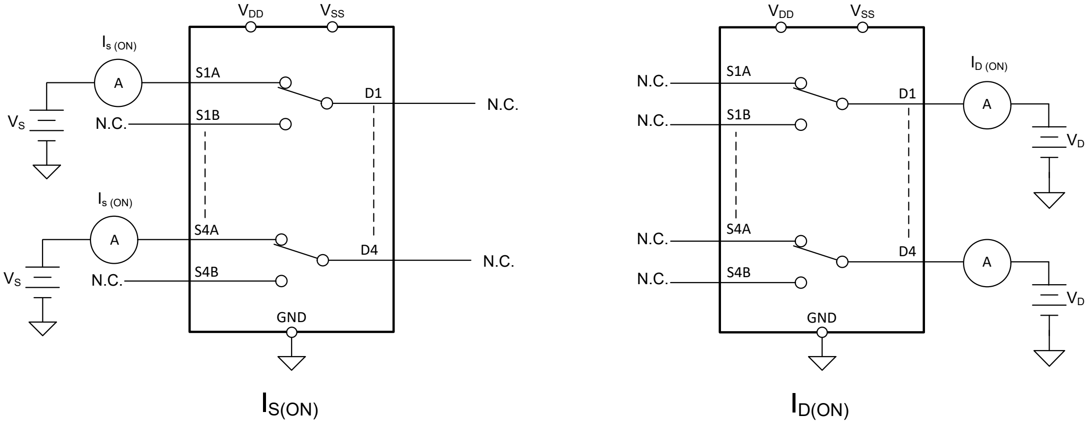


Figure 6-3. On-Leakage Measurement Setup

6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

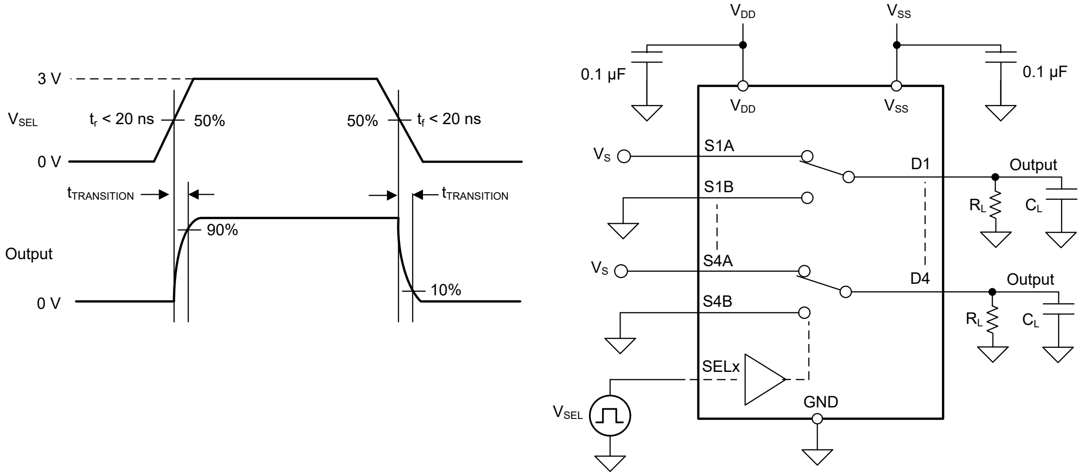


Figure 6-4. Transition-Time Measurement Setup

6.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-5 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-5 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

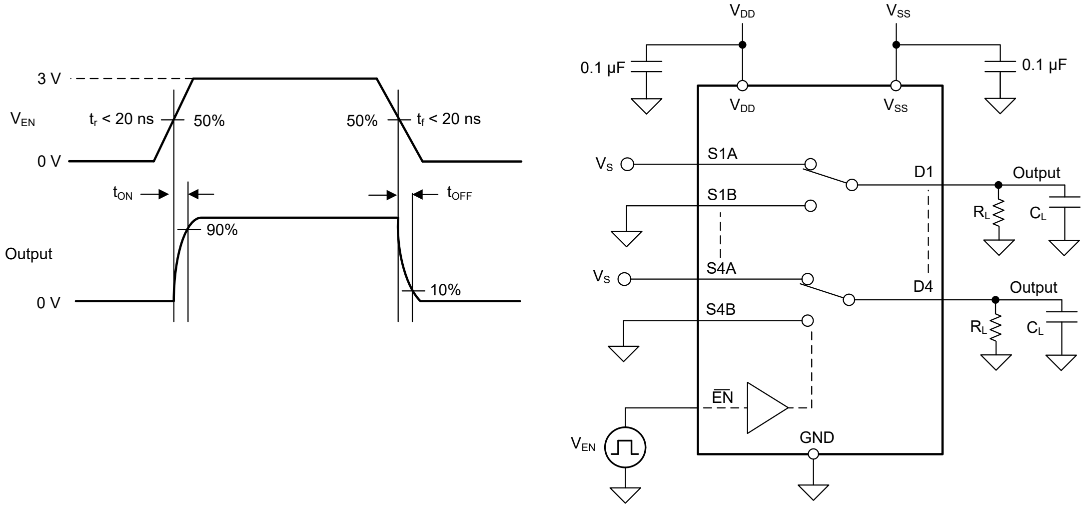


Figure 6-5. Turn-On and Turn-Off Time Measurement Setup

6.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

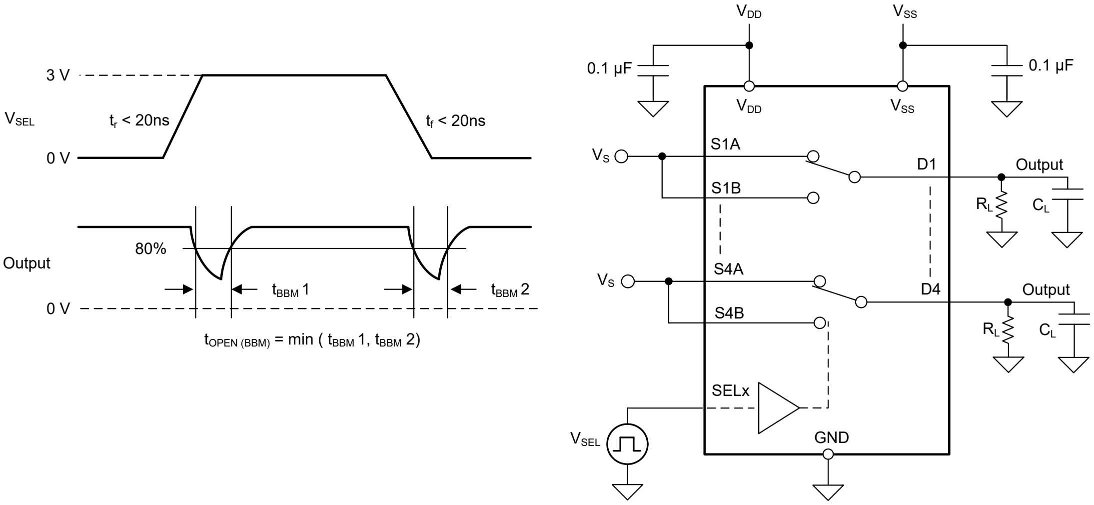


Figure 6-6. Break-Before-Make Delay Measurement Setup

6.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

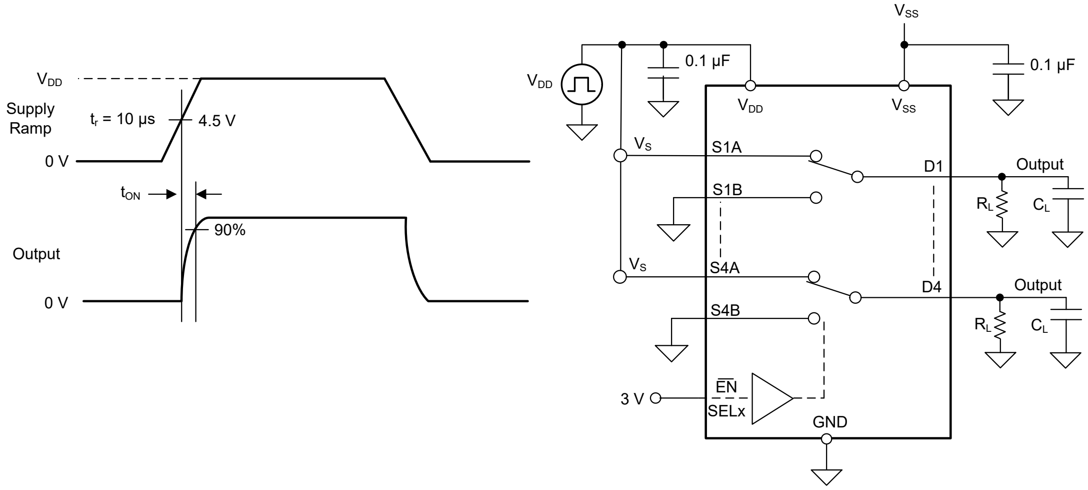


Figure 6-7. $t_{ON\ (VDD)}$ Time Measurement Setup

6.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

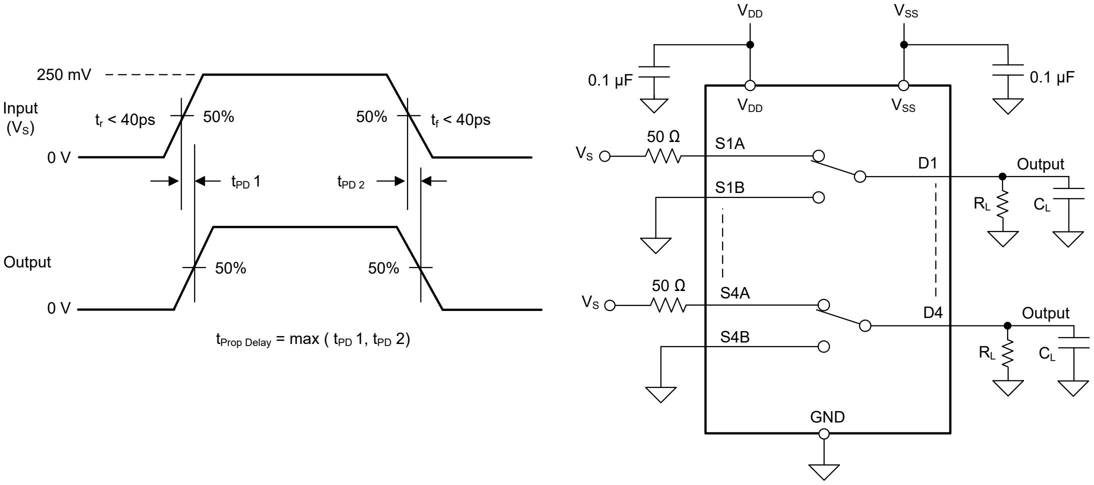


Figure 6-8. Propagation Delay Measurement Setup

6.9 Charge Injection

The TMUX6234 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. Figure 6-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

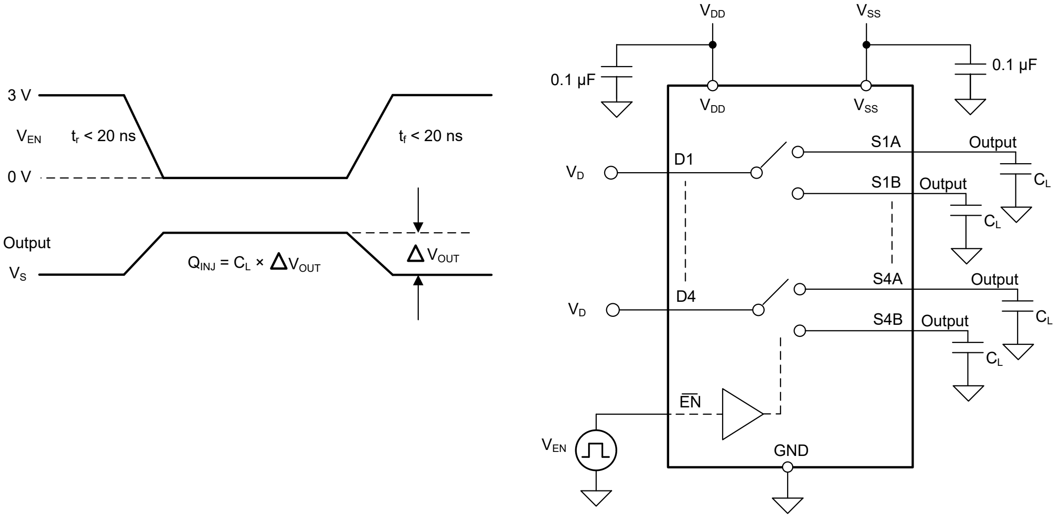


Figure 6-9. Charge-Injection Measurement Setup

6.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-10 shows the setup used to measure, and the equation used to calculate off isolation.

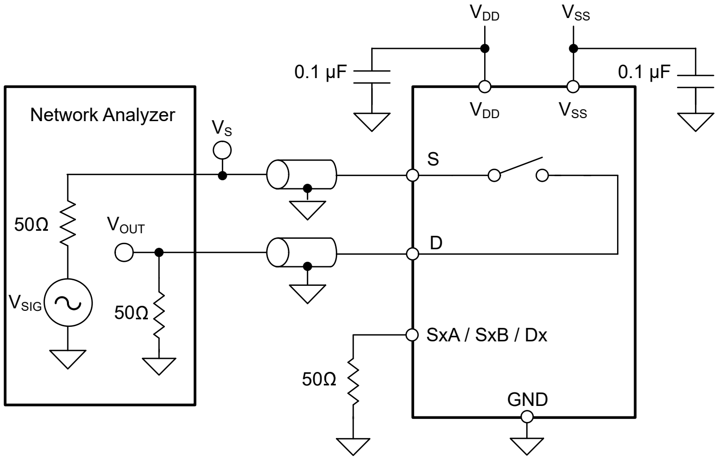


Figure 6-10. Off Isolation Measurement Setup

6.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-11 shows the setup used to measure and the equation used to calculate crosstalk.

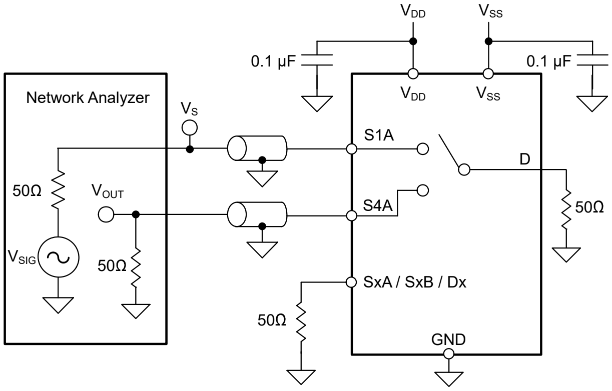


Figure 6-11. Crosstalk Measurement Setup

6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 6-12 shows the setup used to measure bandwidth.

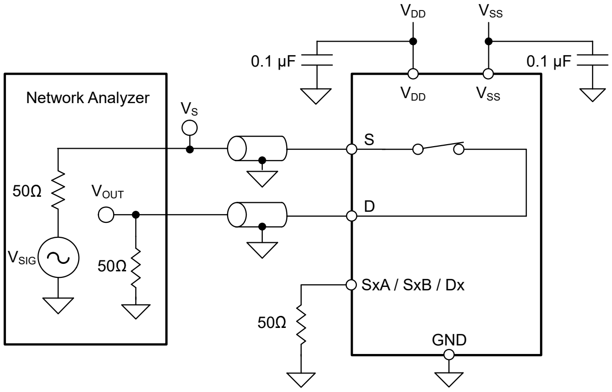


Figure 6-12. Bandwidth Measurement Setup

6.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD.

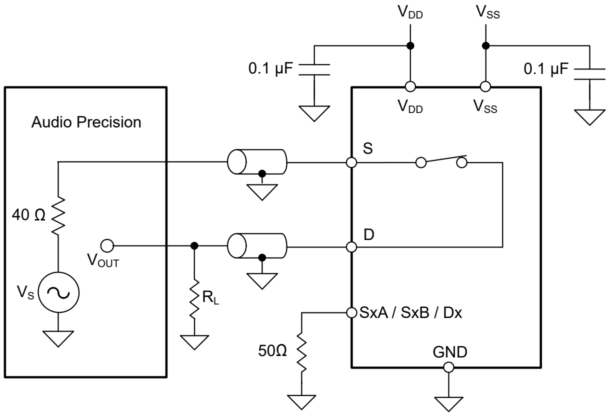


Figure 6-13. THD Measurement Setup

6.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

The below shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.

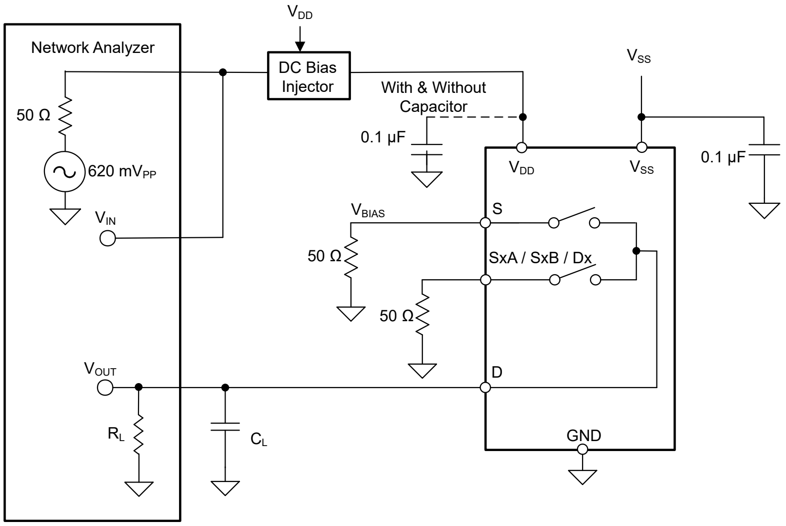


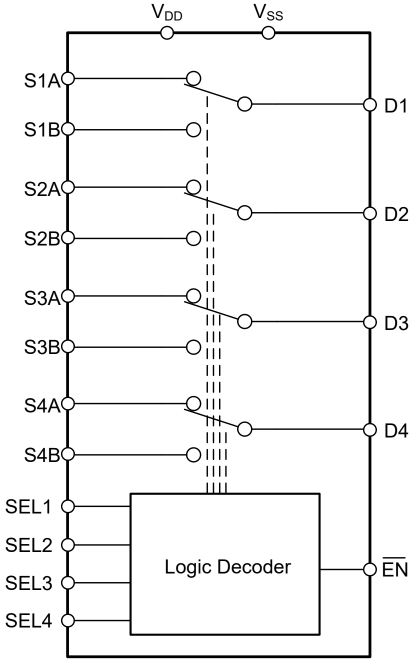
Figure 6-14. ACPSRR Measurement Setup

7 Detailed Description

7.1 Overview

The TMUX6234 contains four independently controlled SPDT switches with an $\overline{EN}$ pin to enable or disable all four switches.

7.2 Functional Block Diagram



TMUX6234

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX6234 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input or output voltage for the TMUX6234 ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX6234 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the switch to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. Refer to *Simplifying Design with 1.8 V logic Muxes and Switches* for more information on 1.8 V logic implementations.

7.3.4 Fail-Safe Logic

TMUX6234 supports Fail-Safe Logic on the control input pins ($\overline{EN}$ and SELx) allowing it to operate up to 36 V, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the TMUX6234 logic input pins to ramp up to +36 V while V_{DD} and V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +36 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

7.3.5 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX62xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX62xx family of switches and multiplexers to be used in harsh environments. Refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability* for more information on latch-up immunity.

7.3.6 Ultra-Low Charge Injection

Figure 7-1 shows how the TMUX6234 has a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

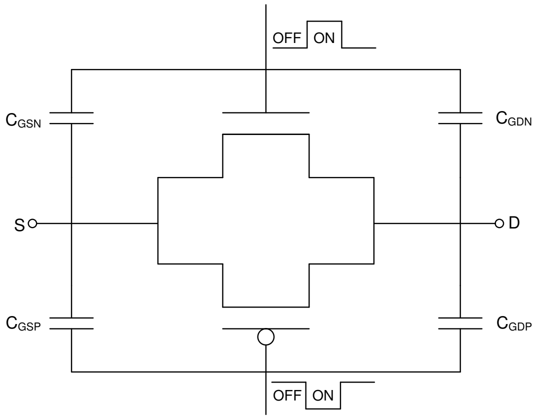


Figure 7-1. Transmission Gate Topology

The TMUX6234 contains specialized architecture to reduce charge injection on the source (Sx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the drain (D). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the drain (D) instead of the source (Sx). As a general rule of thumb, Cp should be 20x larger than the equivalent load capacitance on the source (Sx).

7.4 Device Functional Modes

The enable $\overline{\text{EN}}$ pin is an active-low logic pin that controls the connection between the source (SxA and SxB) and drain (Dx) pins of the device. The TMUX6234 SELx logic control inputs determine which source pin is connected to the drain pin for each channel. When the $\overline{\text{EN}}$ pin of the TMUX6234 is pulled low, the SELx logic control inputs determine which source input is selected. When the $\overline{\text{EN}}$ pin is pulled high, all of the switches are in an open state regardless of the state of the SELx logic control inputs. The control pins can be as high as 36V.

The TMUX6234 can be operated without any external components except for the supply decoupling capacitors. The $\overline{\text{EN}}$ and SELx pins have internal pull-down resistors of 4MΩ. If unused, $\overline{\text{EN}}$ and SELx pins should be tied to GND to ensure the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (Sx or Dx) should be connected to GND.

7.5 Truth Tables

Table 7-1 shows the truth tables for the TMUX6234.

Table 7-1. TMUX6234 Truth Table

$\overline{\text{EN}}$	SEL1	SEL2	SEL3	SEL4	Selected Source Pins Connected to Drain Pins
0	0	X(1)	X	X	S1B to D1
0	1	X	X	X	S1A to D1
0	X	0	X	X	S2B to D2
0	X	1	X	X	S2A to D2
0	X	X	0	X	S3B to D3
0	X	X	1	X	S3A to D3
0	X	X	X	0	S4B to D4
0	X	X	X	1	S4A to D4
1	X	X	X	X	Hi-Z (OFF)

(1) *X* means *do not care*.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX6234 is part of the precision switches and multiplexers family of devices. The TMUX6234 offers low R_{ON}, low on and off leakage currents and low charge injection performance. These features makes the TMUX6234 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

8.2 Typical Application

One application of the TMUX6234 is for input control of a power amplifier gate driver. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate voltage. The wide dual supply range of ±4.5 V to ±18 V allows the switch to work with GaN power amplifiers and the wide single supply range 4.5 V to 36 V works well with LDMOS power amplifiers.

Figure 8-1 shows the TMUX6234 configured for control of a multi-channel power amplifier application.

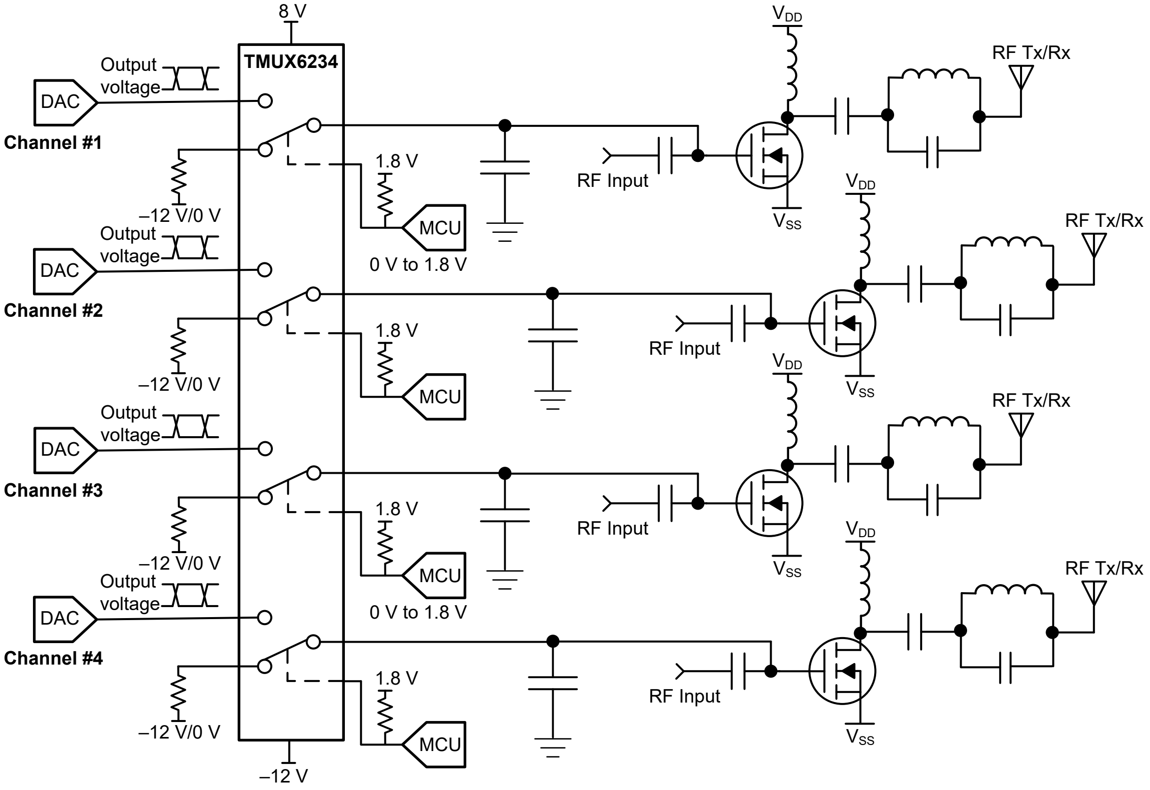


Figure 8-1. Power Amplifier Gate Driver

8.2.1 Design Requirements

Use the parameters listed in Table 8-1 for this design example.

Table 8-1. Design Parameters

PARAMETERS	VALUES	
	GAN application	LDMOS application
Supply (V_{DD})	8 V	
Supply (V_{SS})	-12 V	
Signal range	-12 V to 0 V	0 V to 5 V
Control logic	1.8 V compatiable (up to 36 V)	
SEL1 - SEL4	Controlled independently for each power amplifier channel	

8.2.2 Detailed Design Procedure

The application shown in Figure 8-1 demonstrates how to toggle between the DAC output and a low signal voltage for control of a power amplifier. A device such as the TMUX6234 that supports multiple supply voltage combinations allows the system designer to use a single switch across platforms with different power amplifier topologies such as GaN or LDMOS implementations. Using a multi-channel switch like the TMUX6234 allows the system to improve density by implementing a smaller solution size. Multiple channels of the TMUX6234 can be utilized to switch additional stages of a single power amplifier channel. Or multiple channel switches can be used on different power amplifier stages in high channel count communicaitons equipment such as a 32 transmist (TX), 32 receive (RX) active antenna system mMIMIO (AAS). Each channel of the TMUX6234 has independent control signals allowing for overal system flexibility. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pins of the switch or the golbal enable pin. The TMUX6234 can support 1.8 V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. All inputs to the switch must fall within the recommend operating conditions of the TMUX6234 including signal range and continuous current. For this design with a positive supply of 8 V on V_{DD}, and negative supply of -12 V on V_{SS}, the signal range can be 8 V to -12 V. The maximum continuous current (I_{DC}) is captured in the *Recommended Operating Conditions table* for a range of supply voltage cases.

8.2.3 Application Curve

The low on-resistance and fast switching times of TMUX6234 make this device ideal for implementing high channel count switching applications. Figure 8-2 shows the plot for transition time vs temperature for the TMUX6234.

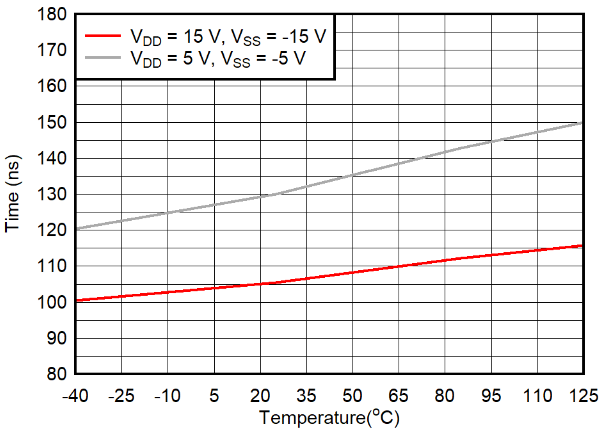


Figure 8-2. Transition Time vs Temperature

8.3 Power Supply Recommendations

The TMUX6234 operates across a wide supply range of ±4.5 V to ±18 V (4.5 V to 36 V in single-supply mode). The TMUX6234 also performs well with asymmetrical supplies such as V_{DD} = 18 V and V_{SS} = –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. Use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at the V_{DD} and V_{SS} pins to ground for an improved supply noise immunity. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems or systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

8.4 Layout

8.4.1 Layout Guidelines

A reflection can occur when a PCB trace turns a corner at a 90° angle. A reflection occurs primarily because of the change of width of the trace. The trace width increases to 1.414 times the width at the apex of the turn. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

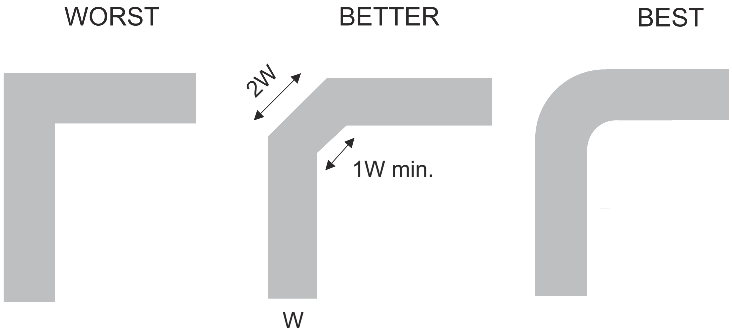


Figure 8-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 8-4 illustrates an example of a PCB layout with the TMUX6234. Some key considerations are:

- Decouple the supply pins with a 0.1 µF and 1 µF capacitor, placed lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.4.2 Layout Example

Figure 8-4 shows an example board layout for the TMUX6234.

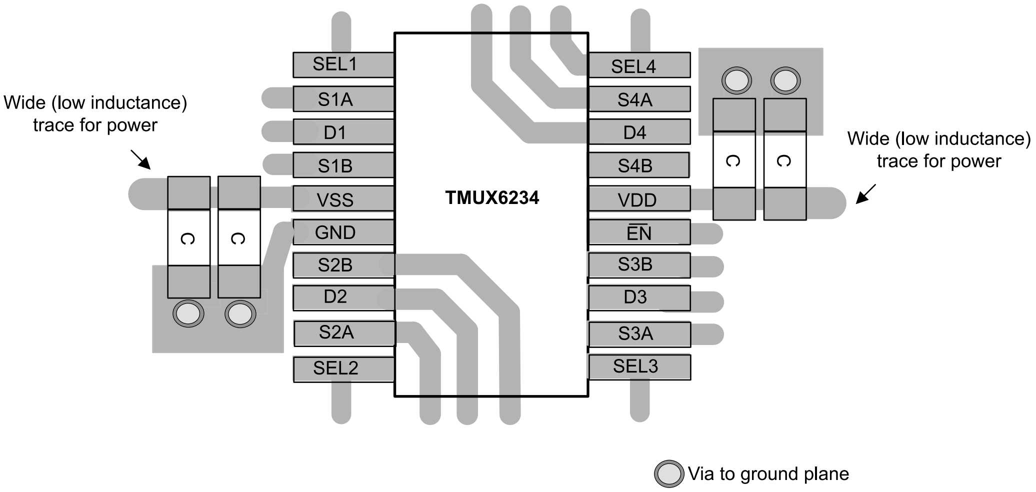


Figure 8-4. TMUX6234PW Layout Example

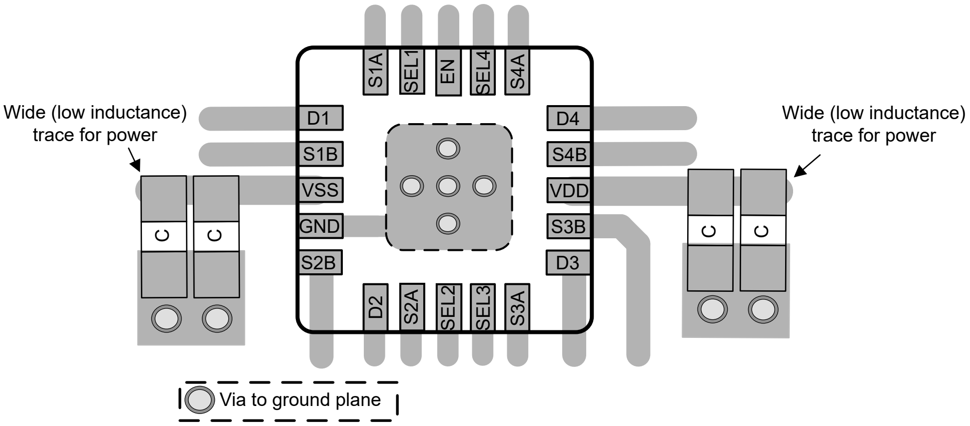


Figure 8-5. TMUX6234RRQ Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief.
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief.
- Texas Intruments, *Implications of Slow or Floating CMOS Inputs* application note.
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide.
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application report.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* application report.
- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability* application report.
- Texas Instruments, *QFN/SON PCB Attachment* applicaion report.
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2022) to Revision C (July 2024) **Page**

- Updated ESD HBM value..4
- Updated IIH max specification..6

Changes from Revision A (August 2021) to Revision B (December 2022)	**Page**
• Changed the status of the PW package from: *preview* to: *active*	1

Changes from Revision * (June 2021) to Revision A (August 2021)	**Page**
• Changed the document status from: *Advanced Information* to: *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX6234PWR	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T234
TMUX6234PWR.B	Active	Production	TSSOP (PW) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T234
TMUX6234RRQR	Active	Production	WQFN (RRQ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX X234
TMUX6234RRQR.B	Active	Production	WQFN (RRQ) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX X234

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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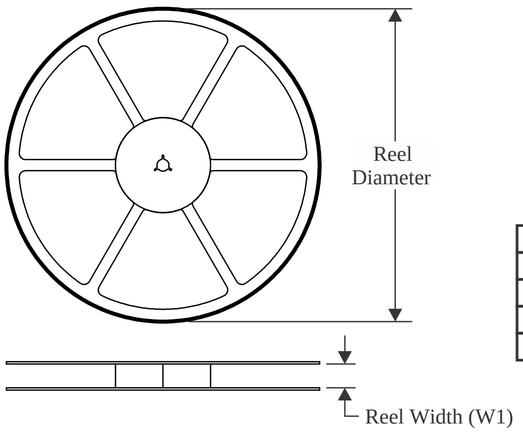
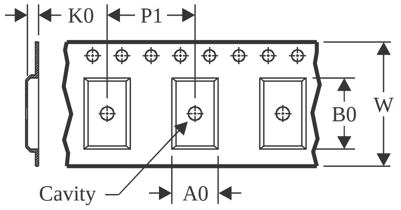
TAPE AND REEL INFORMATION

REEL DIMENSIONS

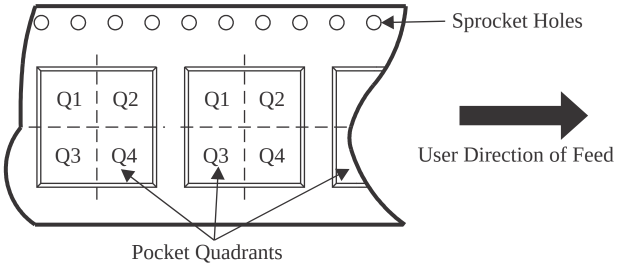


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

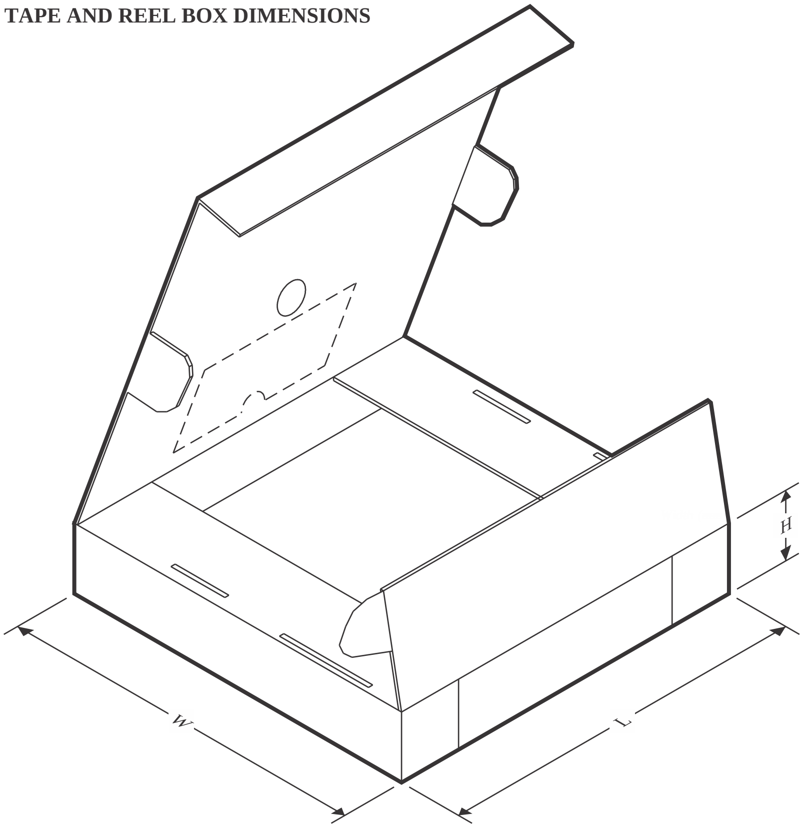
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

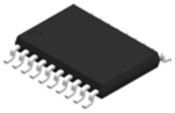
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6234PWR	TSSOP	PW	20	3000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TMUX6234RRQR	WQFN	RRQ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

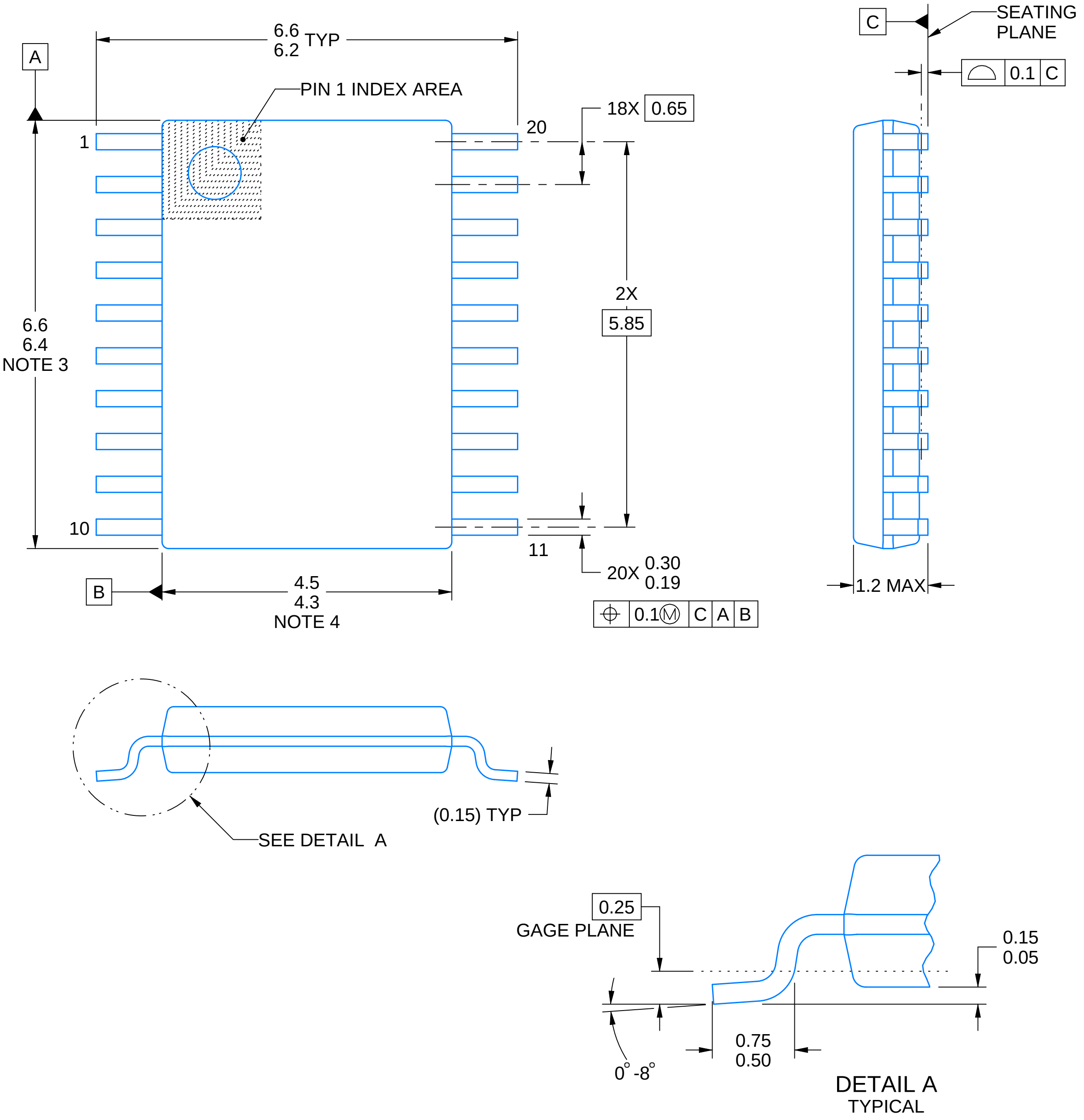
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6234PWR	TSSOP	PW	20	3000	353.0	353.0	32.0
TMUX6234RRQR	WQFN	RRQ	20	3000	367.0	367.0	35.0



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

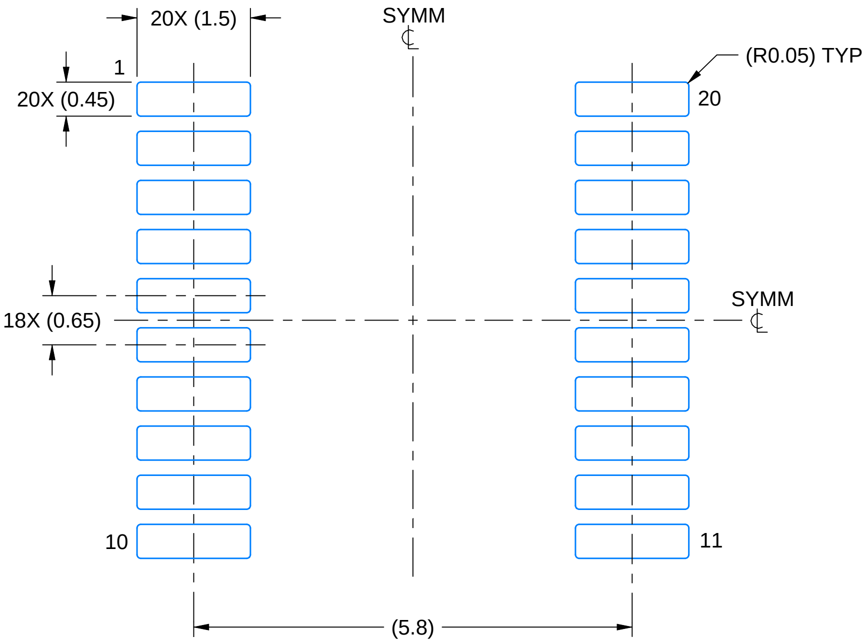
SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

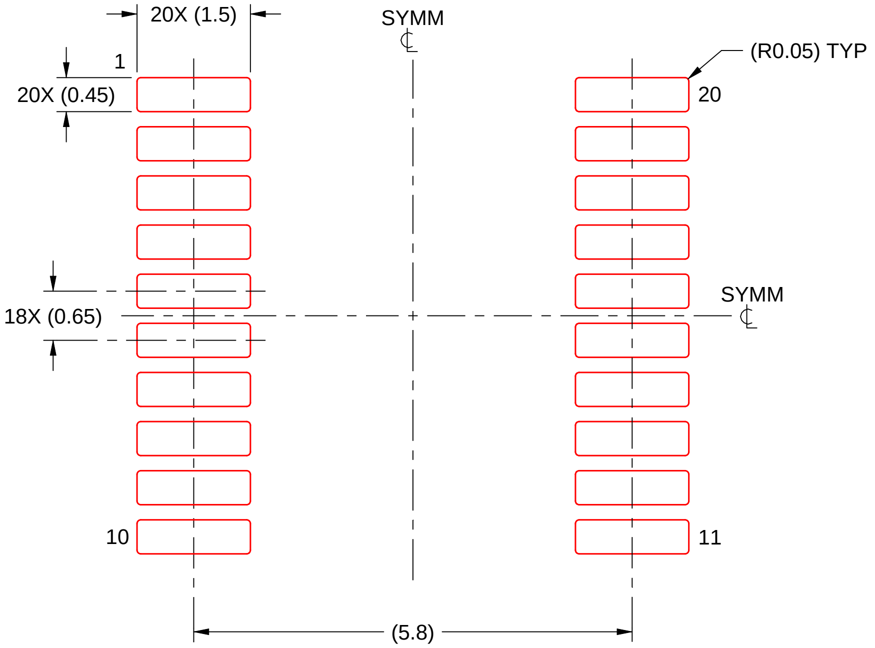
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

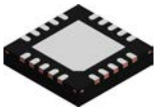
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

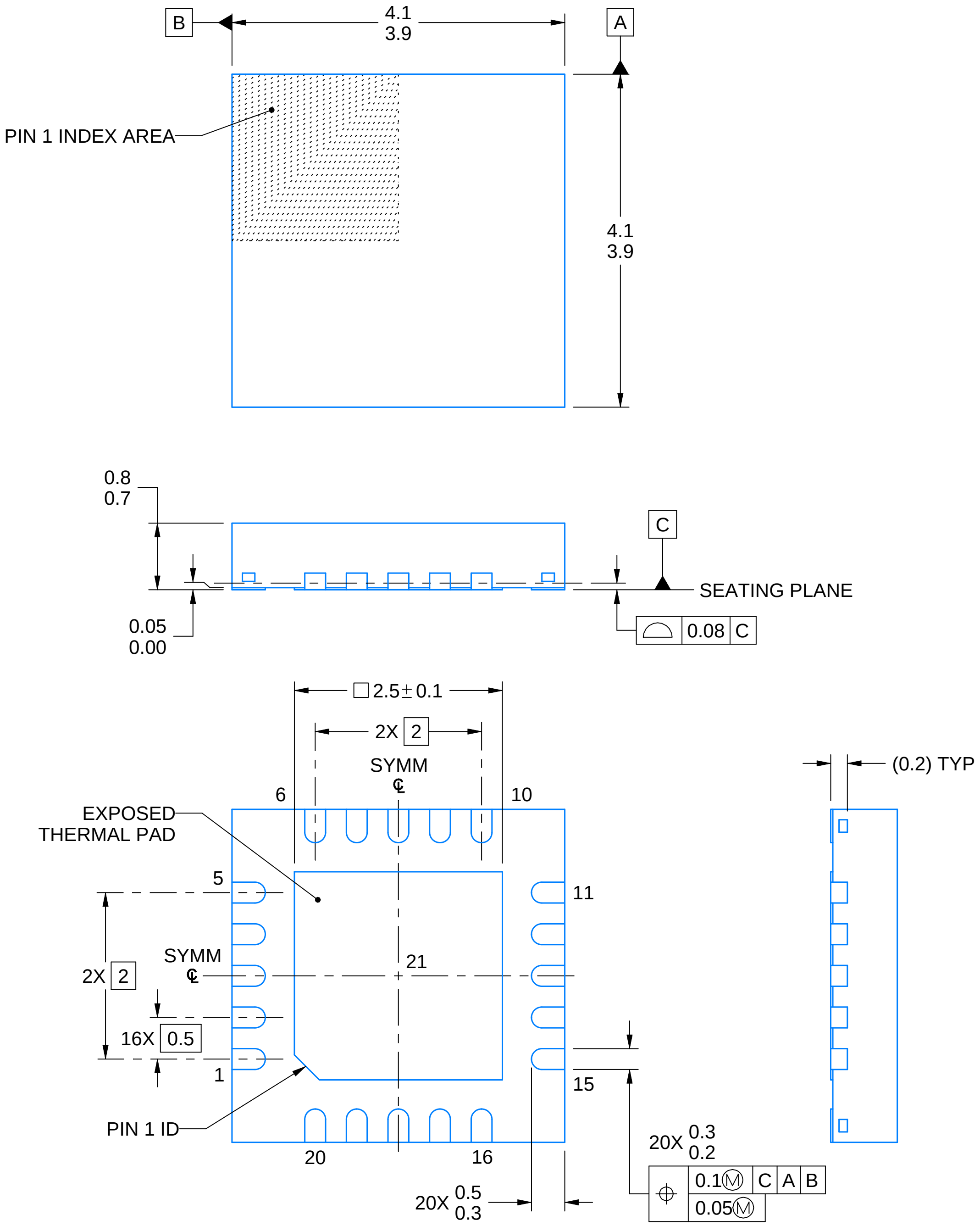


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

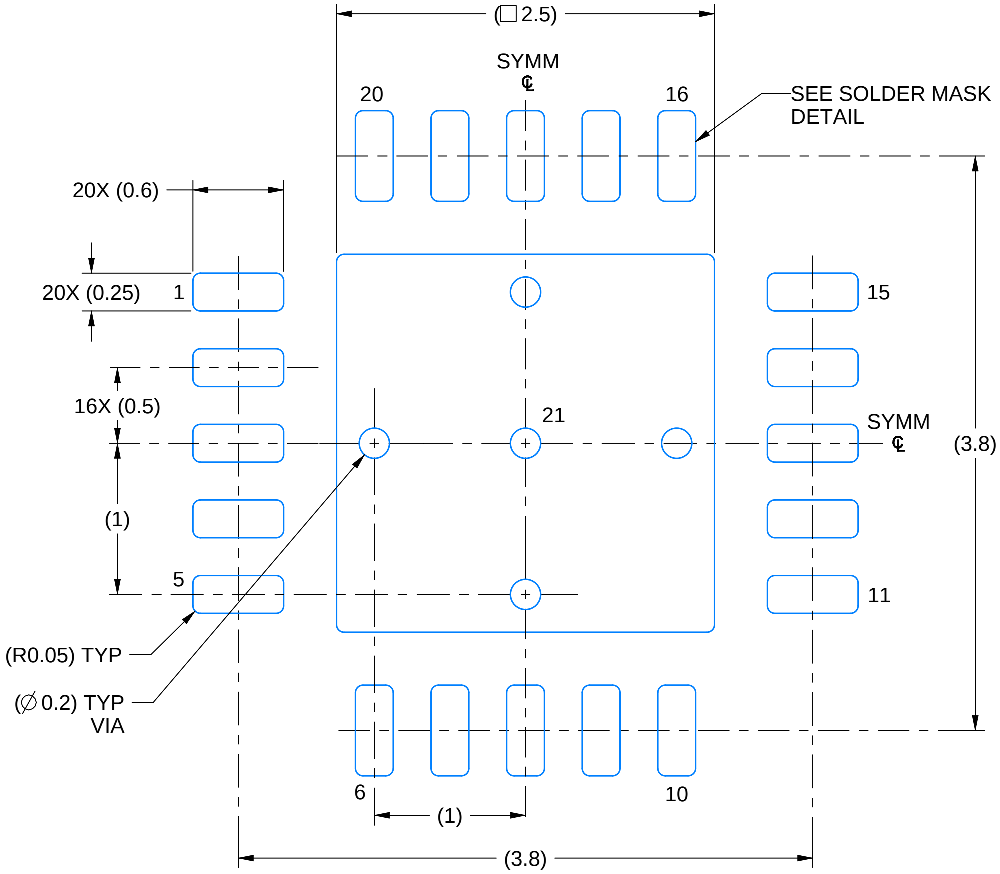




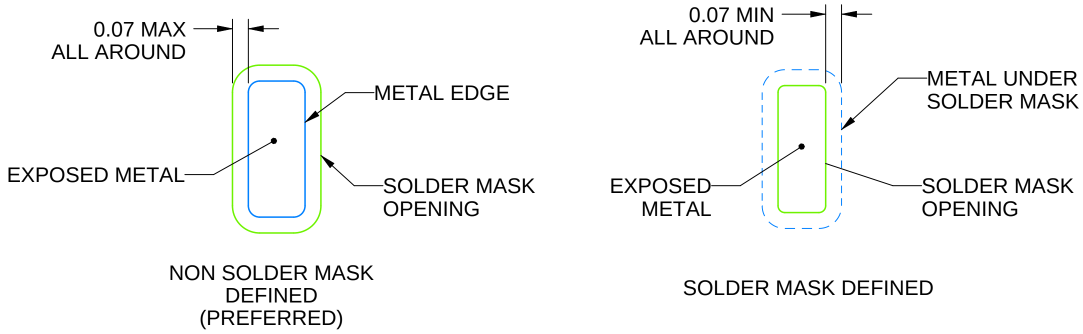
4224817/A 03/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



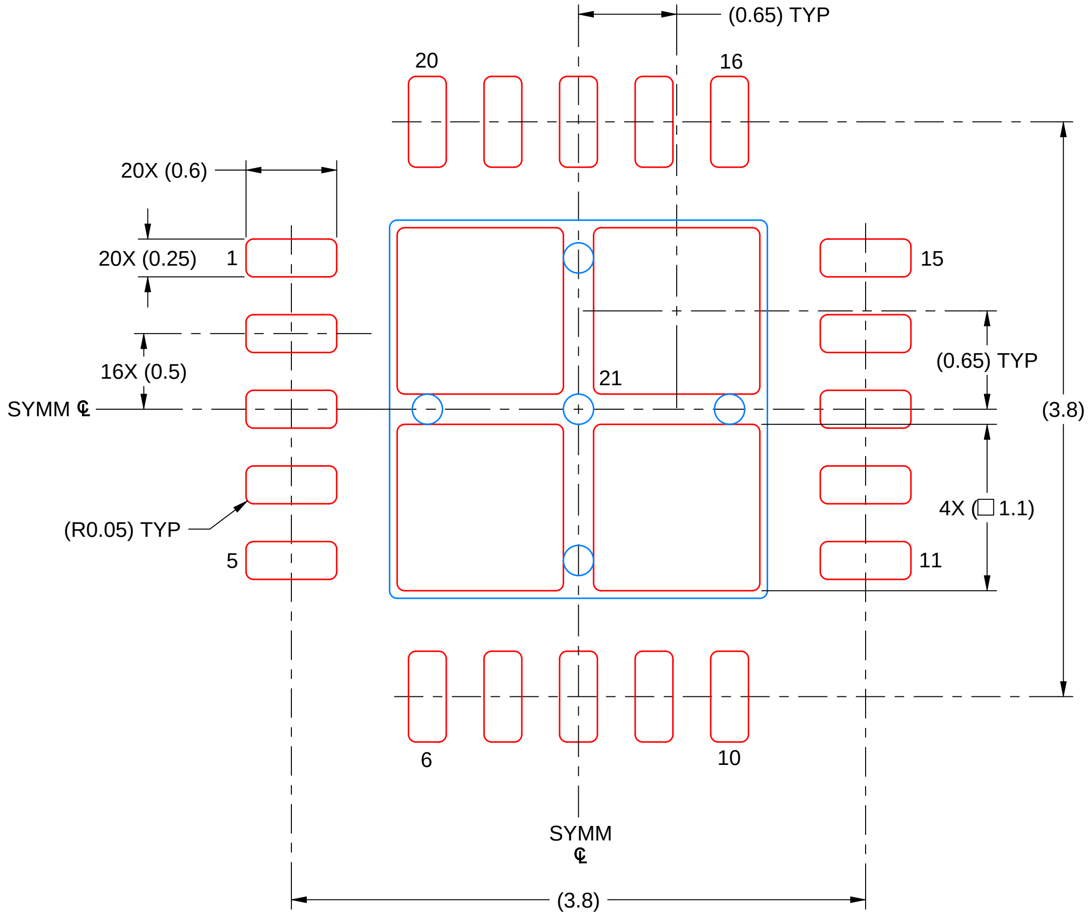
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224817/A 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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