![Texas Instruments logo]

TMUX541x 50V, 21Ω, 1:1 (SPST) 4-Channel Switches with 1.8V Logic

1 Features

- Dual supply range: ±4.5V to ±25V
- Single supply range: 4.5V to 50V
- Asymmetric dual supply support (For example: V_{DD} = 37.5V, V_{SS} = -12.5V)
- 1.8V logic compatible
- Low on-resistance: 21Ω (typical)
- Low on-capacitance: 9pF (typical)
- Ultra-low on-resistance flatness: 0.005Ω (typical)
- Low on-leakage current: 0.01nA (typical), 35nA (maximum)
- Low charge injection: 13pC (typical)
- –40°C to +125°C operating temperature
- Rail-to-rail operation
- Bidirectional operation
- Break-before-make switching (TMUX5413)

2 Applications

- Sample-and-hold circuits
- Feedback gain switching
- Signal isolation
- Semiconductor test equipment
- Programmable logic controllers (PLC)
- Factory automation and control
- Professional Audio Equipment
- Instrumentation: lab, analytical, and portable
- Data acquisition systems (DAQ)
- Optical test equipment

3 Description

The TMUX541x is a general purpose complementary metal-oxide semiconductor (CMOS) switch device with four independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device works with a single supply (4.5V to 50V), dual supplies (±4.5V to ±25V), or asymmetric supplies (such as V_{DD} = 37.5V, V_{SS} = –12.5V). The TMUX541x supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}.
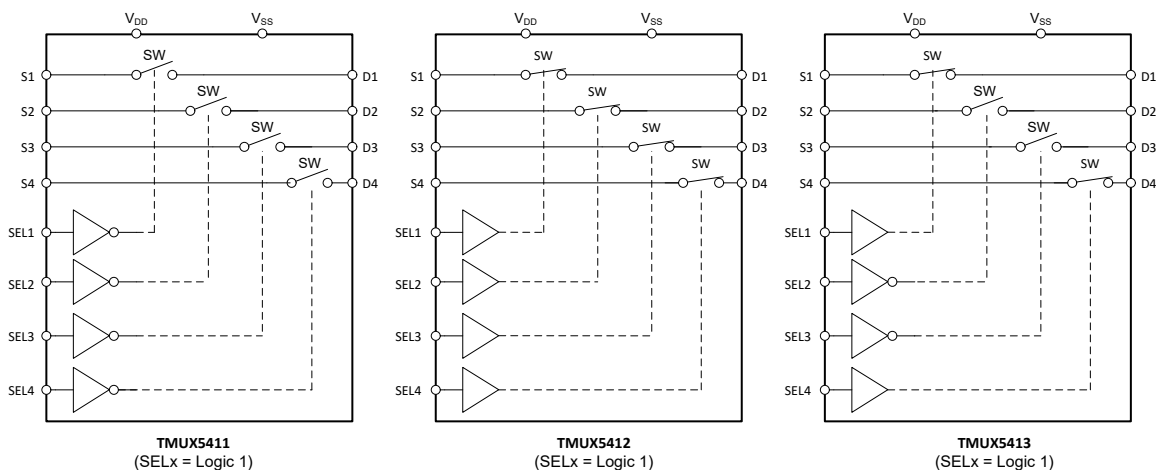
The switches of the TMUX541x are controlled with appropriate logic control inputs on the SELx pins. The TMUX541x exhibits break-before-make switching, allowing the device to be used in cross-point and multiplexing applications.

The TMUX541x is a part of the general purpose switches and multiplexers family of devices emphasizing uses in broad range of applications while reducing BOM cost.

Package Information

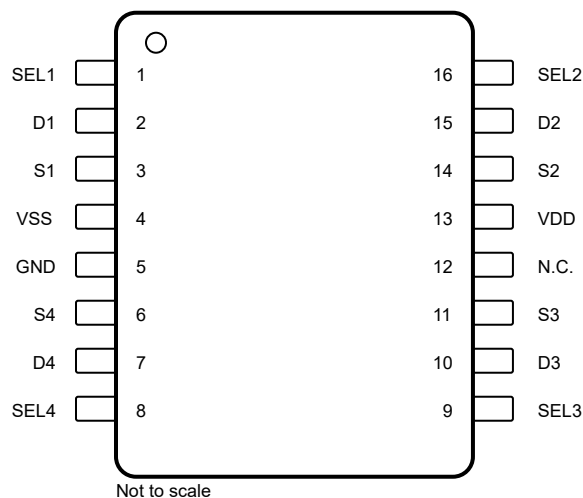| PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TMUX5411 TMUX5412 TMUX5413	PW (TSSOP, 16)	5mm × 6.4mm
	QFN (UQFN, 16)	2.6mm × 1.8mm
	DYY (SOT-23-THIN, 16)	3.26mm x 4.2mm
	D (SOIC, 16)	9.9mm x 6mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

TMUX541x Block Diagram

⚠ An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. ADVANCE INFORMATION for preproduction products; subject to change without notice.

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4 Pin Configuration and Functions

Not to scale

Figure 4-1. 16-Pin PW (TSSOP) & DYY (SOT-23-THN) Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	TSSOP & SOT-23-THN		
D1	2	I/O	Drain pin 1. Can be an input or output.
D2	15	I/O	Drain pin 2. Can be an input or output.
D3	10	I/O	Drain pin 3. Can be an input or output.
D4	7	I/O	Drain pin 4. Can be an input or output.
GND	5	P	Ground (0 V) reference.
N.C.	12	—	No internal connection. Can be shorted to GND or left floating
S1	3	I/O	Source pin 1. Can be an input or output.
S2	14	I/O	Source pin 2. Can be an input or output.
S3	11	I/O	Source pin 3. Can be an input or output.
S4	6	I/O	Source pin 4. Can be an input or output.
SEL1	1	I	Logic control input 1, has internal pull-down resistor. Controls channel 1 state as provided in Table 7-2.
SEL2	16	I	Logic control input 2, has internal pull-down resistor. Controls channel 2 state as provided in Table 7-2.
SEL3	9	I	Logic control input 3, has internal pull-down resistor. Controls channel 3 state as provided in Table 7-2.
SEL4	8	I	Logic control input 4, has internal pull-down resistor. Controls channel 4 state as provided in Table 7-2.
VDD	13	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND
VSS	4	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10 µF between VSS and GND. In single-supply applications, this pin should be connected to ground.

(1)   I = input, O = output, I/O = input and output, P = power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		55	V
V_{DD}		−0.5	55	V
V_{SS}		−55	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	−0.5	55	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	-30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}−0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)	-30	30	mA
T_A	Ambient temperature	−55	150	°C
T_{stg}	Storage temperature	−65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins[1]	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ [1]	Power supply voltage differential		4.5		50	V
V_{DD}	Positive power supply voltage		4.5		50	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)		V_{SS}		V_{DD}	V
$V_{SEL} - V_{SS}$	Address or enable pin voltage		0		48	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)		-30		30	mA
T_A	Ambient temperature		−40		125	°C
V_{IH}	Logic Input High [2]	Logic Inputs (SEL / EN pins)	1.3		48	V
V_{IL}	Logic Input Low	Logic Inputs (SEL / EN pins)	0		0.8	V

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ ($V_{DD} - V_{SS}$) ≤ 50 V, and the minimum V_{DD} is met.
(2) Please note the VIH is limited by the following constraints: $V_{SEL} - V_{SS}$ ≤ 48V

5.4 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = −15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = −10 V to +10 V I_D = −10 mA	25°C		21	26	Ω
			−40°C to +85°C			32	Ω
			−40°C to +125°C			37	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = −10 V to +10 V I_D = −10 mA	25°C		0.1	0.25	Ω
			−40°C to +85°C			0.35	Ω
			−40°C to +125°C			0.45	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = −10 V to +10 V I_S = −10 mA	25°C		0.005	0.25	Ω
			−40°C to +85°C			0.35	Ω
			−40°C to +125°C			0.45	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = −10 mA	−40°C to +125°C		0.085		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = −16.5 V Switch state is off V_S = +10 V / −10 V V_D = −10 V / + 10 V	25°C	-20	0.01	20	nA
			−40°C to +85°C	-25		25	nA
			−40°C to +125°C	-35		35	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = −16.5 V Switch state is off V_S = +10 V / −10 V V_D = −10 V / + 10 V	25°C	-20	0.01	20	nA
			−40°C to +85°C	-25		25	nA
			−40°C to +125°C	-35		35	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 16.5 V, V_{SS} = −16.5 V Switch state is on V_S = V_D = ±10 V	25°C	-20	0.01	20	nA
			−40°C to +85°C	-25		25	nA
			−40°C to +125°C	-35		35	nA
LOGIC INPUTS (SEL / EN pins)							
I_{IH}	Input leakage current	Logic Inputs = 50V	−40°C to +125°C			1.4	µA
I_{IH}	Input leakage current	Logic Inputs = 1.8V - 5V	−40°C to +125°C			0.6	µA
I_{IL}	Input leakage current		−40°C to +125°C	-1	0.3	1	nA
C_{IN}	Logic input capacitance		−40°C to +125°C		4		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = −16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		105	140	µA
			−40°C to +85°C			155	µA
			−40°C to +125°C			170	µA
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = −16.5 V All Switches OFF	−40°C to +125°C			65	µA
$I_{DD\ (1.8V)}$	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = −16.5 V Logic inputs = 1.8 V	−40°C to +125°C			175	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = −16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		90	110	µA
			−40°C to +85°C			120	µA
			−40°C to +125°C			130	µA
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 16.5 V, V_{SS} = −16.5 V All Switches OFF	−40°C to +125°C			25	µA
$I_{SS\ (1.8V)}$	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = −16.5 V Logic inputs = 1.8 V	−40°C to +125°C			130	µA

(1)   When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2)   When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

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5.5 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10 V R_L = 1 kΩ, C_L = 35 pF	25°C		240	265	ns
			–40°C to +85°C			275	ns
			–40°C to +125°C			285	ns
t_{OFF}	Turn-off time from control input	V_S = 10 V R_L = 1 kΩ, C_L = 35 pF	25°C		80	100	ns
			–40°C to +85°C			105	ns
			–40°C to +125°C			110	ns
t_{BBM}	Break-before-make time delay (TMUX5413 Only)	V_S = 10 V, R_L = 1 kΩ, C_L = 35 pF	25°C		180		ns
			–40°C to +85°C			205	ns
			–40°C to +125°C			210	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 1 kΩ, C_L = 35 pF	25°C		0.04		ms
			–40°C to +85°C			0.05	ms
			–40°C to +125°C			0.06	ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		400		ps
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		13		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		-100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		-82		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz	25°C		-110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz	25°C		-100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V	25°C		400		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		-1.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		-59		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.001		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		5		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		5		pF
$C_{S(ON)},$ $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		9		pF

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5.6 48 V Single Supply: Electrical Characteristics

V_{DD} = +48 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +48 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 5 V to 43 V I_D = –10 mA	25°C		21	26	Ω
			–40°C to +85°C			32	Ω
			–40°C to +125°C			40	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 5 V to 43 V I_D = –10 mA	25°C		0.2	0.25	Ω
			–40°C to +85°C			0.3	Ω
			–40°C to +125°C			0.35	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 5 V to 43 V I_D = –10 mA	25°C		0.04	0.25	Ω
			–40°C to +85°C			0.35	Ω
			–40°C to +125°C			0.45	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 24 V, I_S = –10 mA	–40°C to +125°C		0.085		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 48 V, V_{SS} = 0 V Switch state is off V_S = 43 V / 1 V V_D = 1 V / 43 V	25°C	-20	0.01	20	nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–35		35	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 48 V, V_{SS} = 0 V Switch state is off V_S = 43 V / 1 V V_D = 1 V / 43 V	25°C	-20	0.01	20	nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–35		35	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 44 V, V_{SS} = 0 V Switch state is on V_S = V_D = 40 V or 1 V	25°C	-20	0.01	20	nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	-35		35	nA
LOGIC INPUTS (SEL / EN pins)							
I_{IL}	Input leakage current		–40°C to +125°C	–0.01	–0.001		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 48 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		125	155	µA
			–40°C to +85°C			170	µA
			–40°C to +125°C			180	µA
$I_{DD\ (1.8V)}$	V_{DD} supply current	V_{DD} = 48 V, V_{SS} = 0 V Logic inputs = 1.8 V	–40°C to +125°C			190	µA
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 48 V, V_{SS} = 0 V All Switches OFF	–40°C to +125°C			65	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

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5.7 48 V Single Supply: Switching Characteristics

V_{DD} = +48 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +48 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 18 V R_L = 1 kΩ, C_L = 35 pF	25°C		225	250	ns
			–40°C to +85°C			255	ns
			–40°C to +125°C			260	ns
t_{OFF}	Turn-off time from control input	V_S = 18 V R_L = 1 kΩ, C_L = 35 pF	25°C		90	110	ns
			–40°C to +85°C			115	ns
			–40°C to +125°C			120	ns
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 1 kΩ, C_L = 35 pF	–40°C to +125°C		0.01		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		475		ps
Q_{INJ}	Charge injection	V_S = 24 V, C_L = 100 pF	25°C		13		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		-100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		-82		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		-110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz	25°C		-100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		400		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		-1.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		-62		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 24 V, V_{BIAS} = 24 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.001		%
$C_{S(OFF)}$	Source off capacitance	V_S = 24 V, f = 1 MHz	25°C		5		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 24 V, f = 1 MHz	25°C		5		pF
$C_{S(ON)},$ $C_{D(ON)}$	On capacitance	V_S = 24 V, f = 1 MHz	25°C		9		pF

5.8 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA	25°C		42	50	Ω
			–40°C to +85°C			75	Ω
			–40°C to +125°C			70	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA	25°C		0.4	0.8	Ω
			–40°C to +85°C			0.85	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA	25°C		21	25	Ω
			–40°C to +85°C			35	Ω
			–40°C to +125°C			40	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA	–40°C to +125°C		0.085		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	-20	0.01	20	nA
			–40°C to +85°C	-25		25	nA
			–40°C to +125°C	-35		35	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	-20	0.01	20	nA
			–40°C to +85°C	-25		25	nA
			–40°C to +125°C	-35		35	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V	25°C	-20	0.01	20	nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–35		35	nA
LOGIC INPUTS (SEL / EN pins)							
C_{IN}	Logic input capacitance		–40°C to +125°C		5.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		115	135	µA
			–40°C to +85°C			150	µA
			–40°C to +125°C			165	µA
$I_{DD\ (1.8V)}$	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 1.8 V	–40°C to +125°C			170	µA
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 13.2 V, V_{SS} = 0 V All Switches OFF	–40°C to +125°C			50	µA

(1)   When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2)   When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

ADVANCE INFORMATION

5.9 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8 V R_L = 1 kΩ, C_L = 35 pF	25°C		250	300	ns
			–40°C to +85°C			310	ns
			–40°C to +125°C			320	ns
t_{OFF}	Turn-off time from control input	V_S = 8 V R_L = 1 kΩ, C_L = 35 pF	25°C		85	115	ns
			–40°C to +85°C			120	ns
			–40°C to +125°C			125	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 1 kΩ, C_L = 35 pF	25°C		0.06		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		500		ps
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF	25°C		7		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		-100		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		--82		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		--110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz	25°C		-100		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V	25°C		375		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		-1.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz	25°C		-60		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		TBD		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		6		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		6		pF
$C_{S(ON)},$ $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		11.5		pF

ADVANCE INFORMATION

5.10 Typical Characteristics
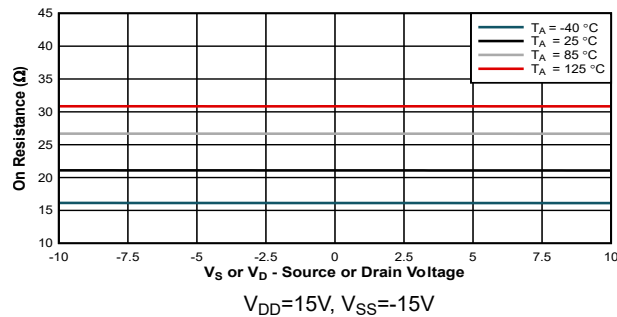
at T_A = 25°C (unless otherwise noted)
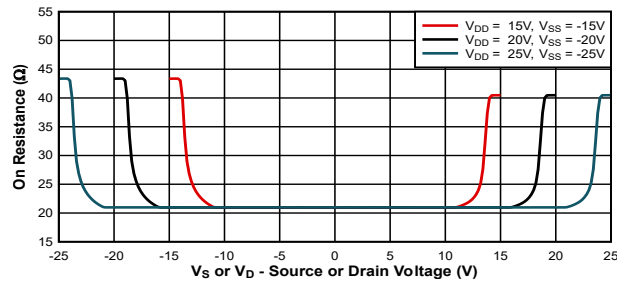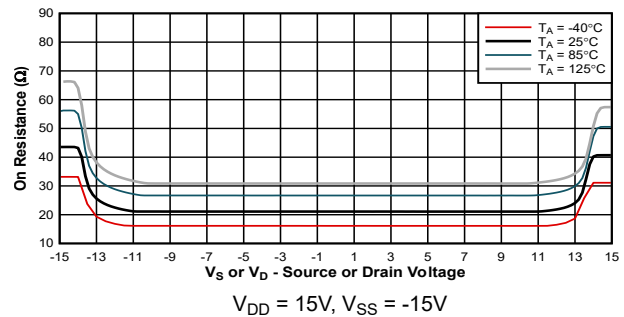

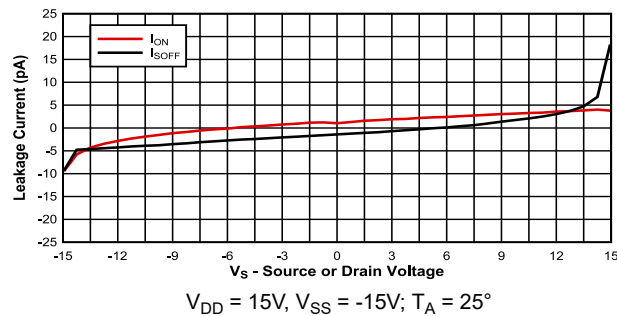Figure 5-1. On-Resistance vs Source or Drain Voltage for Dual Supply
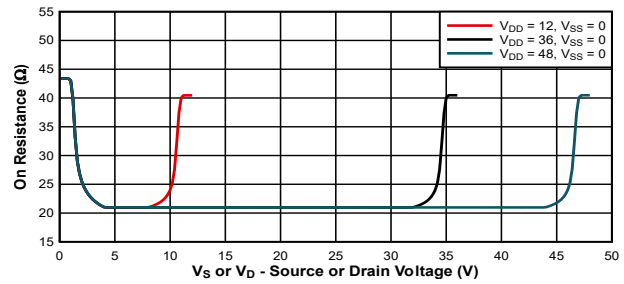
Figure 5-2. On-Resistance vs Source or Drain Voltage for Single Supply

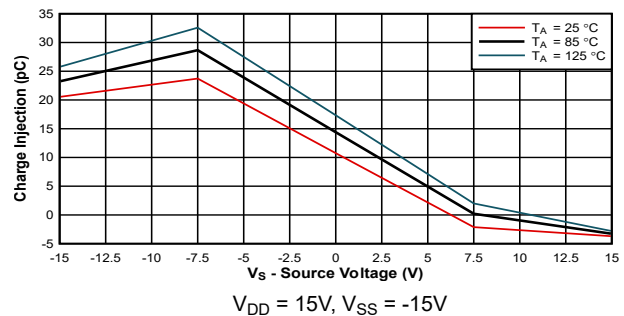
Figure 5-3. On-Resistance vs Source or Drain Operational Voltage (Flat Region)

Figure 5-4. On-Resistance vs Source or Drain Voltage

Figure 5-5. Leakage Current vs Bias Voltage

Figure 5-6. Charge Injection vs Source Voltage

ADVANCE INFORMATION

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:
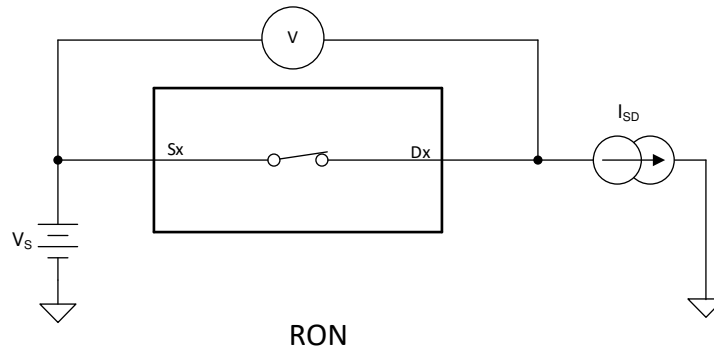

Figure 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

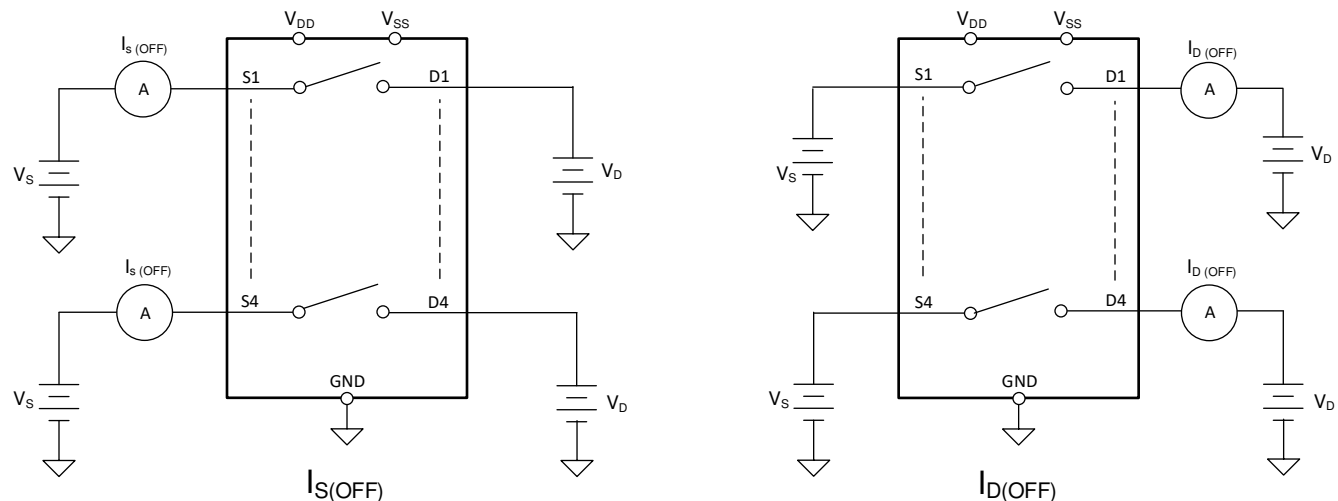Figure 6-2 shows the setup used to measure both off-leakage currents.

Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.
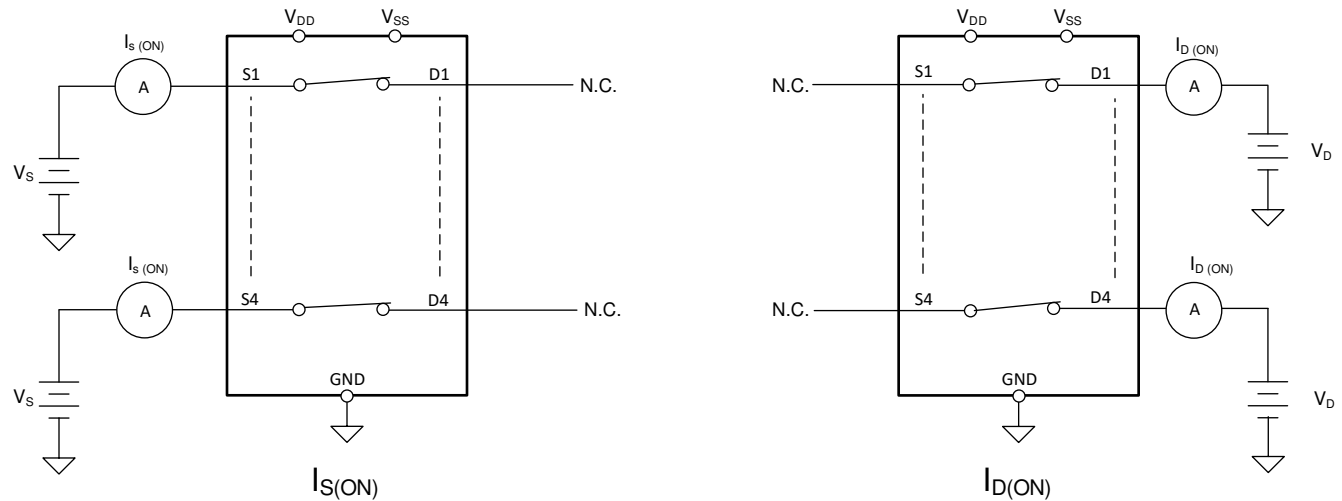
Figure 6-3. On-Leakage Measurement Setup

6.4 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-4 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.
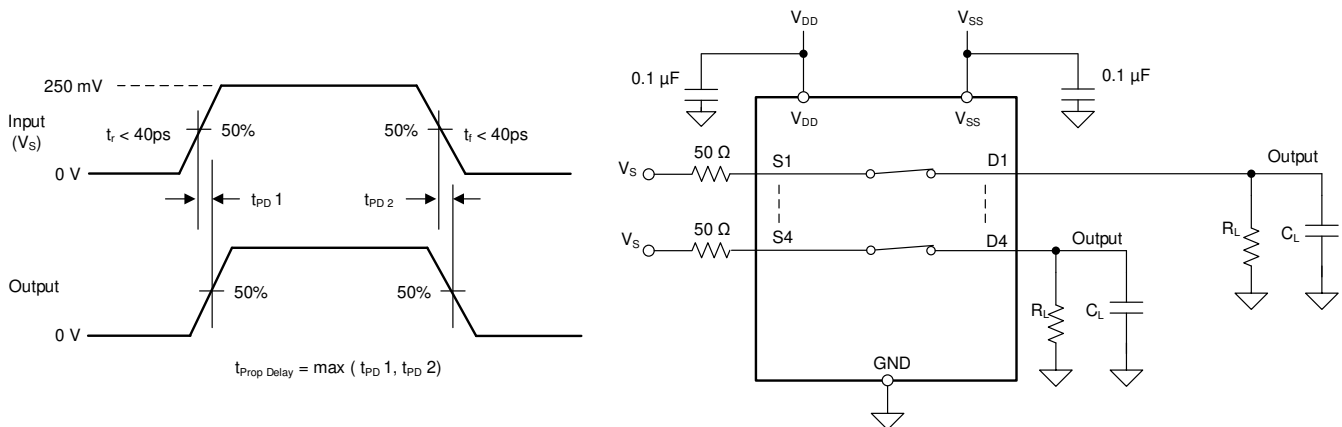
Figure 6-4. Propagation Delay Measurement Setup

ADVANCE INFORMATION

ADVANCE INFORMATION

6.5 Charge Injection

This device has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-5 shows the setup used to measure charge injection from source (Sx) to drain (Dx).
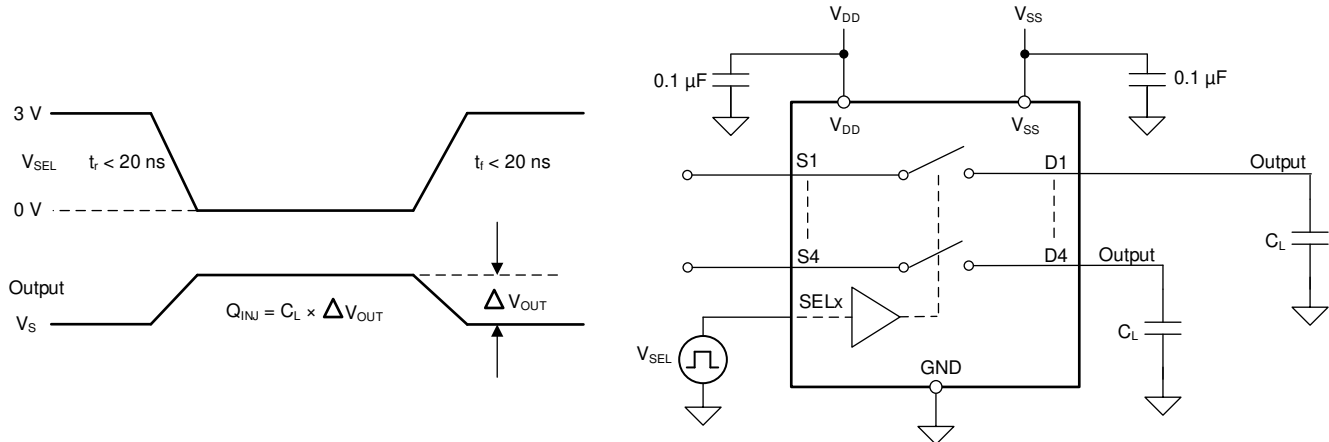
Figure 6-5. Charge-Injection Measurement Setup

6.6 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-6 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

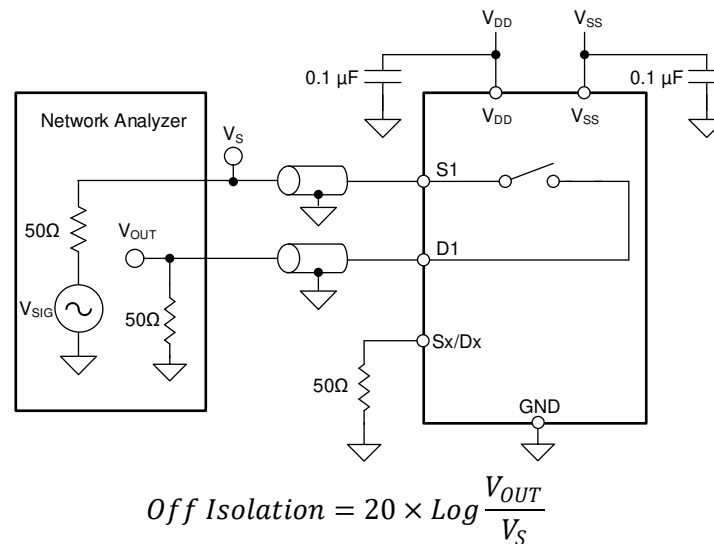$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-6. Off Isolation Measurement Setup

6.7 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-7 shows the setup used to measure, and the equation used to compute crosstalk.

$$Crosstalk = 20 \times Log\frac{V_{OUT}}{V_S}$$
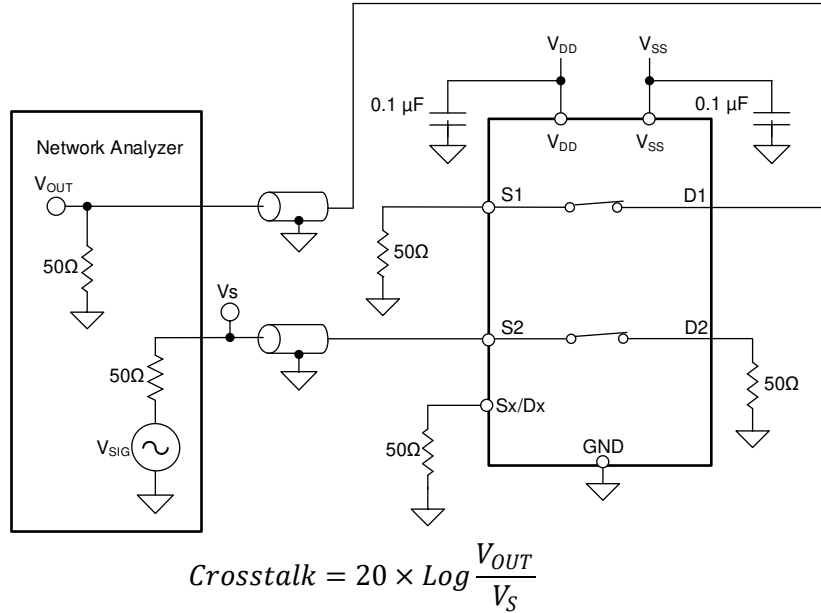
Figure 6-7. Channel-to-Channel Crosstalk Measurement Setup

6.8 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 6-8 shows the setup used to measure bandwidth.

$$Bandwidth = 20 \times Log\frac{V_{OUT}}{V_S}$$
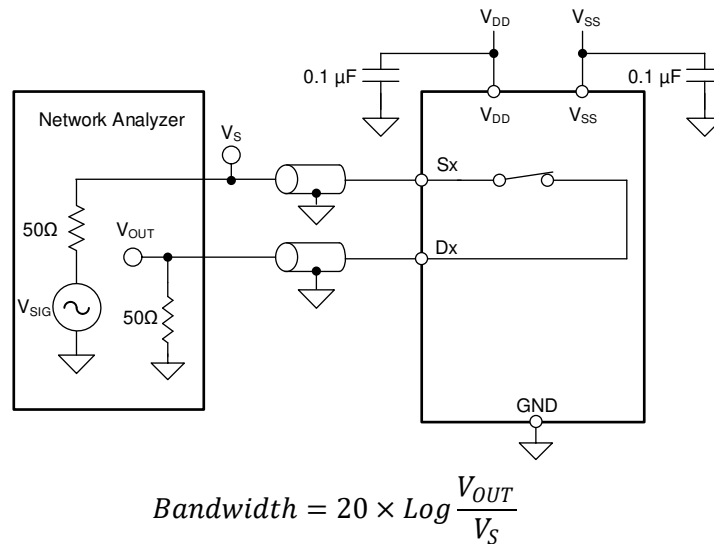
Figure 6-8. Bandwidth Measurement Setup

ADVANCE INFORMATION

ADVANCE INFORMATION

6.9 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.
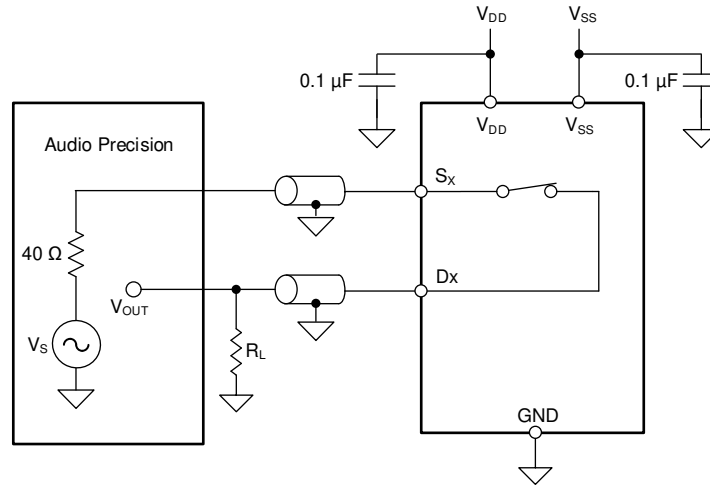
Figure 6-9. THD + N Measurement Setup

6.10 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100 mV$_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

Figure 6-10. AC PSRR Measurement Setup

7 Detailed Description

7.1 Overview

TMUX541x is a 1:1 (SPST), 4-channel switch. This device has four independently selectable single-pole, single-throw switches that are turned-on or tu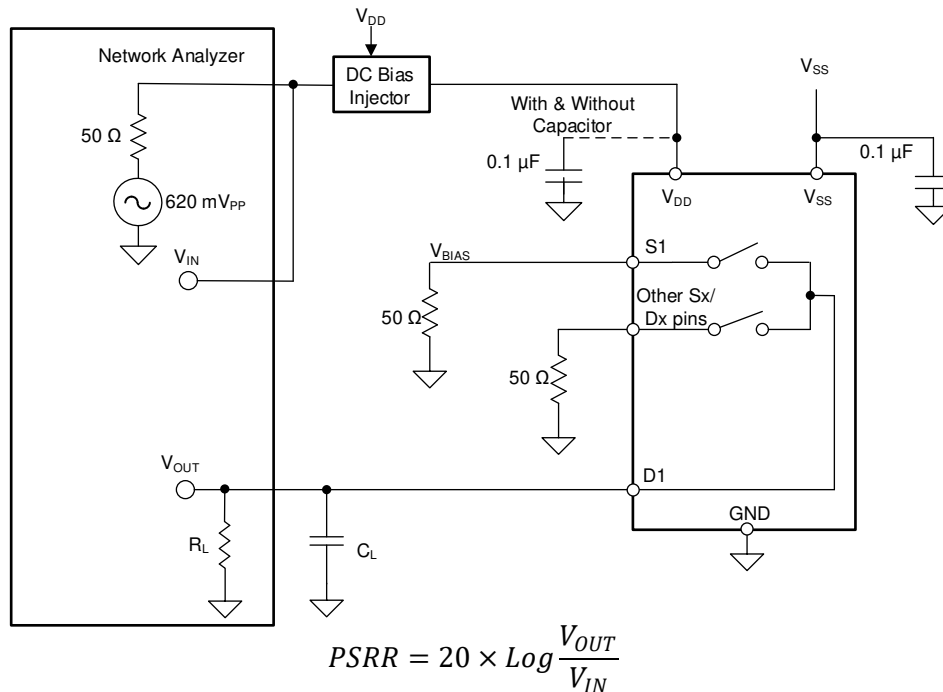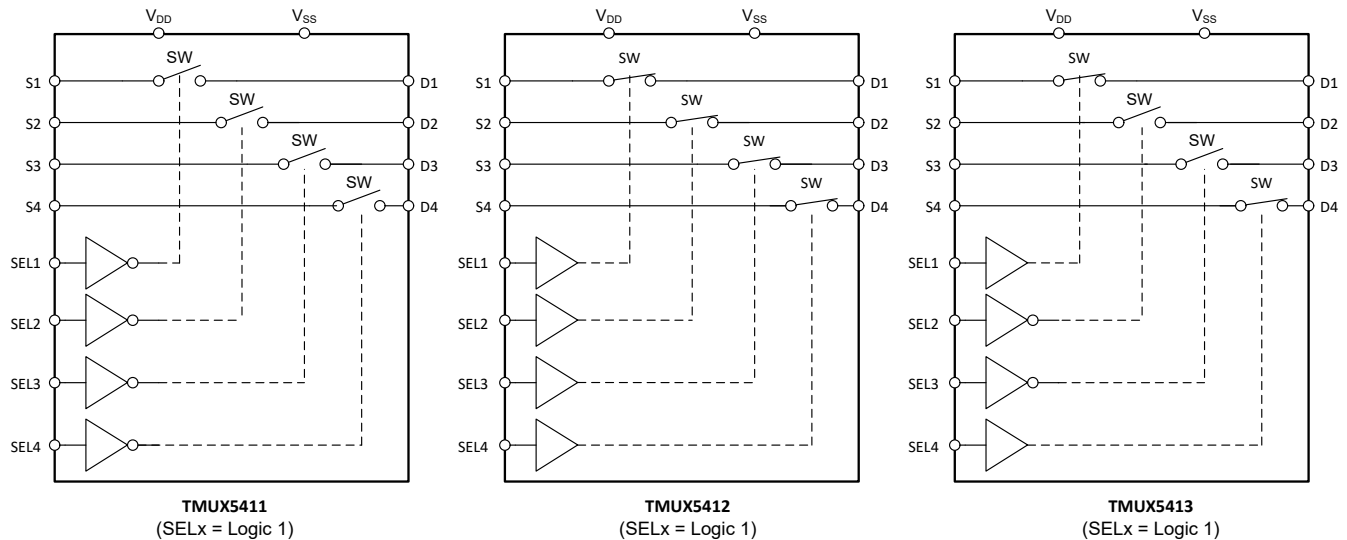rned-off based on the state of the corresponding select pin. This device works well with dual supplies, a single supply, or asymmetric supplies such as V_{DD} = 37.5V, V_{SS} = −12.5V.

7.2 Functional Block Diagram

TMUX5411
(SELx = Logic 1)

TMUX5412
(SELx = Logic 1)

TMUX5413
(SELx = Logic 1)

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX541x conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX541x ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX541x has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the TMUX541x to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

7.3.4 Flat On-Resistance

The TMUX541x is designed with a special switch architecture to produce ultra-flat on-resistance (RON) across most of the switch input operating region. The flat RON response allows the device to be used in a wide variety of applications since the RON is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so unwanted noise is not produced from the device to affect sampling accuracy.

This architecture also keeps RON the same regardless of the supply voltage. The flattest on-resistance region extends roughly from 5 V above VSS to 5 V below VDD. As long as this headroom is maintained, the TMUX541x exhibits an extremely linear response.

7.3.5 Power-Up Sequence Free

The TMUX541x supports any power up sequencing. With the supply rails (VDD and VSS), any rail can be powered on first. Similarly, when powering down the supply rails can be powered down in any order.

ADVANCE INFORMATION

7.4 Device Functional Modes

The TMUX541x has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins operate down to 1.8 V logic and can be as high as 48 V.

The TMUX541x devices can be operated without any external components except for the supply decoupling capacitors. The SELx pins have internal pull-down resistors.

7.4.1 Truth Tables

TMUX5412 Truth Table provides the truth table for TMUX541x.

Table 7-1. TMUX5411 Truth Table

SEL x [1]	CHANNEL x
0	Channel x ON
1	Channel x OFF

Table 7-2. TMUX5412 Truth Table

SEL x [1]	CHANNEL x
0	Channel x OFF
1	Channel x ON

Table 7-3. TMUX5413 Truth Table

SEL1	SEL2	SEL3	SEL4	ON / OFF CHANNELS[1]
0	X	X	X	CHANNEL 1 OFF
1	X	X	X	CHANNEL 1 ON
X	0	X	X	CHANNEL 2 ON
X	1	X	X	CHANNEL 2 OFF
X	X	0	X	CHANNEL 3 ON
X	X	1	X	CHANNEL 3 OFF
X	X	X	0	CHANNEL 4 OFF
X	X	X	1	CHANNEL 4 ON

(1)   x denotes 1, 2, 3, or 4 for the corresponding channel.

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX541x is a part of the general purpose switches and multiplexers family of devices. The device operates with dual supplies (±4.5 V to ±25V), a single supply (4.5 V to 50V), or asymmetric supplies (such as V_{DD} = 37.5 V, V_{SS} = −12.5 V), and offers a true rail-to-rail input and output signal range. The TMUX541x offers a low R_{ON}, low on and off leakage currents, and high bandwidth. These features make the TMUX541x a great option for broad range of high-voltage industrial applications.

8.2 Power Supply Recommendations

The TMUX541x device operates across a wide supply range of ±4.5 V to ±25V (4.5 V to 50V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 37.5 V and V_{SS} = −12.5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always make sure a solid ground (GND) connection is established before supplies are ramped.

ADVANCE INFORMATION

Submit Document Feedback   19

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *When to Replace a Relay with a Multiplexer* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTMUX5412DYYR	Active	Preproduction	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTMUX5412PWR	Active	Preproduction	TSSOP (PW) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
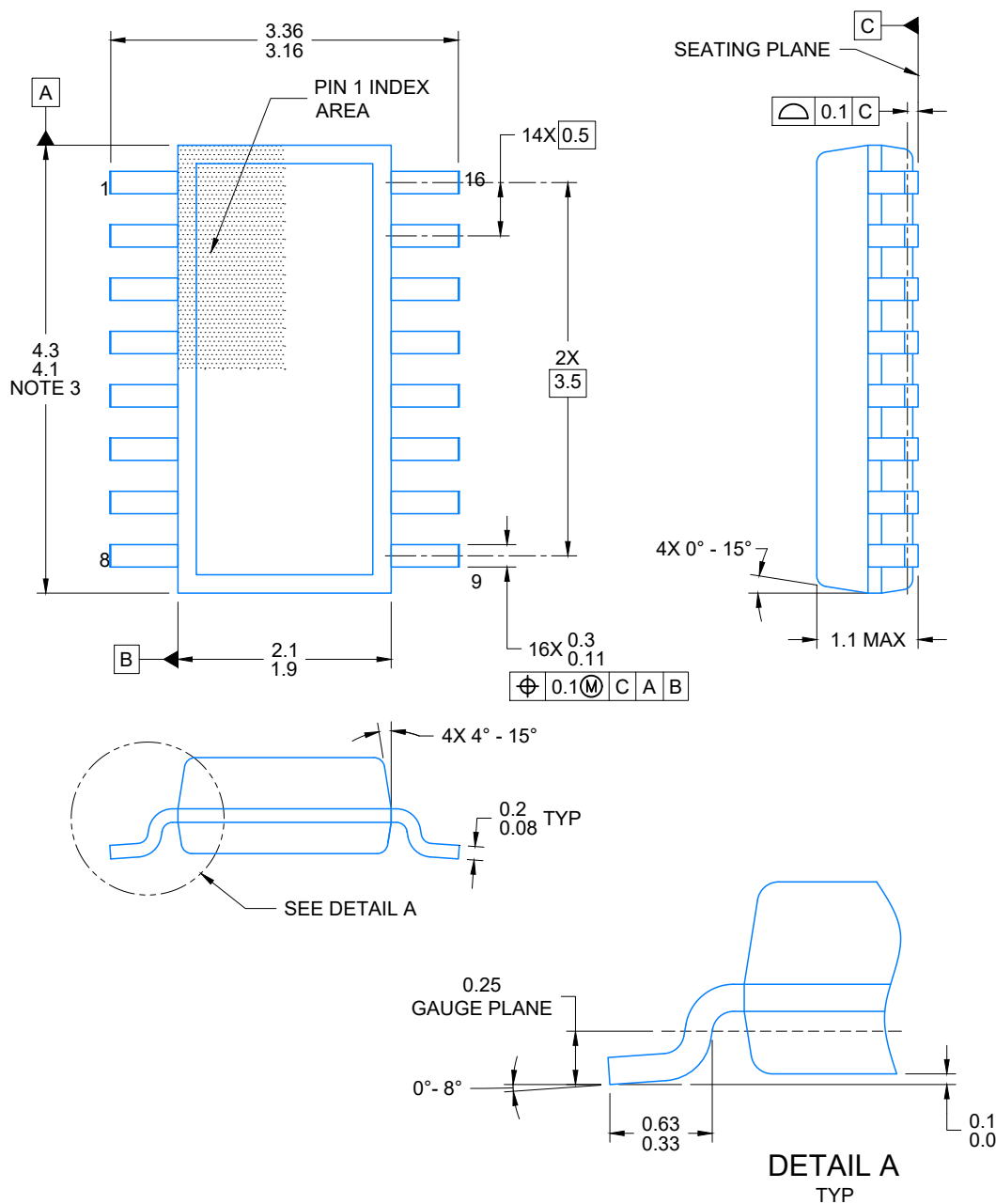
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
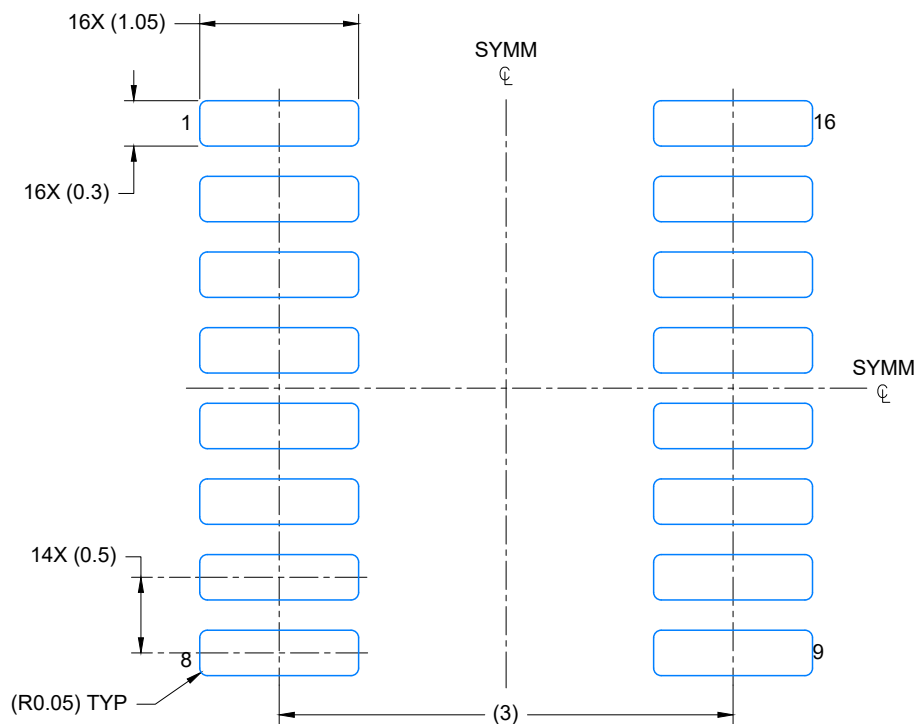
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PLASTIC SMALL OUTLINE

SEATING PLANE

| C |

| 0.1 | C |

3.36 / 3.16

| A |

PIN 1 INDEX AREA

14X | 0.5 |

16

1

4.3 / 4.1 NOTE 3

2X | 3.5 |

8

9

4X 0° - 15°

1.1 MAX

| B |

2.1 / 1.9

16X 0.3 / 0.11

| ⊕ | 0.1 Ⓜ | C | A | B |

4X 4° - 15°

0.2 / 0.08 TYP

SEE DETAIL A

0.25 GAUGE PLANE

0°- 8°

0.63 / 0.33

0.1 / 0.0

DETAIL A
TYP

4224642/D   07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
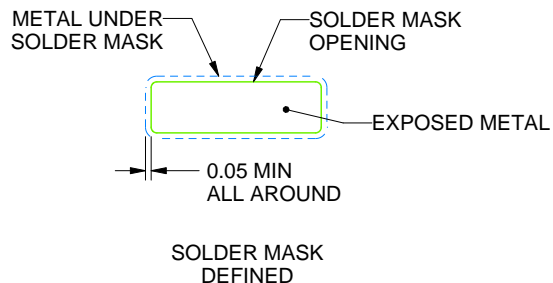5. Reference JEDEC Registration MO-345, Variation AA

16X (1.05)

SYMM

1

16

16X (0.3)

16

SYMM

14X (0.5)

8

9

(R0.05) TYP

(3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.05)

SYMM

1

16X (0.3)

16

SYMM

14X (0.5)

8

9

(R0.05) TYP

(3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D   07/2024

NOTES: (continued)
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

A

6.6
6.2 TYP

PIN 1 INDEX AREA

14X 0.65

16

1

2X

4.55

5.1
4.9
NOTE 3

8

9

16X 0.30
0.17

B

4.5
4.3
NOTE 4

⊕ 0.1 Ⓜ C A B

SEATING
PLANE

C

⌒ 0.1 C

4X (0° -12°)

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0°-8°

0.75
0.50

DETAIL A
TYPICAL

4220204/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

Texas
INSTRUMENTS
www.ti.com

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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