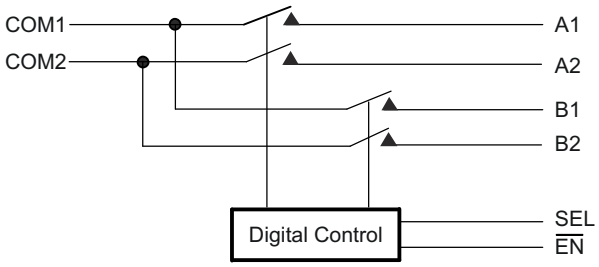
TMUX136 6-GHz, 2-Channel, 2:1 Switch, With Power-Off Isolation

1 Features

- V_{CC} range 2.3 V to 4.8 V
- High performance switch characteristics:
  - Bandwidth (–3 dB): 6.1 GHz
  - R_{ON} (typical): 5.7 Ω
  - C_{ON} (typical): 1.6 pF
- Current consumption: 30 µA (typical)
- Special features:
  - I_{OFF} protection prevents current leakage in Powered-Down state
  - 1.8-V compatible control inputs (SEL, $\overline{EN}$)
- Flow-through pinout simplifies PCB layout
- Compatible with high-speed I^3C signals
- ESD performance:
  - 5-kV Human Body Model (A114B, Class II)
  - 1-kV Charged-Device Model (C101)
- Compact 10-pin UQFN package (1.5-mm × 2-mm, 0.5-mm pitch)

2 Applications

- I^3C (SenseWire)
- Mobile industry processor interface (MIPI)
- Servers
- Handset: smartphone
- Notebook PC
- Tablet: multimedia
- Electronic point-of-sale
- Field instrumentation
- Portable monitor



Simplified Schematic

3 Description

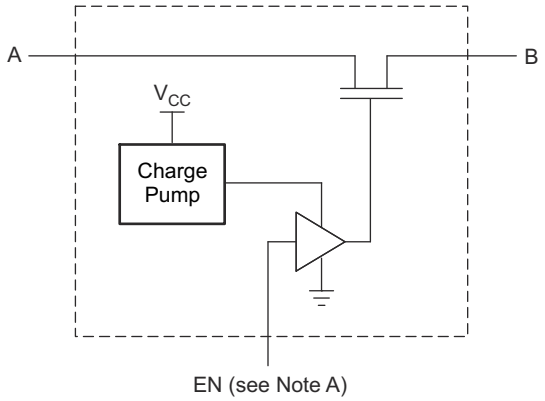
The TMUX136 device is a high performance, 6-GHz, 2-channel, 2:1 switch that will support both differential and single ended signals. The device has a wide V_{CC} range of 2.3 V to 4.8 V and supports a power-off protection feature forcing all I/O pins to be in high-impedance mode when power is not present on the V_{CC} pin. The select pins of TMUX136 are compatible with 1.8-V control voltage, allowing them to be directly interfaced with the General-Purpose I/O (GPIO) from low voltage processors. The flow-through pinout, where inputs and outputs are on opposite sides of the device, simplifies layout routing . This, along with the low on-resistance and low on-capacitance of the device, make the TMUX136 an optimal device for supporting switching a wide range of analog signals and digital communication protocol standards, including high-speed standards such as I^3C.

The TMUX136 comes in a small 10-pin UQFN package with only 1.5 mm × 2 mm in size, which makes it useful when PCB area is limited.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX136	RSE (UQFN, 10)	2 mm × 1.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Note A: EN is the internal enable signal applied to the switch.

Functional Block Diagram

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2020) to Revision E (June 2023)	Page
• Added the *I^3C (SenseWire)* application information to the data sheet	1
• Added the *Package Information* table	1

Changes from Revision C (July 2018) to Revision D (August 2020)	Page
• Added new specification limits to support added temperature range *T_A = -40°C to +125°C*	4

Changes from Revision B (November 2017) to Revision C (July 2018)	Page
• Changed pin 6 To: $\overline{EN}$, pin 7 To: COM2, and pin 8 To: COM1 in Figure 9-19	17

Changes from Revision A (October 2017) to Revision B (November 2017)	Page
• Changed Pin 7 From: COM1 To: COM2	3
• Changed Pin 8 From: COM2 To: COM1	3

Changes from Revision * (August 2017) to Revision A (October 2017)	Page
• Changed the HBM value From: ±3500 To: ±5000 in the *ESD Ratings* table	4

5 Pin Configuration and Functions

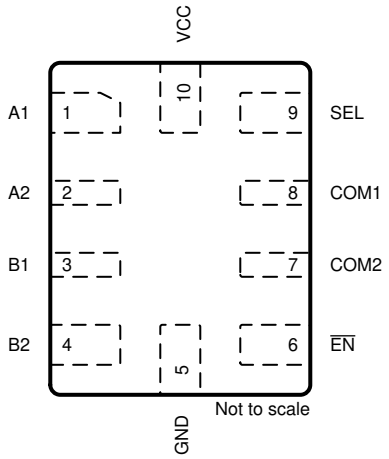


Figure 5-1. RSE Package, 10-Pin UQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	A1	I/O	Signal path A1
2	A2	I/O	Signal path A2
3	B1	I/O	Signal path B1
4	B2	I/O	Signal path B2
5	GND	—	Ground
6	$\overline{EN}$	I	Enable (active low)
7	COM2	I/O	Common signal path 2
8	COM1	I/O	Common signal path 1
9	SEL	I	Switch select (logic Low = COM to A PORT Logic High = COM to B PORT)
10	V_{CC}	—	Supply voltage

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(3)		–0.3	5.5	V
$V_{I/O}$	Input-output DC voltage(3)		–0.3	5.5	V
V_{SEL}, $V_{\overline{EN}}$	Digital input voltage (SEL, $\overline{EN}$)		–0.3	5.5	V
I_K	Input-output port diode current	VI/O < 0	–50		mA
I_{IK}	Digital logic input clamp current(3)	VI < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	4.8	V
$V_{I/O}$	Analog voltage	0	3.6	V
V_{SEL}, $V_{\overline{EN}}$	Digital input voltage (SEL, $\overline{EN}$)	0	V_{CC}	V
T_{RAMP} (V_{CC})	Power supply ramp time requirement (V_{CC})	100	1000	µs/V
$I_{I/O}$	Continuous current through I/O signal path (COMx, Ax, Bx) T_A = –40°C to +85°C		±20	mA
$I_{I/O}$	Continuous current through I/O signal path (COMx, Ax, Bx) T_A = –40°C to +125°C		±10	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TMUX136 RSE (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	191.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	117.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	117.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to +85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A PORT SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.7 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA		5.7	9	Ω
		V_{CC} = 2.3 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA		5.7	9.5	
		V_{CC} = 2.7 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA T_A = –40°C to +125°C			13	
		V_{CC} = 2.3 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA T_A = –40°C to +125°C			13	
ΔR_{ON}	ON-state resistance match between signal path 1 and 2	V_{CC} = 2.3 V	$V_{I/O}$ = 1.65 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON(FLAT)}$	ON-state resistance flatness	V_{CC} = 2.3 V	$V_{I/O}$ = 1.65 V to 3.45 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.8 V	Switch OFF, V_B = 1.65 V to 3.45 V, V_{COM} = 0 V	–2		2	µA
			Switch OFF, V_B = 1.65 V to 3.45 V, V_{COM} = 0 V T_A = –40°C to +125°C	–15		15	
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, V_B = 1.65 V to 3.45 V, V_{COM} = NC	–10		10	µA
			Switch ON or OFF, V_B = 1.65 V to 3.45 V, V_{COM} = NC T_A = –40°C to +125°C	–50		50	
I_{ON}	ON leakage current	V_{CC} = 4.8 V	Switch ON, V_B = 1.65 V to 3.45 V, V_{COM} = NC	–2		2	µA
			Switch ON, V_B = 1.65 V to 3.45 V, V_{COM} = NC T_A = –40°C to +125°C	–15		15	
		V_{CC} = 2.3 V	Switch ON, V_B = 1.65 V to 3.45 V, V_{COM} = NC	–125		125	
			Switch ON, V_B = 1.65 V to 3.45 V, V_{COM} = NC T_A = –40°C to +125°C	–175		175	
B PORT SWITCH							
R_{ON}	ON-state resistance	V_{CC} = 2.3 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		4.6	7.5	Ω
			$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA T_A = –40°C to +125°C			12	

6.5 Electrical Characteristics (continued)

T_A = –40°C to +85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔR_{ON}	ON-state resistance match between signal path 1 and 2	V_{CC} = 2.3 V	$V_{I/O}$ = 0.4 V, I_{ON} = –8 mA		0.1		Ω
R_{ON} (FLAT)	ON-state resistance flatness	V_{CC} = 2.3 V	$V_{I/O}$ = 0 V to 0.4 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{CC} = 4.8 V	Switch OFF, V_A = 0 V to 3.6 V, V_{COM} = 0 V	–2		2	µA
			Switch OFF, V_A = 0 V to 3.6 V, V_{COM} = 0 V T_A = –40°C to +125°C	–15		15	
I_{OFF}	Power-off leakage current	V_{CC} = 0 V	Switch ON or OFF, V_A = 0 V to 3.6 V, V_{COM} = NC	–10		10	µA
			Switch ON or OFF, V_A = 0 V to 3.6 V, V_{COM} = NC T_A = –40°C to +125°C	–50		50	
I_{ON}	ON leakage current	V_{CC} = 4.8 V	Switch ON, V_A = 0 V to 3.6 V, $V_{D±}$ = NC	–2		2	µA
		V_{CC} = 4.8 V	Switch ON, V_A = 0 V to 3.6 V, $V_{D±}$ = NC T_A = –40°C to +125°C	–15		15	
		V_{CC} = 2.3 V	Switch ON, V_A = 0 V to 3.6 V, V_B = NC	–125		125	
		V_{CC} = 2.3 V	Switch ON, V_A = 0 V to 3.6 V, V_B = NC T_A = –40°C to +125°C	–175		175	
DIGITAL CONTROL INPUTS (SEL, $\overline{EN}$)							
V_{IH}	Input logic high	V_{CC} = 2.3 V to 4.8 V T_A = –40°C to +125°C		1.3			V
V_{IL}	Input logic low	V_{CC} = 2.3 V to 4.8 V T_A = –40°C to +125°C				0.6	V
I_{IN}	Input leakage current	V_{CC} = 4.8 V, $V_{I/O}$ = 0 V to 3.6 V, V_{IN} = 0 to 4.8 V		–10		10	µA

6.6 Dynamic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{ON}	PORT B ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.6	2	pF
	PORT A ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V, f = 240 MHz	Switch ON		1.4	2	pF
C_{OFF}	PORT B OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V f = 240 MHz	Switch OFF		1.4	2	pF
	PORT A OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 0 or 3.3 V f = 240 MHz	Switch OFF		1.6	2	pF
C_I	Digital input capacitance	V_{CC} = 3.3 V, V_I = 0 or 2 V			2.2		pF
O_{ISO}	OFF Isolation	V_{CC} = 2.3 V to 4.8 V, R_L = 50 Ω, f = 240 MHz	Switch OFF		–34		dB
X_{TALK}	Crosstalk	V_{CC} = 2.3 V to 4.8 V, R_L = 50 Ω, f = 240 MHz	Switch ON		–37		dB
BW	–3-dB bandwidth	V_{CC} = 2.3 V to 4.8 V, R_L = 50 Ω,	Switch ON		6.1		GHz
SUPPLY							
V_{CC}	Power supply voltage			2.3		4.8	V
I_{CC}	Positive supply current	V_{CC} = 4.8 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF			30	50	μA
		V_{CC} = 4.8 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF T_A = –40°C to +125°C				70	
$I_{cc, HZ}$	Power supply current in high-Z mode	V_{CC} = 4.8 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF, $\overline{OE}$ = H			5	10	μA
		V_{CC} = 4.8 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V, Switch ON or OFF, $\overline{OE}$ = H T_A = –40°C to +125°C				20	

6.7 Timing Requirements

				MIN	NOM	MAX	UNIT
t_{pd}	Propagation delay		R_L = 50 Ω, C_L = 5 pF, V_{CC} = 2.3 V to 4.8 V		100		ps
t_{switch}	Switching time (SEL to output)					600	ns
$t_{ZH, ZL}$	Enable time ($\overline{EN}$ to output)	$V_{I/O}$ = 3.3 V or 0 V			100		μs
$t_{HZ, LZ}$	Disable time ($\overline{EN}$ to output)				200		ns
$t_{SK(P)}$	Skew of opposite transitions of same output				20		ps

6.8 Typical Characteristics

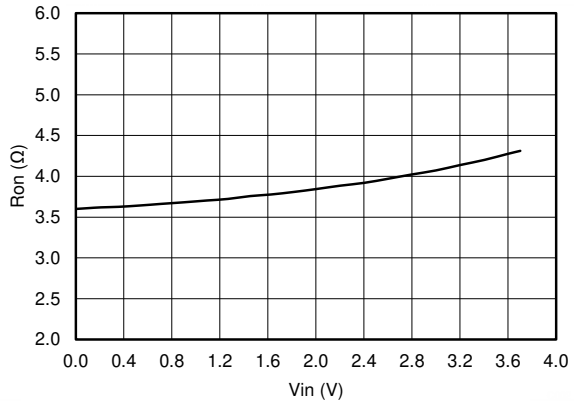


Figure 6-1. ON-Resistance vs $V_{I/O}$

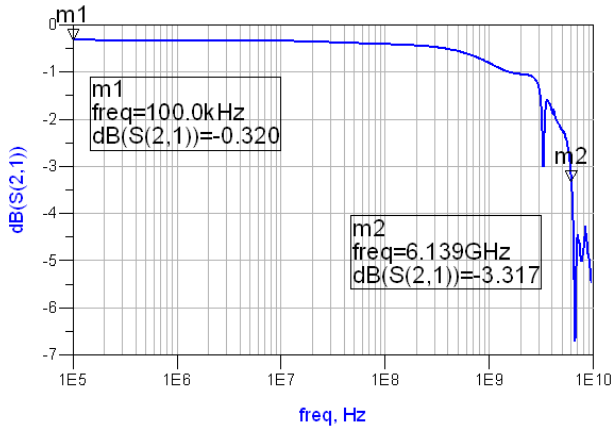


Figure 6-2. Bandwidth

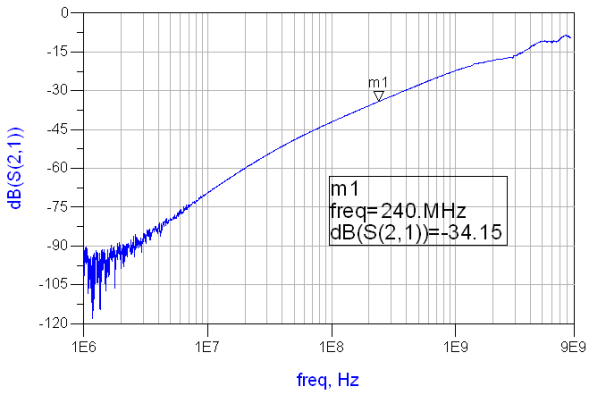


Figure 6-3. Off Isolation

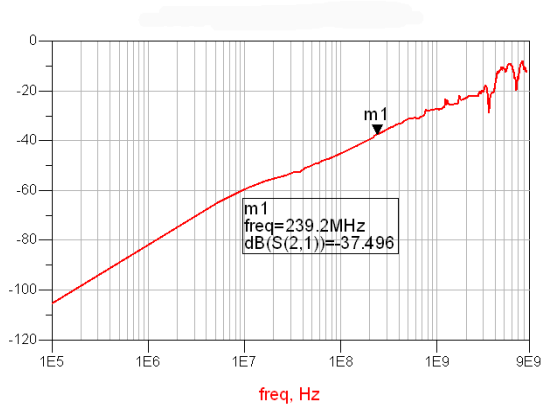
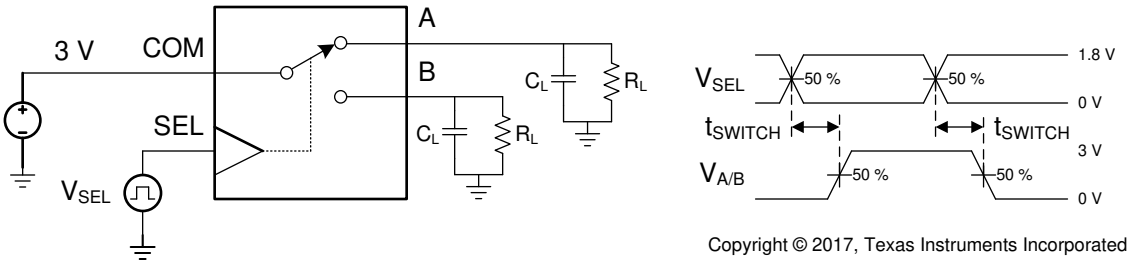


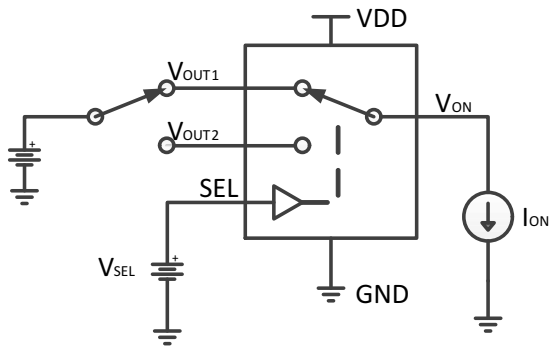
Figure 6-4. Cross Talk

7 Parameter Measurement Information



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r < 5 ns, t_f < 5 ns.
B. C_L includes probe and jig capacitance.

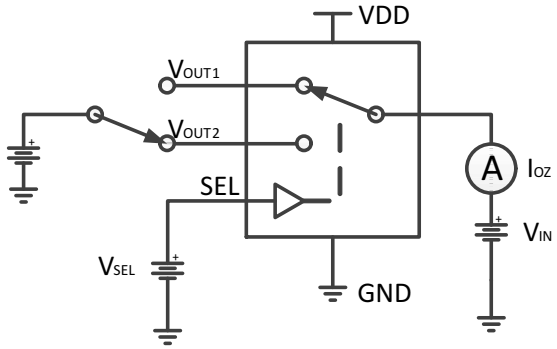
Figure 7-1. Timing Diagram



Channel ON

R_{ON} = (V_{ON} – $V_{I/O1}$) / I_{ON} or (V_{ON} – $V_{I/O2}$) / I_{ON}
V_{SEL} = H or L

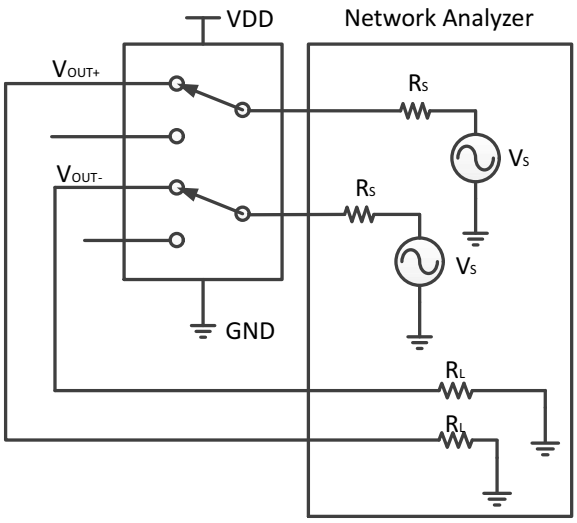
Figure 7-2. ON-State Resistance (R_{ON})



Channel OFF

V_{SEL} = H or L

Figure 7-3. OFF Leakage Current (I_{OZ})



Channel ON

V_{SEL} = H or L
R_S=R_L=50Ω

Figure 7-4. Bandwidth (BW)

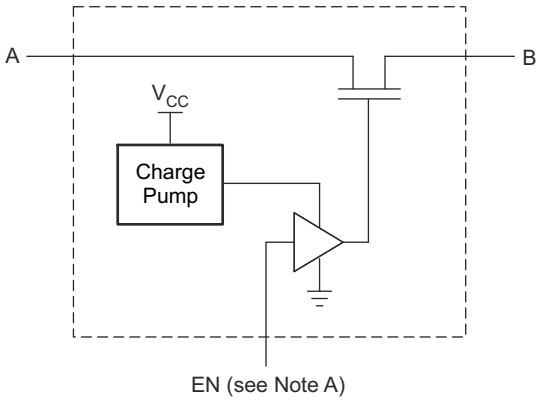
8 Detailed Description

8.1 Overview

The TMUX136 device is a 2-channel, 2:1, switch specifically designed for the switching of high-speed signals in handset and consumer applications, such as cell phones, tablets, and notebooks but may be used for any high speed application. The wide bandwidth (6.1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs and will support both single-ended and differential signals. The device also has a low power mode that reduces the power consumption to 5 µA for portable applications with a battery or limited power budget.

The TMUX136 device integrates ESD protection cells on all pins, is available in a tiny UQFN package (1.5 mm × 2 mm) and is characterized over the free-air temperature range from –40°C to +125°C.

8.2 Functional Block Diagram



Note A: EN is the internal enable signal applied to the switch.

8.3 Feature Description

8.3.1 Low Power Mode

The TMUX136 has a low power mode that reduces the power consumption to 5 µA while the device is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{EN}$ must be supplied with a logic High signal.

8.4 Device Functional Modes

8.4.1 High Impedance Mode

The TMUX136 has a high impedance mode that places all the signal paths in a Hi-Z state while the device is not in use. As provided in Table 8-1, to put the device in high impedance mode and disable the switch, the bus-switch enable pin $\overline{EN}$ must be supplied with a logic *High* signal.

Table 8-1. Function Table

SEL	$\overline{EN}$	SWITCH STATUS
X	High	Both A PORT and B PORT switches in High-Z
Low	Low	COM to A PORT
High	Low	COM to B PORT

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

There are many applications in which microprocessors or controllers have a limited number of I/Os. The TMUX136 solution can effectively expand the limited I/Os by switching between multiple buses to interface them to a single microprocessor or controller. A common application where the TMUX136 is as a I3C 1:2 multiplexer. In this application, the TMUX136 is used to route communicating between different DDR modules from a single controller within a server, as shown in Figure 9-1. The high bandwidth of the TMUX136 will preserve signal integrity at even the fastest communication protocols that may be used in server applications, such as I^3C.

9.2 Typical Application

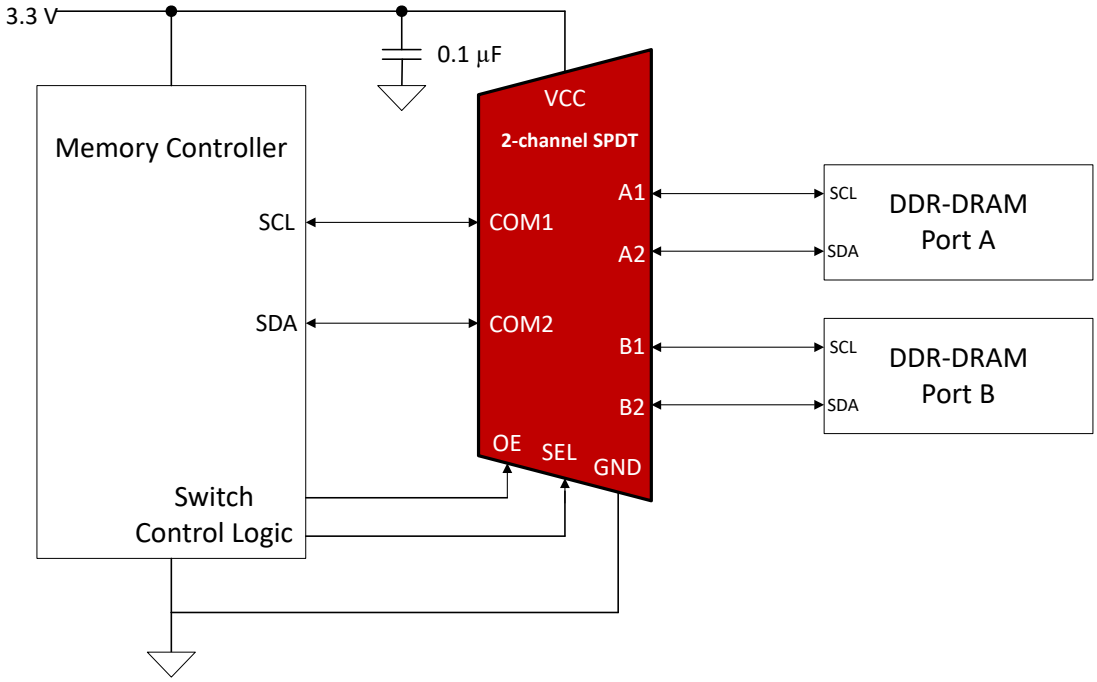


Figure 9-1. Typical Application

The TMUX136 supports I^3C standard by maintaining signal integrity through the switch. Table 9-1 details how the TMUX136 specifications make this device optimal for switching I^3C signals.

Table 9-1. TMUX136 I^3C Compatibility

	I^3C Requirements	TMUX136 Specification
Voltage (I/O)	1.0 V, 1.2 V, 1.8 V, 3.3 V	0-3.6 V
Frequency	Up to 12.5 MHz	6 GHz Bandwidth
Capacitance	50 pF maximum bus capacitance	<2 pF On/Off Capacitance

9.2.1 Design Requirements

The TMUX136 has internal 6-MΩ pull-down resistors on SEL and $\overline{EN}$, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL allows the PORT A channel to be selected by default. The internal pull-down resistor on $\overline{EN}$ enables the switch when power is applied to V_{CC}.

9.2.2 Detailed Design Procedure

The TMUX136 can operate without any external components; however, TI recommends that unused pins must be connected to ground through a 50-Ω resistor to prevent signal reflections back into the device.

9.2.3 Application Curves

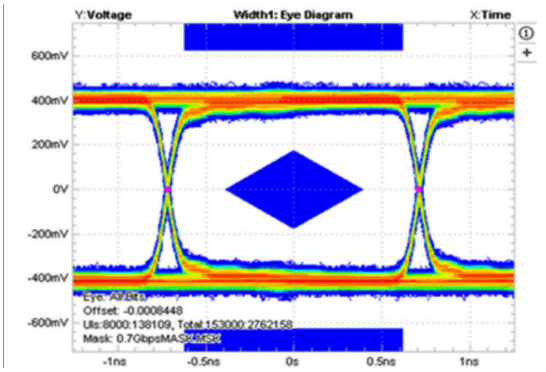


Figure 9-2. Eye Pattern: 0.7 Gbps with No Device

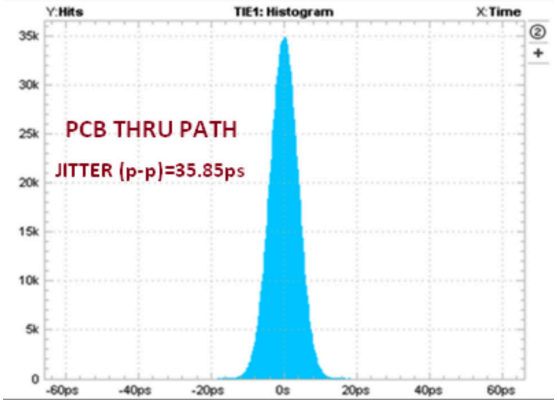
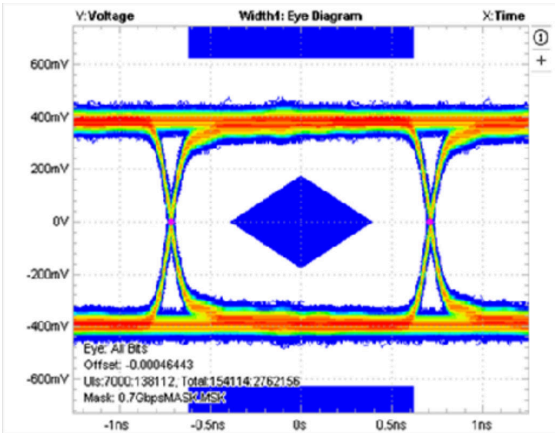
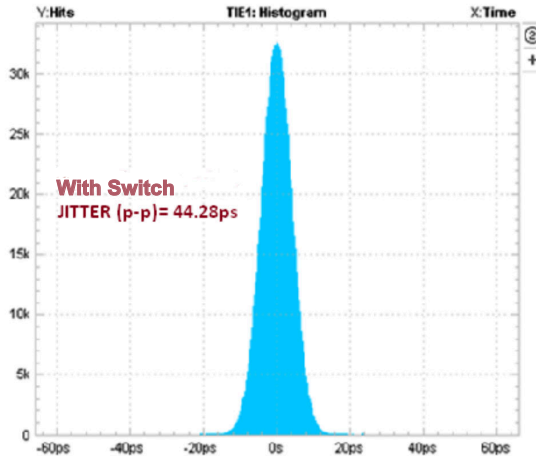


Figure 9-3. Time Interval Error Histogram: 0.7 Gbps with No Device



The TMUX136 contributes only 8.4 ps of peak-to-peak jitter for 0.7-Gbps data rate

Figure 9-4. Eye Pattern: 0.7 Gbps with Switch



The TMUX136 contributes only 8.4 ps of peak-to-peak jitter for 0.7-Gbps data rate

Figure 9-5. Time Interval Error Histogram: 0.7 Gbps with Switch

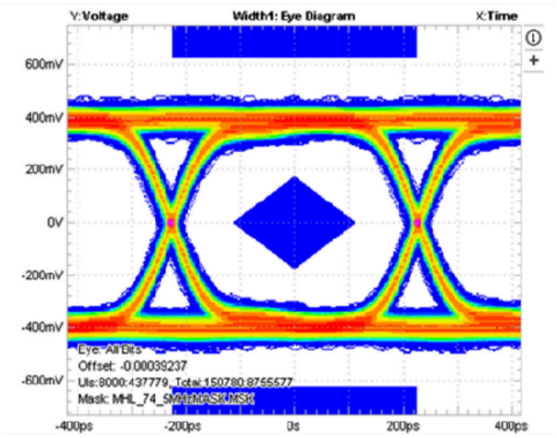


Figure 9-6. Eye Pattern: 2.2 Gbps with No Device

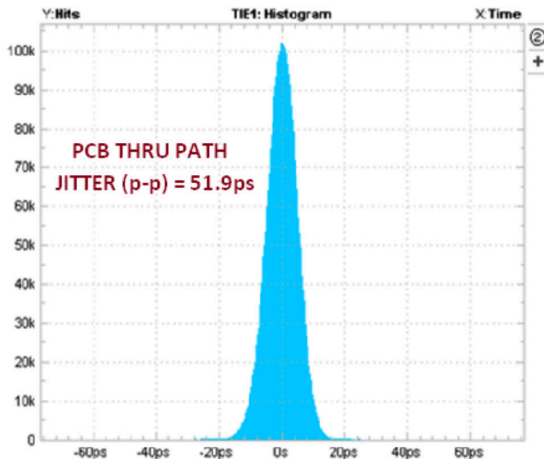
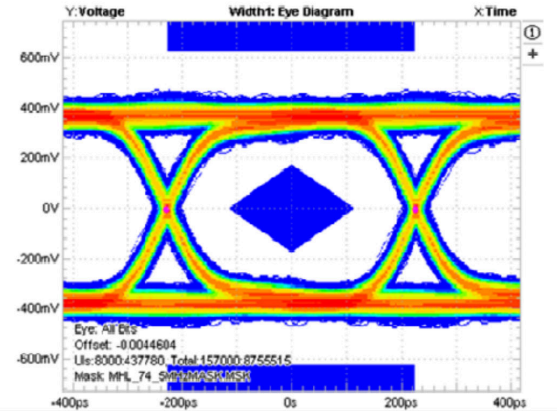
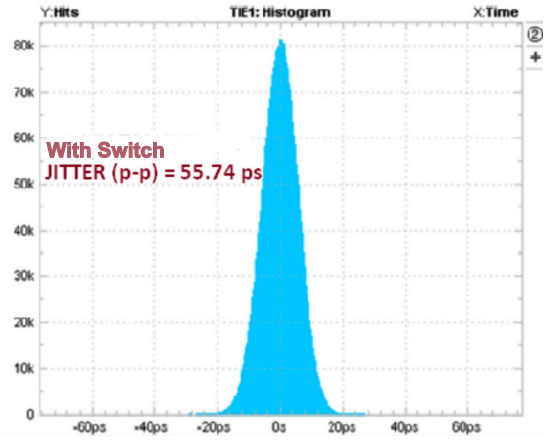


Figure 9-7. Time Interval Error Histogram: 2.2 Gbps with No Device



The TMUX136 contributes only 3.8 ps of peak-to-peak jitter for 2.2-Gbps data rate

Figure 9-8. Eye Pattern: 2.2 Gbps with Switch



The TMUX136 contributes only 3.8 ps of peak-to-peak jitter for 2.2-Gbps data rate

Figure 9-9. Time Interval Error Histogram: 2.2 Gbps with Switch

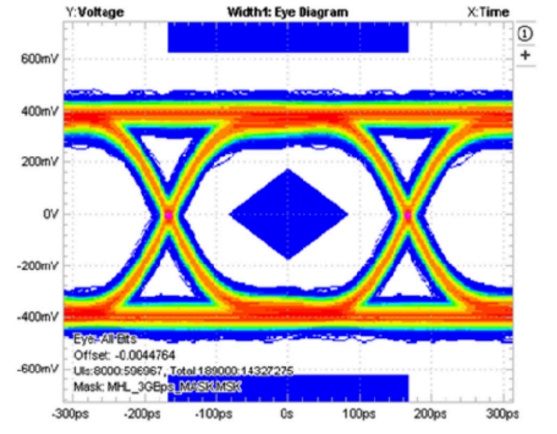


Figure 9-10. Eye Pattern: 3 Gbps with No Device

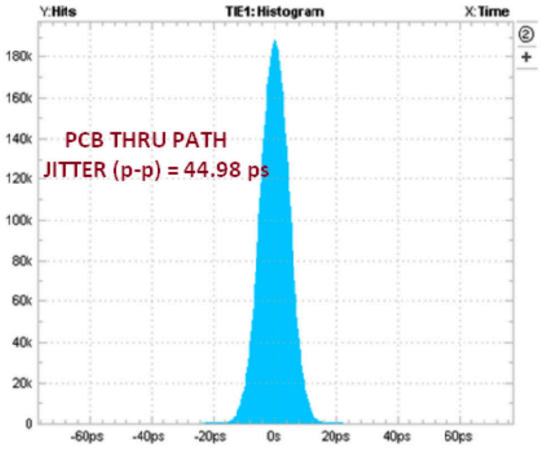
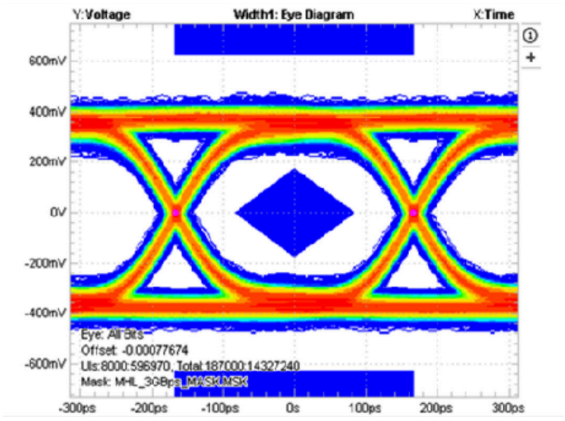
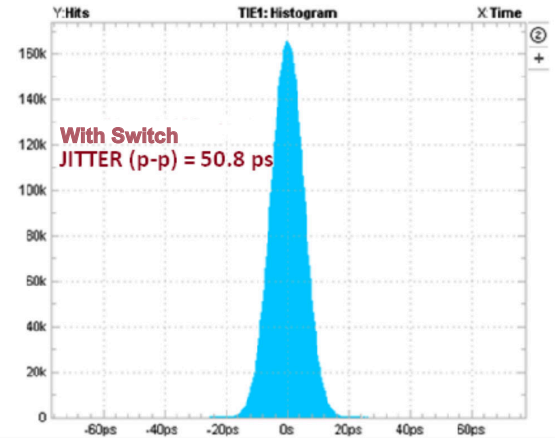


Figure 9-11. Time Interval Error Histogram: 3 Gbps with No Device



The TMUX136 contributes only 5.8 ps of peak-to-peak jitter for 3-Gbps data rate

Figure 9-12. Eye Pattern: 3 Gbps with Switch



The TMUX136 contributes only 5.8 ps of peak-to-peak jitter for 3-Gbps data rate

Figure 9-13. Time Interval Error Histogram: 3 Gbps with Switch

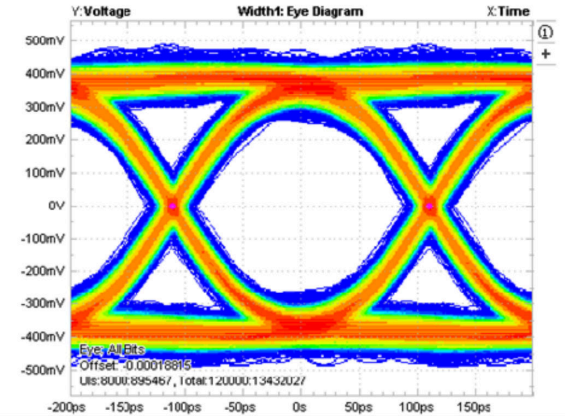


Figure 9-14. Eye Pattern: 4.5 Gbps with No Device

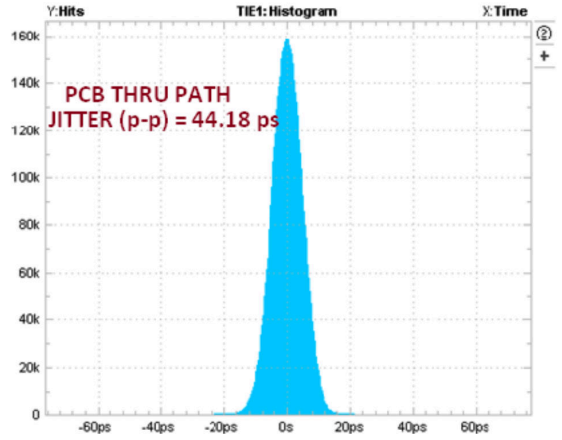
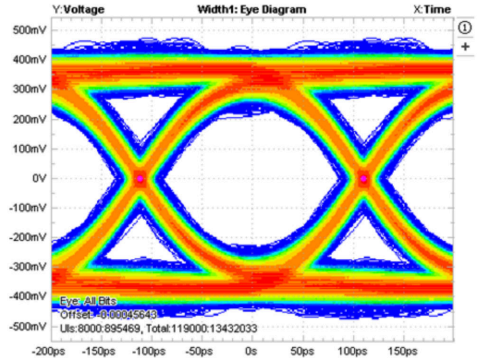
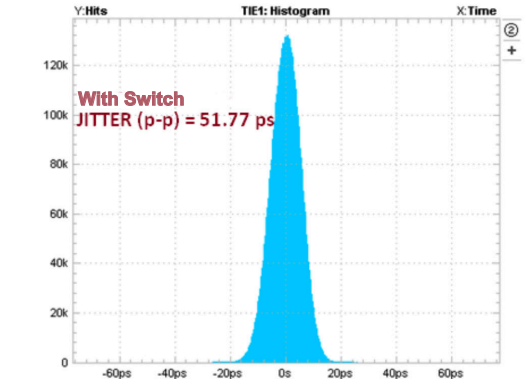


Figure 9-15. Time Interval Error Histogram: 4.5 Gbps with No Device



The TMUX136 contributes only 7.6 ps of peak-to-peak jitter for 4.5-Gbps data rate

Figure 9-16. Eye Pattern: 4.5 Gbps with Switch



The TMUX136 contributes only 7.6 ps of peak-to-peak jitter for 4.5-Gbps data rate

Figure 9-17. Time Interval Error Histogram: 4.5 Gbps with Switch

9.3 Power Supply Recommendations

TI recommends placing a bypass capacitor as close to the supply pin V_{CC} as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

9.4 Layout

9.4.1 Layout Guidelines

Place supply bypass capacitors as close to V_{CC} pin as possible and avoid placing the bypass capacitors near the high speed traces.

The high-speed signal paths must should be no more than 4 inches long; otherwise, the eye diagram performance may be degraded.

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed signals traces because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 9-18.

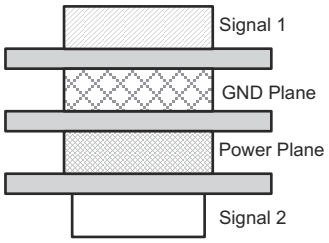


Figure 9-18. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

9.4.2 Layout Example

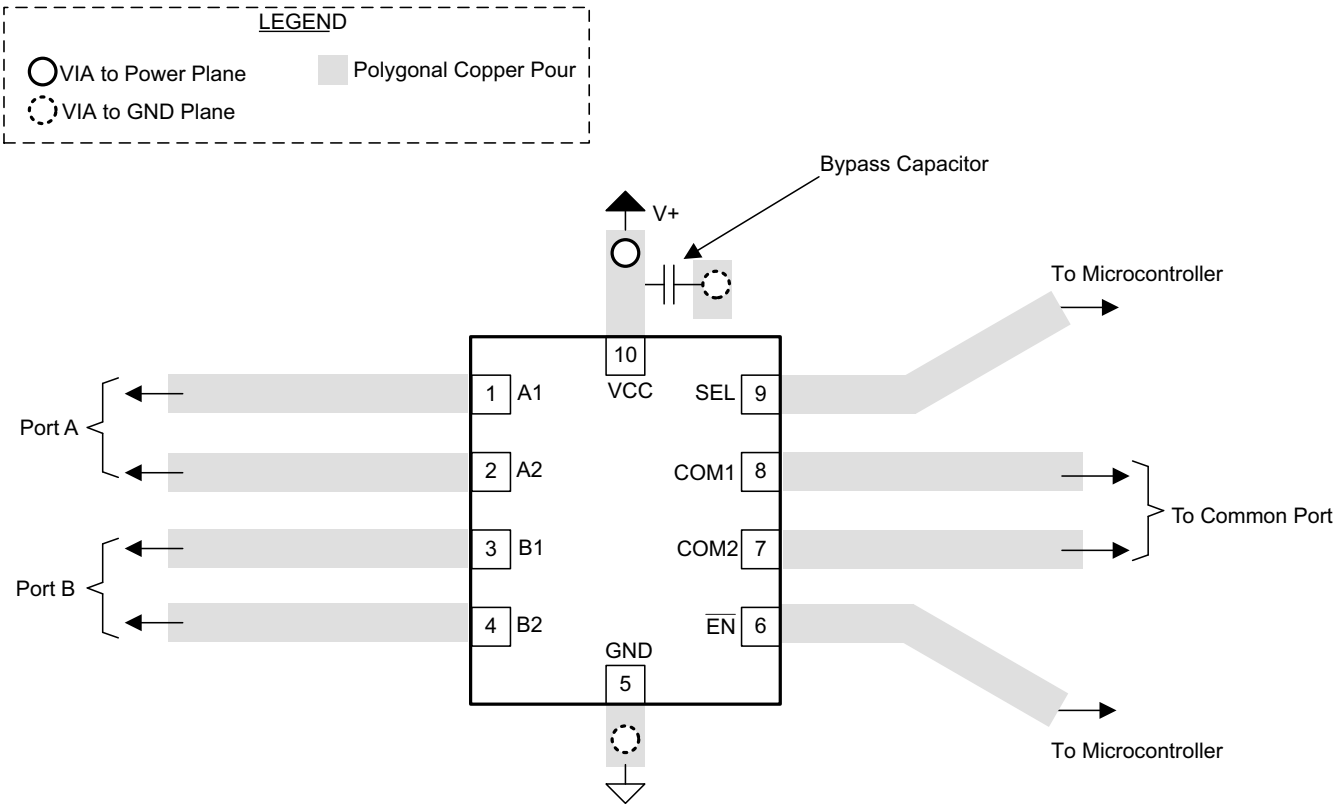


Figure 9-19. Package Layout Diagram

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *High-Speed Layout Guidelines Application Report*
- Texas Instruments, *High-Speed Interface Layout Guidelines*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX136MRSER	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19H
TMUX136MRSER.A	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19H
TMUX136MRSERG4.A	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19H
TMUX136RSER	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19G
TMUX136RSER.A	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19G
TMUX136RSERG4.A	Active	Production	UQFN (RSE) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19G

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

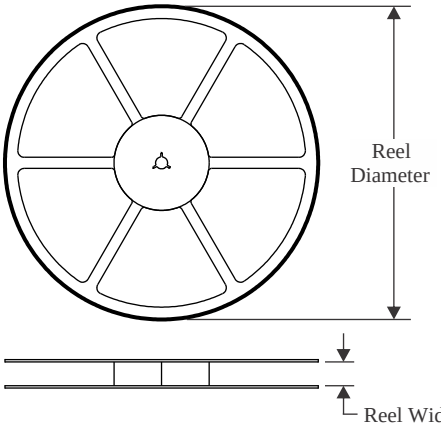
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

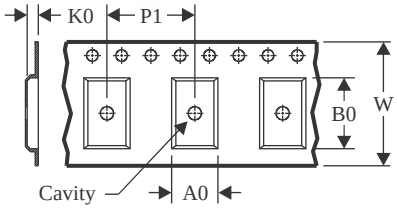
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

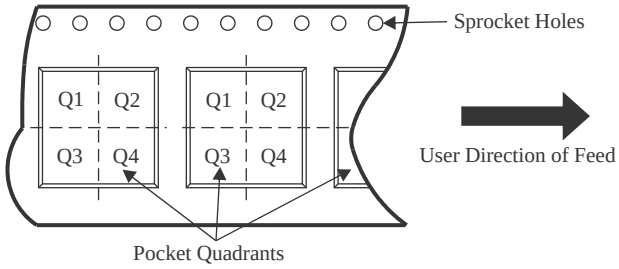


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

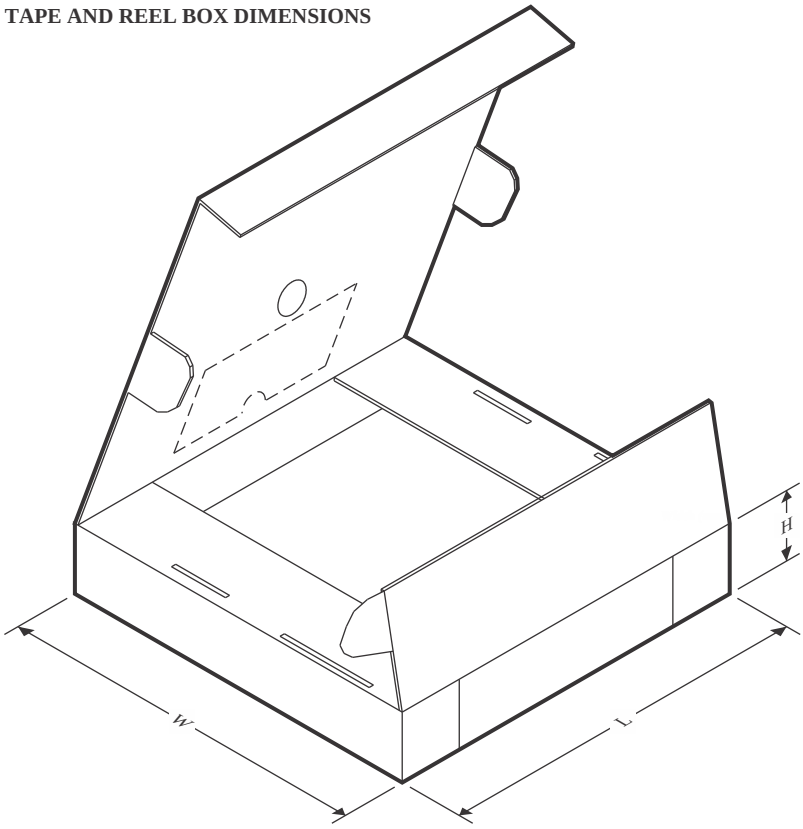
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX136MRSER	UQFN	RSE	10	3000	180.0	9.5	2.2	1.8	0.75	4.0	8.0	Q3
TMUX136RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

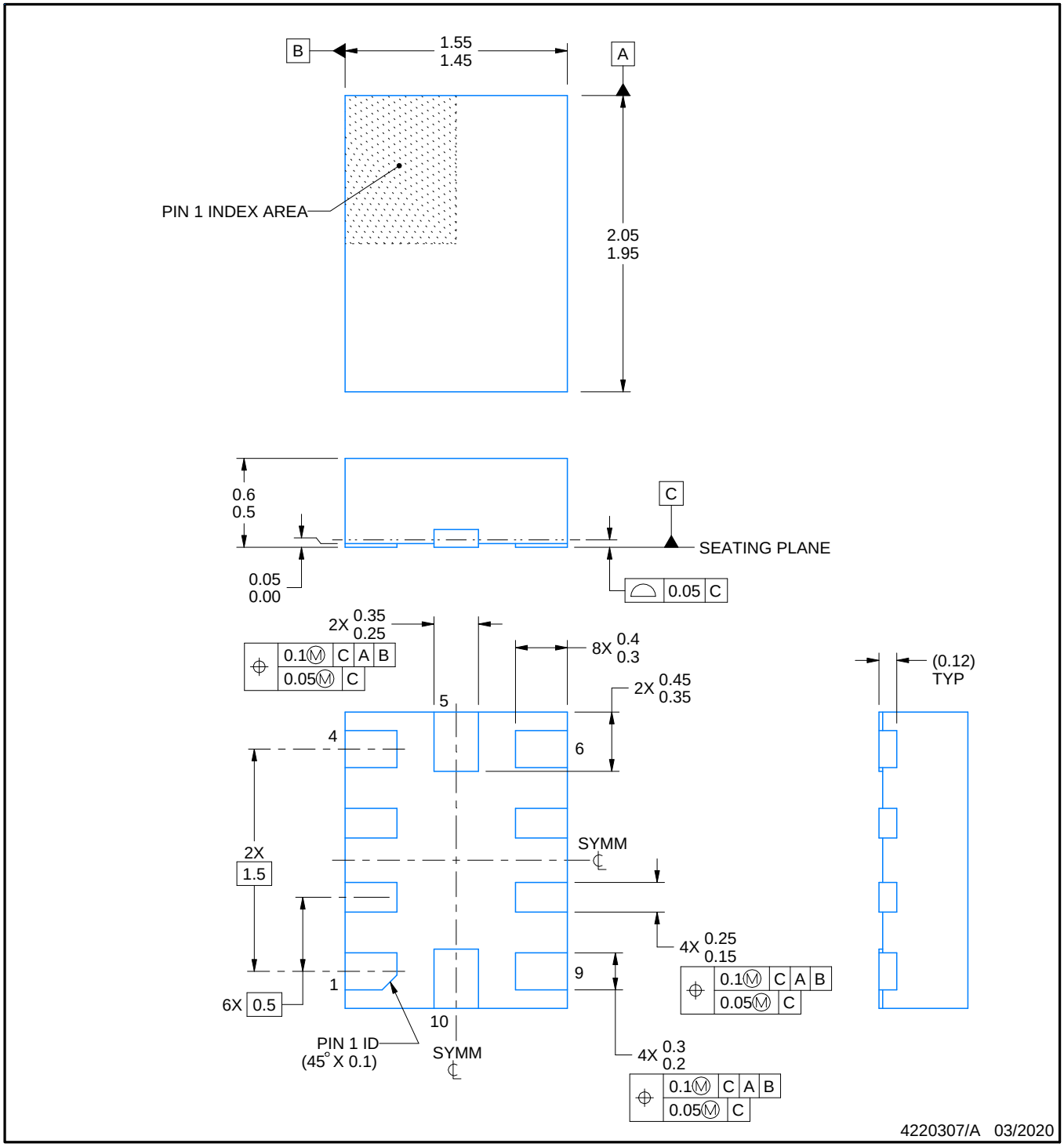
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX136MRSER	UQFN	RSE	10	3000	189.0	185.0	36.0
TMUX136RSER	UQFN	RSE	10	3000	189.0	185.0	36.0

RSE0010A

PACKAGE OUTLINE

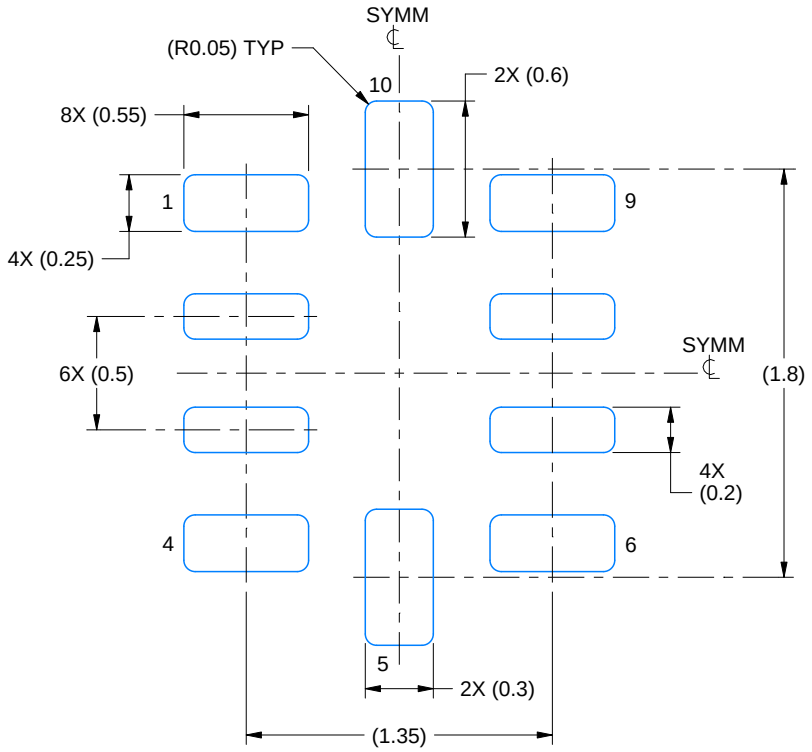
UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

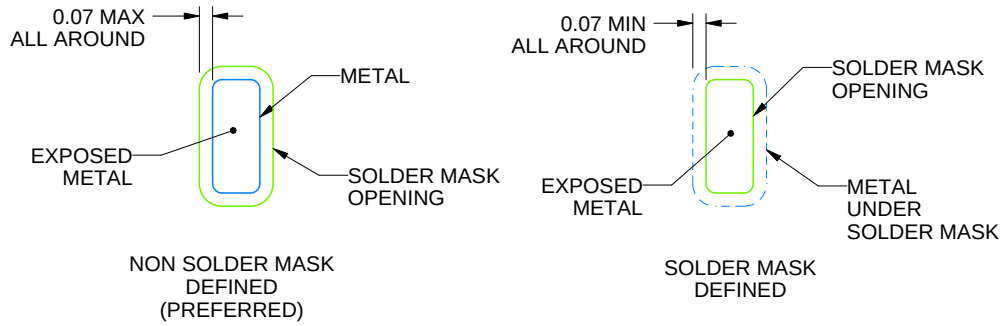


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

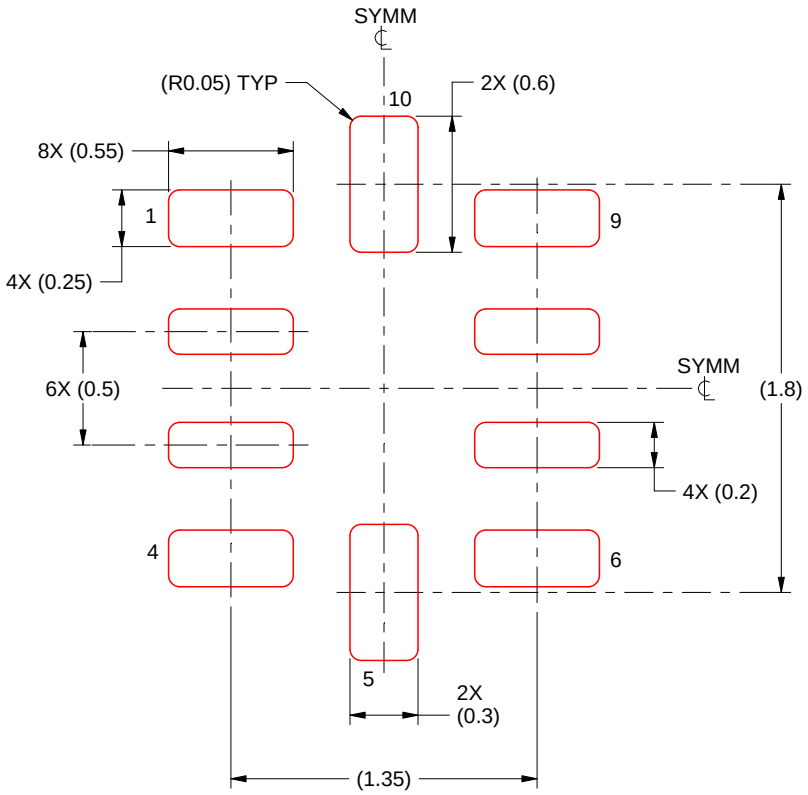


SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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