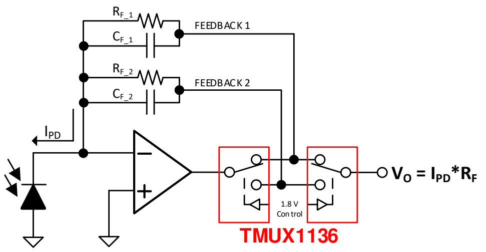
TMUX1136 5V Low-Leakage-Current, 2:1, 2-Channel Precision Analog Switch

1 Features

- Wide supply range: 1.08V to 5.5V
- Low leakage current: 3pA
- Low on-resistance: 2Ω
- Low charge injection: –6pC
- -40°C to +125°C operating temperature
- 1.8V logic compatible
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional signal path
- Break-before-make switching
- ESD protection HBM: 2000V

2 Applications

- Ultrasound scanners
- Patient monitoring and diagnostics
- Blood glucose monitors
- Optical networking
- Optical test equipment
- Remote radio units
- Power amplifier switching
- Data acquisition systems
- ATE test equipment
- Factory automation and industrial controls
- Flow transmitters
- Programmable logic controllers (PLC)
- Analog input modules
- SONAR receivers
- Battery monitoring systems



Application Example

3 Description

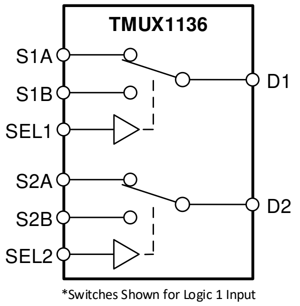
The TMUX1136 is a complementary metal-oxide semiconductor (CMOS) single-pole double-throw (2:1) switch with two independently controlled channels. A wide operating supply of 1.08V to 5.5V makes this device an excellent choice for a broad array of applications from medical equipment to industrial systems. The device supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from GND to V_{DD}. All logic inputs have 1.8V logic compatible thresholds, allowing for both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

The TMUX1136 is part of the precision switches and multiplexers family of devices. These devices have very low on and off leakage currents and low charge injection, allowing them to be used in high precision measurement applications. A low supply current of 3nA and small package options enable use in portable applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX1136	DGS (VSSOP, 10)	3mm × 4.9mm
	DQA (USON, 10)	2.5mm × 1mm

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

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4 Pin Configuration and Functions

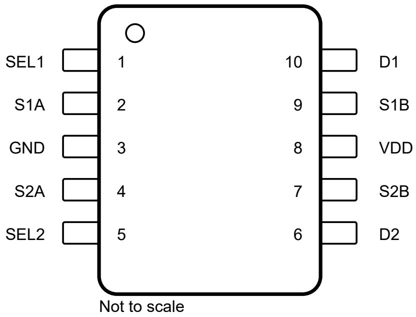


Figure 4-1. DGS Package 10-Pin VSSOP (Top View)

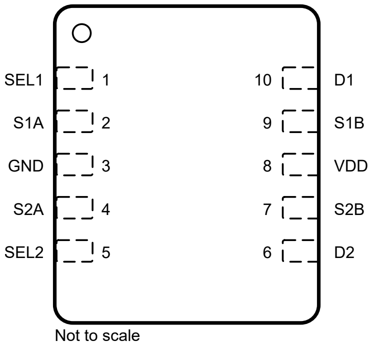


Figure 4-2. DQA Package 10-Pin USON (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
SEL1	1	I	Select pin 1: controls state of switch #1 according to Table 7-1. (Logic Low = S1B to D1, Logic High = S1A to D1)
S1A	2	I/O	Source pin 1A. Can be an input or output.
GND	3	P	Ground (0V) reference
S2A	4	I/O	Source pin 2A. Can be an input or output.
SEL2	5	I	Select pin 2: controls state of switch #2 according to Table 7-1. (Logic Low = S2B to D2, Logic High = S2A to D2)
D2	6	I/O	Drain pin 2. Can be an input or output.
S2B	7	I/O	Source pin 2B. Can be an input or output.
VDD	8	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between V_{DD} and GND.
S1B	9	I/O	Source pin 1B. Can be an input or output.
D1	10	I/O	Drain pin 1. Can be an input or output.

(1) I = input, O = output, I/O = input and output, P = power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	6	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	–0.5	6	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	–30	30	mA
V_S or V_D	Source or drain voltage (SxA, SxB, Dx)	–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (SxA, SxB, Dx)	I_{DC} ± 10 %(3)	I_{DC} ± 10 %(3)	mA
I_S or $I_{D\ (PEAK)}$	Source and drain peak current: (1ms period max, 10% duty cycle maximum) (SxA, SxB, Dx)	I_{peak} ± 10 %(3)	I_{peak} ± 10 %(3)	mA
T_{stg}	Storage temperature	–65	150	°C
P_{tot}	Total power dissipation(4) (5)		500	mW
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) Refer to Recommended Operating Conditions for I_{DC} and I_{Peak} ratings
(4) For DGS(VSSOP) package: P_{tot} derates linearly above TA=53°C by 5.16mW/°C
(5) For DQA(USON) package: P_{tot} derates linearly above TA=63°C by 5.81mW/°C

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (SxA, SxB, Dx)		0		V_{DD}	V
V_{SEL}	Logic control input pin voltage (SELx)		0		5.5	V
T_A	Ambient temperature		–40		125	°C
I_{DC}	Continuous current through switch	Tj = 25°C		150		mA
		Tj = 85°C		120		mA
		Tj = 125°C		60		mA
		Tj = 130°C		50		mA
I_{peak}	Peak current through switch(1ms period max, 10% duty cycle maximum)	Tj = 25°C		300		mA
		Tj = 85°C		300		mA
		Tj = 125°C		180		mA
		Tj = 130°C		160		mA

5.4 Thermal Information

THERMAL METRIC(1)		TMUX1136		UNIT
		DGS (VSSOP)	DQA (USON)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.9	172.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.1	79.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	116.5	72.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	22.0	9.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	114.6	71.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics (V_{DD} = 5V ±10 %)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		2	4	Ω
			–40°C to +85°C			4.5	Ω
			–40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		0.85		Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.6	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 5V Switch Off V_D = 4.5V / 1.5V V_S = 1.5V / 4.5V Refer to Section 6.2	25°C	–0.08	±0.005	0.08	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.9		0.9	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5V Switch On V_D = V_S = 2.5V Refer to Section 6.3	25°C	–0.025	±0.003	0.025	nA
			–40°C to +85°C	–0.3		0.3	nA
			–40°C to +125°C	–0.95		0.95	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5V Switch On V_D = V_S = 4.5V / 1.5V Refer to Section 6.3	25°C	–0.1	±0.01	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	1.49		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							

5.5 Electrical Characteristics (V_{DD} = 5V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.003		μA
			–40°C to +125°C			1	μA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 3V R_L = 200Ω, C_L = 15pF Refer to Section 6.4	25°C		12		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3V R_L = 200Ω, C_L = 15pF Refer to Section 6.5	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1V R_S = 0Ω, C_L = 1nF Refer to Section 6.6	25°C		–6		pC
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.7	25°C		–65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.7	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.8	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.8	25°C		–80		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF Refer to Section 6.9	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 4.5V, V_D is 1.5V or when V_S is 1.5V, V_D is 4.5V.

5.6 Electrical Characteristics (V_{DD} = 3.3V ±10 %)

at T_A = 25°C, V_{DD} = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		3.7	8.8	Ω
			–40°C to +85°C			9.5	Ω
			–40°C to +125°C			9.8	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		0.13		Ω
			–40°C to +85°C			0.4	Ω
			–40°C to +125°C			0.5	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		1.9		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		2.2		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3V Switch Off V_D = 3V / 1V V_S = 1V / 3V Refer to Section 6.2	25°C	–0.05	±0.001	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA

5.6 Electrical Characteristics (V_{DD} = 3.3V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3V Switch On V_D = V_S = 3V / 1V Refer to Section 6.3	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.35		0.35	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	1.35		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		-40°C to 125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.003		µA
			–40°C to +125°C			0.8	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 2V R_L = 200Ω, C_L = 15pF Refer to Section 6.4	25°C		14		ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			21	ns
t_{OPEN} (BBM)	Break before make time	V_S = 2V R_L = 200Ω, C_L = 15pF Refer to Section 6.5	25°C		9		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1V R_S = 0Ω, C_L = 1nF Refer to Section 6.6	25°C		–6		pC
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.7	25°C		–65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.7	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.8	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.8	25°C		–80		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF Refer to Section 6.9	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 3V, V_D is 1V or when V_S is 1V, V_D is 3V.

5.7 Electrical Characteristics (V_{DD} = 1.8V ±10 %)

at T_A = 25°C, V_{DD} = 1.8V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							

5.7 Electrical Characteristics (V_{DD} = 1.8V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 1.8V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.98V Switch Off V_D = 1.62V / 1V V_S = 1V / 1.62V Refer to Section 6.2	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98V Switch On V_D = V_S = 1.62V / 1V Refer to Section 6.3	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.001		µA
			–40°C to +125°C			0.85	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to Section 6.4	25°C		28		ns
			–40°C to +85°C			44	ns
			–40°C to +125°C			44	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to Section 6.5	25°C		16		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1V R_S = 0Ω, C_L = 1nF Refer to Section 6.6	25°C		–3		pC
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.7	25°C		–65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.7	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.8	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.8	25°C		–80		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF	25°C		220		MHz

5.7 Electrical Characteristics (V_{DD} = 1.8V ±10 %) (continued)

at T_A = 25°C, V_{DD} = 1.8V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 1.62V, V_D is 1V or when V_S is 1V, V_D is 1.62V.

5.8 Electrical Characteristics (V_{DD} = 1.2V ±10 %)

at T_A = 25°C, V_{DD} = 1.2V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0V to V_{DD} I_{SD} = 10mA Refer to Section 6.1	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32V Switch Off V_D = 1V / 0.8V V_S = 0.8V / 1V Refer to Section 6.2	25°C	–0.05	±0.003	0.05	nA
			–40°C to +85°C	–0.1		0.1	nA
			–40°C to +125°C	–0.5		0.5	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32V Switch On V_D = V_S = 1V / 0.8V Refer to Section 6.3	25°C	–0.1	±0.005	0.1	nA
			–40°C to +85°C	–0.5		0.5	nA
			–40°C to +125°C	–2		2	nA
LOGIC INPUTS (SELx)							
V_{IH}	Input logic high		–40°C to +125°C	0.96		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0V or 5.5V	25°C		0.003		µA
			–40°C to +125°C			0.7	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Transition time between channels	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to Section 6.4	25°C		55		ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			190	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1V R_L = 200Ω, C_L = 15pF Refer to Section 6.5	25°C		28		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_D = 1V R_S = 0Ω, C_L = 1nF Refer to Section 6.6	25°C		–2		pC

5.8 Electrical Characteristics (V_{DD} = 1.2V ±10 %) (continued)

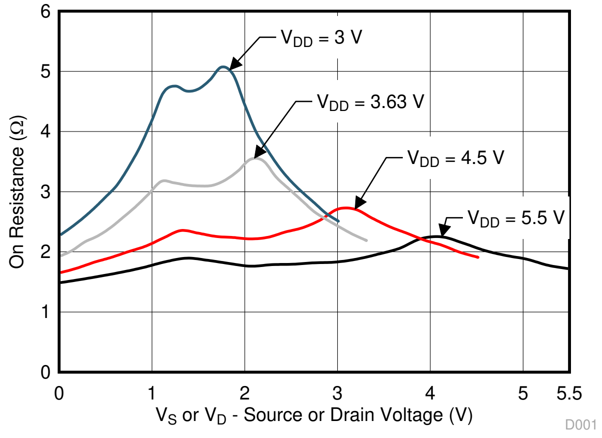
at T_A = 25°C, V_{DD} = 1.2V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
O_{ISO}	Off Isolation	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.7	25°C		–65		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.7	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50Ω, C_L = 5pF f = 1MHz Refer to Section 6.8	25°C		–100		dB
		R_L = 50Ω, C_L = 5pF f = 10MHz Refer to Section 6.8	25°C		–80		dB
BW	Bandwidth	R_L = 50Ω, C_L = 5pF	25°C		220		MHz
C_{SOFF}	Source off capacitance	f = 1MHz	25°C		6		pF
C_{SON} C_{DON}	On capacitance	f = 1MHz	25°C		20		pF

(1) When V_S is 1V, V_D is 0.8V or when V_S is 0.8V, V_D is 1V.

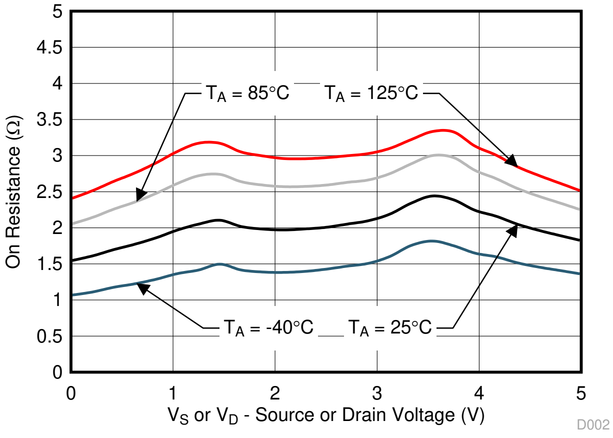
Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



T_A = 25°C

Figure 5-1. On-Resistance vs Source or Drain Voltage

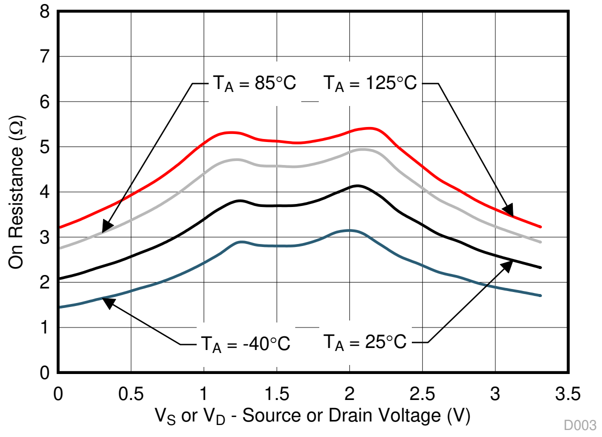


V_{DD} = 5V

Figure 5-2. On-Resistance vs Temperature

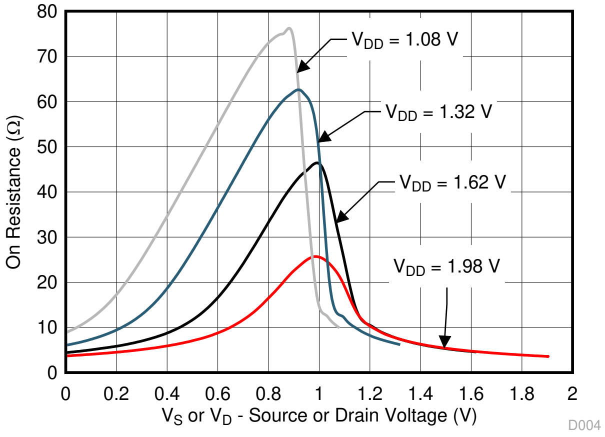
Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



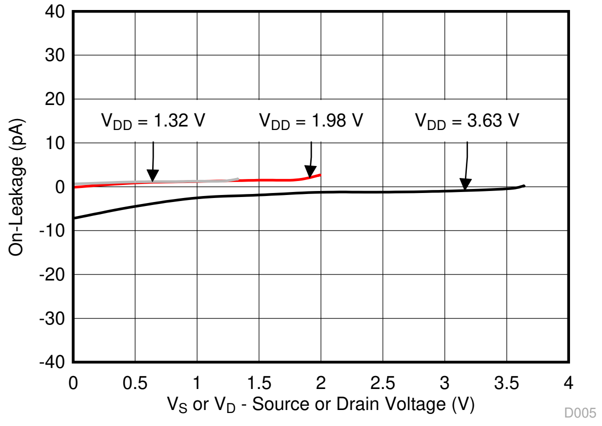
V_{DD} = 3.3V

Figure 5-3. On-Resistance vs Temperature



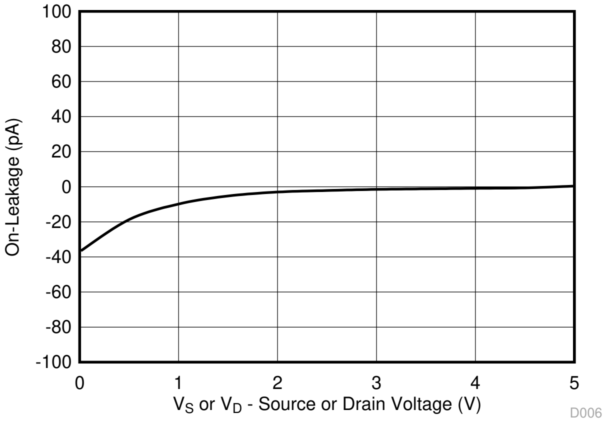
T_A = 25°C

Figure 5-4. On-Resistance vs Source or Drain Voltage



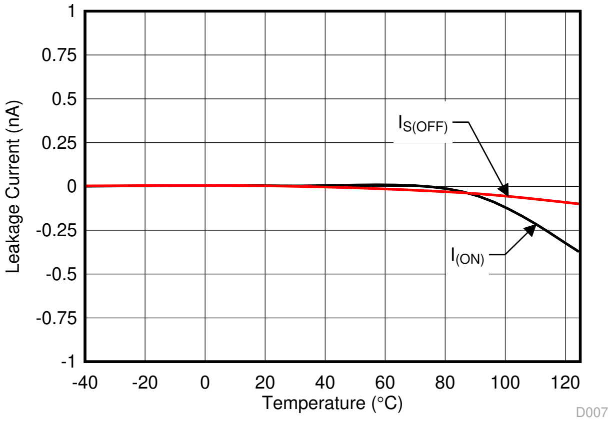
T_A = 25°C

Figure 5-5. On-Leakage vs Source or Drain Voltage



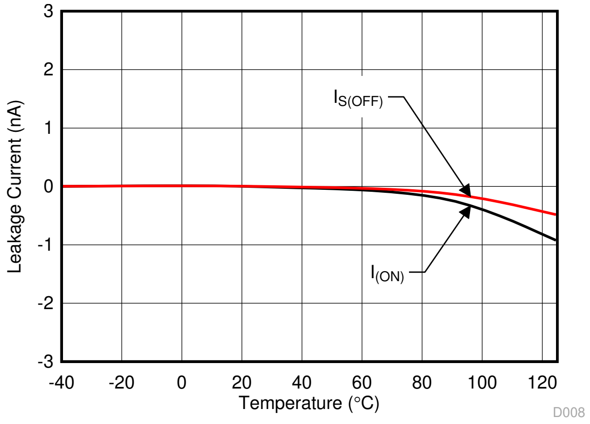
V_{DD} = 5V

Figure 5-6. On-Leakage vs Source or Drain Voltage



V_{DD} = 3.3V

Figure 5-7. Leakage Current vs Temperature

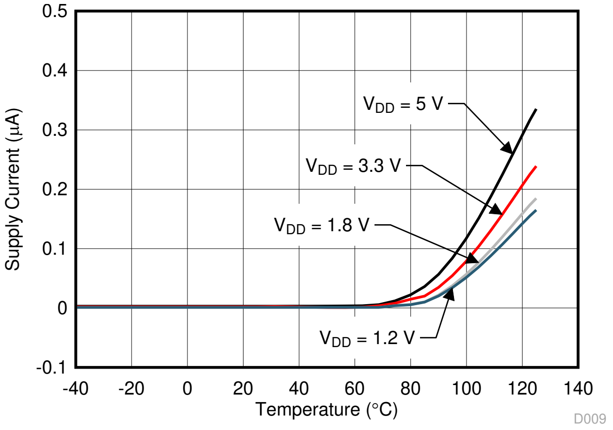


V_{DD} = 5V

Figure 5-8. Leakage Current vs Temperature

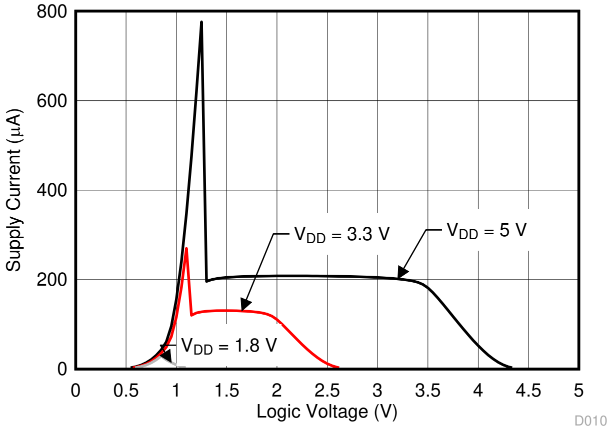
Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



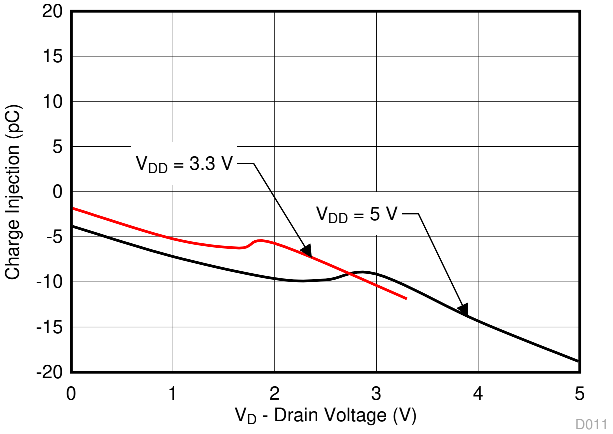
V_{SEL} = V_{DD} V

Figure 5-9. Supply Current vs Temperature



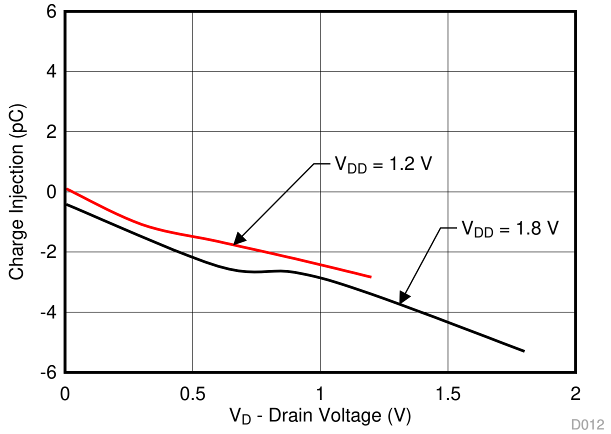
T_A = 25°C

Figure 5-10. Supply Current vs Logic Voltage



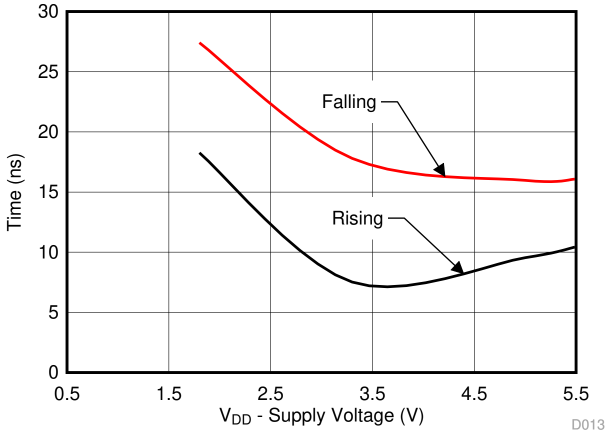
T_A = -40°C to 125°C

Figure 5-11. Charge Injection vs Drain Voltage



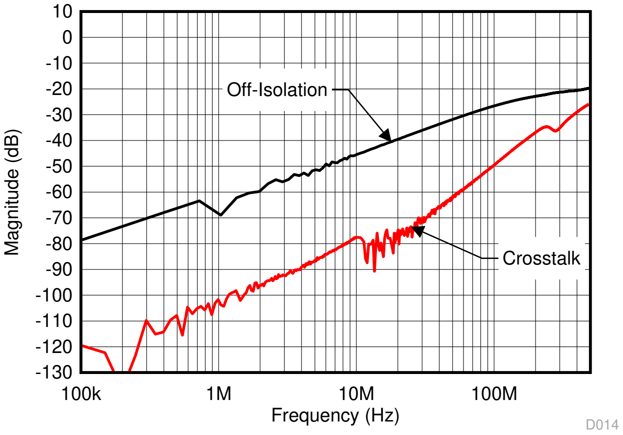
T_A = -40°C to 125°C

Figure 5-12. Charge Injection vs Drain Voltage



T_A = 25°C

Figure 5-13. Output $T_{TRANSITION}$ vs Supply Voltage

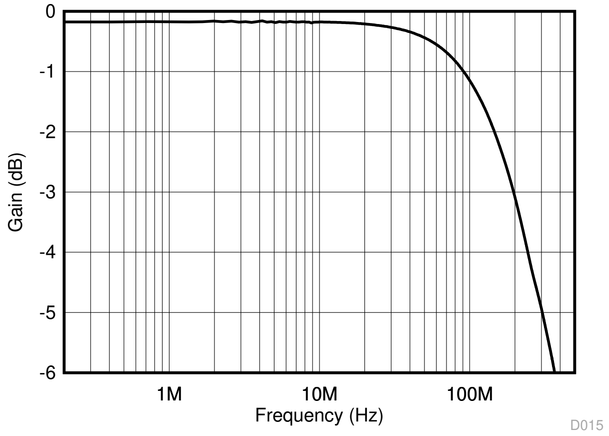


T_A = -40°C to 125°C

Figure 5-14. Xtalk and Off-Isolation vs Frequency

Typical Characteristics

at T_A = 25°C, V_{DD} = 5V (unless otherwise noted)



T_A = -40°C to 125°C

Figure 5-15. On Response vs Frequency

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 6-1. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

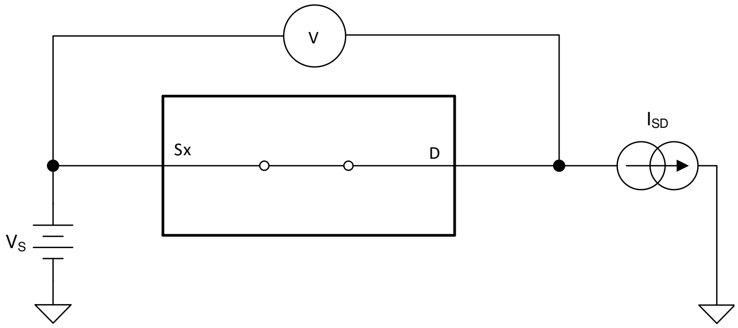


Figure 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

Source and drain off-leakage current is defined as the leakage current flowing into or out of the source or drain pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$ and $I_{D(OFF)}$. Figure 6-2 shows the setup used to measure off-leakage current.

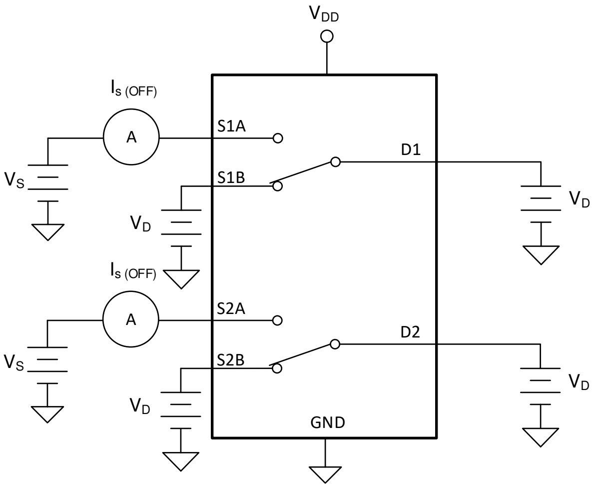


Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$. Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$. Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

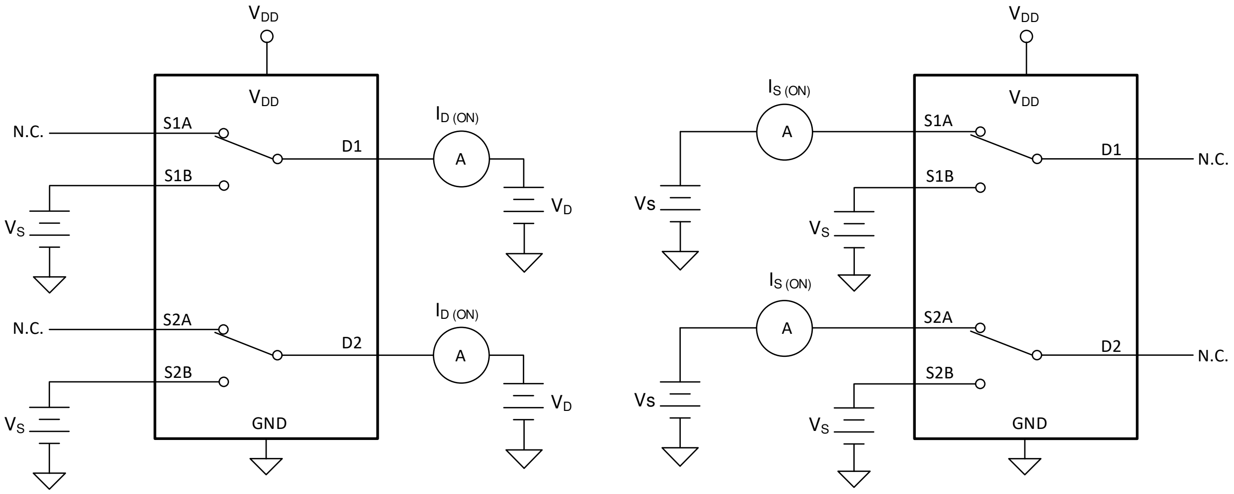


Figure 6-3. On-Leakage Measurement Setup

6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

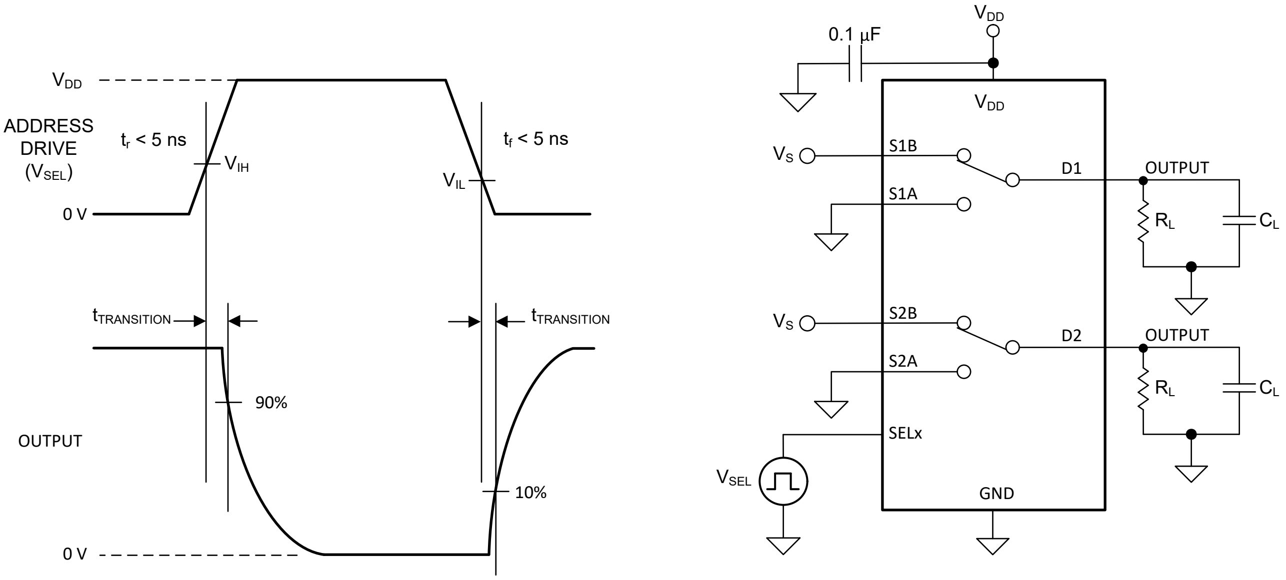


Figure 6-4. Transition-Time Measurement Setup

6.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

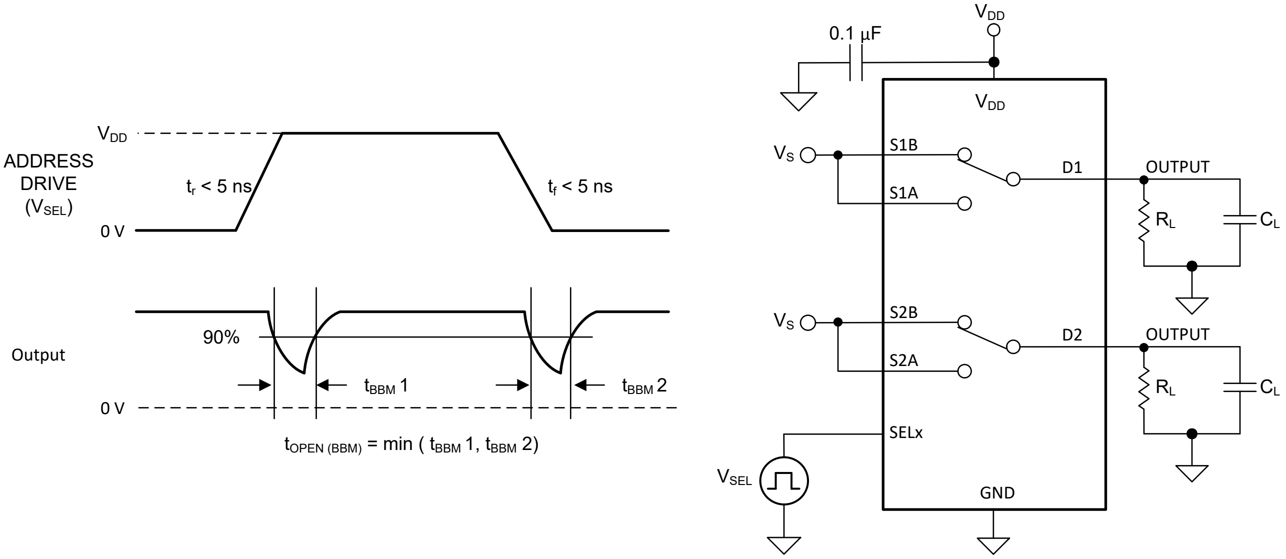


Figure 6-5. Break-Before-Make Delay Measurement Setup

6.6 Charge Injection

The TMUX1136 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-6 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

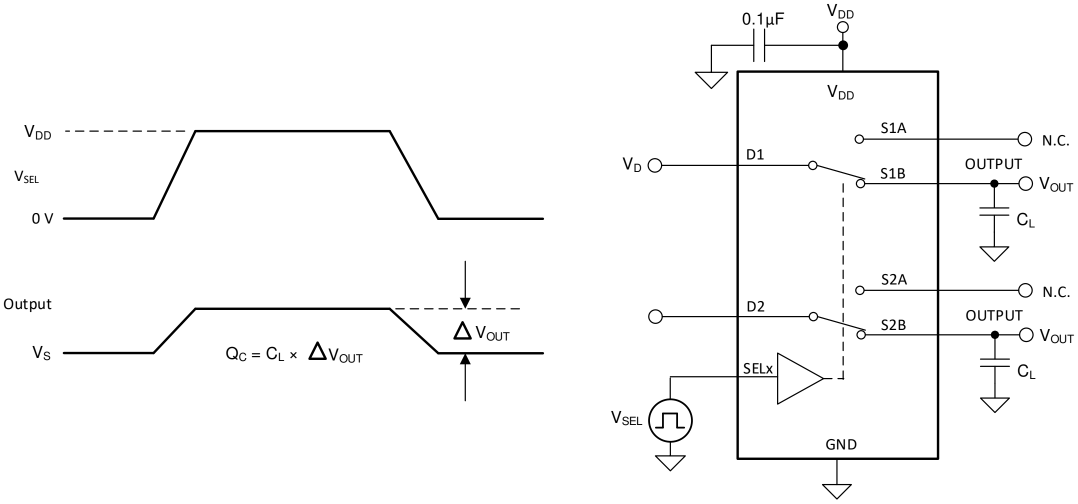


Figure 6-6. Charge-Injection Measurement Setup

6.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-7 shows the setup used to measure, and the equation used to calculate off isolation.

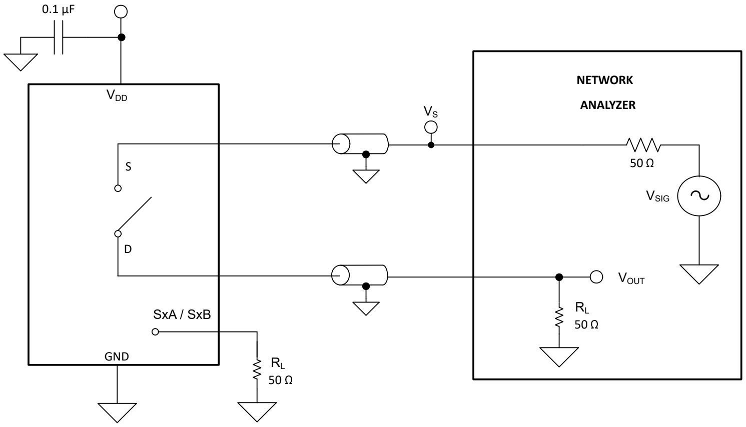


Figure 6-7. Off Isolation Measurement Setup

$$Off\ Isolation\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \tag{1}$$

6.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-8 shows the setup used to measure, and the equation used to calculate crosstalk.

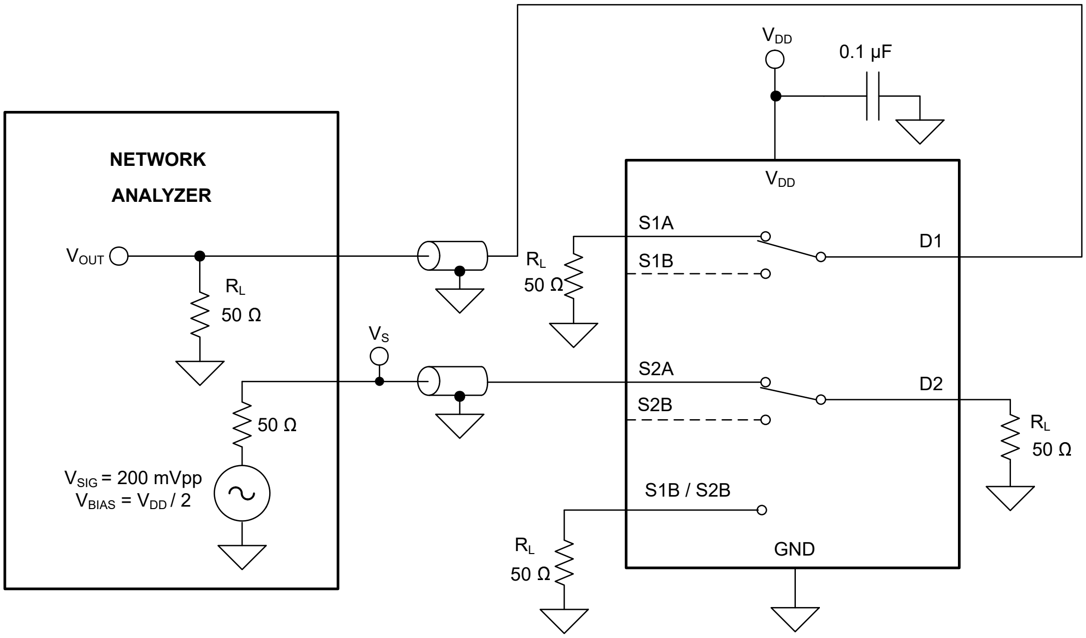


Figure 6-8. Crosstalk Measurement Setup

$$Channel - to - Channel\ Crosstalk\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \tag{2}$$

6.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 6-9 shows the setup used to measure bandwidth.

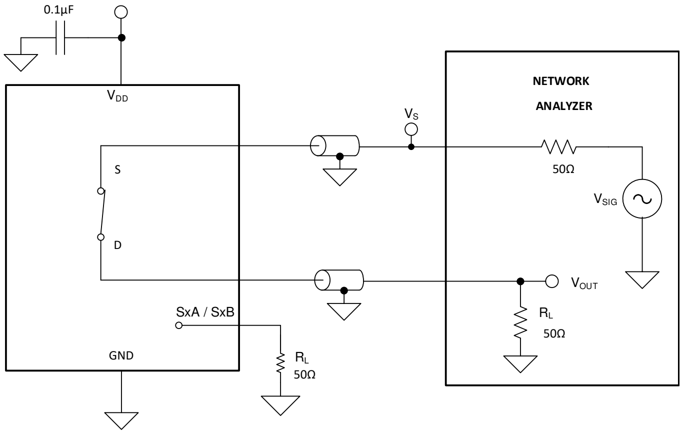


Figure 6-9. Bandwidth Measurement Setup

7 Detailed Description

7.1 Functional Block Diagram

The TMUX1136 is a 2:1 (SPDT), 2-channel analog switch with two independently controlled channels. Each channel is controlled with a single select (SELx) control pin to toggle between source inputs.

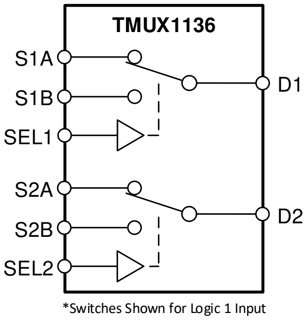


Figure 7-1. TMUX1136 Functional Block Diagram

7.2 Feature Description

7.2.1 Bidirectional Operation

The TMUX1136 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

7.2.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1136 ranges from GND to V_{DD}.

7.2.3 1.8V Logic Compatible Inputs

The TMUX1136 has 1.8V logic compatible control for the logic control inputs (SELx). The logic input threshold scales with supply but still provides 1.8V logic control when operating at 5.5V supply voltage. 1.8V logic level inputs allow the TMUX1136 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. The current consumption of the TMUX1136 increases when using 1.8V logic with higher supply voltage as shown in Figure 5-10. For more information on 1.8V logic implementations refer to *Simplifying Design with 1.8V logic Muxes and Switches*.

7.2.4 Fail-Safe Logic

The TMUX1136 supports Fail-Safe Logic on the control input pins (SELx) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1136 to be ramped to 5.5V while V_{DD} = 0V. Additionally, the feature enables operation of the TMUX1136 with V_{DD} = 1.2V while allowing the select pin to interface with a logic level of another device up to 5.5V.

7.2.5 Ultra-low Leakage Current

The TMUX1136 provides extremely low on-leakage and off-leakage currents. The TMUX1136 is capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultra-low leakage currents. Figure 7-2 shows typical leakage currents of the TMUX1136 versus temperature.

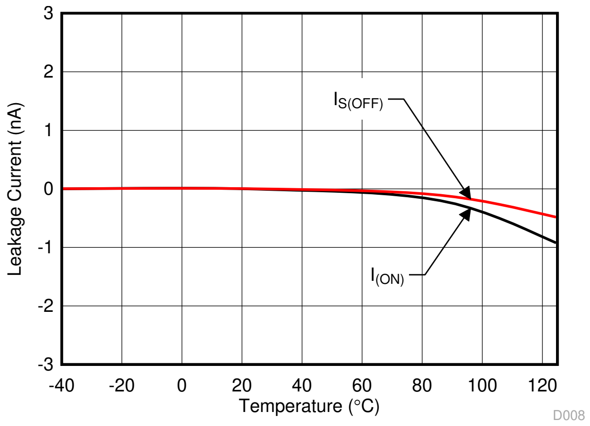


Figure 7-2. Leakage Current vs Temperature

7.2.6 Ultra-low Charge Injection

The TMUX1136 has a transmission gate topology, as shown in Figure 7-3. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

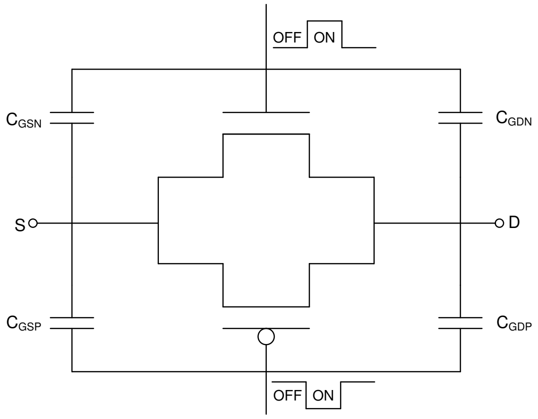


Figure 7-3. Transmission Gate Topology

The TMUX1136 has special charge-injection cancellation circuitry that reduces the drain-to-source charge injection to -6pC at V_D = 1V as shown in Figure 7-4.

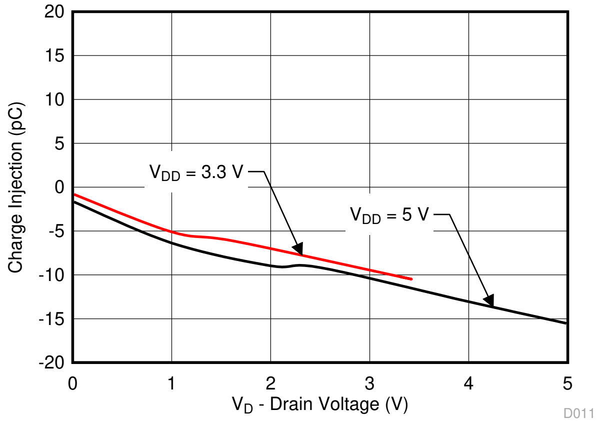


Figure 7-4. Charge Injection vs Drain Voltage

7.3 Device Functional Modes

The select (SELx) pins of the TMUX1136 controls which source is connected to the drain pins of the device. When a signal path is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5V.

7.3.1 Truth Tables

Table 7-1. TMUX1136 Truth Table

CONTROL LOGIC (SELx)	Selected Source (SxA or SxB) Connected To Drain (Dx) Pin
0	S1B to D1 S2B to D2
1	S1A to D1 S2A to D2

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX11xx family offers ultra-low input/output leakage currents and low charge injection. These devices operate up to 5.5V, and offer true rail-to-rail input and output of both analog and digital signals. The TMUX1136 has a low on-capacitance which allows faster settling time when multiplexing inputs in the time domain. These features make the TMUX11xx devices a family of precision, high-performance switches and multiplexers for low-voltage applications.

8.2 Typical Application

Figure 8-1 shows an example circuit where the TMUX1136 is used to switch different feedback networks of a transimpedance amplifier (TIA). The application uses a 2-channel SPDT switch in order to optimize the tradeoffs of low leakage current and on resistance of the switch.

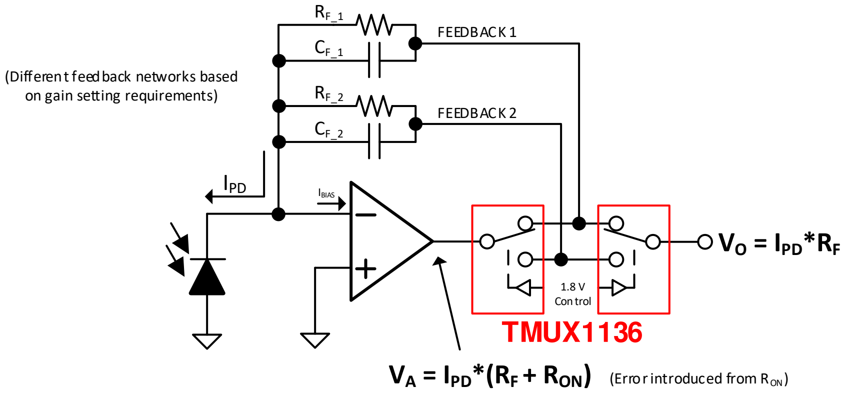


Figure 8-1. Transimpedance Amplifier Feedback Switching

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	5V
Input / Output signal range	1nA to 10μA
Control logic thresholds	1.8V compatible

8.2.2 Detailed Design Procedure

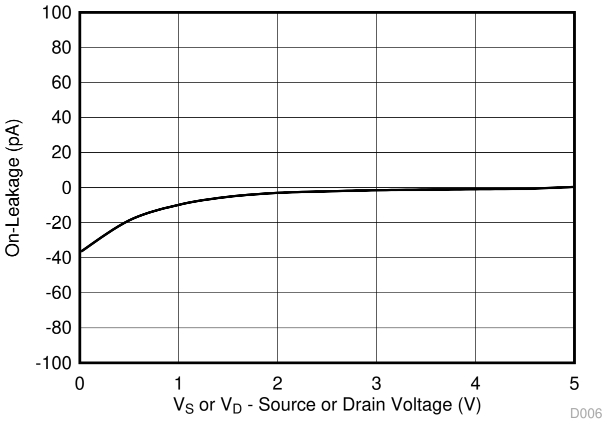
The TMUX1136 can operate without any external components except for the supply decoupling capacitors. All inputs passing through the switch must fall within the recommend operating conditions of the TMUX1136, including signal range and continuous current. For this design with a supply of 5V the signal range can be 0V to 5V, and the max continuous current can be 30mA.

Photodiodes commonly have a current output that ranges from a few hundred picoamps to tens of microamps based on the amount of light being absorbed. Difference feedback networks can be switched into a transimpedance amplifier in order to scale the output voltage to maximize system dynamic range. Typical feedback resistance is in the 10s-100s of kilo-ohms range where the on resistance of a switch would have minimal impact on system accuracy. However, some applications will have larger photodiode currents due to light exposure and can require a feedback resistor as low as 100Ω. Analog switches and multiplexers commonly have a tradeoff between on-resistance and leakage current, which will both lead to overall system error. Figure 8-1 shows how to configure a multi-channel analog switch to eliminate the impact from on-resistance and select a device optimized for low leakage currents. The drawback of this architecture is that the output impedance of the TIA stage is now the on-resistance of the multiplexer since the second channel is outside the feedback loop. This is commonly an acceptable tradeoff as the on-resistance of the TMUX1136 is very low, 2Ω typical.

The TMUX1136 has a typical On-leakage current of less than 10pA which would lead to an accuracy well within 1% of a full scale 10µA signal. The low ON and OFF capacitance of the TMUX1136 improves system stability by minimizing the total capacitance on the output of the amplifier. Lower capacitance leads to less overshoot and ringing in the system which can cause the amplifier circuit to go unstable if the phase margin is not at least 45°. Refer to *Improve Stability Issues with Low C_{ON} Multiplexers* for more information on calculating the phase margin vs. percent overshoot..

8.2.3 Application Curve

The TMUX1136 is capable of switching signals with minimal distortion because of the ultra-low leakage currents and low On-resistance. Figure 8-2 shows how the leakage current of the TMUX1136 varies with different input voltages.



T_A = 25°C

Figure 8-2. On-Leakage vs Source or Drain Voltage

8.3 Power Supply Recommendations

The TMUX1136 operates across a wide supply range of 1.08V to 5.5V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

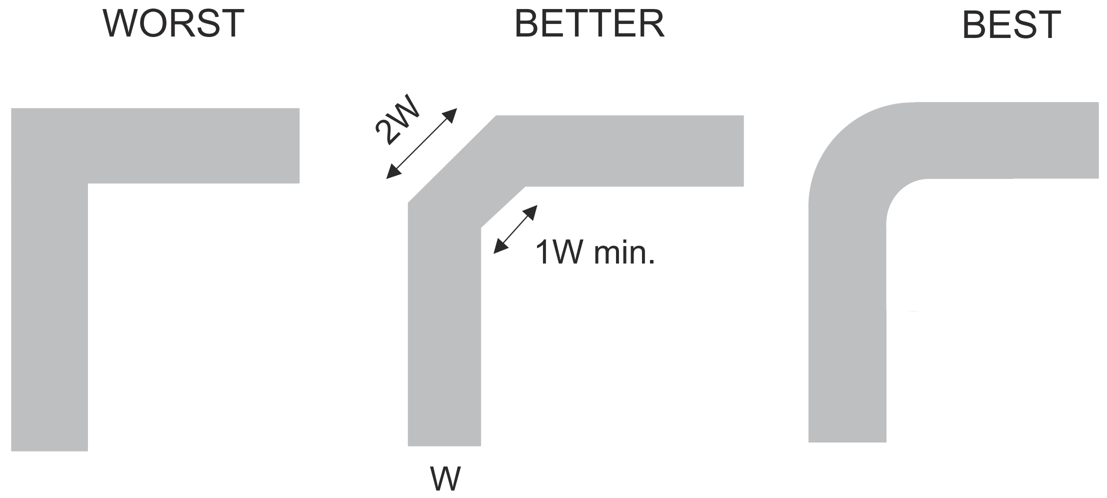


Figure 8-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 8-4 shows an example of a PCB layout with the TMUX1136. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

8.4.2 Layout Example

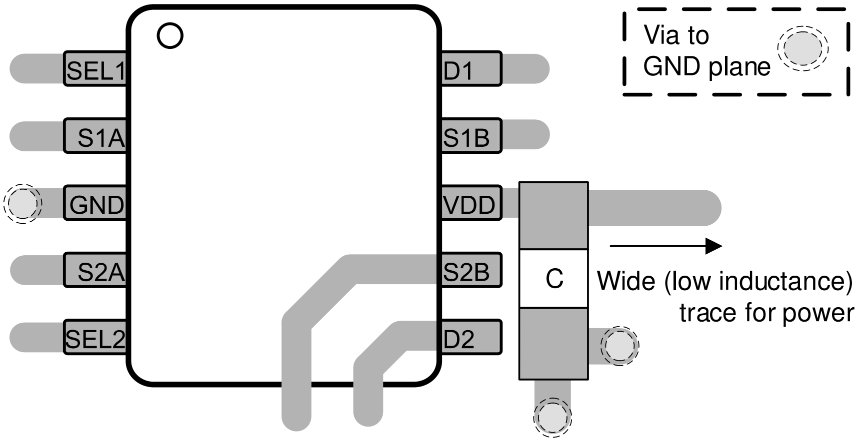


Figure 8-4. TMUX1136 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Ultrasonic Gas Meter Front-End With MSP430™ Reference Design*.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit*.
- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches*.
- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.
- Texas Instruments, *QFN/SON PCB Attachment*.
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2019) to Revision B (February 2024)	**Page**
• Updated Is or Id (Continuous Current) values	4
• Added Ipeak values to *Recommended Operating Conditions* table	4

Changes from Revision * (June 2019) to Revision A (July 2019)	**Page**
• Deleted the *Product Preview* note from the DQA package in the *Device Information* table	1
• Deleted the *Product Preview* note from the DQA package in the *Pin Configuration and Functions* section	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX1136DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	1136
TMUX1136DGSR.A	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1136
TMUX1136DQAR	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	136
TMUX1136DQAR.A	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	136
TMUX1136DQARG4.A	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	136

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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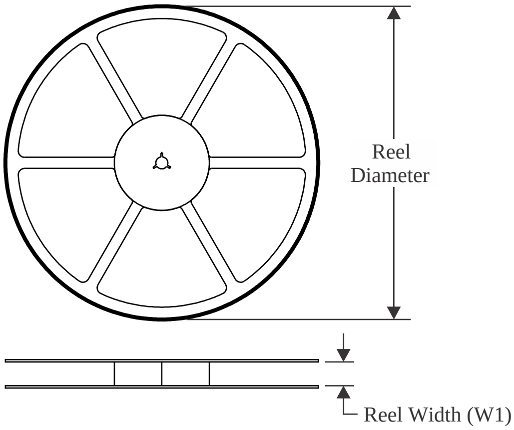
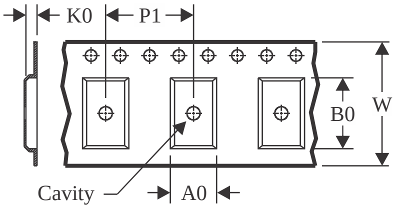
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

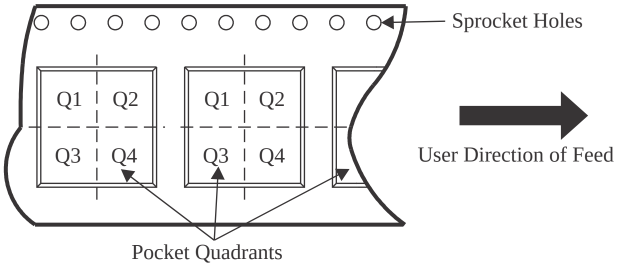


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

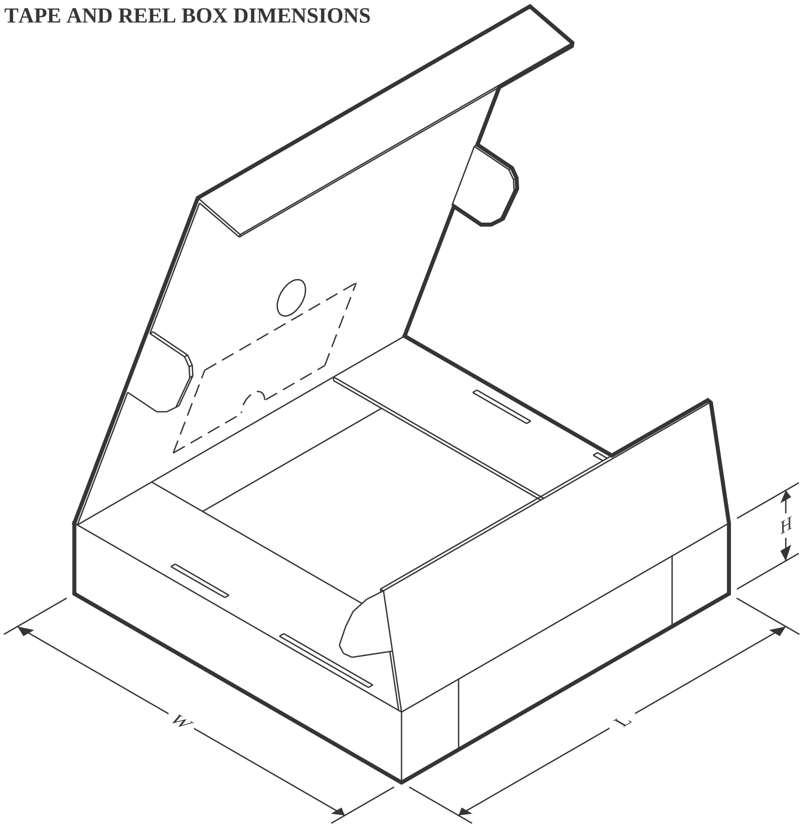
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1136DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TMUX1136DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

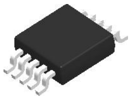
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1136DGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TMUX1136DQAR	USON	DQA	10	3000	189.0	185.0	36.0

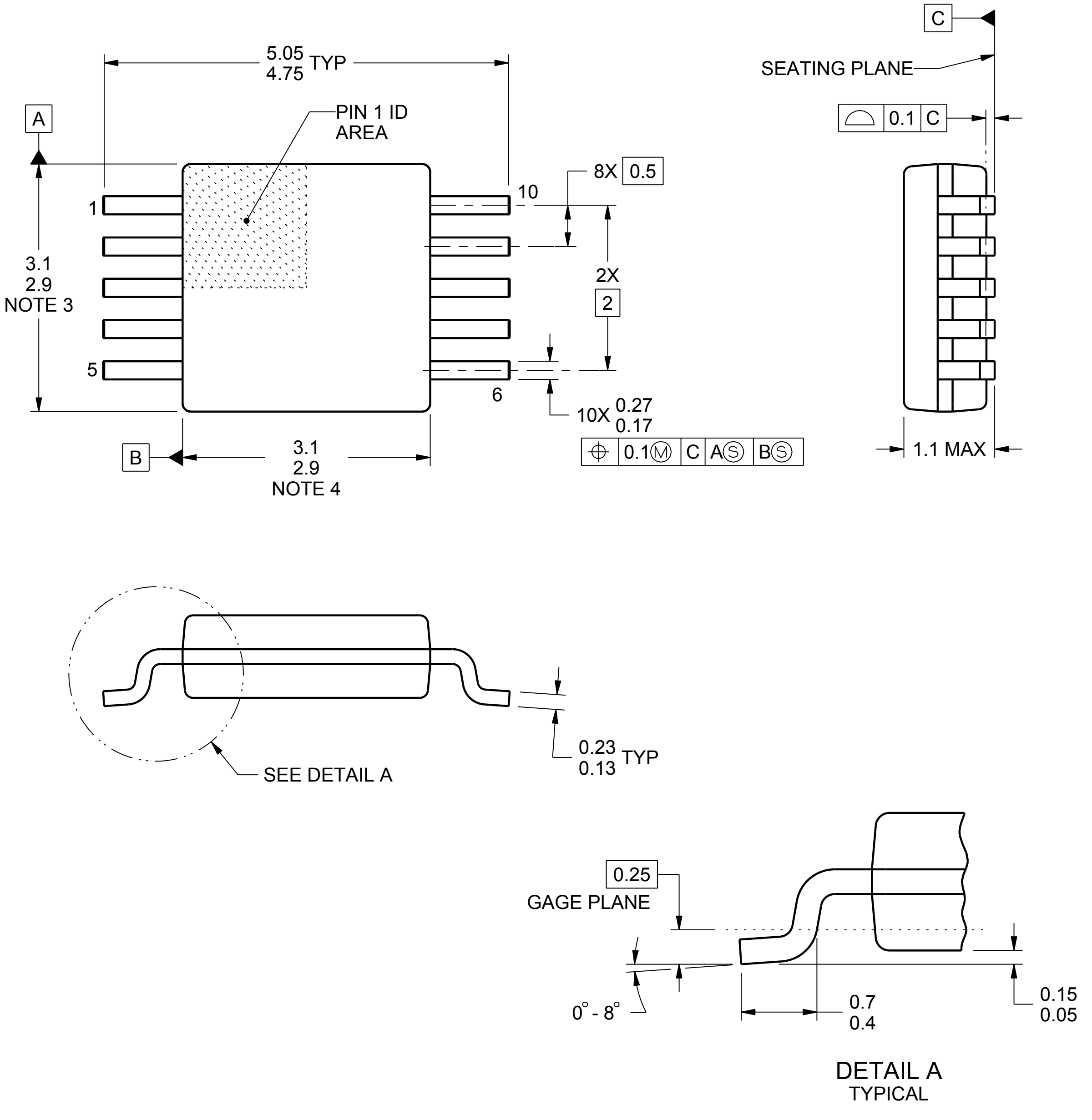
PACKAGE OUTLINE



DGS0010A

VSSOP - 1.1 mm max height

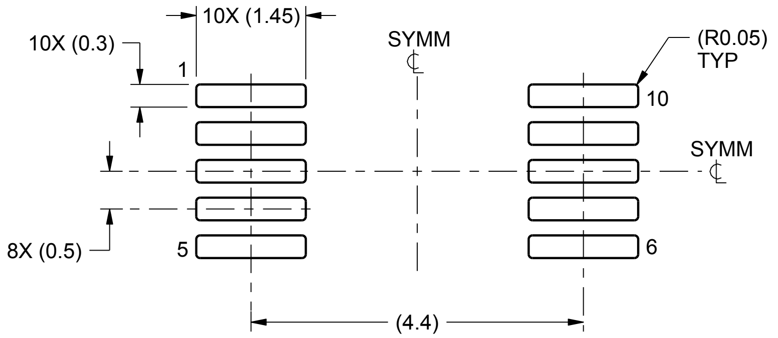
SMALL OUTLINE PACKAGE



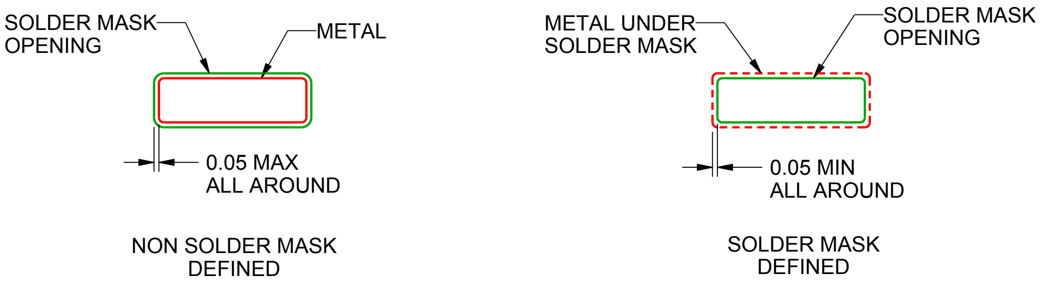
4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

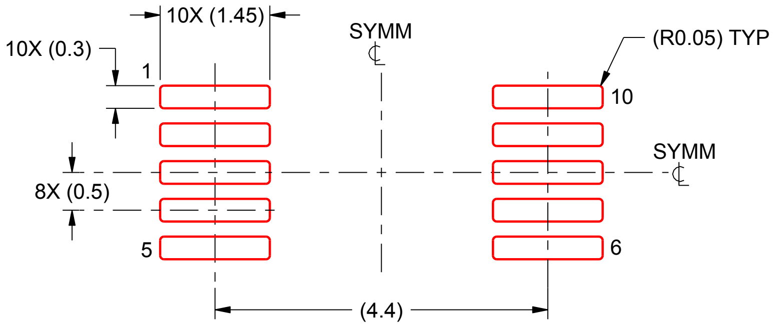


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

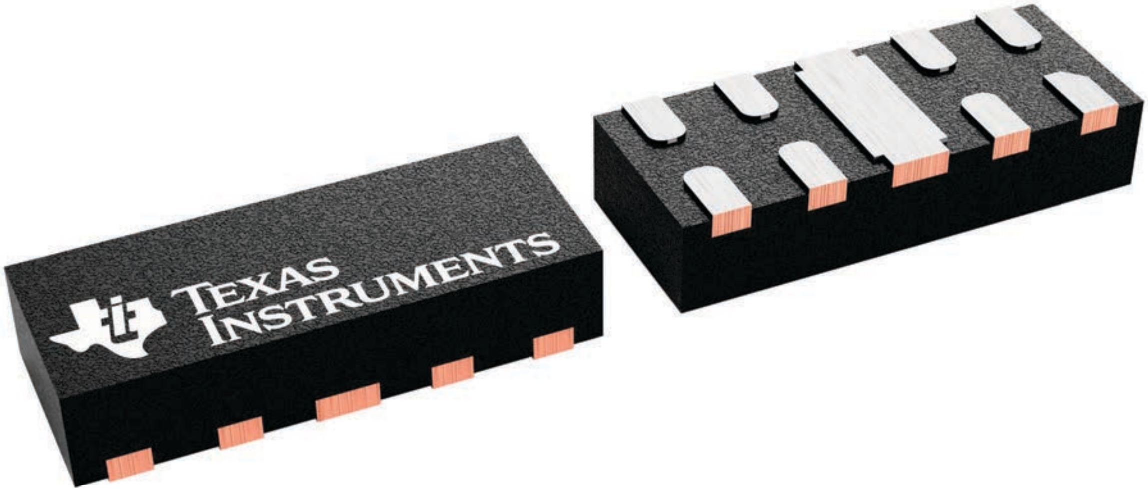
DQA 10

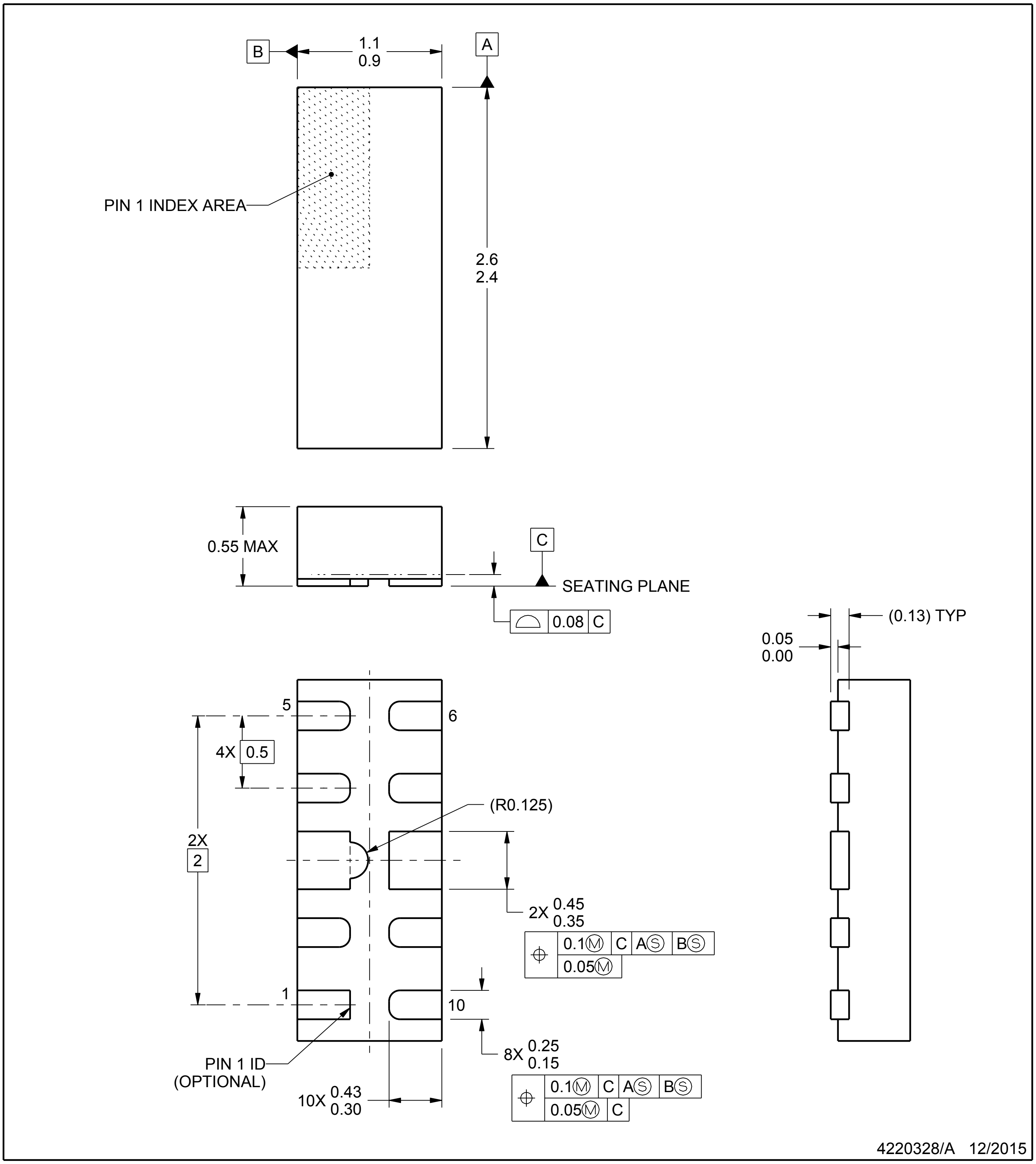
USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

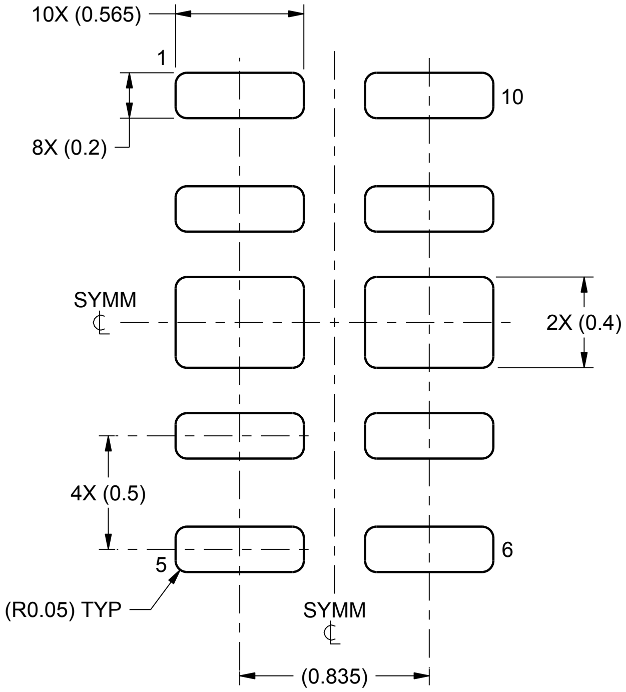
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



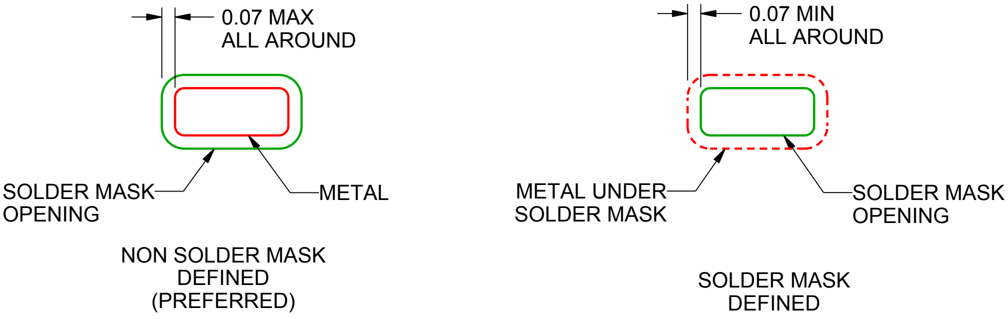


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

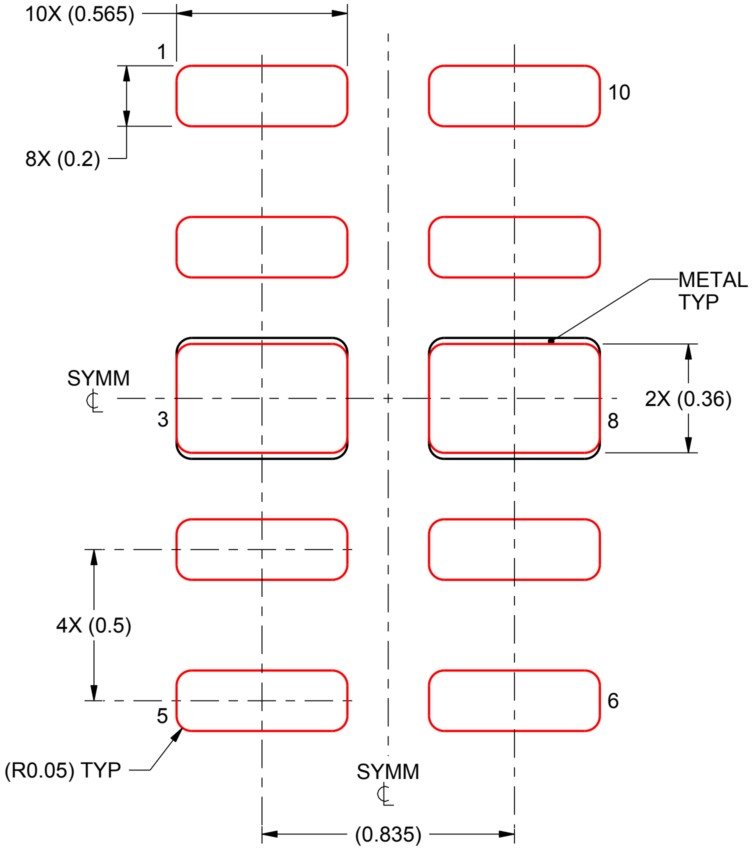
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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