TMCS1133-Q1 AEC-Q100, Precision 1MHz Hall-Effect Current Sensor With Reinforced Working Voltage, Overcurrent Detection and Ambient Field Rejection

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- High continuous current capability: $80A_{RMS}$
- Robust reinforced isolation
- High accuracy
  - Sensitivity error: ±0.1%
  - Sensitivity thermal drift: ±20ppm/°C
  - Sensitivity lifetime drift: ±0.2%
  - Offset error: ±0.2mV
  - Offset thermal drift: ±10μV/°C
  - Offset lifetime drift: ±0.2mV
  - Non-linearity: ±0.1%
- High immunity to external magnetic fields
- Fast Response
  - Signal bandwidth: 1MHz
  - Response time: 120ns
  - Propagation delay: 50ns
  - Overcurrent detection response: 100ns
- Operating supply range: 3V to 5.5V
- Bidirectional and unidirectional current sensing
- Multiple sensitivity options:
  - Ranging from 20mV/A to 150mV/A
- Safety related certifications
  - UL 1577 Component Recognition Program
  - IEC/CB 62368-1

2 Applications

- Onboard charger
- DC/DC converter
- Rotor excitation
- HVAC compressor
- High-voltage PDU
- EV charging

3 Description

The TMCS1133-Q1 is a galvanically isolated Hall-effect current sensor with industry leading isolation and accuracy. An output voltage proportional to the input current is provided with excellent linearity and low drift at all sensitivity options. Precision signal conditioning circuitry with built-in drift compensation is capable of less than 1.4% maximum sensitivity error over temperature and lifetime with no system level calibration, or less than 0.9% maximum sensitivity error including both lifetime and temperature drift with a one-time calibration at room temperature.

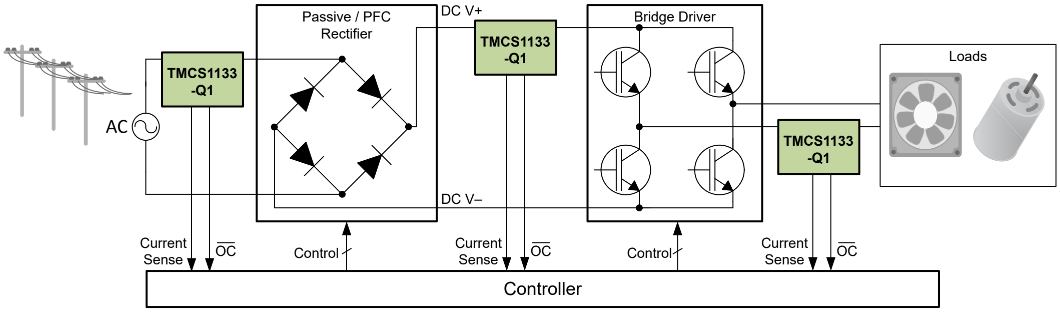
AC or DC input current flows through an internal conductor generating a magnetic field measured by integrated, on-chip, Hall-effect sensors. Core-less construction eliminates the need for magnetic concentrators. Differential Hall sensors reject interference from stray external magnetic fields. Low conductor resistance increases measurable current ranges up to ±96A while minimizing power loss and easing thermal dissipation requirements. Insulation capable of withstanding $5kV_{RMS}$, coupled with a minimum of 8mm creepage and clearance, provides high levels of reliable lifetime reinforced working voltage. Integrated shielding enables excellent common-mode rejection and transient immunity.

Fixed sensitivity allows the device to operate from a single 3V to 5.5V power supply, eliminating ratiometry errors and improving supply noise rejection.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMCS1133-Q1	DVG (SOIC, 10)	10.3mm × 10.3mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

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4 Device Comparison

Table 4-1. Device Comparison

PRODUCT(3)	SENSITIVITY	ZERO CURRENT OUTPUT VOLTAGE	I_{IN} LINEAR MEASUREMENT RANGE(1)	
			V_S = 5V	V_S = 3.3V
TMCS1133A1A-Q1	25mV/A	2.5V	±96A(2)	–96A to 28A(2)
TMCS1133A2A-Q1	50mV/A		±48A(2)	–48A to 14A(2)
TMCS1133A3A-Q1	75mV/A		±32A	–32A to 9.3A
TMCS1133A4A-Q1	100mV/A		±24A	–24A to 7A
TMCS1133A5A-Q1	150mV/A		±16A	–16A to 4.7A
TMCS1133B7A-Q1	20mV/A	1.65V	–77.5A to 163A(2)	±77.5A(2)
TMCS1133B1A-Q1	25mV/A		–62A to 130A(2)	±62A(2)
TMCS1133B8A-Q1	33mV/A		–47A to 98.5A(2)	±47A(2)
TMCS1133B2A-Q1	50mV/A		–31A to 65A(2)	±31A
TMCS1133B3A-Q1	75mV/A		–20.7A to 43.3A(2)	±20.7A
TMCS1133B4A-Q1	100mV/A		–15.5A to 32.5A	±15.5A
TMCS1133B5A-Q1	150mV/A		–10.3A to 21.7A	±10.3A
TMCS1133C1A-Q1	25mV/A	0.33V	–9.2A to 183A(2)	–9.2A to 115A(2)
TMCS1133C2A-Q1	50mV/A		–4.6A to 91.4A(2)	–4.6A to 57.4A(2)
TMCS1133C9A-Q1	66mV/A		–3.4A to 69.2A(2)	–3.4A to 43.4A(2)
TMCS1133C3A-Q1	75mV/A		–3.1A to 60.9A(2)	–3.1A to 38.3A(2)
TMCS1133C4A-Q1	100mV/A		–2.3A to 45.7A(2)	–2.3A to 28.7A
TMCS1133C5A-Q1	150mV/A		–1.5A to 30.5A	–1.5A to 19.1A

(1) Linear range limited by the maximum output swing to power supply (3V to 5.5V) and ground, not by thermal limitations.
(2) Current levels must remain below both allowable continuous DC/RMS and transient peak current safe operating areas to not exceed device thermal limits. See the *Safe Operating Area* section.
(3) For more information on the device name and device options, see the *Device Nomenclature* section.

5 Pin Configuration and Functions

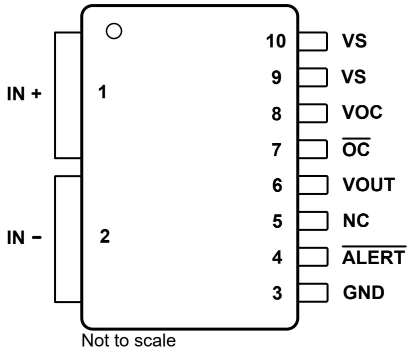


Figure 5-1. DVG Package 10-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN+	Analog Input	Input current positive pin
2	IN–	Analog Input	Input current negative pin
3	GND	Analog	Ground
4	$\overline{\text{ALERT}}$	Digital Output	Sensor diagnostics PWM output, open-drain active low. Connect pin to GND if not used.
5	NC	-	Reserved. Pin can be connected to GND or left floating.
6	VOUT	Analog Output	Output voltage
7	$\overline{\text{OC}}$	Digital Output	Overcurrent output, open-drain active low. Connect pin to GND if not used.
8	VOC	Analog Input	Overcurrent threshold. Sets overcurrent threshold. Connect pin to VS if not used.
9	VS	Analog	Power supply
10	VS	Analog	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage		GND – 0.3	6	V
	Analog input	VOC	GND – 0.3	$(V_S) + 0.3$	V
	Analog output	VOUT			
	Digital output	$\overline{\text{ALERT}}$, $\overline{\text{OC}}$			
	No Connection	NC			
T_J	Junction temperature		–65	165	°C
T_{stg}	Storage temperature		–65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Operating supply voltage	3	5	5.5	V
T_A (1)	Operating free-air temperature	–40		125	°C

(1) Input current safe operating area is constrained by junction temperature. Recommended condition based on use with the *TMCS1133xEVM*. Input current rating is derated for elevated ambient temperatures.

6.4 Thermal Information

THERMAL METRIC(1)		TMCS1133(2)	UNIT
		DVG (SOIC-W-10)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	
Ψ_{JT}	Junction-to-top characterization parameter	4.4	
Ψ_{JB}	Junction-to-board characterization parameter	8.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Applies when device is mounted on the *TMCS1133xEVM* with 40A input current. For more details, see the *Safe Operating Area* section.

6.5 Power Ratings

V_S = 5.5V, T_A = 125°C, T_J = 165°C, device soldered on the *TMCS1133xEVM*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)				2.0	W
P_{D1}	Maximum power dissipation (current input, side-1)	I_{IN} = 44A			1.9	W
P_{D2}	Maximum power dissipation by (side-2)	V_S = 5.5V, I_Q = 14.5mA, no loads			0.1	W

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	≥ 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	≥ 8	mm
CTI	Comparative tracking index	DIN EN 60112; IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600V_{RMS}	I-IV	
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1697	V_{PK}
V_{IOWM}	Maximum reinforced isolation working voltage	AC voltage (sine wave); Time Dependent Dielectric Breakdown (TDDB) test, < 1ppm fail rate, see *Input Isolation* section.	950	V_{RMS}
			1343	V_{DC}
	Maximum basic isolation working voltage	AC voltage (sine wave); Time Dependent Dielectric Breakdown (TDDB) test, < 1000ppm fail rate, see *Input Isolation* section.	1200	V_{RMS}
			1697	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = \sqrt{2} \times V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 62368-1, 1.2/50µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	10000	V_{PK}
q_{pd}	Apparent charge(3)	Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤5	pC
C_{IO}	Barrier capacitance, input to output(4)	$V_{IO} = 0.4 \sin(2\pi ft)$, f = 1MHz	0.6	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	Ω
		V_{IO} = 500V at T_S = 150°C	$>10^{9}$	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Take care to maintain the creepage and clearance distance of the board design to make sure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Creepage and clearance on a printed circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

UL	
UL 1577 Component Recognition Program	Certified according to IEC 62368-1 CB
File number: E181974	Certificate number: US-43893-M1-UL

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input current (side 1)(1)	T_J = 165°C, T_A = 25°C, see *Thermal Derating Curve, Side 1*.			80	A_{RMS}
I_S	Safety input, output, or supply current (side 2)(1)	V_I = 5V, T_J = 165°C, T_A = 25°C, see *Thermal Derating Curve, Side 2*.			1.35	
P_S	Safety input, output, or total power(1)	T_J = 165°C, T_A = 25°C, see *Thermal Derating Curve, Both Sides*.			6.8	W
T_S	Safety temperature(1)				165	℃

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S must not be exceeded. These limits vary with the ambient temperature, T_A as shown in the *Safe Operating Area* section when used in the *TMCS1133xEVM*.

6.9 Electrical Characteristics

at T_A = 25°C, V_S = 5V on TMCS1133AxA-Q1, V_S = 3.3V on TMCS1133BxA-Q1 and TMCS1133CxA-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
R_{IN}	Input Conductor Resistance	IN+ to IN–		0.7		mΩ
R_{IN}	Input Conductor Resistance Temperature Drift	T_A= –40ºC to 125ºC		2.1		µΩ/°C
$I_{IN,MAX}$	Maximum Continuous Input Current[1]	T_A= 25ºC		80		A_{RMS}
		T_A= 125ºC		44		
OUTPUT						
S	Sensitivity	TMCS1133x7A-Q1		20		mV/A
		TMCS1133x1A-Q1		25		
		TMCS1133x8A-Q1		33		
		TMCS1133x2A-Q1		50		
		TMCS1133x9A-Q1		66		
		TMCS1133x3A-Q1		75		
		TMCS1133x4A-Q1		100		
		TMCS1133x5A-Q1		150		
S	Sensitivity	TMCS1133xAA-Q1		37-46		mV/A
S	Sensitivity	TMCS1133D7A, V_{REF} = 1.5V		20		mV/A
S	Sensitivity	TMCS1133DAA, V_{REF} = 1.5V		37-46		mV/A
e_S	Sensitivity Error	0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.1	±0.4	%
e_S	Sensitivity Error	TMCS1133D7A, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.1	±0.4	%
e_S	Sensitivity Error	TMCS1133DAA, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.1	±0.4	%
$S_{drift,therm}$	Sensitivity Thermal Drift	0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = −40°C to 125°C		±20	±50	ppm/°C
$S_{drift,therm}$	Sensitivity Thermal Drift	TMCS1133xAA, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = −40°C to 125°C		±20	±50	ppm/°C
$S_{drift,therm}$	Sensitivity Thermal Drift	TMCS1133D7A, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = −40°C to 125°C		±20	±50	ppm/°C
$S_{drift,therm}$	Sensitivity Thermal Drift	TMCS1133DAA, 0.05V ≤ V_{OUT} ≤ V_S − 0.2V, T_A = −40°C to 125°C		±20	±50	ppm/°C
$S_{drift, life}$	Sensitivity Lifetime Drift[2]	0.05V ≤ V_{OUT} ≤ V_S − 0.2V		±0.2	±0.5	%
e_{NL}	Nonlinearity Error	V_{OUT} = 0.1V to V_S – 0.1V		±0.1		%
$V_{OUT,0A}$	Zero Current Output Voltage	TMCS1133AxA-Q1, I_{IN} = 0A		2.5		V
		TMCS1133BxA-Q1, I_{IN} = 0A		1.65		
		TMCS1133CxA-Q1, I_{IN} = 0A		0.33		
$V_{OUT,0A}$	Zero Current Output Voltage	TMCS1133DxA-Q1, I_{IN} = 0A		1.5		V
V_{OE}	Output Voltage Offset Error	TMCS1133x7A-Q1, I_{IN} = 0A		±0.2	±1	mV
		TMCS1133x1A-Q1, I_{IN} = 0A		±0.2	±1	
		TMCS1133x8A-Q1, I_{IN} = 0A		±0.2	±1	
		TMCS1133x2A-Q1, I_{IN} = 0A		±0.3	±2	
		TMCS1133x9A-Q1, I_{IN} = 0A		±0.3	±2	
		TMCS1133x3A-Q1, I_{IN} = 0A		±0.4	±3	
		TMCS1133x4A-Q1, I_{IN} = 0A		±0.5	±4	
V_{OE}	Output Voltage Offset Error	TMCS1133xAA-Q1, I_{IN} = 0A		±0.3	±2	mV
V_{OE}	Output Voltage Offset Error	TMCS1133D7A, I_{IN} = 0A, V_S = 3.3V		±0.2	±1	mV
V_{OE}	Output Voltage Offset Error	TMCS1133DAA, I_{IN} = 0A, V_S = 3.3V		±0.3	±2	mV

6.9 Electrical Characteristics (continued)

at T_A = 25°C, V_S = 5V on TMCS1133AxA-Q1, V_S = 3.3V on TMCS1133BxA-Q1 and TMCS1133CxA-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OE,\ drift,\ therm}$	Output Voltage Offset Thermal Drift	TMCS1133x7A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±10	±25	µV/°C
		TMCS1133x1A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±10	±25	
		TMCS1133x8A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±10	±25	
		TMCS1133x2A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±10	±30	
		TMCS1133x9A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±10	±30	
		TMCS1133x3A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±10	±30	
		TMCS1133x4A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±15	±40	
		TMCS1133x5A-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±15	±40	
$V_{OE,\ drift,\ therm}$	Output Voltage Offset Thermal Drift	TMCS1133xAA-Q1, I_{IN} = 0A, T_A = –40°C to 125°C		±10	±30	µV/°C
$V_{OE,\ drift,\ therm}$	Output Voltage Offset Thermal Drift	TMCS1133D7A, I_{IN} = 0A, V_S = 3.3V, T_A = −40°C to 125°C		±10	±25	µV/°C
$V_{OE,\ drift,\ therm}$	Output Voltage Offset Thermal Drift	TMCS1133DAA, I_{IN} = 0A, V_S = 3.3V, T_A = −40°C to 125°C		±10	±30	µV/°C
$I_{OS,\ drift,\ life}$	Offset Lifetime Drift(2)	Input Referred, $V_{OUT,0A}$ / S, I_{IN} = 0A		±10	±24	mA
PSRR	Power Supply Rejection Ratio	Input Referred, V_S = 3V to 5.5V, T_A= –40ºC to 125ºC		±15	±50	mA/V
PSRR	Power Supply Rejection Ratio	TMCS1133xAA, V_S = 3V to 5.5V, T_A = −40°C to 125°C		±1	±4	mV/V
CMTI	Common Mode Transient Immunity(3)	V_{CM} = 1000V, ΔV_{OUT} < 200mV, 1µs		150		kV/µs
CMRR	Common Mode Rejection Ratio	Input Referred, DC to 60Hz		5		µA/V
CMFR	Common Mode Field Rejection	Uniform External Magnetic Field, Input Referred, DC to 1kHz			10	mA/mT
	Input Noise Density	Input Referred, Full Bandwidth		130		µA/√Hz
	Output Noise	TMCS1133D7A, I_{IN} = 0A, V_S = 3.3V, Full Bandwidth		3.4		mV_{RMS}
	Output Noise	TMCS1133DAA, I_{IN} = 0A, V_S = 3.3V, Full Bandwidth		8.5		mV_{RMS}
$C_{L,MAX}$	Maximum Capacitive Load	VOUT to GND		4.7		nF
	Short Circuit Output Current	VOUT short to GND, short to V_S		50		mA
$Swing_{VS}$	Swing to V_S Power Supply Rail	R_L = 10kΩ to GND, T_A= –40ºC to 125ºC		V_S – 0.02	V_S – 0.05	V
$Swing_{GND}$	Swing to GND			5	10	mV
BANDWIDTH & RESPONSE						
BW	Analog Bandwidth	- 3dB Gain		1.1		MHz
SR	Slew Rate(4)	Output rate of change between reaching 10% and 90% of final value as shown in *Figure 7-2* with a 100ns input step		8		V/µs
t_r	Response Time(4)	Time between input and output reaching 90% of final values, as shown in *Figure 7-2* with a 100ns input step and a 1V output transition		120		ns
t_{pd}	Propagation Delay(4)	Time between input and output reaching 10% of final values as shown in *Figure 7-2* with a 100ns input step and a 1V output transition		50		ns
	Current Overload Recovery Time			300		ns
OVER CURRENT DETECTION						
V_{OC}	Over Current Detection Threshold Voltage	V_{OC} = S x I_{OC} / 2.5	0.3		V_S	V
	V_{OC} Pin Input Impedance		120			kΩ

6.9 Electrical Characteristics (continued)

at T_A = 25°C, V_S = 5V on TMCS1133AxA-Q1, V_S = 3.3V on TMCS1133BxA-Q1 and TMCS1133CxA-Q1 (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OC}	Over Current Detection Threshold	TMCS1133xAA, V_S = 5 V	23		375	A
	Over Current Hysteresis	TMCS1133x7A-Q1		8.4		A
		TMCS1133x1A-Q1		4.5		
		TMCS1133x8A-Q1		3.4		
		TMCS1133x2A-Q1		3.5		
		TMCS1133x9A-Q1		2.5		
		TMCS1133x3A-Q1		2.2		
		TMCS1133x4A-Q1		1.4		
		TMCS1133x5A-Q1		2.7		
	Over Current Hysteresis	TMCS1133xAA-Q1		3.5		A
	Vover Current Threshold Error	T_A = –40°C to 125°C		±2	±10	%
	Over Current Detection Response Time	I_{IN} step = 120% of I_{OC}		100	250	ns
$\overline{\text{OC}}_{,\text{OL}}$	$\overline{\text{OC}}$ Pin Pull-down Voltage	I_{OL} = 3mA, T_A = –40°C to 125°C	GND	0.07	0.2	V
DIAGNOSTICS						
$\overline{\text{ALERT}}$	Output Frequency			8		kHz
	Output Duty Cycle, Active Low	Thermal Alert		80		%
		Sensor Alert		50		
		Thermal and Sensor Alert		20		
	$\overline{\text{ALERT}}$ Pin Pull-down Voltage	I_{OL} = 3mA. T_A = –40°C to 125°C	GND	0.07	0.2	V
POWER SUPPLY						
V_S	Supply Voltage	T_A = –40ºC to 125ºC	3.0		5.5	V
I_Q	Quiescent Current	T_A = 25ºC		11	14	mA
		T_A = –40ºC to 125ºC			14.5	mA
	Power On Time	Time from V_S > 3V to valid output		34		ms

(1) Thermally limited by junction temperature, see *Absolute Maximum Ratings*. Applies when device mounted on *TMCS1133xEVM*. For more details, see the *Safe Operating Area* section.

(2) Lifetime and environmental drift specifications based on three lot AEC-Q100 qualification stress test results. Typical values are population mean +1σ from worst case stress test condition. Maximum values are tested device population mean ±6σ. Devices tested in AEC-Q100 qualification stayed within maximum limits for all stress conditions. See *Lifetime and Environmental Stability* section for more details.

(3) Refer to the *Common-Mode Transient Immunity* section for details on common-mode transient response.

(4) Refer to the *Transient Response Parameters* section for details on transient response of the device.

6.10 Typical Characteristics

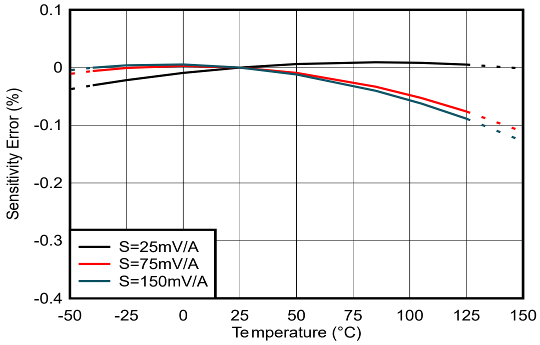


Figure 6-1. Sensitivity Error vs Temperature

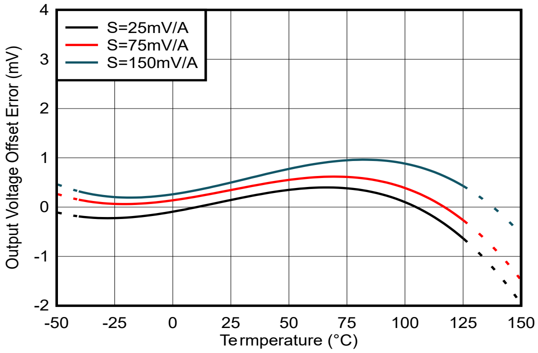


Figure 6-2. Offset Error vs Temperature: TMCS1133Axx-Q1 Device Options

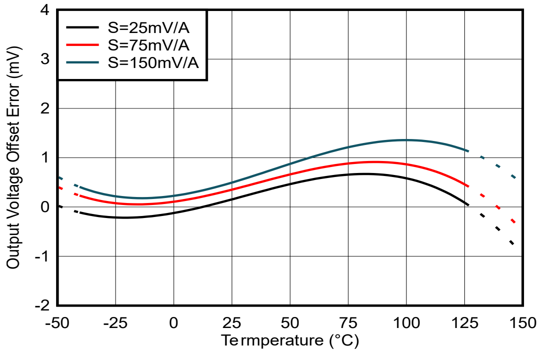


Figure 6-3. Offset Error vs Temperature: TMCS1133Bxx-Q1 Device Options

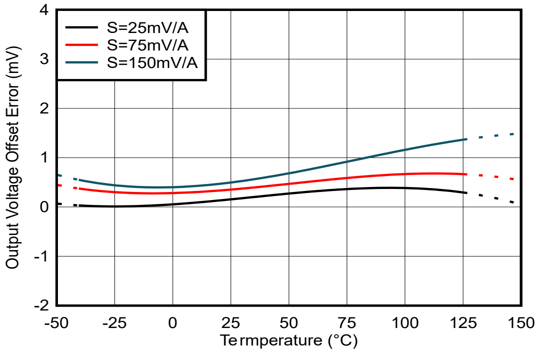


Figure 6-4. Offset Error vs Temperature: TMCS1133Cxx-Q1 Device Options

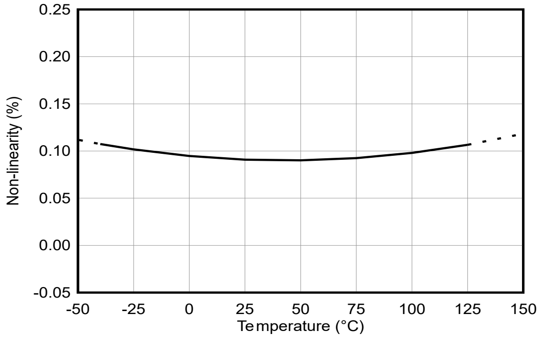
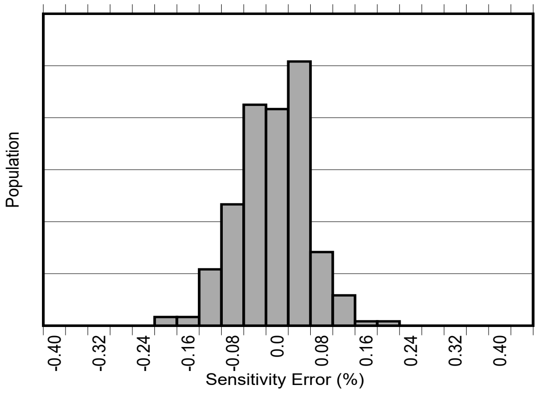


Figure 6-5. Non-Linearity vs Temperature



All sensitivities

Figure 6-6. Sensitivity Error Production Distribution

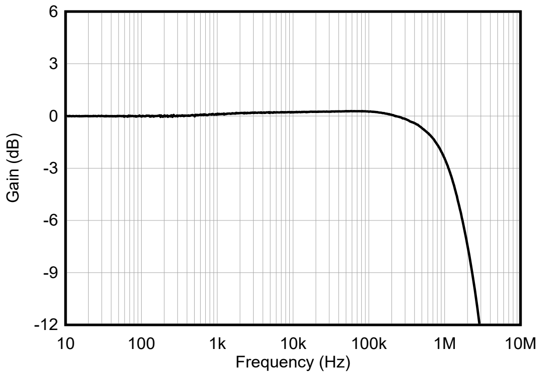


Figure 6-7. Sensitivity vs Frequency, All Gains Normalized to 1Hz

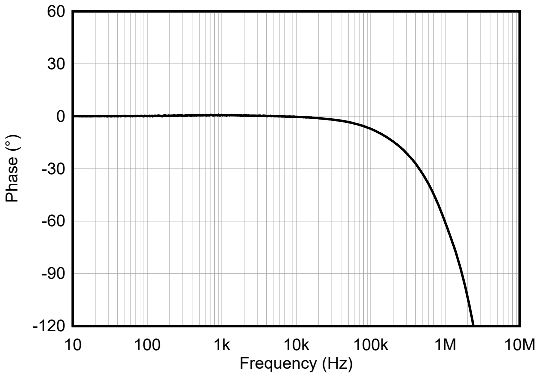


Figure 6-8. Phase vs Frequency, All Gains

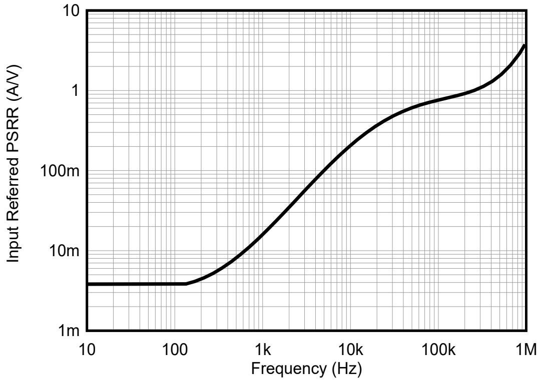


Figure 6-9. PSRR vs Frequency

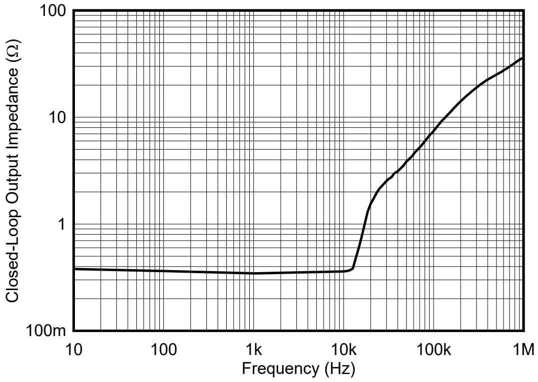


Figure 6-10. Output Impedance vs Frequency

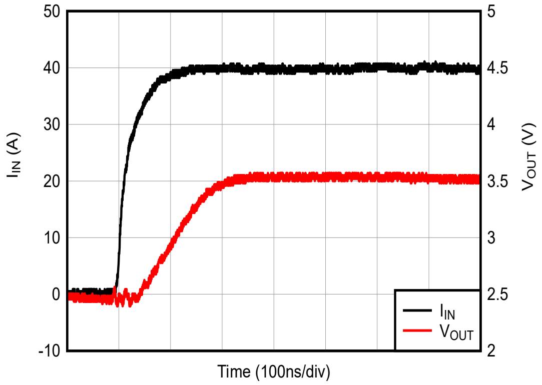


Figure 6-11. Voltage Output Step Response, Rising

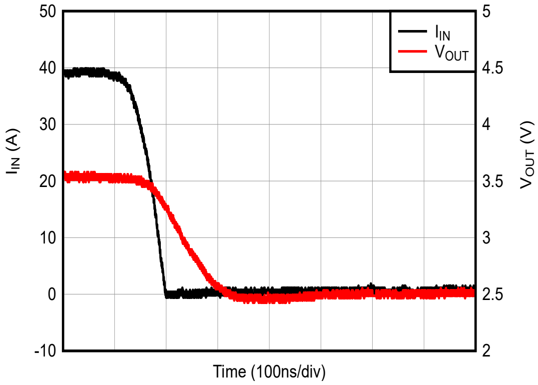


Figure 6-12. Voltage Output Step Response, Falling

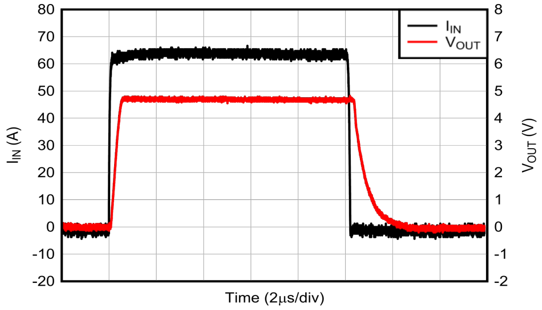


Figure 6-13. Current Overload Response

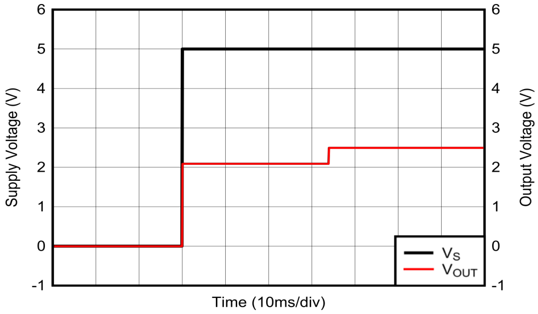


Figure 6-14. Startup Transient Response

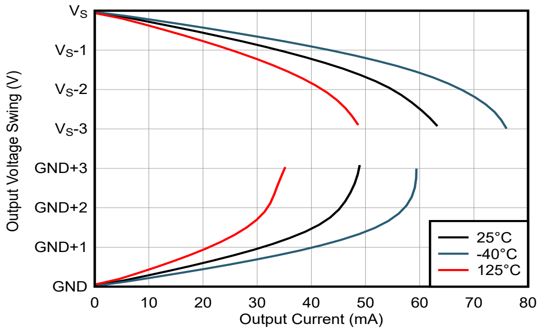


Figure 6-15. Output Swing vs Output Current

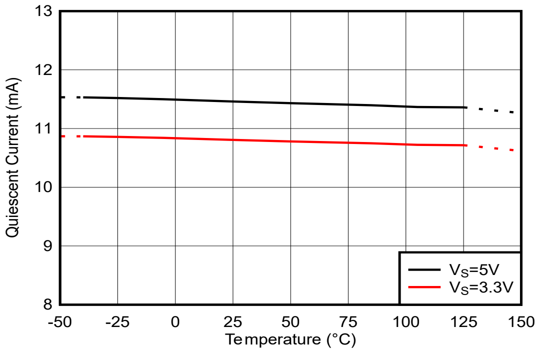


Figure 6-16. Quiescent Current vs Temperature

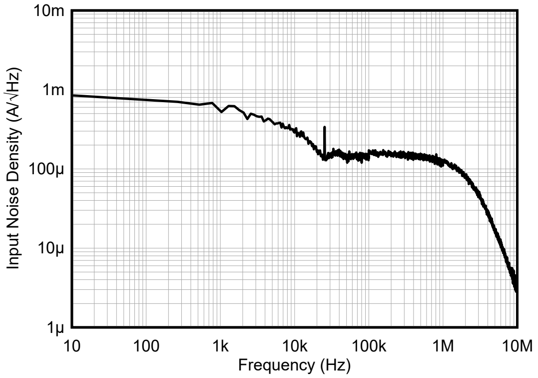


Figure 6-17. Input-Referred Noise Density vs Frequency

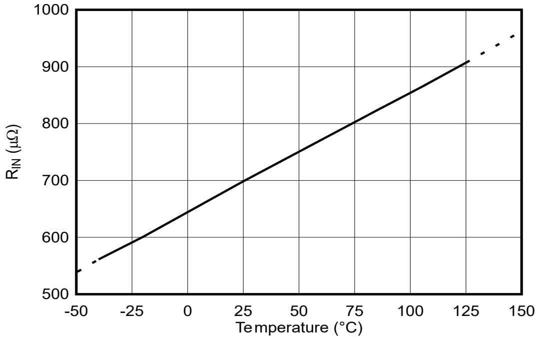


Figure 6-18. Input Conductor Resistance vs Temperature

6.10.1 Insulation Characteristics Curves

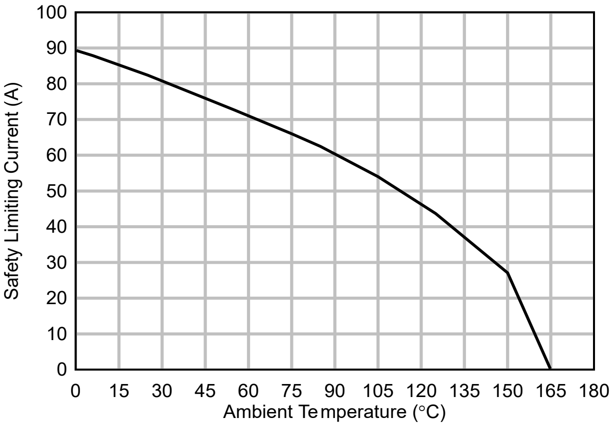


Figure 6-19. Thermal Derating Curve for Safety-Limiting Current, Side 1

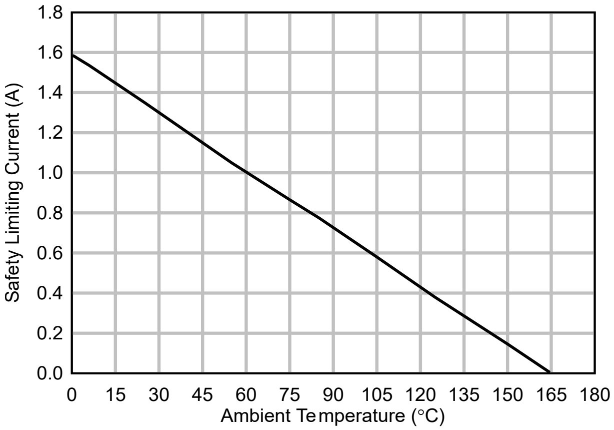


Figure 6-20. Thermal Derating Curve for Safety-Limiting Current, Side 2

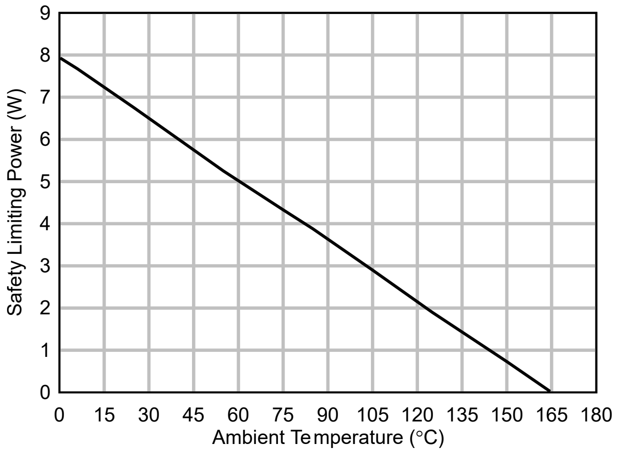


Figure 6-21. Thermal Derating Curve for Safety-Limiting Power

7 Parameter Measurement Information

7.1 Accuracy Parameters

The ideal first-order transfer function of the TMCS1133-Q1 is given by Equation 1, where the output voltage is a linear function of input current. The accuracy of the device is quantified both by the error terms in the transfer function parameters, as well as by nonidealities that introduce additional error terms not in the simplified linear model. See *Total Error Calculation Examples* for example calculations of total error, including all device error terms.

$$V_{OUT} = (I_{IN} \times S) + V_{REF} \quad (1)$$

where

- V_{OUT} is the analog output voltage.
- I_{IN} is the isolated input current.
- S is the sensitivity of the device.
- V_{REF} is the zero current reference output voltage for the device variant.

7.1.1 Sensitivity Error

Sensitivity is the proportional change in the sensor output voltage due to a change in the input conductor current. This sensitivity is the slope of the first-order transfer function of the sensor (see Figure 7-1). The sensitivity of the TMCS1133-Q1 is tested and calibrated at the factory for high accuracy.

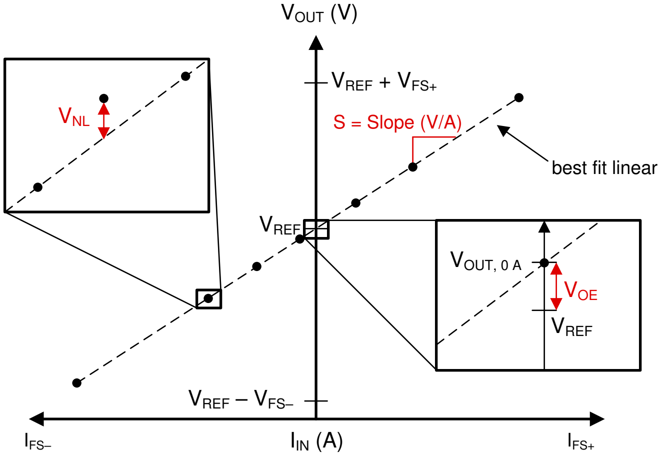


Figure 7-1. Sensitivity, Offset, and Nonlinearity Error

Sensitivity error e_S is the deviation from ideal sensitivity and is defined in Equation 2 as the variation of the best-fit measured sensitivity from the ideal sensitivity.

$$e_S = \frac{(S_{fit} - S_{ideal})}{S_{ideal}} \quad (2)$$

where

- e_S is the sensitivity error.
- S_{fit} is the best fit sensitivity.
- S_{Ideal} is the ideal sensitivity.

Sensitivity thermal drift $S_{drift,therm}$ is the change in sensitivity with temperature and is reported in ppm/°C. To calculate sensitivity error at any given temperature T use Equation 3 to multiply the sensitivity thermal drift by the change in temperature from 25°C and add that value to the sensitivity error at 25°C.

$$e_{S,\Delta T} = e_{S,25°C} + (S_{drift,therm} \times \Delta T) \quad (3)$$

where

- $S_{drift,therm}$ is the sensitivity drift over temperature in ppm/°C.
- ΔT is the change in device temperature from 25°C.

Sensitivity lifetime drift $S_{drift,life}$ is the change in sensitivity due to operational and environmental stresses over the entire lifetime of the device, and is reported as a worst-case percentage change in sensitivity over lifetime at 25°C.

7.1.2 Offset Error and Offset Error Drift

Offset error is the deviation from the ideal output with zero input current and most often limits measurement accuracy at low input current levels. Offset error can be referred to the output as offset voltage error or referred to the input as offset current error. When divided by device sensitivity, S, output voltage offset error V_{OE} is input referred as input current offset error I_{OS} (see Equation 4). Offset error referred to the input (RTI) allows for more direct comparisons or offset error with input current. Regardless of whether offset error is referred to the input as current offset error I_{OS}, or to the output as voltage offset error V_{OE}, offset error is a single error source and must only be included once in either input-referred or output-referred error calculations.

$$I_{OS} = \frac{V_{OE}}{S} \tag{4}$$

As shown in Figure 7-1, the output voltage offset error V_{OE} of the TMCS1133-Q1 is the difference between the zero current output voltage $V_{OUT,0A}$ and the zero current output reference voltage V_{REF} (see Equation 5).

$$V_{OE} = V_{OUT,\,0A} - V_{REF} \tag{5}$$

The output offset error V_{OE} includes magnetic offset error in the Hall sensor, offset voltage error in the signal chain, and offset error in the internal zero current output reference voltage V_{REF}.

Offset drift is the change in the offset as a function of temperature T. Output offset drift is reported in µV/°C. To calculate offset error at any given temperature, multiply the offset drift by the change in temperature and add that value to the offset error at 25°C (see Equation 6).

$$V_{OE,\,\Delta T} = V_{OE,\,25°C} + \left(V_{OE,\,drift} \times \Delta T\right) \tag{6}$$

where

- $V_{OE,drift}$ is the output voltage offset drift with temperature in µV/°C.
- ΔT is the change in device temperature from 25°C.

7.1.3 Nonlinearity Error

Nonlinearity is the deviation of the output voltage from a linear relationship to the input current. Nonlinearity voltage, as shown in Figure 7-1, is the maximum voltage deviation from the best-fit line based on measured parameters (see Equation 7).

$$V_{NL} = V_{OUT,\,meas} - \left[\left(I_{meas} \times S_{fit}\right) + V_{OUT,\,0A}\right] \tag{7}$$

where

- $V_{OUT,meas}$ is the voltage output at maximum deviation from best fit.
- I_{meas} is the input current at maximum deviation from best fit.
- S_{fit} is the best-fit sensitivity of the device.
- $V_{OUT,0A}$ is the device zero current output voltage.

Nonlinearity error for the TMCS1133-Q1 is specified as a percentage of the full-scale output range, V_{FS} (see Equation 8).

$$e_{NL} = \frac{V_{NL}}{V_{FS}} \tag{8}$$

7.1.4 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) is the change in device offset due to variations in supply voltage. Use Equation 9 to calculate input referred offset errors caused by supply variations on TMCS1133Axx-Q1 variants. Use Equation 10 to calculate input referred offset errors caused by supply variations on TMCS1133Bxx-Q1 and TMCS1133Cxx-Q1 variants.

$$e_{PSRR,\,A} = \mathrm{PSRR} \times (V_S - 5V) \tag{9}$$

$$e_{PSRR,\,B} = e_{PSRR,\,C} = \mathrm{PSRR} \times (V_S - 3.3V) \tag{10}$$

where

- PSRR is the input referred power supply rejection ratio in mA/V.
- V_S is the operational supply voltage.

7.1.5 Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) quantifies the effective input current error due to varying voltage on the isolated input of the device. Due to magnetic coupling and galvanic isolation of the current signal, the TMCS1133-Q1 has very high rejection of input common-mode voltage. Use Equation 11 to calculate the error contribution from the input common-mode voltage V_{CM}.

$$e_{CMRR} = \mathrm{CMRR} \times V_{CM} \tag{11}$$

where

- CMRR is the input-referred common-mode rejection in µA/V.
- V_{CM} is the operational AC or DC voltage on the input of the device.

7.1.6 External Magnetic Field Errors

The TMCS1133-Q1 suppresses interference from external magnetic fields generated by adjacent high-current carrying conductors, nearby motors, magnets, or any other sources of stray magnetic fields. Common-mode field rejection (CMFR) quantifies the effective input-referred error caused by stray magnetic fields. Use Equation 12 to calculate error contributions from stray external magnetic fields B_{EXT}.

$$e_{Bext} = B_{EXT} \times \mathrm{CMFR} \tag{12}$$

where

- B_{EXT} is the intensity of the external magnetic field in mT.
- CMRF is the common-mode field rejection in mA/mT.

7.2 Transient Response Parameters

Critical TMCS1133-Q1 transient step response parameters are shown in Figure 7-2. Propagation delay, t_{pd}, is the time period between the input current waveform reaching 10% of the final value and the output voltage, V_{OUT}, reaching 10% of the final value. Response time, t_r, is the time period between the input current reaching 90% of the final value and the output voltage reaching 90% of the final value, for an input current step sufficient to cause a 1V change in the output voltage. Slew rate, SR, is defined as the rate of change between the output voltage reaching 10% and 90% of the final value during the sufficiently fast input current step.

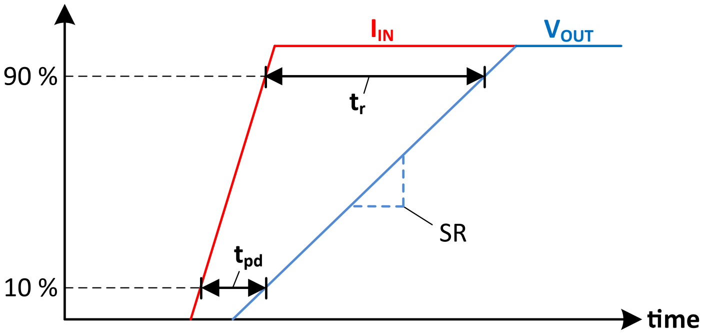


Figure 7-2. Transient Step Response

7.2.1 CMTI, Common-Mode Transient Immunity

CMTI is the capability of the device to tolerate a rising or falling voltage step on the input without coupling significant disturbance on the output signal. The device is specified for the maximum common-mode transition rate when the output signal does not experience a disturbance greater than 200mV lasting longer than 1µs, as shown in Figure 7-3 with a 150kV/µs common-mode input step. Higher edge rates than the specified CMTI can be supported with sufficient filtering or blanking time after common-mode transitions.

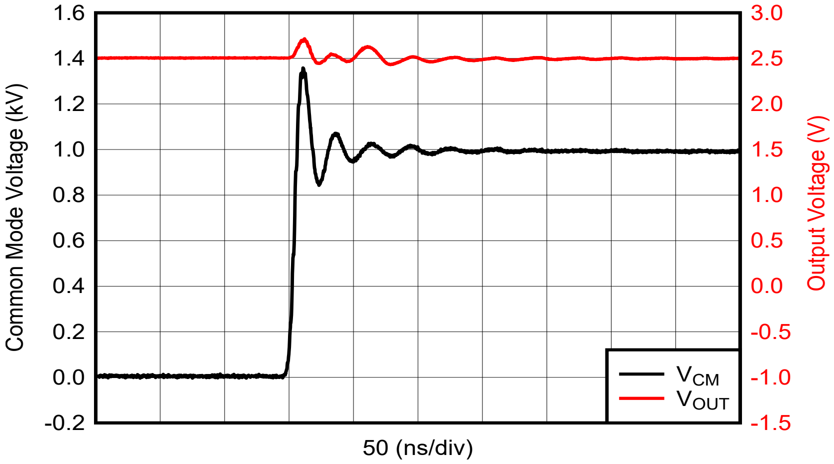


Figure 7-3. Common-Mode Transient Response

7.3 Safe Operating Area

The isolated input current safe operating area (SOA) of the TMCS1133-Q1 is constrained by self-heating due to power dissipation in the input conductor. Depending upon the use case, the SOA is constrained by multiple conditions, including exceeding maximum junction temperature, Joule heating in the leadframe, or leadframe fusing under extremely high currents. These mechanisms depend greatly on input current amplitude and duration, along with ambient thermal conditions.

Current SOA strongly depends on the thermal environment and design of the system-level printed circuit board (PCB). Multiple thermal variables control the transfer of heat from the device to the surrounding environment, including air flow, ambient temperature, and PCB construction and design. All ratings are for a single TMCS1133-Q1 device mounted on the *TMCS1133xEVM* , or equivalent PCB design with no air flow under specified ambient temperature conditions. Device use profiles must satisfy continuous current conduction SOA capabilities for the thermal environment planned for system operation.

7.3.1 Continuous DC or Sinusoidal AC Current

The longest thermal time constants of device packaging and PCBs are in the order of seconds; therefore, any continuous DC or sinusoidal AC periodic waveform with a frequency higher than 1Hz can be evaluated based on the RMS continuous-current levels. The continuous-current capability has a strong dependence upon the operating ambient temperature range expected in operation. Figure 7-4 shows the maximum continuous current-handling capability of the device when mounted on the *TMCS1133xEVM* . Current capability falls off at higher ambient temperatures because of the reduced thermal transfer from junction-to-ambient and increased power dissipation in the leadframe. By improving the thermal design of an application, the SOA can be extended to higher currents at elevated temperatures. Using larger and heavier copper power planes, providing air flow over the board, or adding heat sinking structures to the area of the device can all improve thermal performance.

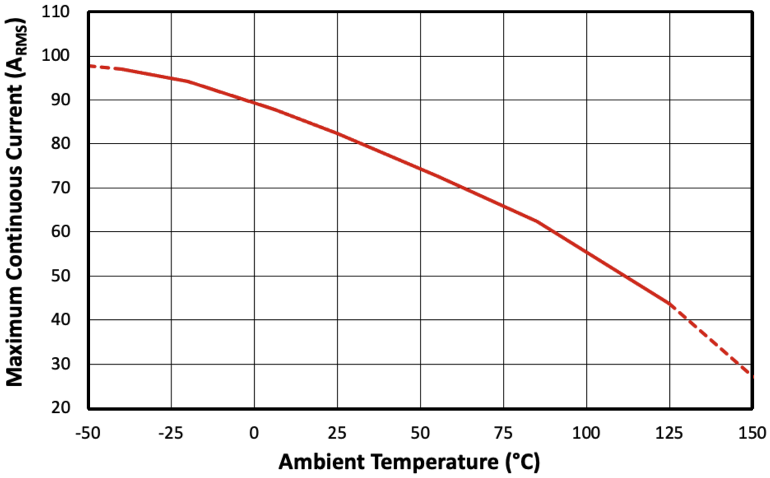


Figure 7-4. Maximum Continuous RMS Current vs Ambient Temperature

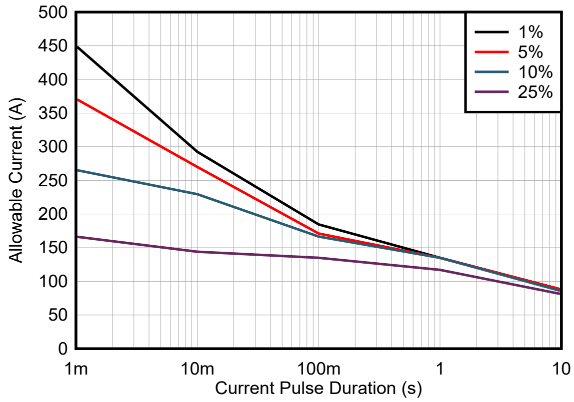
7.3.2 Repetitive Pulsed Current SOA

For applications where current is pulsed between a high current and no current, the allowable capabilities are limited by short-duration heating iwn the leadframe. The TMCS1133-Q1 can tolerate higher current ranges under some conditions, however, for repetitive pulsed events, the current levels must satisfy both the pulsed current SOA and the RMS continuous current constraint. Pulse duration, duty cycle, and ambient temperature all impact the SOA for repetitive pulsed events. Figure 7-5, Figure 7-6, Figure 7-7, and Figure 7-8 illustrate repetitive stress levels based on test results from the *TMCS1133xEVM* under which parametric performance and isolation integrity is not impacted post-stress for multiple ambient temperatures. At high duty cycles or long pulse durations, this limit approaches the continuous current SOA for a RMS value defined by Equation 13.

$$I_{IN,\ RMS} = I_{IN,\ P} \times \sqrt{D} \tag{13}$$

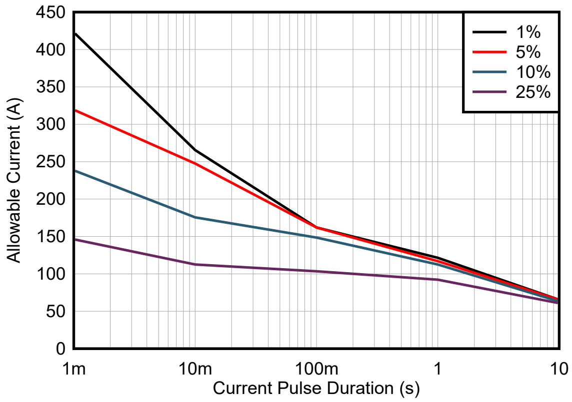
where

- $I_{IN,RMS}$ is the RMS input current level
- $I_{IN,P}$ is the pulse peak input current
- D is the pulse duty cycle



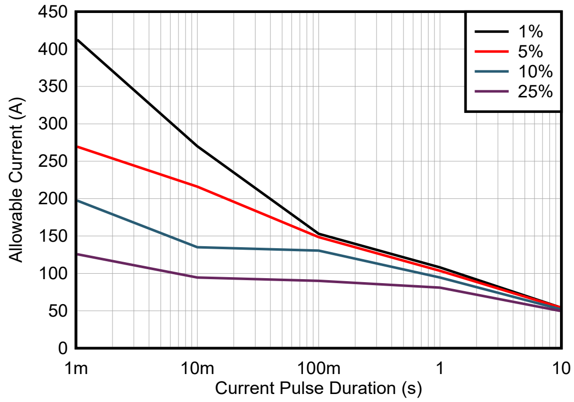
T_A = 25°C

Figure 7-5. Maximum Repetitive Pulsed Current vs. Pulse Duration



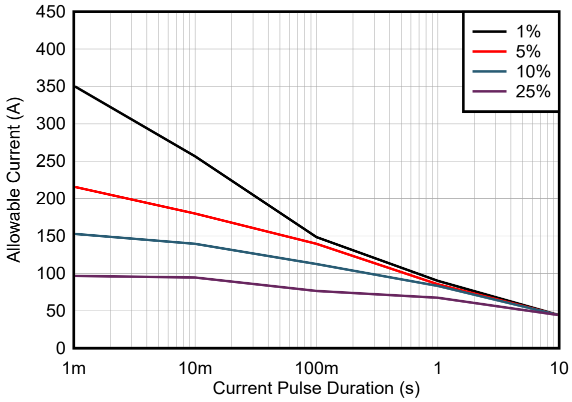
T_A = 85°C

Figure 7-6. Maximum Repetitive Pulsed Current vs. Pulse Duration



T_A = 105°C

Figure 7-7. Maximum Repetitive Pulsed Current vs. Pulse Duration



T_A = 125°C

Figure 7-8. Maximum Repetitive Pulsed Current vs. Pulse Duration

7.3.3 Single Event Current Capability

Single higher-current events that are shorter duration can be tolerated by the TMCS1133-Q1 , because the junction temperature does not reach thermal equilibrium within the pulse duration. Figure 7-9 shows the short-circuit duration curve for the device for single current-pulse events, where the leadframe resistance changes after stress. This level is reached before a leadframe fusing event, but must be considered an upper limit for short duration SOA. For long-duration pulses, the current capability approaches the continuous RMS limit at the given ambient temperature.

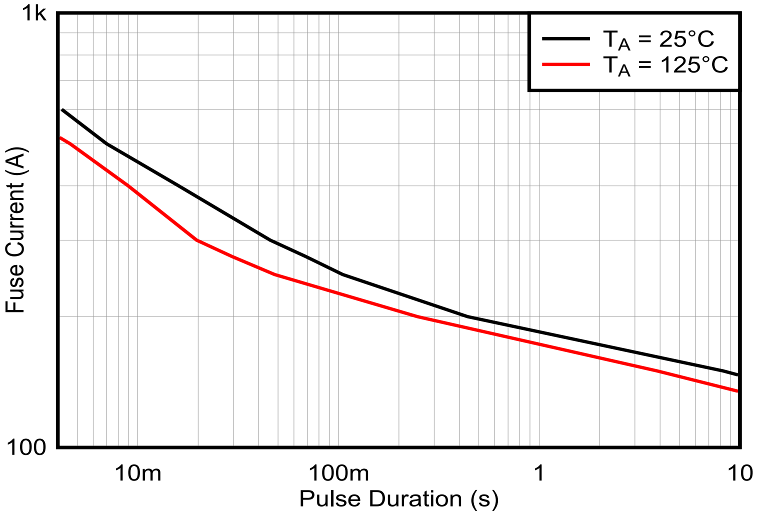


Figure 7-9. Single-Pulse Leadframe Capability

8 Detailed Description

8.1 Overview

The TMCS1133-Q1 is a precision Hall-effect current sensor, providing high levels of reliable reinforced isolation working voltage, ambient field rejection and high current carrying capability. A maximum total lifetime error of less than 1.4% can be achieved with no system level calibration, or less than 1% maximum total error can be achieved with a one-time room temperature calibration (including both temperature and lifetime drift). Numerous device options are provided for both unidirectional and bidirectional current measurements. The input current flows through a conductor between the isolated input current pins. The conductor has a 0.7mΩ resistance at room temperature and accommodates up to 44A_{RMS} of continuous current at 125°C ambient temperature when used with printed circuit boards of comparable thermal design, such as the *TMCS1133xEVM* . The low-ohmic leadframe path reduces power dissipation compared to alternative current measurement methodologies, and does not require any external passive components, isolated supplies, or control signals on the high-voltage side. The magnetic field generated by the input current is sensed by a Hall sensor and amplified by a precision signal chain. The device can be used for both AC and DC current measurements and has a bandwidth of 1MHz. There are multiple fixed-sensitivity device options to choose from, providing a wide variety of bidirectional linear current sensing ranges from ±10A to ±96A, as well as unidirectional linear current sensing ranges from 19A to 183A. The TMCS1133-Q1 can operate with a low voltage supply ranging from 3V to 5.5V, and is optimized for high accuracy and temperature stability, with both offset and sensitivity compensated across the entire operating temperature range.

8.2 Functional Block Diagram

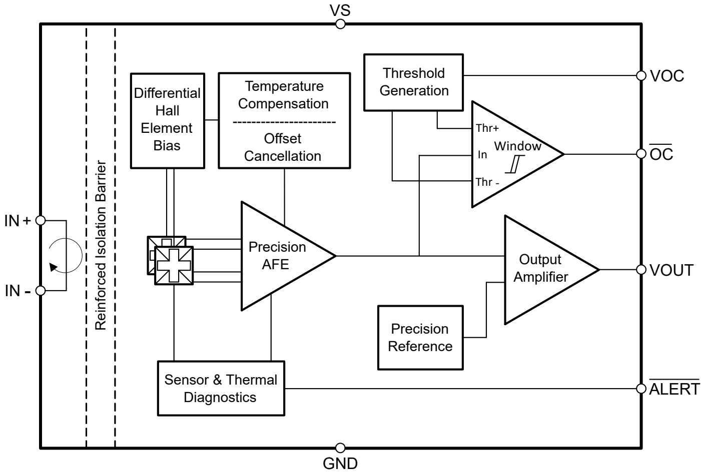


Figure 8-1. Function Block Diagram

8.3 Feature Description

8.3.1 Current Input

Input current to the TMCS1133-Q1 passes through the isolated high-voltage side of the package leadframe into and out of the IN+ and IN– pins. The current flowing through the package generates a magnetic field that is proportional to the input current, which is measured by an integrated on-chip galvanically-isolated, precision Hall sensor. As a result of the electrostatic shielding on the Hall sensor die, only the magnetic field generated by the input current is measured, thus limiting input voltage switching pass-through to the circuitry. This configuration allows for direct measurement of currents with high-voltage transients without signal distortion on the current-sensor output. The leadframe conductor has a low resistance and a positive temperature coefficient as defined in *Electrical Characteristics*.

8.3.2 Input Isolation

The separation between the input conductor and the Hall sensor die due to the TMCS1133-Q1 construction provides inherent galvanic isolation between package pins 1 and 2 on the high-voltage input side, and package pins 3 through 10 on the low-voltage output side. Insulation capability is defined according to certification agency definitions and using industry-standard test methods as defined in *Section 6.6*. Assessment of device lifetime working voltages follow the IEC 60747-17 standard for basic and reinforced insulation, requiring time-dependent dielectric breakdown (TDDB) data-projection are based on projected failure rates of less than 1 part per million (ppm) for reinforced insulation and less than 1000ppm for basic insulation, and a minimum insulation lifetime of 30 years. For reinforced insulation, the IEC 60747-17 standard also requires additional safety margins of 20% for working voltage, and 50% for insulation lifetime, translating into a minimum required lifetime of 30 years at 800V_{RMS} for the TMCS1133-Q1 .

Figure 8-2 shows the intrinsic capability of the isolation barrier to withstand high-voltage stress over the lifetime of the device. Based on the TDDB data, the intrinsic capability of these devices is 670V_{RMS} with a lifetime > 20 years. Other factors such as operating environment and pollution degree can further limit the working voltage of the component in an end system.

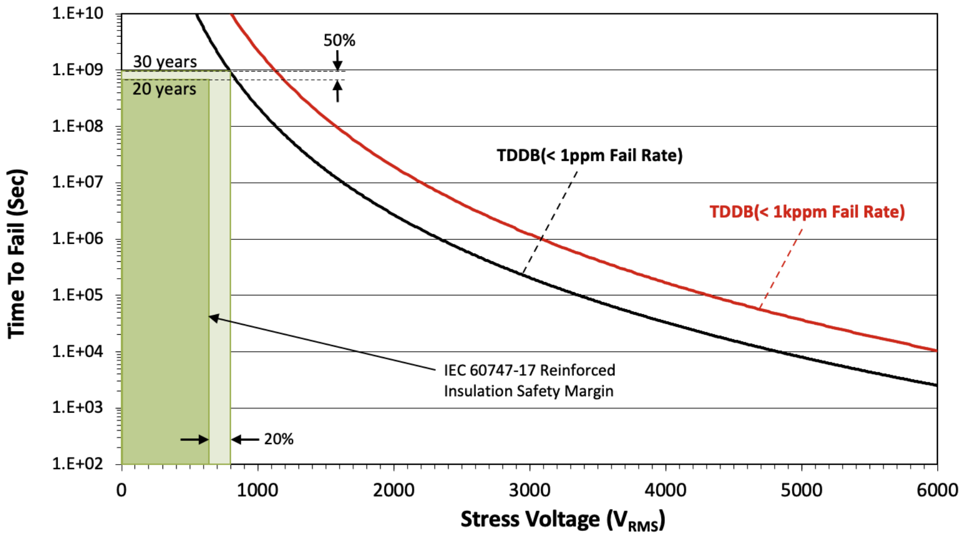


Figure 8-2. Insulation Lifetime

8.3.3 Ambient Field Rejection

The TMCS1133-Q1 is designed to provide high levels of current measurement accuracy in harsh environments. Immunity to interference from stray magnetic fields allows for use in close proximity to high current carrying traces, motor windings, inductors, or any other erroneous source of stray magnetic fields. The TMCS1133-Q1 incorporates differential Hall sensors that are strategically located and configured to reject interference from stray external magnetic fields. Ambient Field Rejection (AFR) limited only by Hall element matching and package leadframe coupling reduces errors from stray magnetic fields.

8.3.4 High-Precision Signal Chain

The TMCS1133-Q1 uses a precision, low-drift signal chain with proprietary sensor linearization techniques to provide a highly accurate and stable current measurement across the full temperature range and lifetime of the device. The device is fully tested and calibrated at the factory to account for any variations in either silicon processing, assembly, or packaging of the device. The full signal chain provides a fixed sensitivity voltage output that is proportional to the current flowing through the leadframe of the isolated input.

8.3.4.1 Temperature Stability

The TMCS1133-Q1 includes a proprietary temperature compensation technique which results in significantly improved parametric drift across the full temperature range. This compensation technique accounts for changes in ambient temperature, self-heating, and package stress. A zero-drift signal chain architecture along with Hall sensor temperature compensation methods enable stable sensitivity while minimizing offset errors across temperature. System-level performance is drastically improved across required operating conditions.

8.3.4.2 Lifetime and Environmental Stability

In addition to large thermal drift, typical magnetic current sensors suffer an additional 2% to 3% drift in sensitivity due to aging over the lifetime of the device. The same proprietary compensation techniques used in the TMCS1133-Q1 to reduce temperature drift are also used to greatly reduce lifetime drift due to aging from stress and environmental conditions especially at high operating temperatures. As shown in the *Electrical Characteristics*, the TMCS1133-Q1 has industry leading lifetime sensitivity drift realized after Highly Accelerated Stress Tests (HAST) at 130°C and 85% relative humidity (RH) during standard three lot AEC-Q100 qualifications. Low sensitivity and offset drift within the bounds specified in the *Electrical Characteristics* are also observed after 1000 hour, 125°C high temperature operating life stress tests are performed as prescribed by AEC-Q100 qualifications. These tests mimic typical device lifetime operation, and show device performance variation due to aging is vastly improved compared with typical magnetic current sensors. Figure 8-3 and Figure 8-4 show the sensitivity and offset drift after a 1000 hour, 125°C high temperature operating life stress test as specified by AEC-Q100. Device operational performance varies over the lifetime of the device. This test mimics typical device lifetime operations and shows the likelihood of the device vastly improving performance compared to typical magnetic sensors.

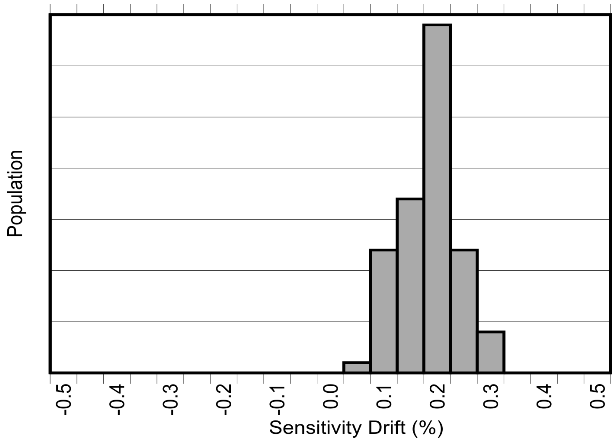


Figure 8-3. Sensitivity Error Drift After AEC-Q100 High Temperature Operating Life Stress Test

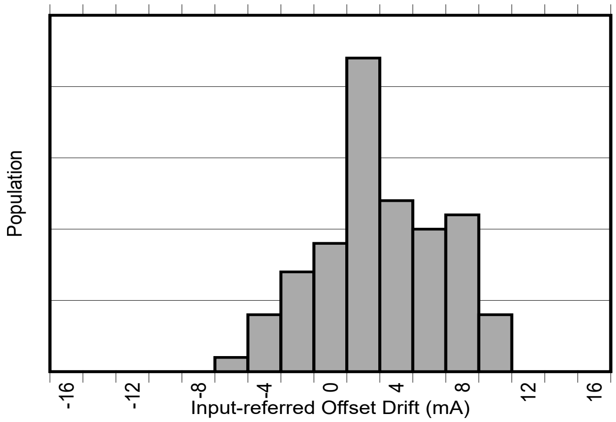


Figure 8-4. Input-Referred Offset Drift After AEC-Q100 High Temperature Operating Life Stress Test

8.3.5 Internal Reference Voltage

The TMCS1133-Q1 has a precision internal reference that determines the zero current output voltage, $V_{OUT,0A}$. Overall current sensing dynamic range can be optimized by choosing either of the three different zero current output voltage options listed in the *Device Comparison* table. These extremely low-drift precision zero current reference options are listed in Equation 14, Equation 15 , Equation 16 and Equation 17. These equations are for precise bidirectional or unidirectional current measurements using various supply voltages ranging between 3.0V to 5.5V.

$$\text{TMCS11xxAxx-Q1} \rightarrow V_{OUT,0A} = V_{REF} = 2.5\text{V} \tag{14}$$

$$\text{TMCS1133Bxx-Q1} \rightarrow V_{OUT,0A} = V_{REF} = 1.65\text{V} \tag{15}$$

$$\text{TMCS1133Dxx-Q1} \rightarrow V_{OUT,0A} = V_{REF} = 1.5\text{V} \tag{16}$$

$$\text{TMCS1133Cxx-Q1} \rightarrow V_{OUT,0A} = V_{REF} = 0.33\text{V} \tag{17}$$

8.3.6 Current-Sensing Measurable Ranges

The zero current reference voltage, V_{REF}, along with device sensitivity, S, and supply voltage, V_S, determine the TMCS1133-Q1 linear input current measurement ranges listed in the *Device Comparison* table. The maximum linear output voltage, $V_{OUT,max}$, is limited to 100mV less than the supply voltage as shown in Equation 18. The minimum linear output voltage, $V_{OUT,min}$, is limited to 100mV above ground as shown in Equation 19.

$$V_{OUT,\,max} = V_S - 100\text{mV} \tag{18}$$

$$V_{OUT,\,min} = 100\text{mV} \tag{19}$$

Overall maximum dynamic range can be optimized with proper device selection by referring minimum and maximum linear output voltage swing to minimum and maximum linear input current range by dividing output voltage by sensitivity, S (see Equation 20 and Equation 21).

$$I_{IN,\,max+} = \frac{(V_{OUT,\,max} - V_{OUT,\,0A})}{S} \tag{20}$$

$$I_{IN,\ max-} = \frac{(V_{OUT,0A} - V_{OUT,min})}{S} \quad (21)$$

where

- $I_{IN,max+}$ is the maximum linear measurable positive input current.
- $I_{IN,max–}$ is the maximum linear measurable negative input current.
- S is the sensitivity of the device variant.
- $V_{OUT,0A}$ is the appropriate zero current output voltage.

As examples for determining linear input current measurement range, consider TMCS11xxA2A-Q1, TMCS11xxB2A-Q1, and TMCS11xxC2A-Q1 devices, all with 50mV/A sensitivity as shown in the *Device Comparison* table. When used with a 5V supply, the TMCS11xxA2A-Q1 has a balanced ±48A bidirectional linear current measurement range about the 2.5V zero current output reference voltage, V_{REF}, as shown in Figure 8-5. When used with a 3.3V supply, the TMCS11xxB2A-Q1 has a balanced ±31A bidirectional linear current measurement range about the 1.65V zero current output reference voltage. If used with a 5V supply, the linear current measurement range of the TMCS11xxB2A-Q1 can be extended from –31A to 65A as shown in Figure 8-5. The TMCS11xxC2A-Q1 with a 0.33V zero current reference voltage is intended for measuring unidirectional currents. When used with a 3.3V supply the TMCS11xxC2A-Q1 has a unidirectional linear current measurement range from –5A to 57A which can be extended from –5A to 91.4A when used with a 5V supply.

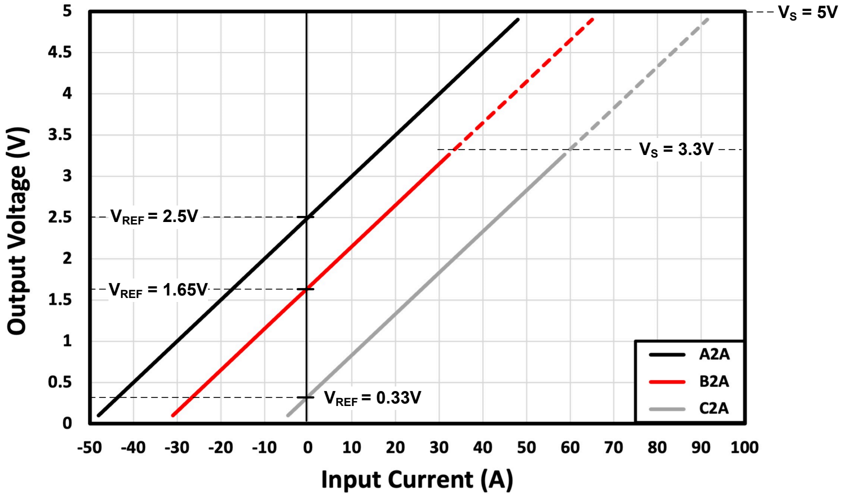


Figure 8-5. Output Voltage Relationship to Input Current for TMCS11xxx2A-Q1

8.3.7 Overcurrent Detection

In addition to the precision analog signal, the TMCS1133-Q1 also offers a fast digital overcurrent detection response. The Overcurrent Detection (OCD) circuit provides an open-drain comparator output that can be used to trigger a warning or initiate a system shutdown to prevent damage from excessive current flow caused by short circuits, motor stalls, or other unintended system conditions. This fast digital response can be configured on both bidirectional and unidirectional devices to assert based on a signal that is anywhere from half to over twice the full-scale analog measurement range.

Use of this fast digital output $\overline{OC}$ instead of the precision analog output VOUT to detect overcurrent events outside the nominal operating current range allows for higher dynamic range with higher sensitivity optimized for the nominal operating current range. Use of this fast digital output $\overline{OC}$ also allows for lower overall signal noise from lower analog signal bandwidth than often needed when using the analog signal chain to detect fast overcurrent events.

8.3.7.1 Setting The User Configurable Overcurrent Threshold

The desired overcurrent threshold, I_{OC}, is set by applying an external voltage, V_{OC}, to the VOC pin according to Equation 22.

$$V_{OC} = \frac{S \times I_{OC}}{2.5} \tag{22}$$

where

- S is the device sensitivity in V/A.
- I_{OC} is the desired overcurrent threshold in A.
- V_{OC} is the voltage applied that sets the overcurrent threshold in V.

An example of how to set the desired overcurrent threshold, I_{OC}, is shown in Section 8.3.7.1.2. Regardless of which TMCS1133-Q1 sensitivity variant is chosen or which zero current output voltage option is selected, Equation 22 applies when calculating overcurrent threshold voltage V_{OC}. A digital-to-analog converter (DAC) can be used to set the desired overcurrent threshold I_{OC}, or a simple external resistor divider circuit can be used as shown in Section 8.3.7.1.1.

8.3.7.1.1 Setting Overcurrent Threshold Using Power Supply Voltage

A simple external resistor divider driven from the power supply as shown in Figure 8-6 can be used to generate the external overcurrent voltage V_{OC} applied to the VOC pin to set the desired overcurrent threshold I_{OC} according to Equation 22.

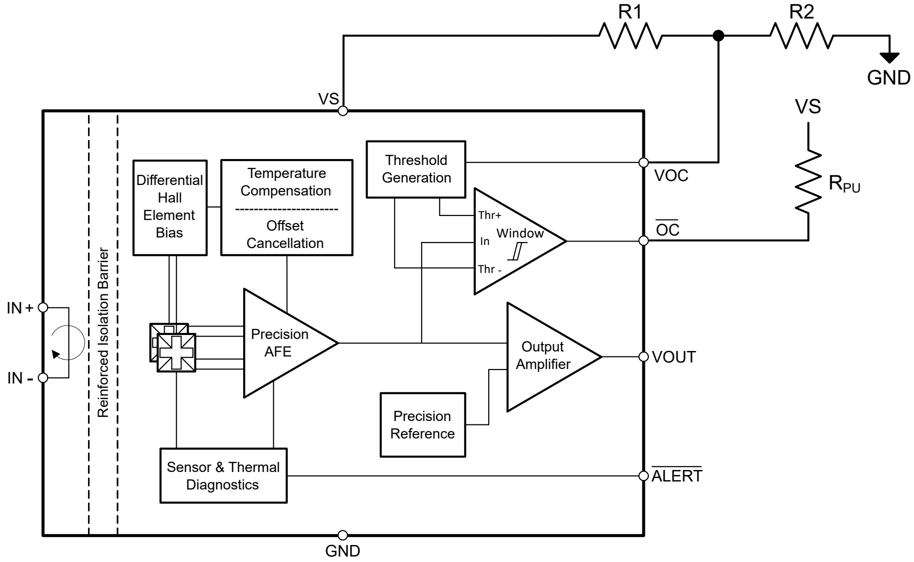


Figure 8-6. User Configurable Overcurrent Threshold Using Power Supply Voltage

When using a resistor divider as shown in Figure 8-6, R2 must be less than 10kΩ to mitigate the impact of the VOC input impedance on overcurrent threshold accuracy.

8.3.7.1.2 Setting Overcurrent Threshold Example

For example, to set a desired overcurrent threshold to I_{OC} = ±50A on bidirectional TMCS1133A3A-Q1 or TMCS1133B3A-Q1 devices with ±32A linear measurement range, as well as on the unidirectional TMCS1133C3A-Q1 device, size the resistors R1 and R2 to apply a voltage V_{OC} = 1.5V to the VOC pin according to Equation 22.

with

- TMCS1133A3A-Q1, TMCS1133B3A-Q1 and TMCS1133B3A-Q1 device sensitivity, S = 0.075V/A.
- Desired overcurrent threshold, I_{OC} = ±50A.
- Applied overcurrent threshold voltage V_{OC} = 1.5V.

8.3.7.2 Overcurrent Output Response

Figure 8-7 shows the active-low overcurrent digital output $\overline{OC}$ response to bidirectional overcurrent events. When the input current exceeds $|\pm I_{OC}|$ on a bidirectional device, the fast $\overline{OC}$ pin is pulled low. The input current must return to within ±I_{OC} by more than a hysteresis current I_{Hys} before the $\overline{\text{OC}}$ pin resets back to the normal high-state.

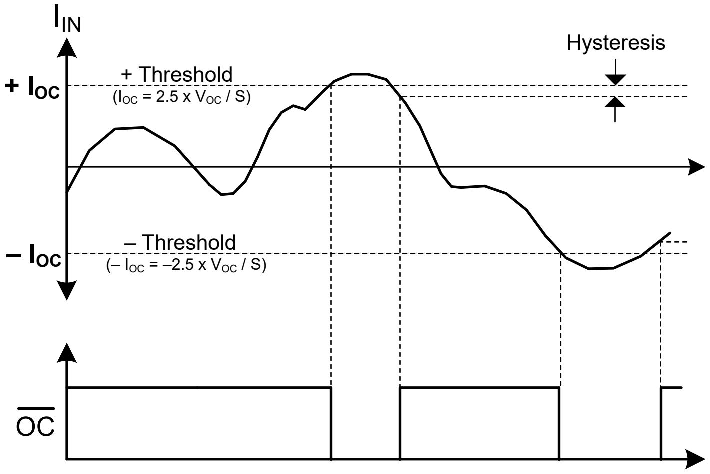


Figure 8-7. Overcurrent Output Response

8.3.8 Sensor Diagnostics

Built-in self-diagnostic features are incorporated in the TMCS1133-Q1 to warn when operating conditions invalidate current sensor measurements. Two critical conditions being monitored are sensor temperature and sensitivity.

8.3.8.1 Thermal Alert

As discussed in the *Safe Operating Area* section, high levels of input current can generate excessive heat inside the TMCS1133-Q1 . High input currents, coupled with elevated ambient temperatures and printed circuit board thermal design can cause the TMCS1133-Q1 to overheat and be permanently damaged by exceeding maximum allowed junction temperatures. A thermal alert occurs when the internal temperature approaches the maximum allowed junction temperature.

8.3.8.2 Sensor Alert

In addition to temperature, sensor sensitivity and offset are constantly being monitored inside the TMCS1133-Q1 . A sensor alert occurs in the unlikely event Hall sensor sensitivity or offset is out of range compared with factory set limits.

The active-low $\overline{\text{ALERT}}$ output signal can be used to decipher which of four diagnostic states the TMCS1133-Q1 resides. As shown in Figure 8-8, the duty cycle of the 8kHz PWM output signal indicates which, neither, or both of the thermal and sensor operating condition warnings exist.

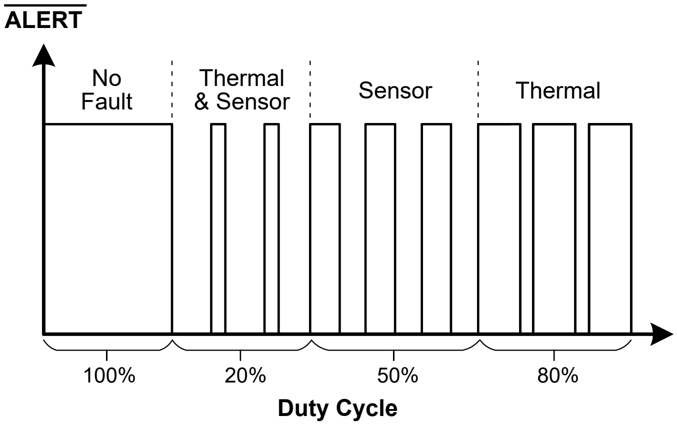


Figure 8-8. Sensor Diagnostics Waveform

8.4 Device Functional Modes

8.4.1 Power-Down Behavior

As a result of the inherent galvanic isolation of the device, very little consideration must be paid to powering down the device, as long as the limits in the *Absolute Maximum Ratings* table are not exceeded on any pins. The isolated current input and the low-voltage signal chain can be decoupled in operational behavior, as either can be energized with the other shutdown, as long as the isolation barrier capabilities are not exceeded. The low-voltage power supply can be powered down while the isolated input is still connected to an active high-voltage signal or system.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The key feature sets of the TMCS1133-Q1 provide significant advantages in any application where an isolated current measurement is required.

- Galvanic isolation provides a high isolated working voltage and excellent immunity to input voltage transients.
- Hall-based measurement simplifies system level designs without the need for a power supply on the high-voltage (HV) side.
- An input current path through the low impedance conductor minimizes power dissipation.
- Excellent accuracy and low temperature drift eliminate the need for multipoint calibrations without sacrificing system performance.
- A wide operating supply range enables a single device to function across a wide range of voltage levels.

These advantages increase system-level performance while minimizing complexity for any application where precision current measurements must be made on isolated currents. Specific examples and design requirements are detailed in the following section.

9.1.1 Total Error Calculation Examples

Users can calculate the total error for any arbitrary device condition and current level. Consider error sources like input-referred offset current (I_{OS}), Common Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio

(PSRR), sensitivity error, nonlinearity, as well as errors caused by any external magnetic fields (B_{EXT}). Compare each of these error sources in percentage terms, as some are significant drivers of error and some have inconsequential impact to current measurement error. Offset (Equation 23), CMRR (Equation 24), PSRR, and external magnetic field error (Equation 26) are all referred to the input, and so are divided by the actual input current I_{IN} to calculate percentage errors. For sensitivity error and nonlinearity error calculations, the percentage limits explicitly specified in the *Electrical Characteristics* table can be used.

$$e_{Ios} = \frac{I_{OS}}{I_{IN}} \times 100\% = \frac{V_{OE}}{S \times I_{IN}} \times 100\% \tag{23}$$

$$e_{CMRR} = \frac{CMRR \times V_{CM}}{I_{IN}} \times 100\% \tag{24}$$

$$e_{PSRR,A} = \frac{PSRR \times (V_S - 5V)}{I_{IN}} \times 100\% \; ; \; e_{PSRR,B} = e_{PSRR,C} = \frac{PSRR \times (V_S - 3.3V)}{I_{IN}} \times 100\% \tag{25}$$

$$e_{Bext} = \frac{B_{EXT} \times CMFR}{I_{IN}} \times 100\% \tag{26}$$

where

- V_{OE} is the output-referred offset voltage error.
- V_{CM} is the input common-mode voltage.
- $e_{PSRR,A}$ is the power supply rejection error for TMCS1133Axx-Q1 devices.
- $e_{PSRR,B}$ is the power supply rejection error for TMCS1133Bxx-Q1 devices.
- $e_{PSRR,C}$ is the power supply rejection error for TMCS1133Cxx-Q1 devices.
- V_S is the supply voltage.
- CMFR is the common-mode magnetic field rejection.

When calculating error contributions across temperature, only offset error and sensitivity error contributions vary significantly. To determine the offset error across temperature, use Equation 27 to calculate total input-referred offset error current, I_{OS}, at any ambient temperature, T_A.

$$e_{Ios,\Delta T} = \frac{V_{OE,25°C} + \left(V_{OE,drift} \times |\Delta T|\right)}{S \times I_{IN}} \times 100\% \tag{27}$$

where

- $V_{OE,25°C}$ is the output-referred offset error at 25°C.
- $V_{OE,drift}$ is the output-referred offset drift with temperature in µV/°C.
- ΔT is the change in temperature from 25°C.
- S is the sensitivity of the device variant.

Sensitivity error at 25°C is specified as $e_{S,25°C}$ in the *Electrical Characteristics* table along with sensitivity variation over temperature as sensitivity thermal drift $S_{drift,therm}$ in ppm/°C. To determine the sensitivity error across temperature, use Equation 28 to calculate sensitivity error at any ambient temperature, T_A, over the given application operating ambient temperature range between –40°C and 125°C.

$$e_{S,\Delta T} = e_{S,25°C} + \left(S_{drift,therm} \times |\Delta T| \times 100\%\right) \tag{28}$$

To accurately calculate the total expected error of the device, the contributions from each of the individual components above must be understood in reference to operating conditions. To account for the individual error sources that are statistically uncorrelated, use a root sum square (RSS) error calculation to calculate total error. For the TMCS1133-Q1 , only the input-referred offset current (I_{OS}), CMRR, and PSRR are statistically correlated. These error terms are lumped in an RSS calculation to reflect this nature, as shown in Equation 29 for room temperature and in Equation 30 across a given temperature range. The same methodology can be applied for calculating typical total error by using the appropriate error term specification.

$$e_{RSS} = \sqrt{(e_{Ios}+e_{PSRR}+e_{CMRR})^2 + (e_{Bext})^2 + (e_S)^2 + (e_{NL})^2} \tag{29}$$

$$e_{RSS,\Delta T} = \sqrt{(e_{Ios,\Delta T}+e_{PSRR}+e_{CMRR})^2 + (e_{Bext})^2 + (e_{S,\Delta T})^2 + (e_{NL})^2} \tag{30}$$

The total error calculation has a strong dependence on the actual input current, therefore always calculate total error across the dynamic range that is required. These curves asymptotically approach the sensitivity and nonlinearity error at high current levels, and approach infinity at low current levels due to offset error terms with input current in the denominator. Key figures of merit for any current-measurement system include the total error percentage at full-scale current, as well as the dynamic range of input current over which the error remains below some key level. Figure 9-1 shows the RSS maximum total error as a function of input current for a TMCS1133A2A-Q1 at room temperature and across the full temperature range with a 5.25V supply.

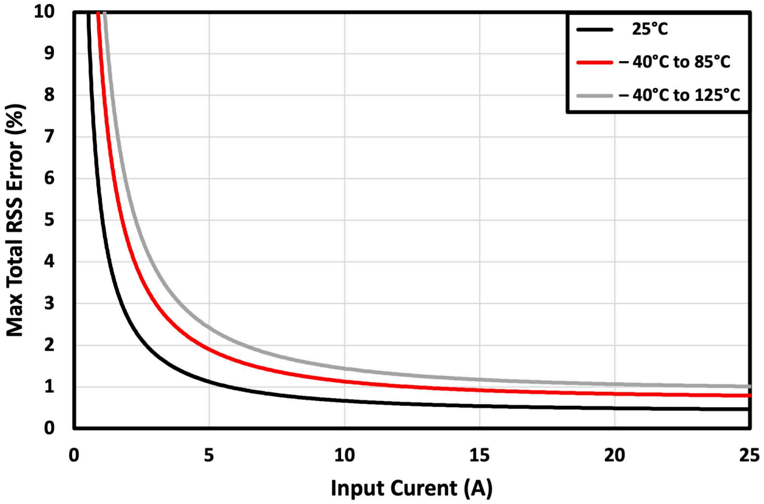


Figure 9-1. RSS Error vs Input Current

9.1.1.1 Room-Temperature Error Calculations

For room-temperature total error calculations, specifications across temperature and drift are ignored. As an example, consider a TMCS1133B2A-Q1 with a supply voltage (V_S) of 3.1V and a worst-case common-mode excursion of 600V to calculate operating-point specific parameters. Consider a measurement error due to an external 400μT magnetic field generated by a 20A_{DC} current flowing through an adjacent trace or conductor that is 10mm away. The full-scale current range of the device in specified conditions is slightly greater than ±31A, as shown in the *Device Comparison* table. In this case, the calculating error at both 25A and 12.5A highlights error dependencies on the input-current level. Table 9-1 shows the individual error components and RSS maximum total error calculations at room temperature under the conditions specified. Relative to other errors, the additional errors from CMRR, external ambient magnetic fields B_{EXT} and nonlinearity are negligible, and can typically be excluded from total error calculations.

Table 9-1. Total Error Calculation: Room Temperature Example

ERROR COMPONENT	SYMBOL	EQUATION	ERROR AT I_{IN} = 25A	ERROR AT I_{IN} = 12.5A
Input offset error	e_{Ios}	$e_{Ios} = \frac{I_{OS}}{I_{IN}} \times 100\% = \frac{V_{OE}}{S \times I_{IN}} \times 100\% = \frac{\pm 2mV}{50mV/A \times I_{IN}} \times 100\%$	±0.16%	±0.32%
PSRR error	e_{PSRR}	$e_{PSRR} = \frac{PSRR \times (V_S - 3.3)}{I_{IN}} \times 100\%$	±0.04%	±0.08%
CMRR error	e_{CMRR}	$e_{CMRR} = \frac{CMRR \times V_{CM}}{I_{IN}} \times 100\%$	±0.01%	±0.02%
External Field error	e_{Bext}	$e_{Bext} = \frac{B_{EXT} \times CMFR}{I_{IN}} \times 100\%$	±0.02%	±0.03%
Sensitivity error	e_S	Specified in *Electrical Characteristics*	±0.4%	±0.4%
Nonlinearity error	e_{NL}	Specified in *Electrical Characteristics*	±0.1%	±0.1%
RSS total error	e_{RSS}	$e_{RSS} = \sqrt{(e_{Ios}+e_{PSRR}+e_{CMRR})^2 + (e_{Bext})^2 + (e_S)^2 + (e_{NL})^2}$	0.46%	0.59%

9.1.1.2 Full-Temperature Range Error Calculations

To calculate total error across any specific temperature range, use Equation 29 and Equation 30 for RSS maximum total errors, similar to the example for room temperatures. Conditions from the example in *Room-Temperature Error Calculations* are replaced with the respective equations and error components for a –40°C to 85°C temperature range below in Table 9-2.

Table 9-2. Total Error Calculation: –40°C to 85°C Example

ERROR COMPONENT	SYMBOL	EQUATION	ERROR AT I_{IN} = 25A	ERROR AT I_{IN} = 12.5A
Input offset error	$e_{Ios,\Delta T}$	$e_{Ios,\Delta T} = \frac{V_{OE,25^{\circ}C} + (V_{OE,drift} \times \lvert\Delta T\rvert)}{S \times I_{IN}} \times 100\%$	±0.30%	±0.61%
PSRR error	e_{PSRR}	$e_{PSRR} = \frac{PSRR \times (V_S - 3.3)}{I_{IN}} \times 100\%$	±0.04%	±0.08%
CMRR error	e_{CMRR}	$e_{CMRR} = \frac{CMRR \times V_{CM}}{I_{IN}} \times 100\%$	±0.01%	±0.02%
External Field error	e_{Bext}	$e_{Bext} = \frac{B_{EXT} \times CMFR}{I_{IN}} \times 100\%$	±0.02%	±0.03%
Sensitivity error	$e_{S,\Delta T}$	$e_{S,\Delta T} = e_{S,25^{\circ}C} + (S_{drift,therm} \times \lvert\Delta T\rvert \times 100\%)$	±0.70%	±0.70%
Nonlinearity error	e_{NL}	Specified in *Electrical Characteristics*	±0.1%	±0.1%
RSS total error	$e_{RSS,\Delta T}$	$e_{RSS,\Delta T} = \sqrt{(e_{Ios,\Delta T}+e_{PSRR}+e_{CMRR})^2+(e_{Bext})^2+(e_{S,\Delta T})^2+(e_{NL})^2}$	0.79%	1.00%

9.2 Typical Application

In many applications, power must be converted from AC sources for use in DC circuitry. Some type of controlled power factor correction (PFC) stage is typically needed to improve power transfer efficiency. Faster and faster power switches are being used in modern PFC stages to reduce overall size and to improve power transfer efficiency. Often, the PFC stage of AC to DC converters is connected directly to AC power grids. A primary challenge to sensing in PFC stages is that the current sensor is subjected to large voltage spikes coming from the high-voltage (HV) power grid along with large transients coming from high speed power switches during charge transfer. Inherent isolation in the TMCS1133-Q1 construction helps overcome these challenges by providing high levels of isolation between the HV current sensing nodes and low-voltage control circuitry, with high common-mode transient immunity (CMTI). Figure 9-2 shows the use of the TMCS1133-Q1 measuring phase currents in a common AC to DC converter stage.

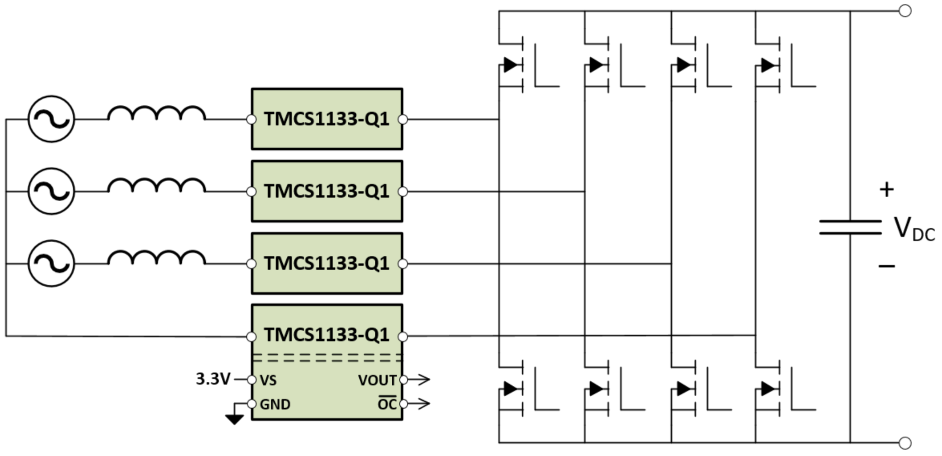


Figure 9-2. AC to DC Converter Current Sensing

9.2.1 Design Requirements

For a 3-phase current sensing application, make sure to provide linear sensing across the expected current range, and make sure that the device remains within working thermal constraints. A single TMCS1133-Q1 can be used to measure current in each phase if necessary. For this example, consider a nominal supply of 5V but a minimum of 4.9V to include for some supply variation. Maximum output swings are defined according to TMCS1133-Q1 specifications, and a full-scale current measurement of ±20A is required.

Table 9-3. Example Application Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
$V_{S,nom}$	5V
$V_{S,min}$	4.9V
$I_{IN,FS}$	±20A

9.2.2 Detailed Design Procedure

The primary design parameter for using the TMCS1133-Q1 is the optimum sensitivity variant based on the required measured current levels and the selected supply voltage. Positive and negative currents are measured in this in-line phase current application example, therefore select a bidirectional variant. The TMCS1133-Q1 has a precision internal reference voltage that determines the zero current output voltage, $V_{OUT,0A}$.

The internal reference voltage on TMCS1133AxA-Q1 variants, with zero current output voltage $V_{OUT,0A}$ = 2.5V is intended for bidirectional current measurements when used with 5V power supplies. The internal reference voltage on TMCS1133BxA-Q1 variants, with zero current output voltage $V_{OUT,0A}$ = 1.65V is intended for bidirectional current measurements when used with 3.3V power supplies. Further consideration of noise and integration with an ADC can be explored, but is beyond the scope of this application design example. The TMCS1133-Q1 output voltage V_{OUT} is proportional to the input current I_{IN} as defined by Equation 31 with output offset set by $V_{OUT,0A}$.

$$V_{OUT} = (I_{IN} \times S) + V_{OUT,\,0A} \tag{31}$$

Design of the sensing solution focuses on maximizing the sensitivity of the device while maintaining linear measurement over the expected current input range. The TMCS1133-Q1 has a linear measurable current range that is constrained by either the positive swing to supply or negative swing to ground. To account for the operating margin, consider the previously defined minimum possible supply voltage $V_{S,min}$ = 4.9V. With the previous parameters, the maximum linear output voltage $V_{OUT,max}$ is defined by Equation 32 and the minimum linear output voltage $V_{OUT,min}$ is defined by Equation 33.

$$V_{OUT,\,max} = V_{S,\,min} - 100mV \tag{32}$$

$$V_{OUT,\,min} = 100mV \tag{33}$$

Design parameters for this example application are shown in Table 9-4 along with the calculated output range.

Table 9-4. Example Application Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{OUT,max}$	4.8V
$V_{OUT,0A}$	2.5V
$V_{OUT,max} - V_{OUT,0A}$	2.3V

These design parameters result in a maximum positive linear output voltage swing of ±2.3V about $V_{OUT,0A}$ = 2.5V. To determine which sensitivity variant of the TMCS1133-Q1 most fully uses this linear range, use Equation 34 to calculate the maximum current range for a bidirectional current $\pm I_{IN,max}$.

$$I_{IN,\,max} = \frac{\left(V_{OUT,\,max} - V_{OUT,\,0A}\right)}{S} \tag{34}$$

where

- S is the sensitivity of the relevant AxA variant.

Table 9-5 shows the calculation for each gain variant of the TMCS1133-Q1 with the appropriate sensitivities.

Table 9-5. Maximum Full-Scale Current Ranges With 2.3V Positive Output Swing

VARIANT	SENSITIVITY	$I_{IN,max}$
TMCS1133A1A-Q1	25mV/A	±92A
TMCS1133A2A-Q1	50mV/A	±46A
TMCS1133A3A-Q1	75mV/A	±30.6A
TMCS1133A4A-Q1	100mV/A	±23A
TMCS1133A5A-Q1	150mV/A	±15.3A

In general, the highest sensitivity variant is selected to provide the lowest maximum input current range that is larger than the desired full-scale current range. For the design parameters in this example, the TMCS1133A4A-Q1 with sensitivity of 100mV/A is the proper selection because the maximum ±23A linear measurable range is larger than the desired ±20A full-scale current range.

9.2.3 Application Curve

To illustrate high levels of isolation achievable between noisy high-voltage current sensing nodes and low-voltage precision current measurement and control circuitry, Figure 9-3 shows the output signal from the TMCS1133-Q1 in a noisy in-phase PWM motor control example. In this example with a large induction motor under no load, no PWM edge interference is seen on the current sensor output with high-voltage PWM switching on the current sensor input, as is often pronounced on many current sensors.

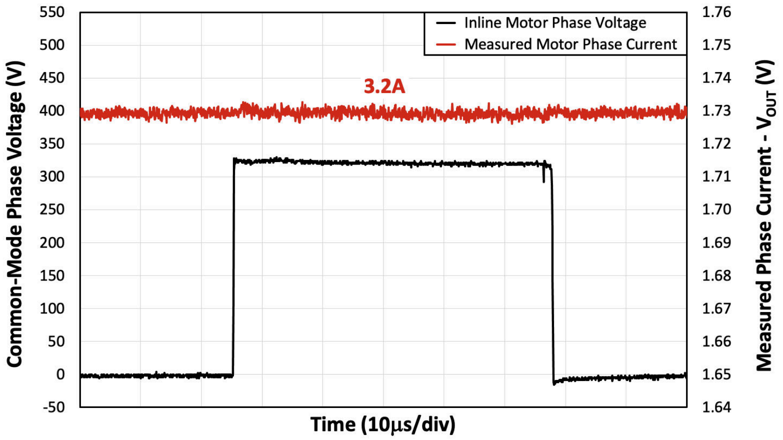


Figure 9-3. Inline Motor Current-Sense Input and Output Signals

9.3 Power Supply Recommendations

The TMCS1133-Q1 only requires a power supply (V_S) on the low-voltage isolated side, which powers the analog circuitry independent of the isolated current input. V_S determines the full-scale output range of the analog output V_{OUT}, and can be supplied with any voltage between 3V and 5.5V. To filter noise in the power-supply path, place a low-ESR decoupling capacitor of 0.1µF between V_S and GND pins as close as possible to the supply and ground pins of the device. More decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. When used in extremely noisy environments, ferrite beads can be added close to the supply pin as shown in Figure 9-4 to target and suppress high-frequency noise coupled on to system supply.

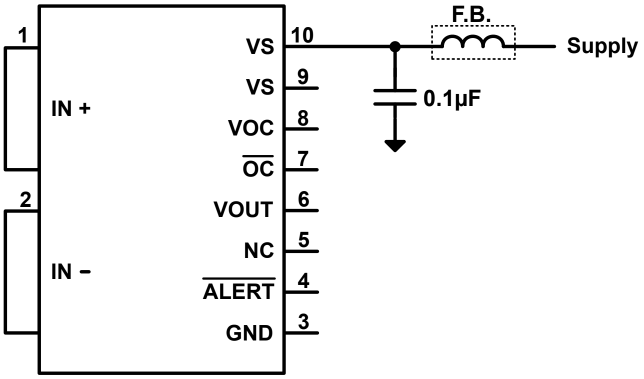


Figure 9-4. Power Supply Noise Filtering

The TMCS1133-Q1 power supply V_S can be sequenced independently of current flowing through the input. However, there is a power-on delay between V_S reaching the recommended operating voltage and the analog output validation. During this power-on time, the output voltage V_{OUT} can transition between GND and V_S as the output transfers from a high impedance reset state to the active drive state. If this behavior must be avoided, then provide a stable supply voltage V_S for longer than the power-on time prior to applying input current.

9.4 Layout

9.4.1 Layout Guidelines

The TMCS1133-Q1 is specified for a continuous current handling capability on the *TMCS1133xEVM* which uses 4oz copper planes. This current capability is fundamentally limited by the maximum device junction temperature and the thermal environment, primarily the PCB layout and design. To maximize current-handling capability and thermal stability of the device, take care with PCB layout and construction to optimize the thermal capability. Efforts to improve the thermal performance beyond the design and construction of the *TMCS1133xEVM* can result in increased continuous-current capability due to higher heat transfer to the ambient environment. Keys to improving thermal performance of the PCB include:

- Use large copper planes for both input current path and isolated power planes and signals.
- Use heavier copper PCB construction.
- Place thermal via *farms* around the isolated current input.
- Provide airflow across the surface of the PCB.

9.4.2 Layout Example

An example layout, shown in Figure 9-5, is from the *TMCS1133xEVM User's Guide* . Device performance is targeted for thermal and magnetic characteristics of this layout, which provides optimal current flow from the terminal connectors to the device input pins while large copper planes enhance thermal performance.

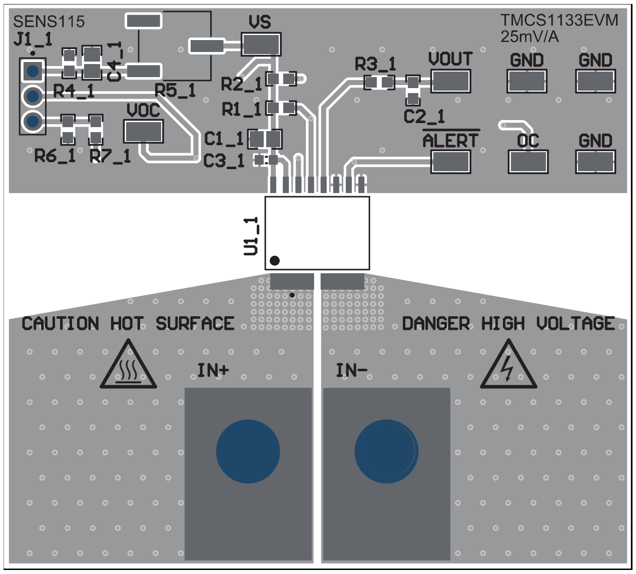


Figure 9-5. Recommended Board Layout

10 Device and Documentation Support

10.1 Device Nomenclature

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *DVG*), the temperature range, and the device speed range, in megahertz.

For orderable part numbers of *TMCS1133-Q1* devices in the *SOIC* package types, see the Package Option Addendum of this document, ti.com, or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *Silicon Errata*.

10.2 Device Support

10.2.1 Development Support

For development tool support see the following:

- Texas Instruments, *TMCS1133xEVM*

10.3 Documentation Support

10.3.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TMCS1133xEVM User's Guide*
- Texas Instruments, *Isolation Glossary*, application note

10.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2025) to Revision B (June 2025) **Page**

- Changed TMCS110AxB orderable statuses from *Advanced Information* to *Production Data* 1
- Updated the number formatting for tables, figures, and cross-references throughout the document 1
- Added Power Ratings to the *Specifications* 5
- Added Safety-Related Certification to the *Specifications* 5
- Added Safety Limiting Values to the *Specifications* 5
- Updated the VIORM in the *Insulation Specifications* section from 1344V to 1697V peak.......... 6
- Updated the reinforced isolation working voltage in the *Insulation Specifications* section from 600V to 950V RMS.......... 6
- Updated the reinforced isolation working voltage in the *Insulation Specifications* section from 849V to 1343V DC.......... 6
- Updated the basic isolation working voltage in the *Insulation Specifications* section from 950V to 1200V RMS.......... 6
- Updated the basic isolation working voltage in the *Insulation Specifications* section from 950V to 1697V DC. 6
- Added the Input-Referred Noise Density vs Frequency graph to the *Typical Characteristics* 11
- Added the Insulation Characteristics Curves to the *Typical Characteristics* 11
- Added the Input Isolation section to *Feature Description* for clarification.......... 22

Changes from Revision * (February 2025) to Revision A (February 2025) **Page**

- Updated the number formatting for tables, figures, and cross-references throughout the document 1

- Added the *Setting The User Configurable Overcurrent Threshold*, *Setting Overcurrent Threshold Using Power Supply Voltage*, *Setting Overcurrent Threshold Using Internal Reference Voltage*, *Setting Overcurrent Threshold Example*, and *Overcurrent Output Response sections* to the *Overcurrent Detection* section.........25

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMCS1133A1AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133A1AQ1
TMCS1133A1AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133A1AQDVGRQ	1133A1AQ1
TMCS1133A2AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133A2AQ1
TMCS1133A2AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133A2AQDVGRQ	1133A2AQ1
TMCS1133A3AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133A3AQ1
TMCS1133A3AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133A3AQDVGRQ	1133A3AQ1
TMCS1133A4AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133A4AQ1
TMCS1133A4AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133A4AQDVGRQ	1133A4AQ1
TMCS1133A5AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133A5AQ1
TMCS1133A5AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133A5AQDVGRQ	1133A5AQ1
TMCS1133B1AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133B1AQ1
TMCS1133B1AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133B1AQDVGRQ	1133B1AQ1
TMCS1133B2AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133B2AQ1
TMCS1133B2AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133B2AQDVGRQ	1133B2AQ1
TMCS1133B3AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133B3AQ1
TMCS1133B3AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133B3AQDVGRQ	1133B3AQ1
TMCS1133B4AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133B4AQ1
TMCS1133B4AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133B4AQDVGRQ	1133B4AQ1
TMCS1133B5AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133B5AQ1
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TMCS1133B7AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133B7AQ1

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMCS1133B7AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133B7AQDVGRQ	1133B7AQ1
TMCS1133B8AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133B8AQ1
TMCS1133B8AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133B8AQDVGRQ	1133B8AQ1
TMCS1133C1AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133C1AQ1
TMCS1133C1AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133C1AQDVGRQ	1133C1AQ1
TMCS1133C2AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133C2AQ1
TMCS1133C2AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133C2AQDVGRQ	1133C2AQ1
TMCS1133C3AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133C3AQ1
TMCS1133C3AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133C3AQDVGRQ	1133C3AQ1
TMCS1133C4AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133C4AQ1
TMCS1133C4AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133C4AQDVGRQ	1133C4AQ1
TMCS1133C5AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133C5AQ1
TMCS1133C5AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133C5AQDVGRQ	1133C5AQ1
TMCS1133C9AQDVGRQ1	Active	Production	SOIC (DVG) | 10	2000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1133C9AQ1
TMCS1133C9AQDVGRQ1.A	Active	Production	null (null) |	2000 | LARGE T&R	-	SN	Level-2-260C-1 YEAR	See TMCS1133C9AQDVGRQ	1133C9AQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMCS1133-Q1 :

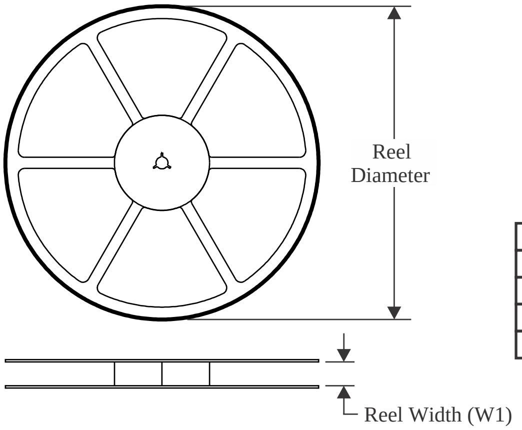
- Catalog : TMCS1133

NOTE: Qualified Version Definitions:

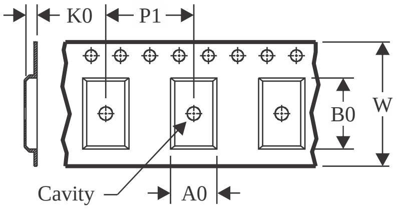
  - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

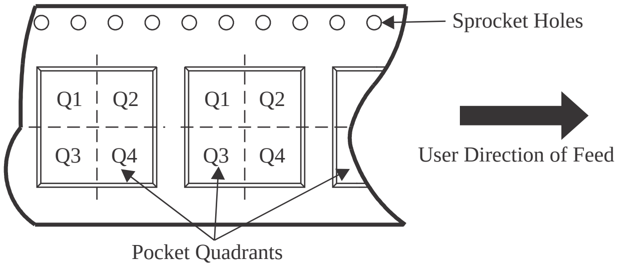


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

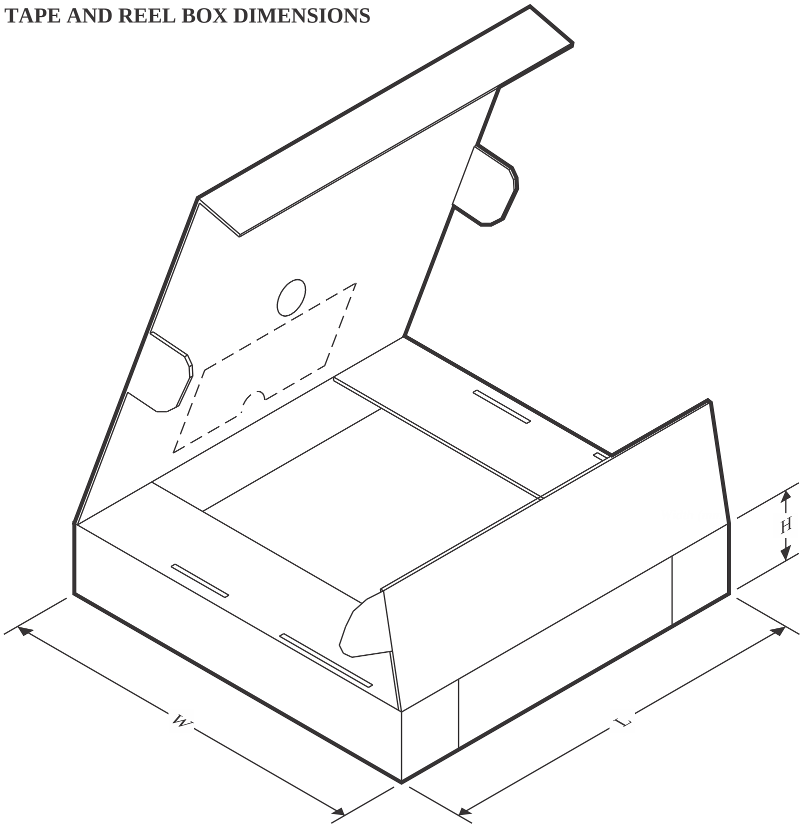


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMCS1133A1AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133A2AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133A3AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133A4AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133A5AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133B1AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133B2AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133B3AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133B4AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133B5AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133B7AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133B8AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133C1AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133C2AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133C3AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133C4AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMCS1133C5AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TMCS1133C9AQDVGRQ1	SOIC	DVG	10	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



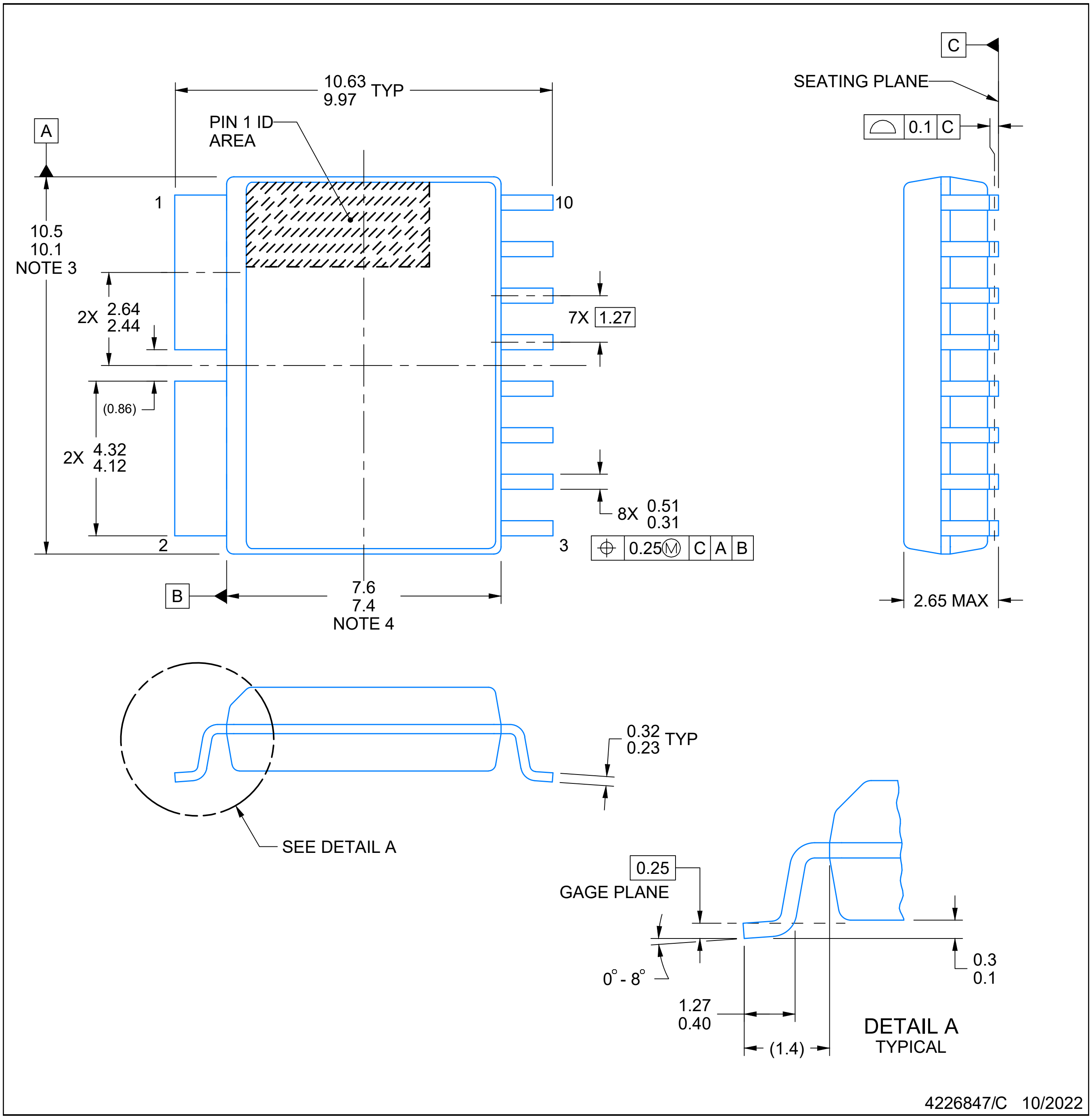
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMCS1133A1AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133A2AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133A3AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133A4AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133A5AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133B1AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133B2AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133B3AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133B4AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133B5AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133B7AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133B8AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133C1AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133C2AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133C3AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133C4AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133C5AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0
TMCS1133C9AQDVGRQ1	SOIC	DVG	10	2000	350.0	350.0	43.0

DVG0010A

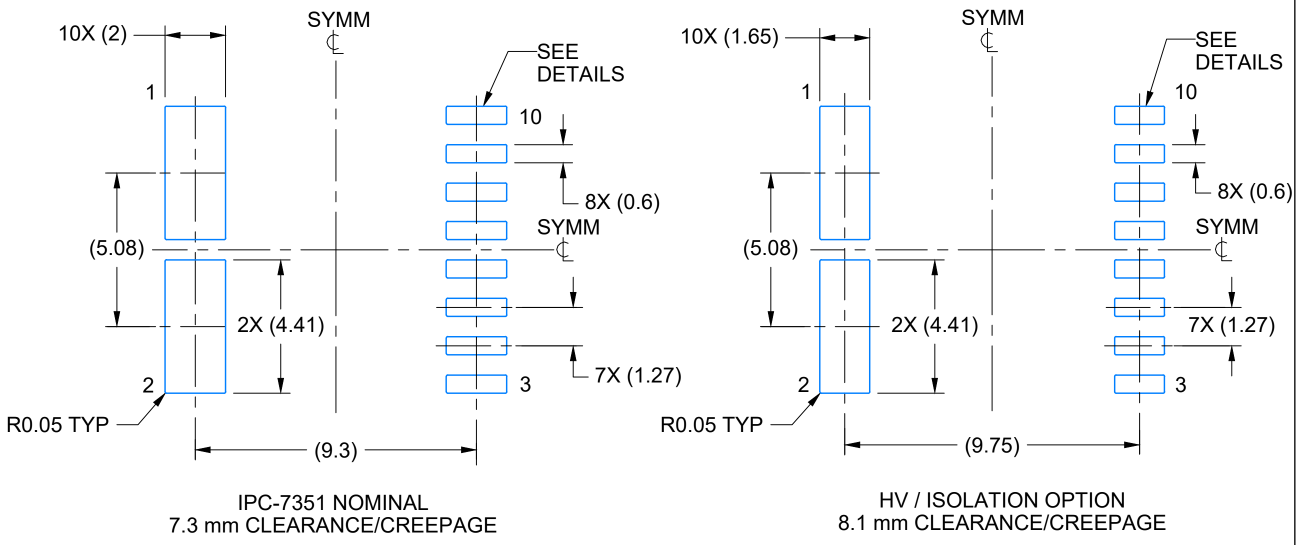
SOIC - 2.65 mm max height

SMALL OUTLINE PACKAGE

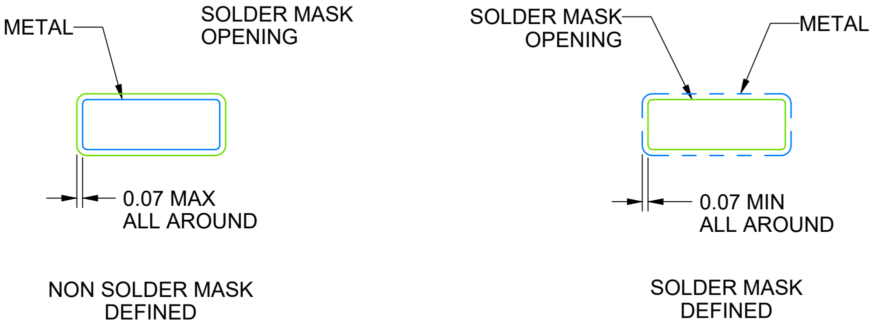


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



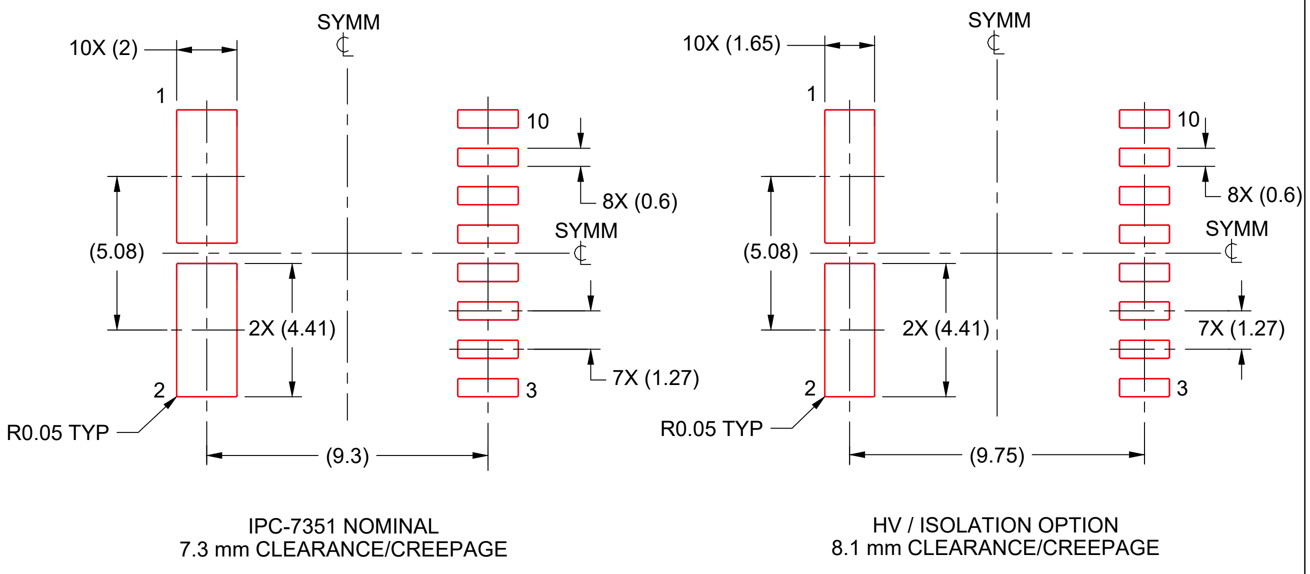
LAND PATTERN EXAMPLE
SCALE:4X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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