TMAG5173-Q1 High-Precision 3D Hall-Effect Sensor With I²C Interface

1 Features

- High-precision linear 3D Hall-effect sensor to optimize position sensing speed and accuracy:
  - Sensitivity room temperature error, X, Y, Z axes: ±2.5% (maximum)
  - Sensitivity mismatch temperature drift X-Y axes: ±2% (maximum)
  - X-Y angle measurement room temperature error: ±1.1° (maximum)
  - X-Y angle measurement temperature drift: ±1.2° (maximum)
  - 20kSPS conversion rate for single axis
- Functional Safety-Compliant:
  - Developed for functional safety applications
  - Documentation available to aid ISO 26262 system design
  - Systematic capability up to ASIL D
  - Hardware integrity up to ASIL B or SIL 2
- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to 125°C
- Configurable power modes including:
  - 8nA (typical) sleep mode current
- Selectable linear magnetic range at X, Y, or Z axis:
  - TMAG5173x1-Q1: ±40mT, ±80mT
  - TMAG5173x2-Q1: ±133mT, ±266mT
- Interrupt signal from user-defined magnetic and temperature threshold cross
- Configurable unipolar and omnipolar switch function
- Integrated angle CORDIC calculation with gain and offset adjustment
- Configurable averaging filter for noise reduction
- I²C interface with cyclic redundancy check (CRC):
  - Maximum 1MHz I²C clock speed
- Conversion trigger by I²C or dedicated $\overline{\text{INT}}$ pin
- Integrated temperature compensation for multiple magnet types
- Built-in temperature sensor
- 2.3V to 3.6V supply range
- I²C and $\overline{\text{INT}}$ pin tolerance: 5.5V (maximum)

2 Applications

- Steering column control
- Steering wheel control
- Shifter systems
- E-bikes
- Actuators
- Door module
- Power seats
- Magnetic proximity switch

3 Description

The TMAG5173-Q1 is a low-power linear 3D Hall-effect sensor designed for a wide range of automotive and industrial applications. This device integrates three independent Hall-effect sensors in the X, Y, and Z axes. A precision analog signal-chain supports applications requiring narrow design tolerance. Integrated safety mechanisms enable robust functional safe system design. The device can be used in 1D linear measurements, 2D angle measurements, 3D joystick measurements, magnetic threshold cross detection, and various user configurable switch function applications. The digital filter option allows up to 32 times sensor data integration for improved noise performance. The I²C interface, while supporting multiple operating V_{CC} ranges, ensures seamless data communication with microcontrollers. The device has an integrated temperature sensor available for multiple system functions, such as thermal budget check or temperature compensation calculation for a given magnetic field.

The TMAG5173-Q1 supports multiple operating modes (including wake-up and sleep mode) to optimize the system power consumptions and operating speed. During the active mode the device performs continuous conversions autonomously. During standby mode the $\overline{\text{INT}}$ pin or I²C communication can be used by a microcontroller to trigger a new conversion. During the sleep mode the device consumes ultra-low power and retains the configuration register values.

An integrated angle calculation engine (CORDIC) provides full 360° angular position information for both on-axis and off-axis topologies with an angle resolution of 1/16 degree. The angle calculation is performed for any of the X-Y, Y-Z, or Z-X planes based off the user configuration register selection. The device features magnetic gain and offset correction to mitigate the impact of system mechanical error sources.

The TMAG5173-Q1 can be configured through the user registers to enable any combination of magnetic axes and temperature channel conversions. The device supports several I²C read frames along with cyclic redundancy check and diagnostic status communications.

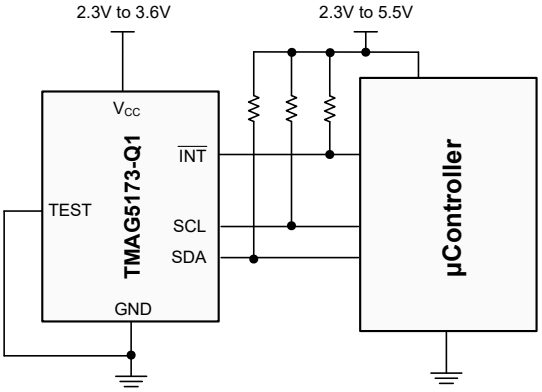
The TMAG5173-Q1 is offered in four different factory-programmed I^2C addresses. The device also supports additional I^2C addresses through the modification of a user-configurable I^2C address register. Each orderable part can be configured to select one of two magnetic field ranges that suits the magnet strength and component placement during system calibration.

The device performs consistently across a wide ambient temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMAG5173-Q1	DBV (SOT-23, 6)	2.9mm × 2.8mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Block Diagram

Table of Contents

4 Pin Configuration and Functions

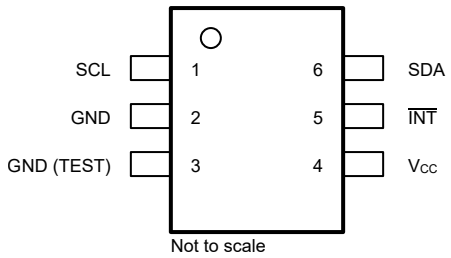


Figure 4-1. DBV Package, 6-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SCL	IO	Serial clock.
2	GND	GND	Ground
3	GND (TEST)	I	TI Test Pin. Connect to ground in application.
4	V_{CC}	P	Supply voltage
5	$\overline{INT}$	IO	Interrupt input/output. If not used and connected to ground, set MASK_INTB = 1b.
6	SDA	IO	Serial data.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Main supply voltage	–0.3	4	V
I_{OUT}	Output current, SDA, $\overline{INT}$	0	10	mA
V_{OUT}	Output voltage, SDA, $\overline{INT}$	–0.3	7	V
V_{IN}	Input voltage, SCL, SDA, , $\overline{INT}$	–0.3	7	V
B_{MAX}	Magnetic flux density		Unlimited	T
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 6, 3, and 4)	±700	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)
over recommended V_{Vcc} range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VCC}	Main supply voltage	2.3		3.6	V
V_{OUT}	Output voltage, SDA, $\overline{INT}$	0		5.5	V
I_{OUT}	Output current, SDA, $\overline{INT}$			2	mA
V_{IH}	Input HIGH voltage, SCL, SDA, $\overline{INT}$	0.7			V_{VCC}
V_{IL}	Input LOW voltage, SCL, SDA, $\overline{INT}$			0.3	V_{VCC}
T_A	Operating free air temperature	–40		125	C

5.4 Thermal Information

THERMAL METRIC(1)		TMAG5173-Q1 DBV (6-SOT23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	30.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)
over recommended V_{Vcc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA, $\overline{INT}$						
V_{OL}	Output LOW voltage, SDA, $\overline{INT}$ pin	I_{OUT} = 2 mA	0		0.4	V
I_{OZ}	Output leakage current, SDA, $\overline{INT}$ pin	Output disabled V_{OZ} = 5.5V			±100	nA
tFALL_$\overline{INT}$	$\overline{INT}$ output fall time	R_{PU} = 10 kΩ C_L = 20pF V_{PU} = 1.7 V to 5.5 V		6		ns
tINT ($\overline{INT}$)	$\overline{INT}$ Interrupt time duration during pulse mode	INT_MODE = 001b or 010b		10		µs
tINT (SCL)	SCL Interrupt time duration	INT_MODE = 011b or 100b		10		µs
DC POWER SECTION						
VCC_{UV}	Under voltage threshold at V_{CC}		1.9	2.1	2.2	V
I_{ACTIVE}	Active mode current X, Y, Z or thermal sensor active conversion	LP_LN = 0b		2.4		mA
		LP_LN = 1b		3.0		mA
$I_{STANDBY}$	Standby mode current	Device in trigger mode, no conversion started		0.45		mA
I_{SLEEP}	Sleep mode current			8		nA
AVERAGE POWER DURING WAKE-UP AND SLEEP (W&S) MODE						
I_{CC_DCM}	W&S mode current consumption, LP_LN = 0b, 1x averaging	Wake-up interval 1-ms, magnetic 1-ch conversion, V_{CC} =3.6V		160		µA
		Wake-up interval 1-ms, magnetic 1-ch conversion, V_{CC} =2.3V		156		µA
		Wake-up interval 1-ms, 4-ch conversion, V_{CC} =3.6V		240		µA
		Wake-up interval 1-ms, 4-ch conversion, V_{CC} =2.3V		233		µA
		Wake-up interval 1000-ms, magnetic 1-ch conversion, V_{CC} =3.6V		1.21		µA
		Wake-up interval 1000-ms, magnetic 1-ch conversion, V_{CC} =2.3V		1.00		µA
		Wake-up interval 1000-ms, 4-ch conversion, V_{CC} =3.6V		1.22		µA
		Wake-up interval 1000-ms, 4-ch conversion, V_{CC} =2.3V		1.02		µA

5.6 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)
over recommended V_{Vcc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SENS_RANGE}	Temperature sensing range		–40		150	℃
T_{SENS}	Temperature output(1)	T_A = 25°C	23	25	27	℃
T_{SENS_RES}	Temperature sensing resolution (in 16-bit format)			58		LSB/℃
T_{SENS_T0}	Reference temperature for T_{ADC_T0}			25		℃
T_{ADC_T0}	Temperature result in decimal value for T_{SENS_T0}			17508		
T_{SENS_ER}	Temperature error(1)	T_A = –40℃ to 125℃		±0.5	±3.5	℃

over operating free-air temperature range (unless otherwise noted)
over recommended V_{Vcc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NRMS_T	RMS (1 Sigma) temperature noise	CONV_AVG = 101b		0.05		℃
		CONV_AVG = 000b		0.3		℃

(1) The temperature data is collected with T_CH_EN =1h and at least one magnetic channel enabled

5.7 Magnetic Characteristics For A1, B1, C1, D1

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$B_{IN\_A1\_X\_Y}$	Linear magnetic range[1]	x_y_RANGE = 0b		±40		mT
		x_y_RANGE = 1b		±80		mT
$B_{IN\_A1\_Z}$		z_RANGE = 0b		±40		mT
		z_RANGE = 1b		±80		mT
$SENS_{A1}$	Sensitivity, X, Y, or Z axis	±40 mT range		844		LSB/mT
		±80 mT range		425		LSB/mT
$SENS_{ER\_PC\_25C\_A1}$	Sensitivity error, X, Y, Z axis	T_A = 25°C		±0.4%	±2.5%	
$SENS_{ER\_PC\_TEMP\_A1}$	Sensitivity temperature drift from 25°C value; X, Y, Z axis[2]			±2.0%	±4.8%	
$SENS_{LER\_XY\_A1}$	Sensitivity linearity error, X, Y-axis	T_A = 25°C		±0.10%		
$SENS_{LER\_Z\_A1}$	Sensitivity linearity error, Z axis	T_A = 25°C		±0.10%		
$SENS_{MS\_XY\_A1}$	Sensitivity mismatch among X-Y axes	T_A = 25°C		±0.40%	±2.1%	
$SENS_{MS\_Z\_A1}$	Sensitivity mismatch among Y-Z, or X-Z axes	T_A = 25°C		±0.40%	±2.0%	
$SENS_{MS\_DR\_XY\_A1}$	Sensitivity mismatch temperature drift from 25°C value; X-Y axes[2]			±0.4%	±2.0%	
$SENS_{MS\_DR\_Z\_A1}$	Sensitivity mismatch temperature drift from 25°C value; Y-Z, or X-Z axes[2]			±0.4%	±5.4%	
$SENS_{LDR\_A1}$	Sensitivity lifetime drift, X, Y, Z axis	T_A = 25°C		±1.0%	±3.74%	
B_{off_A1}	Offset	T_A = 25°C		±100	±700	µT
$B_{off\_TC\_A1}$	Offset temperature drift from –40°C to 25°C[2]			±1.2	±7.85	µT/°C
	Offset temperature drift from 25°C to 125°C[2]			±1.0	±5.85	µT/°C
$B_{off\_DR\_A1}$	Offset lifetime drift	T_A = 25°C		±100		µT
$N_{RMS\_XY\_A1}$	RMS (1 sigma) magnetic noise (X or Y-axis) T_A = 25°C	LP_LN = 0b CONV_AVG = 000b		92		µT
		LP_LN = 1b CONV_AVG = 000b		82.5		µT
		LP_LN = 0b CONV_AVG = 101b		16.75		µT
		LP_LN = 1b CONV_AVG = 101b		15		µT
$N_{RMS\_Z\_A1}$	RMS (1 sigma) magnetic noise (Z axis) T_A = 25°C	LP_LN = 0b CONV_AVG = 000b		53		µT
		LP_LN = 1b CONV_AVG = 000b		48.8		µT
		LP_LN = 0b CONV_AVG = 101b		9.4		µT
		LP_LN = 1b CONV_AVG = 101b		8.6		µT
$A_{ERR\_X\_Z\_101\_A1}$	X-Z or Y-Z angle error in full 360-degree rotation, 40-mT range, TEMPCO = 0h, T_A = 25°C[3]	CONV_AVG = 101b		±0.4	±1.2	Degree
$A_{ERR\_X\_Y\_101\_A1}$	X-Y angle error in full 360-degree rotation, 80-mT range, TEMPCO = 0h, T_A = 25°C[3]	CONV_AVG = 101b		±0.35	±1.1	Degree
$A_{DR\_X\_Z\_101\_A1}$	X-Z or Y-Z angle temperature drift from 25°C value in full 360-degree rotation; 40-mT range, TEMPCO = 0h[3]	CONV_AVG = 101b		±0.9	±2.5	Degree

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{DR\_X\_Y\_101\_A1}$	X-Y angle temperature drift from 25°C value in full 360-degree rotation; 80-mT range, TEMPCO = 0h(3)	CONV_AVG = 101b		±0.4	±1.2	Degree

(1) Use only up to 90% of the linear magnetic range in the application
(2) Temperature drift is specified for full operating temperature range of –40°C to 125°C. Drift at an intermediate temperature can be estimated using the following examples: drift at 85°C = \((85 – 25) / (125 – 25\)) × (drift); similarly, drift at –20°C = \((25 – (–20\)) / (25 – (–40\))) × (drift).
(3) Angle calculation is performed on-axis after calibrating system mechanical errors including magnet tilt and magnet misalignment.

5.8 Magnetic Characteristics For A2, B2, C2, D2

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$B_{IN\_A2\_X\_Y}$	Linear magnetic range(1)	x_y_RANGE = 0b		±133		mT
		x_y_RANGE = 1b		±266		mT
$B_{IN\_A2\_Z}$		z_RANGE = 0b		±133		mT
		z_RANGE = 1b		±266		mT
$SENS_{A2}$	Sensitivity, X, Y, or Z axis	±133 mT range		263		LSB/mT
		±266 mT range		132		LSB/mT
$SENS_{ER\_PC\_25C\_A2}$	Sensitivity error, X, Y, Z axis	T_A = 25°C		±0.8%	±3.3%	
$SENS_{ER\_PC\_TEMP\_A2}$	Sensitivity temperature drift from 25°C value; X, Y, Z axis(2)			±3.0%	±5.5%	
$SENS_{LER\_XY\_A2}$	Sensitivity linearity error, X, Y-axis	T_A = 25°C		±0.10%		
$SENS_{LER\_Z\_A2}$	Sensitivity linearity error, Z axis	T_A = 25°C		±0.10%		
$SENS_{MS\_XY\_A2}$	Sensitivity mismatch among X-Y axes	T_A = 25°C		±0.5%	±2.3%	
$SENS_{MS\_Z\_A2}$	Sensitivity mismatch among Y-Z, or X-Z axes	T_A = 25°C		±1.50%	±4.3%	
$SENS_{MS\_DR\_XY\_A2}$	Sensitivity mismatch temperature drift from 25°C value; X-Y axes(2)			±0.5%	±2.0%	
$SENS_{MS\_DR\_Z\_A2}$	Sensitivity mismatch temperature drift from 25°C value; Y-Z, or X-Z axes(2)			±4.5%	±8.0%	
$SENS_{LDR\_A2}$	Sensitivity lifetime drift, X, Y, Z axis	T_A = 25°C		±1.5%	±4.9%	
B_{off_A2}	Offset	T_A = 25°C		±100	±700	µT
$B_{off\_TC\_A2}$	Offset temperature drift from -40°C to 25°C value(2)			±1.2	±7.0	µT/°C
	Offset temperature drift from 25°C to 125°C value(2)			±1.2	±6.8	µT/°C
$B_{off\_DR\_A2}$	Offset lifetime drift	T_A = 25°C		±100		µT
$N_{RMS\_XY\_A2}$	RMS (1 sigma) magnetic noise (X or Y-axis)	LP_LN =0 b CONV_AVG = 000b		113		µT
		LP_LN = 1b CONV_AVG = 000b		105		µT
		LP_LN = 0b CONV_AVG = 101b		20		µT
		LP_LN = 1b CONV_AVG = 101b		18.6		µT

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$N_{RMS\_Z\_A2}$	RMS (1 sigma) magnetic noise (Z axis)	LP_LN = 0b CONV_AVG = 000b		81.7		µT
		LP_LN = 1b CONV_AVG = 000b		78.4		µT
		LP_LN = 0b CONV_AVG = 101b		13.9		µT
		LP_LN = 1b CONV_AVG = 101b		14		µT
$A_{ERR\_X\_Z\_101\_A2}$	X-Z or Y-Z angle error in full 360-degree rotation; TEMPCO = 0h, T_A = 25°C(3)	CONV_AVG = 101b		±0.25	±1.0	Degree
$A_{ERR\_X\_Y\_101\_A2}$	X-Y angle error in full 360-degree rotation; 133-mT range, TEMPCO = 0h,T_A = 25°C(3)	CONV_AVG = 101b		±0.4	±1.6	Degree
$A_{DR\_X\_Z\_101\_A2}$	X-Z or Y-Z angle temperature drift from 25°C value in full 360-degree rotation; 133-mT range, TEMPCO = 0h(3)	CONV_AVG = 101b		±1.6	±2.9	Degree
$A_{DR\_X\_Y\_101\_A2}$	X-Y angle temperature drift from 25°C value in full 360-degree rotation; 133-mT range, TEMPCO = 0h(3)	CONV_AVG = 101b		±0.4	±1.4	Degree

(1) Use only up to 90% of the linear magnetic range in the application
(2) Temperature drift is specified for full operating temperature range of –40°C to 125°C. Drift at an intermediate temperature can be estimated using the following examples: drift at 85°C = \((85 – 25) / (125 – 25\)) × (drift); similarly, drift at –20°C = \((25 – (–20\)) / (25 – (–40\))) × (drift).
(3) Angle calculation is performed on-axis after calibrating system mechanical errors including magnet tilt and magnet misalignment.

5.9 Magnetic Temp Compensation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TC	Temperature compensation (X, Y, Z-axes)	TEMPCO = 00b		0		%/°C
		TEMPCO = 01b		0.12		%/°C
		TEMPCO = 10b		0.03		%/°C
		TEMPCO = 11b		0.2		%/°C

5.10 I²C Interface Timing

minimum and maximum specifications are over –40°C to 125°C and V_{CC} = 2.3 V to 3.6 V (unless otherwise noted)(1)

		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	1	400	1	1000	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	1.3		0.5		µs
$t_{(SUSTA)}$	Repeated START condition setup time	0.6		0.26		µs
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	0		0		µs
$t_{(SUSTO)}$	STOP condition setup time	0.6		0.26		µs
$t_{(HDDAT)}$	Data hold time(2)	0	900	0	150	ns
$t_{(SUDAT)}$	Data setup time	100		50		ns
$t_{(LOW)}$	SCL clock low period	1.3		0.5		µs
$t_{(HIGH)}$	SCL clock high period	0.6		0.26		µs
t_R	SDA, SCL fall time	20	300		120	ns
t_F	SDA, SCL fall time	20 x (V_{CC} / 5.5 V)	300	20 x (V_{CC} / 5.5 V)	120	ns
t_{LPF}	Glitch suppression filter	50		50		ns

(1) The host and device have the same V_{CC} value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9 µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.

5.11 Power up Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{start\_power\_up}$	Time to go to standby mode after V_{CC} supply voltage crossing V_{CC_MIN}			270		µs
t_{start_sleep}	Time to go to standby mode from sleep mode(1)			50		µs
$t_{start\_measure}$	Time to go into continuous measure mode from standby mode			70		µs
$t_{measure}$	Conversion time	CONV_AVG = 000b, OPERATING_MODE =10b, only one channel enabled		50		µs
		CONV_AVG = 101b, OPERATING_MODE =10b, only one channel enabled		825		µs
t_{go_sleep}	Time to go into sleep mode after SCL goes high			20		µs

(1) The device will recognize the I2C communication from a primary only during standby or continuous measure modes. While the device is in sleep mode, a valid secondary address will wake up the device but no acknowledge will be sent to the primary. Start up time need to be considered before addressing the device after wake up.

5.12 Timing Diagram

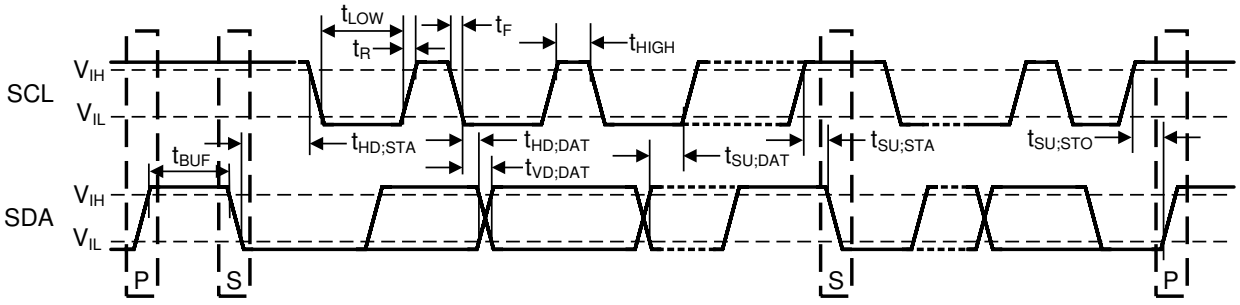


Figure 5-1. I2C Timing Diagram

5.13 Typical Characteristics

at T_A = 25°C typical (unless otherwise noted)

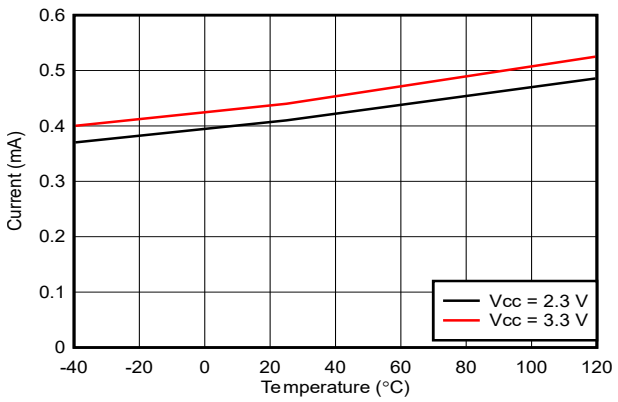


Figure 5-2. Standby Mode ICC vs Temperature

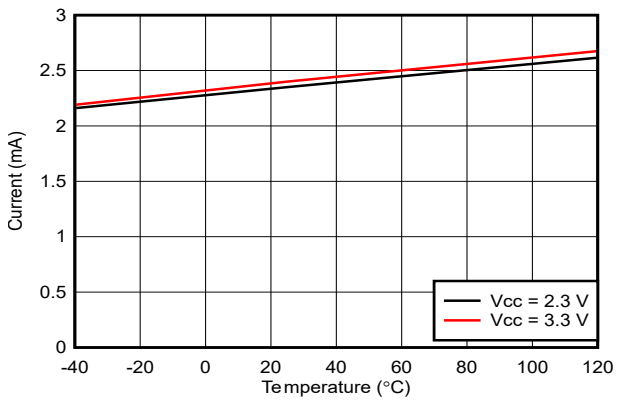


Figure 5-3. Active Mode ICC vs Temperature

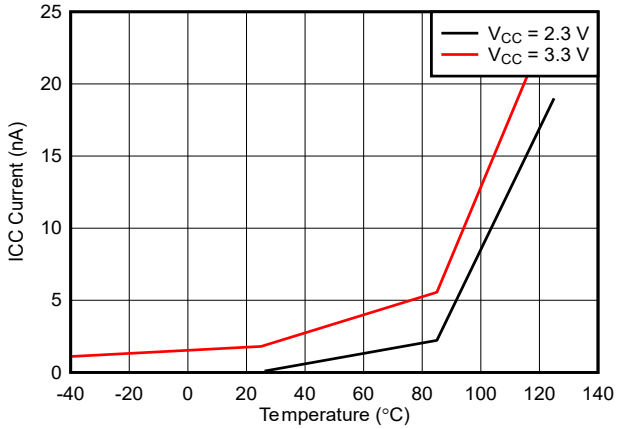


Figure 5-4. Sleep Mode ICC vs Temperature

6 Detailed Description

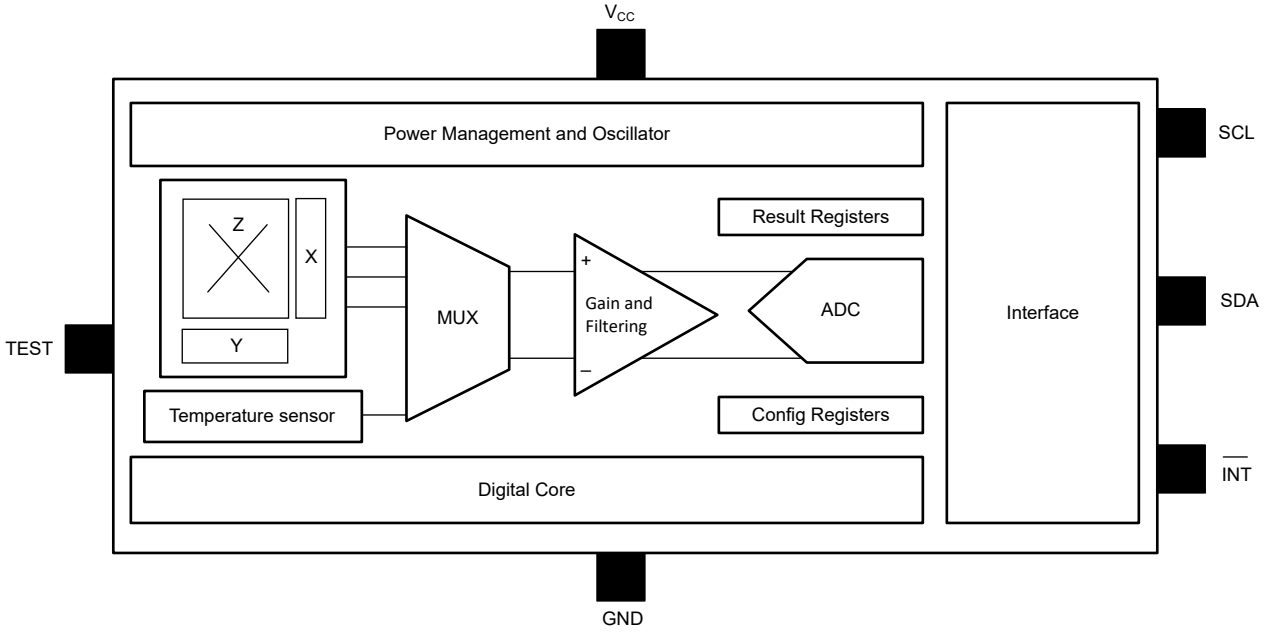
6.1 Overview

The TMAG5173-Q1 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z magnetic data and temperature data) are accessible through the I^2C interface.

The IC consists of the following functional and building blocks:

- The Power Management & Oscillator block contain a low-power oscillator, biasing circuitry, undervoltage detection circuitry, and a fast oscillator.
- The sensing and temperature measurement block contains the Hall biasing, Hall sensors with multiplexers, noise filters, integrator circuit, temperature sensor, and the ADC. The Hall-effect sensor data and temperature data are multiplexed through the same ADC.
- The Interface block contains the I^2C control circuitry, ESD protection circuits, and all the I/O circuits. The TMAG5173-Q1 supports multiple I^2C read frames along with integrated cyclic redundancy check (CRC).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Magnetic Flux Direction

As shown in Figure 6-1, the TMAG5173-Q1 generates positive ADC codes in response to a magnetic north pole in the proximity. Similarly, the TMAG5173-Q1 generates negative ADC codes if magnetic south poles approach from the same directions.

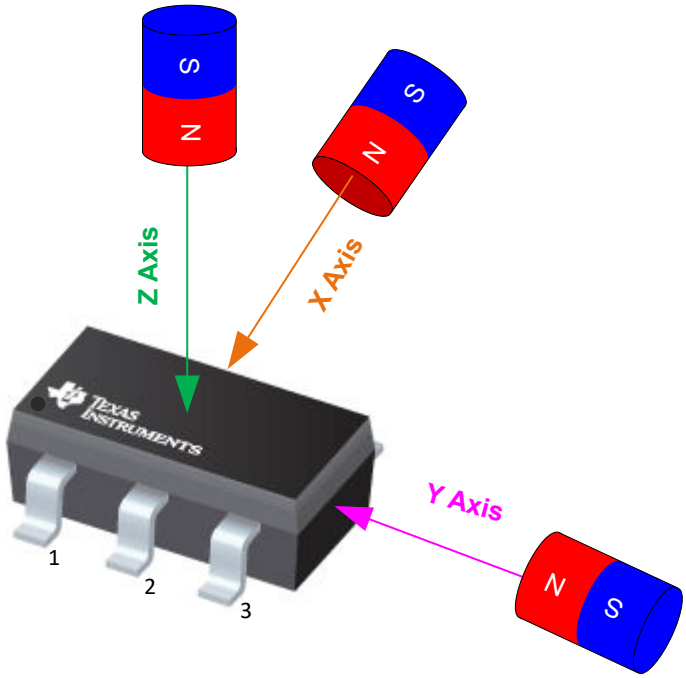


Figure 6-1. Direction of Sensitivity

6.3.2 Sensor Location

Figure 6-2 shows the location of X, Y, Z hall elements inside the TMAG5173-Q1.

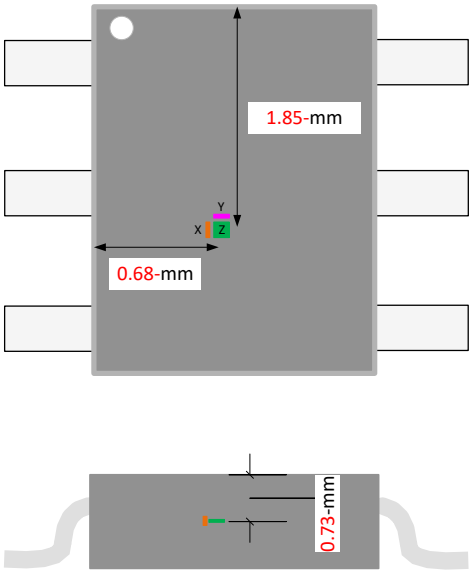


Figure 6-2. Location of X, Y, Z Hall Elements

6.3.3 Interrupt Function

The TMAG5173-Q1 supports flexible and configurable interrupt functions through either the $\overline{INT}$ or the SCL pin. Table 6-1 shows different conversion completion events where result registers and SET_COUNT bits update, and where the bits do not.

Table 6-1. Result Register & SET_COUNT Update After Conversion Completion

INT_MODE	MODE DESCRIPTION	I²C BUS BUSY, NOT TALKING TO DEVICE		I²C BUS BUSY & TALKING TO DEVICE		I²C BUS NOT BUSY	
		RESULT UPDATE?	SET_COUNT UPDATE?	RESULT UPDATE?	SET_COUNT UPDATE?	RESULT UPDATE?	SET_COUNT UPDATE?
000b	No interrupt	Yes	Yes	No	No	Yes	Yes
001b	Interrupt through $\overline{INT}$	Yes	Yes	No	No	Yes	Yes
010b	Interrupt through $\overline{INT}$ except when I²C busy	Yes	Yes	No	No	Yes	Yes
011b	Interrupt through SCL	Yes	Yes	No	No	Yes	Yes
100b	Interrupt through SCL except when I²C busy	No	No	No	No	Yes	Yes

Note

TI does not recommend sharing the same I²C bus with multiple secondary devices when using the SCL pin for interrupt function. The SCL interrupt can corrupt transactions with other secondary devices if present in the same I²C bus.

6.3.3.1 Interrupt Through SCL

Figure 6-3 shows an example for interrupt function through the SCL pin with the device programmed to generate interrupt at magnetic threshold cross event. When the magnetic threshold cross is detected, the device asserts a fixed width interrupt signal through the SCL pin.

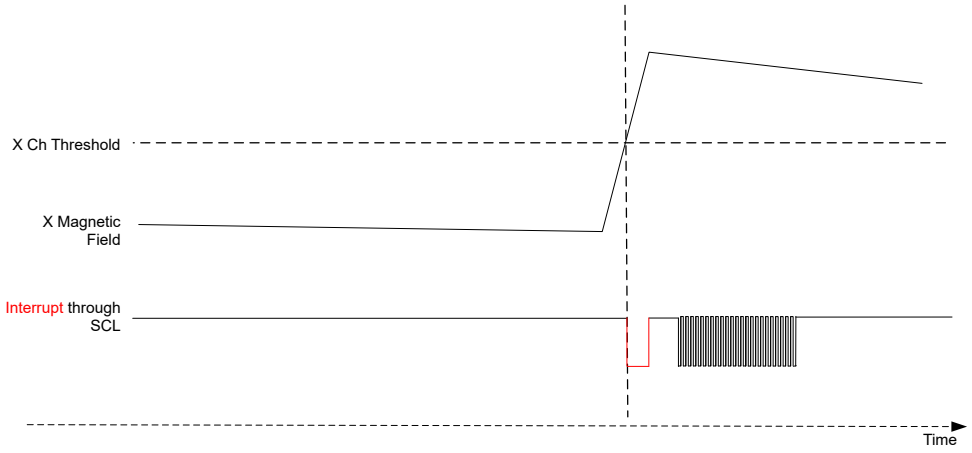


Figure 6-3. Interrupt Through SCL

6.3.3.2 Fixed Width Interrupt Through $\overline{\text{INT}}$

Figure 6-4 shows an example for fixed-width interrupt function through the $\overline{\text{INT}}$ pin. The device is programmed to generate interrupt at magnetic threshold cross event. The INT_STATE register bit is set 1b. When the magnetic threshold cross is detected, the device asserts a fixed width interrupt signal through the $\overline{\text{INT}}$ pin.

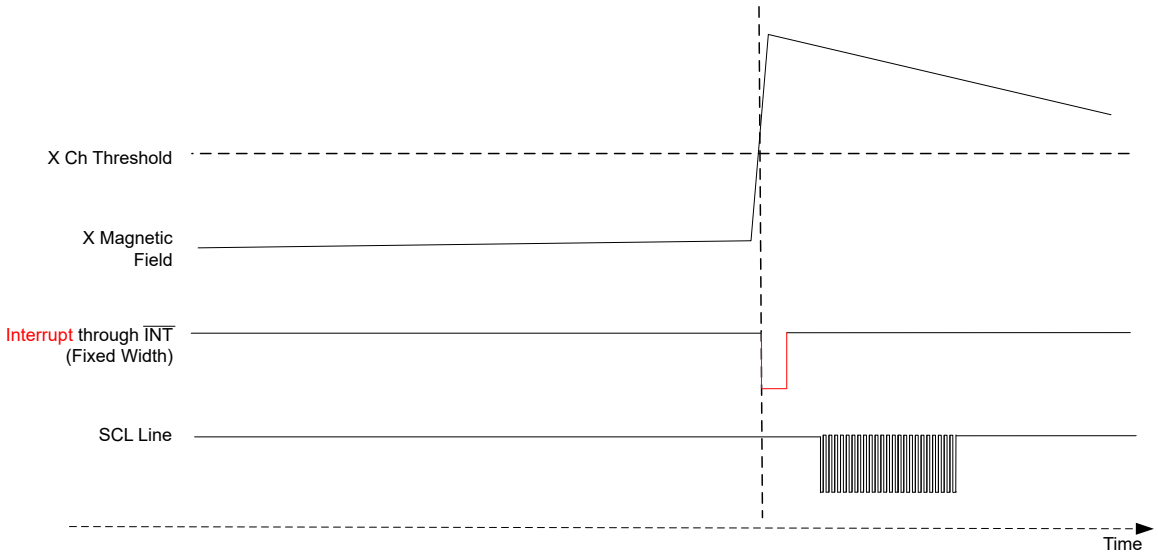


Figure 6-4. Fixed Width Interrupt Through $\overline{\text{INT}}$

6.3.3.3 Latched Interrupt Through $\overline{\text{INT}}$

Figure 6-5 shows an example for latched interrupt function through the $\overline{\text{INT}}$ pin. The device is programmed to generate interrupt at magnetic threshold cross event. The INT_STATE register bit is set 0b. When the magnetic threshold cross is detected, the device asserts a latched interrupt signal through the $\overline{\text{INT}}$ pin. The latched interrupt is cleared only after the device receives a valid address through the SCL line.

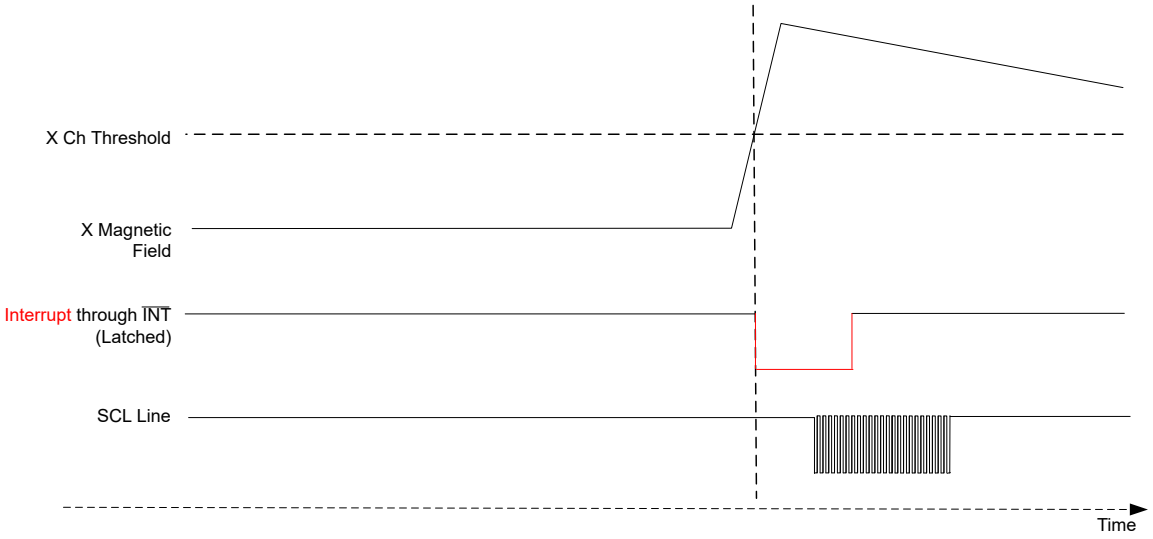


Figure 6-5. Latched Interrupt Through $\overline{INT}$

6.3.4 Device I²C Address

Table 6-2 shows the default factory programmed I²C addresses of the TMAG5173-Q1. The device needs to be addressed with the factory default I²C address after power up. If required, a primary can assign a new I²C address through the I2C_ADDRESS register bits after power up.

Table 6-2. I²C Default Address

DEVICE VERSION	MAGNETIC RANGE	I²C ADDRESS (7 MSB BITS)	I²C WRITE ADDRESS (8-BIT)	I²C READ ADDRESS (8-BIT)
TMAG5173A1	±40 mT, ±80 mT	35h	6Ah	6Bh
TMAG5173B1		22h	44h	45h
TMAG5173C1		78h	F0h	F1h
TMAG5173D1		44h	88h	89h
TMAG5173A2	±133 mT, ±266 mT	35h	6Ah	6Bh
TMAG5173B2		22h	44h	45h
TMAG5173C2		78h	F0h	F1h
TMAG5173D2		44h	88h	89h

6.3.5 Magnetic Range Selection

Table 6-3 shows the magnetic range selection for the TMAG5173-Q1 device. The X, Y, and Z axes range can be selected with the X_Y_RANGE and Z_RANGE register bits.

Table 6-3. Magnetic Range Selection

	RANGE REGISTER SETTING	TMAG5173A1	TMAG5173A2	COMMENT
X, Y Axis Field	X_Y_RANGE = 0b	±40 mT	±133 mT	
	X_Y_RANGE = 1b	±80 mT	±266 mT	Better SNR performance
Z Axis Field	Z_RANGE = 0b	±40 mT	±133 mT	
	Z_RANGE = 1b	±80 mT	±266 mT	Better SNR performance

6.3.6 Update Rate Settings

The TMAG5173-Q1 offers multiple update rates to offer design flexibility to system designers. The different update rates can be selected with the CONV_AVG register bits. Table 6-4 shows different update rate settings for the TMAG5173-Q1.

Table 6-4. Update Rate Settings

OPERATING MODE	REGISTER SETTING	UPDATE RATE			COMMENT
		SINGLE AXIS	TWO AXES	THREE AXES	
X, Y, Z Axis	CONV_AVG = 000b	20.0 kSPS	13.3 kSPS	10.0 kSPS	Fastest update rate
X, Y, Z Axis	CONV_AVG = 001b	13.3 kSPS	8.0 kSPS	5.7 kSPS	
X, Y, Z Axis	CONV_AVG = 010b	8.0 kSPS	4.4 kSPS	3.1 kSPS	
X, Y, Z Axis	CONV_AVG = 011b	4.4 kSPS	2.4 kSPS	1.6 kSPS	
X, Y, Z Axis	CONV_AVG = 100b	2.4 kSPS	1.2 kSPS	0.8 kSPS	
X, Y, Z Axis	CONV_AVG = 101b	1.2 kSPS	0.6 kSPS	0.4 kSPS	Best SNR case

6.4 Device Functional Modes

The TMAG5173-Q1 supports multiple functional modes for wide array of applications as explained in Figure 6-6. A specific functional mode is selected by setting the corresponding value in the OPERATING_MODE register bits. The device starts powering up after V_{CC} supply crosses the minimum threshold as specified in the *Recommended Operating Conditions* (ROC) table.

6.4.1 Standby (Trigger) Mode

The TMAG5173-Q1 goes to standby mode after power up. During this mode the digital circuitry and oscillators are on and the device is ready to accept commands from the microcontroller. Based off the commands the device can start a new conversion, go to power saving mode, or the start data transfer through I^2C interface. A new conversion can be triggered through I^2C command or through $\overline{INT}$ pin. In this mode the device retains the immediate past conversion result data in the corresponding result registers. The time for the device to go from power up to standby mode is listed as $T_{start\_power\_up}$ in the *Power up Timing* table. The $\overline{INT}$ pin can be used to a trigger a new conversion or generate interrupt for the microcontroller. TI does not recommend to use both functions through $\overline{INT}$ pin simultaneously.

6.4.2 Sleep Mode

The TMAG5173-Q1 supports an ultra-low power sleep mode where the device can retain the critical user configuration settings. In this mode the device does not retain the conversion result data. A microcontroller can wake up the device from sleep mode to standby mode through I^2C communications or the $\overline{INT}$ pin. The time for the device to go from sleep mode to standby mode is listed as T_{start_sleep} in the *Power up Timing* table.

6.4.3 Wake-up and Sleep (W&S) Mode

In this mode the TMAG5173-Q1 can be configured to go to sleep and wake up at a certain interval, and measure sensor data based off the SLEEPTIME register bits setting. The device can be set to generate an interrupt through the INT_CONFIG_1 register. When the conversion is complete and the interrupt condition is met, the TMAG5173-Q1 exits the W&S mode and enters standby mode. The last measured data is stored in the corresponding result registers before the device enters standby mode. If the interrupt condition is not met, the device continues in W&S mode to wake up and measure data at the specified interval. A primary can wake up the TMAG5173-Q1 at any time during W&S mode through I^2C bus or $\overline{INT}$ pin. The result interrupt function is not available during W&S mode. The time for the device to go from W&S mode to standby mode is listed as T_{start_sleep} in the *Power up Timing* table.

6.4.4 Continuous Measure Mode

In this mode the TMAG5173-Q1 continuously measures the sensor data per SENSOR_CONFIG & DEVICE_CONFIG register settings. In this mode the result registers can be accessed through the I²C lines. The time for the device to go from standby mode to continuous measure mode is listed as $T_{start\_measure}$ in the *Power up Timing* table.

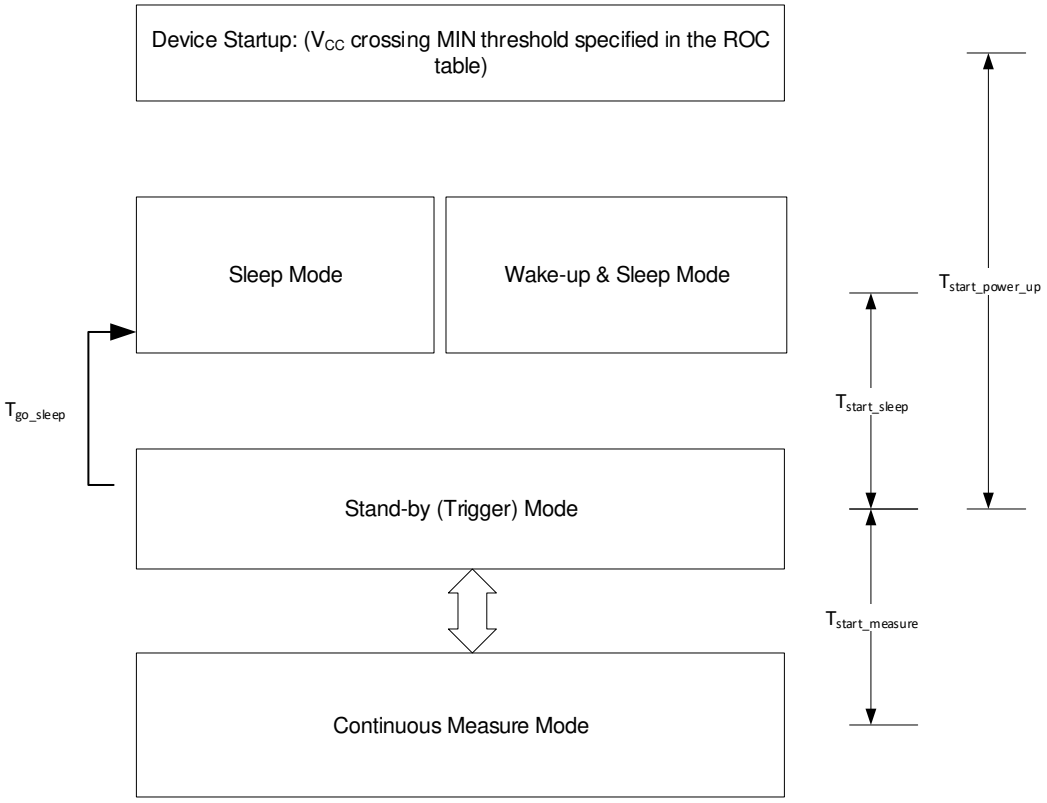


Figure 6-6. TMAG5173-Q1 Operating Modes

Figure 6-6 shows TMAG5173-Q1 operating modes and time references to transition from one mode to another.

Table 6-5. Operating Modes

OPERATING MODE	DEVICE FUNCTION	ACCESS TO USER REGISTERS	RETAIN USER CONFIGURATION
Continuous measure mode	Continuously measures the X, Y, Z axes or temperature data	Yes	Yes
Standby mode	Device is ready to accept I²C commands and start active conversion	Yes	Yes
Wake-up and Sleep Mode	Wakes up at a certain interval to measure the X, Y, Z axes or temperature data	No	Yes
Sleep mode	Device retains key configuration settings, but does not retain the measurement data	No	Yes

6.5 Programming

6.5.1 I²C Interface

The TMAG5173-Q1 offers I²C interface, a two-wire interface to connect low-speed devices like microcontrollers, A/D and D/A converters, I/O interfaces and other similar peripherals in embedded systems.

6.5.1.1 SCL

The SCL is the clock line used to synchronize all data transfers over the I²C bus.

6.5.1.2 SDA

SDA is the bidirectional data line for the I²C interface.

6.5.1.3 I²C Read/Write

The TMAG5173-Q1 supports multiple I²C read and write frames targeting different applications. I2C_RD and CRC_EN bits offers multiple read frames to optimize the read time, data resolution, and data integrity for a select application.

6.5.1.3.1 Standard I²C Write

Figure 6-7 shows an example of standard I²C two byte write command supported by TMAG5173-Q1. The starting byte contains 7-bit secondary device address and a 0 at the R/$\overline{W}$ command bit. The MSB of the second byte contains the conversion trigger bit. Write 1 at this trigger bit to start a new conversion after the register address decoding is completed. The seven LSB bits of the second byte contains the starting register address for the write command. After the two command bytes, the primary device starts to send the data to be written at the corresponding register address. Each successive write byte sends the data for the successive register address in the secondary device.

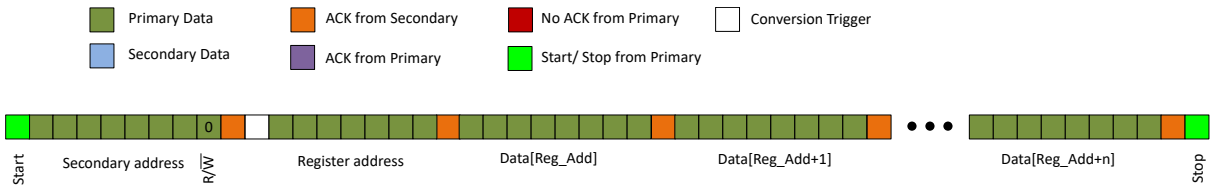


Figure 6-7. Standard I²C Write

6.5.1.3.2 General Call Write

Figure 6-8 shows an example of the general call I²C write command supported by the TMAG5173-Q1. This command is useful to configure multiple I²C devices in a I²C bus simultaneously. The starting byte contains 8-bit 0s. The MSB of the second byte contains the conversion trigger bit. Write a 1 at this trigger bit to start a new conversion after the register address decoding is completed. The seven LSBs of the second byte contains the starting register address for the write command. After the two command bytes, the primary device starts to send the data to be written at the corresponding register address of all the secondary devices in the I²C bus. Each successive write byte sends the data for the successive register address in the secondary devices.

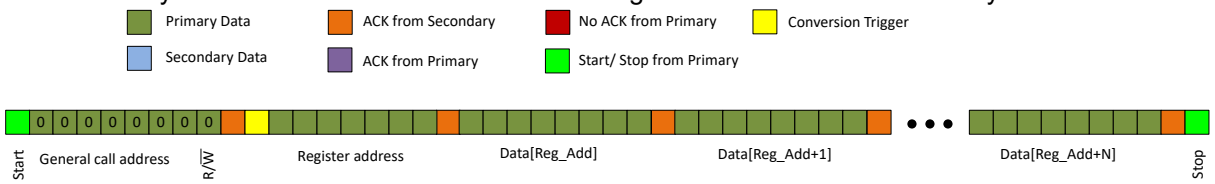


Figure 6-8. General Call I²C Write

6.5.1.3.3 Standard 3-Byte I²C Read

Figure 6-9 and Figure 6-10 show examples of standard I²C three byte read command supported by the TMAG5173-Q1. The starting byte contains 7-bit secondary device address and the R/$\overline{W}$ command bit 0. The MSB of the second byte contains the conversion trigger command bit. Write 1 at this trigger bit to start a new conversion after the register address decoding is completed. The seven LSB bits of the second byte contains the starting register address for the write command. After receiving ACK signal from secondary, the primary sends the secondary address again with R/$\overline{W}$ command bit as 1. The secondary starts to send the corresponding register data. The secondary sends a successive register data with each successive ACK from the primary. If CRC is enabled, the secondary sends the fifth CRC byte based off the CRC calculation of immediate past four register bytes.

Note

In the standard 3-byte read command the TMAG5173-Q1 does not support CRC if the data length is more than four bytes. Initiate successive read commands for larger data stream requiring CRC.

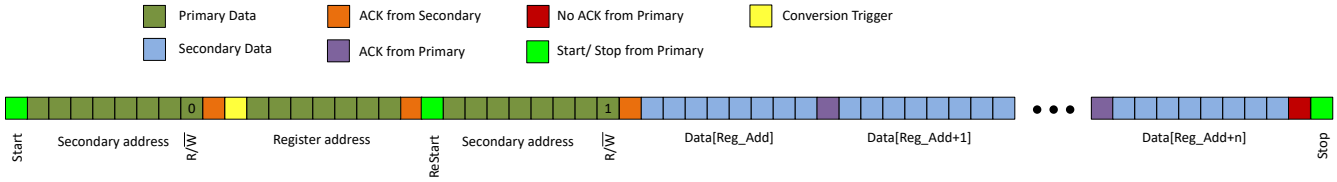


Figure 6-9. Standard 3-Byte I²C Read With CRC Disabled, CRC_EN = 0b

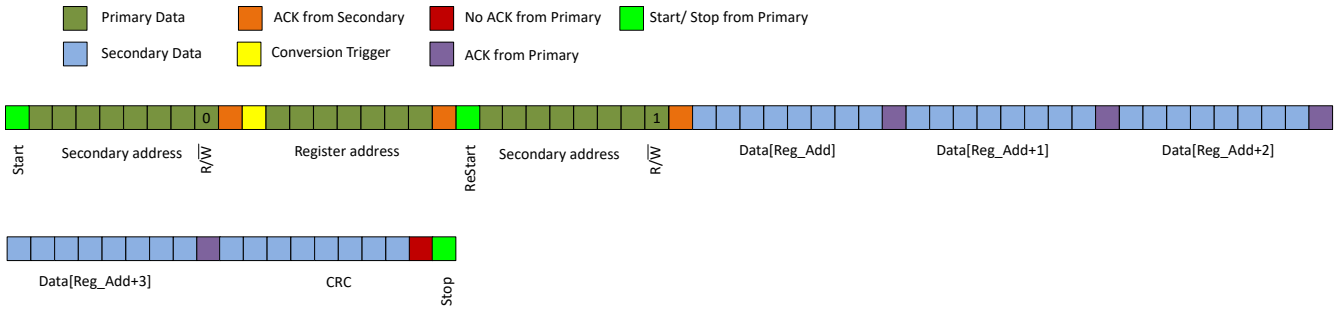


Figure 6-10. Standard 3-Byte I²C Read With CRC Enabled, CRC_EN = 1b

6.5.1.3.4 1-Byte I2C Read Command for 16-Bit Data

Figure 6-11 and Figure 6-12 show examples of 1-byte I²C read command supported by the TMAG5173-Q1. Select I2C_RD =01b to enable this mode. The command byte contains 7-bit secondary device address and a 1 at the R/$\overline{W}$ bit. In this mode, per MAG_CH_EN and T_CH_EN bits setting, the device sends 16-bit data of the enabled channels and the CONV_STATUS register data byte. If CRC is enabled, the device sends an additional CRC byte based off the CRC calculation of the command byte and the data sent in the current packet. When multiple channels are enabled, the sent data follows the T, X, Y, and Z sequence in the successive data bytes.

Figure 6-11. 1-Byte I²C Read Command for 16-Bit Data With CRC Disabled, CRC_EN = 0b

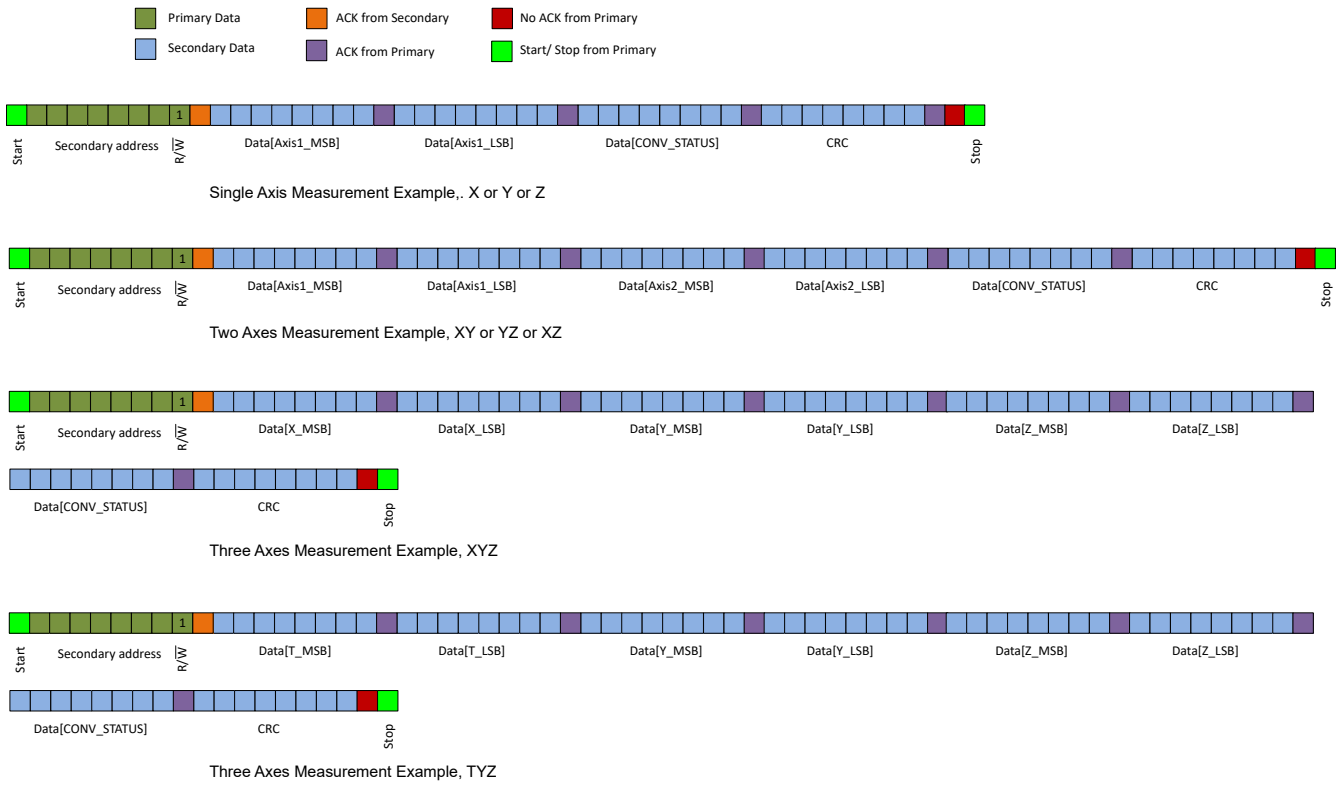


Figure 6-12. 1-Byte I²C Read Command for 16-Bit Data With CRC Enabled, CRC_EN = 1b

Note

In the 1-byte read command for 16-bit data only up to three channels data can be sent when CRC is enabled. This restriction does not apply if CRC is disabled.

6.5.1.3.5 1-Byte I²C Read Command for 8-Bit Data

Figure 6-13 and Figure 6-14 show examples of 1-byte I²C read command supported by the TMAG5173-Q1. Select I2C_RD =10b to enable this mode. The command byte contains 7-bit secondary device address and a 1 at the R/$\overline{W}$ bit. In this mode, per MAG_CH_EN and T_CH_EN bits setting, the device sends 8-bit data of the enabled channels and the CONV_STATUS register data byte. If CRC is enabled, the device sends an additional CRC byte based off the CRC calculation of the command byte and the data sent in the current packet. When multiple channels are enabled, the sent data follows the T, X, Y, and Z sequence in the successive data bytes.

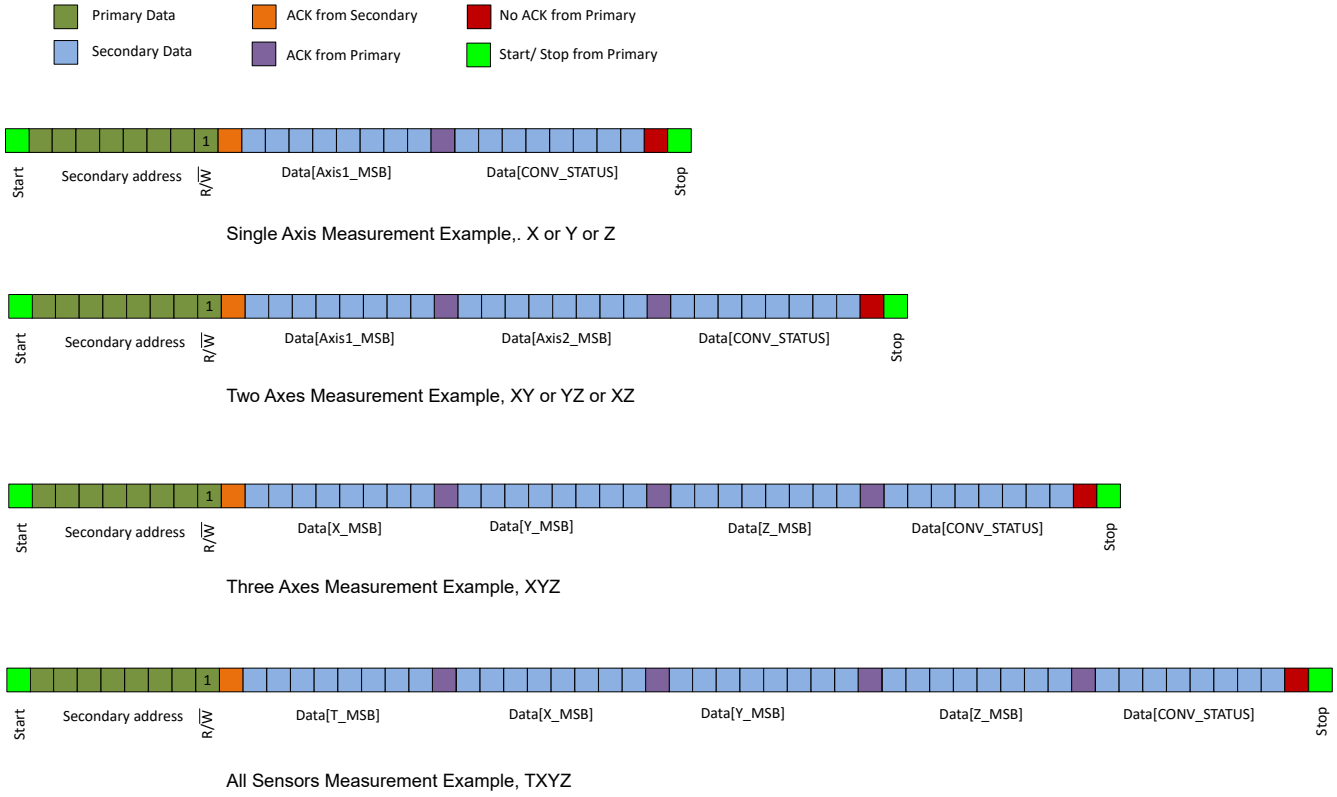


Figure 6-13. 1-Byte I²C Read Command for 8-Bit Data With CRC Disabled, CRC_EN = 0b

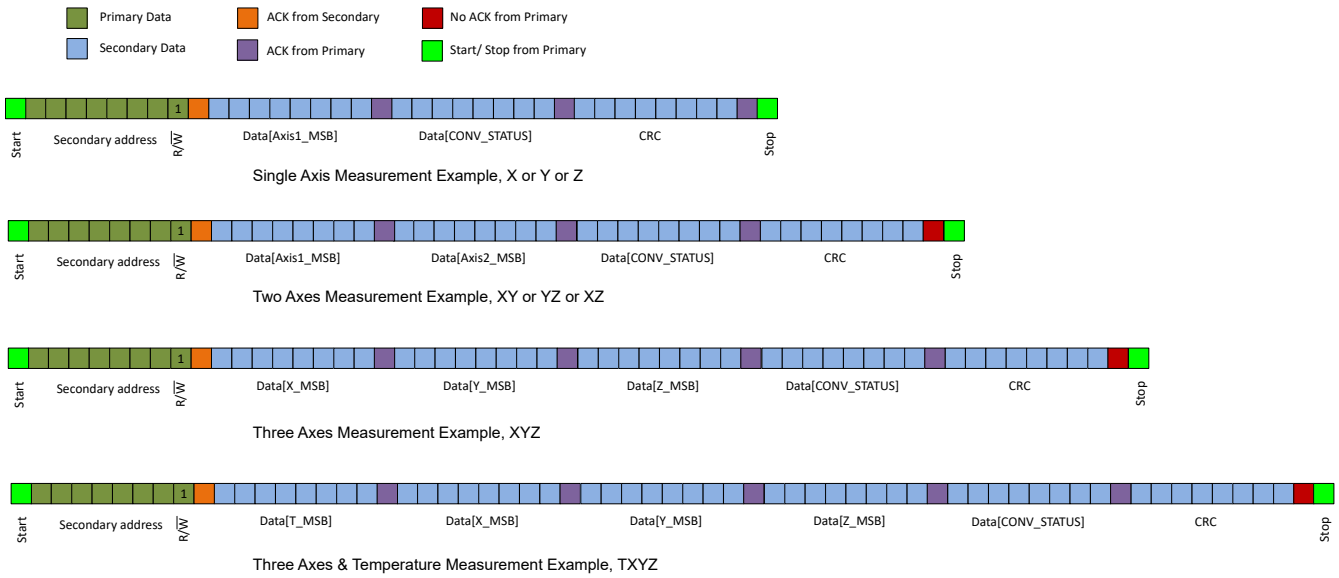


Figure 6-14. 1-Byte I²C Read Command for 8-Bit Data With CRC Enabled, CRC_EN = 1b

Note

In the 1-byte read command for 8-bit data any combinations of channels can be sent without restrictions.

6.5.1.3.6 I²C Read CRC

The TMAG5173-Q1 supports optional CRC during I²C read. The CRC can be enabled through the CRC_EN register bit. The CRC is performed on a data string that is determined by the I²C read type. The CRC information is sent as a single byte after the data bytes. The code is generated by the polynomial $x^8 + x^2 + x + 1$. Initial CRC bits are FFh.

The following equations can be employed to calculate CRC:

d = Data Input, c = Initial CRC (FFh) (1)

newcrc[0] = d[7] ^ d[6] ^ d[0] ^ c[0] ^ c[6] ^ c[7] (2)

newcrc[1] = d[6] ^ d[1] ^ d[0] ^ c[0] ^ c[1] ^ c[6] (3)

newcrc[2] = d[6] ^ d[2] ^ d[1] ^ d[0] ^ c[0] ^ c[1] ^ c[2] ^ c[6] (4)

newcrc[3] = d[7] ^ d[3] ^ d[2] ^ d[1] ^ c[1] ^ c[2] ^ c[3] ^ c[7] (5)

newcrc[4] = d[4] ^ d[3] ^ d[2] ^ c[2] ^ c[3] ^ c[4] (6)

newcrc[5] = d[5] ^ d[4] ^ d[3] ^ c[3] ^ c[4] ^ c[5] (7)

newcrc[6] = d[6] ^ d[5] ^ d[4] ^ c[4] ^ c[5] ^ c[6] (8)

newcrc[7] = d[7] ^ d[6] ^ d[5] ^ c[5] ^ c[6] ^ c[7] (9)

The following examples show calculated CRC byte based off various input data:

I2C Data 00h : CRC = F3h

I2C Data FFh : CRC = 00h

I2C Data 80h : CRC = 7Ah

I2C Data 4Ch : CRC = 10h

I2C Data E0h : CRC = 5Dh

I2C Data 00000000h : CRC = D1h

I2C Data FFFFFFFFh : CRC = 0Fh

6.5.2 Data Definition

6.5.2.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in x_MSB_RESULT and x_LSB_RESULT registers. Figure 6-15 shows that each sensor output stored in a 16-bit 2's complement format in two 8-bit registers. The data can be retrieved as 16-bit format combining both MSB and LSB registers, or as 8-bit format through the MSB register. When Conv_AVG = 0h, the ADC output loads the 12 MSB bits of the 16-bit result along with four LSBs as zeros. When Conv_AVG ≠ 0h, all 16 bits are used to store the results.

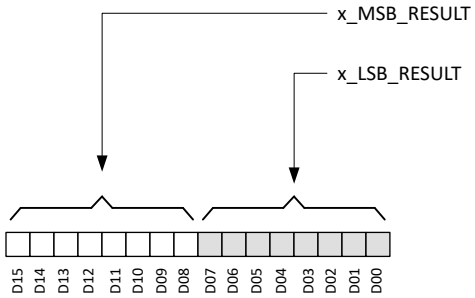


Figure 6-15. Magnetic Sensor Data Definition

The LSB size for each magnetic range is:

- 40mT: 844 LSB/mT
- 80mT: 425 LSB/mT
- 133mT: 263 LSB/mT
- 266mT: 132 LSB/mT

Table 6-6. 16-bit X, Y, Z Magnetic Sensor Data Format. Three decimal places are shown.

Magnetic Field (mT)				x_CH_RESULT	
Range = 40 mT	Range = 80 mT	Range = 133 mT	Range = 266 mT	BINARY	HEX
-38.824	-77.101	-124.593	-248.242	1000 0000 0000 0000	8000h
-19.412	-38.551	-62.297	-124.121	1100 0000 0000 0000	C000h
-0.001	-0.002	-0.004	-0.008	1111 1111 1111 1111	FFFFh
0	0	0	0	0000 0000 0000 0000	0000h
0.001	0.002	0.004	0.008	0000 0000 0000 0001	0001h
19.412	38.551	62.297	124.121	0100 0000 0000 0000	4000h
38.823	77.099	124.589	248.235	0111 1111 1111 1111	7FFFh

6.5.2.2 Temperature Sensor Data

The TMAG5173-Q1 measures temperature from –40°C to 170°C. The T_MSB_RESULT and T_LSB_RESULT registers store the temperature sensor data. Figure 6-16 shows the sensor output stored in a 16-bit 2's complement format in two 8-bit registers. The data can be retrieved as 16-bit format combining both MSB and LSB registers, or as 8-bit format through the MSB register.

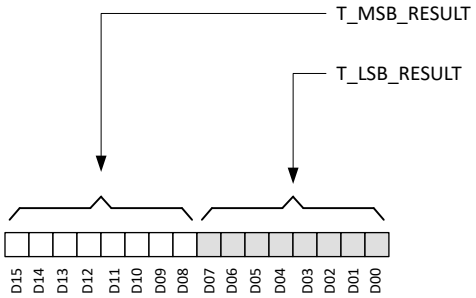


Figure 6-16. Temperature Sensor Data Definition

Use Equation 10 to calculate the measured temperature in degree Celsius for 16-bit data, and use Equation 11 to calculate the measured temperature for 8-bit data.

$$T = T_{SENS\_T0} + \frac{T_{ADC\_T} - T_{ADC\_T0}}{T_{ADC\_RES}} \quad (10)$$

$$T = T_{SENS\_T0} + \frac{256 \times \left(T_{ADC\_T} - \frac{T_{ADC\_T0}}{256}\right)}{T_{ADC\_RES}} \quad (11)$$

where

- T is the measured temperature in degree Celsius
- T_{SENS_T0} as listed in the *Electrical Characteristics* table
- T_{ADC_RES} is the change in ADC code per degree Celsius
- T_{ADC_T0} as listed in the *Electrical Characteristics* table
- T_{ADC_T} is the measured ADC code for temperature T

Table 6-7. 16-Bit Temperature Data Format (Two Decimal Places Shown)

TEMPERATURE (°C)	TEMP_RESULT	
	BINARY	HEX
–40	0011 0101 1010 1010	35AAh
–25	0011 1001 0001 0000	3910h
0	0011 1110 1011 1010	3EBAh
25	0100 0100 0110 0100	4464h
25.02	0100 0100 0110 0101	4465h
85	0101 0001 1111 1100	51FCh
125	0101 1011 0000 1100	5B0Ch

6.5.2.3 Angle and Magnitude Data Definition

The TMAG5173-Q1 calculates the angle from a pair of magnetic axes based off the ANGLE_EN register bits setting. Figure 6-17 shows the angle information stored in the ANGLE_RESULT_MSB and ANGLE_RESULT_LSB registers. Bits D04 to D12 store angle integer value from 0 to 360 degree. Bits D00 to D03 store fractional angle value. The three MSBs are always populated as b000.

For example: a 354.50 degree angle is populated as 0001 0110 0010 1000b and a 17.25 degree angle is populated as 000 0001 0001 0100b.

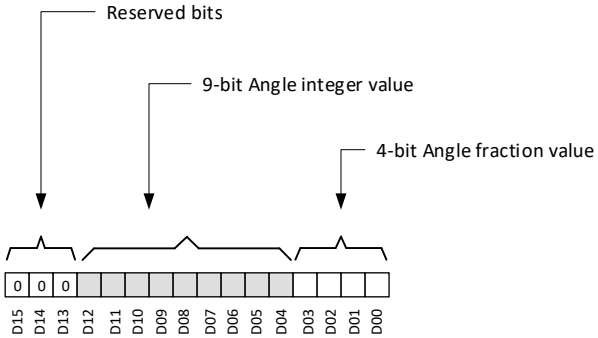


Figure 6-17. Angle Data Definition

Table 6-8. 13-Bit Angle Data Format

ANGLE (°)	ANGLE_RESULT[12:0]	
	BINARY	HEX
0	0 0000 0000 0000	000h
0.0625	0 0000 0000 0001	001h
90	0 0101 1010 0000	5A0h
180	0 1011 0100 0000	B40h
270	1 0000 1110 0000	10E0h
360	1 0110 1000 0000	1680h

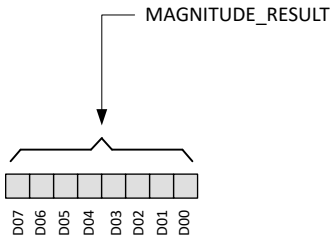
During the angle calculation, use Equation 12 to calculate the resultant vector magnitude.

$$M = \sqrt{MADC_{Ch1}{}^2 + MADC_{Ch2}{}^2} \quad (12)$$

where

- $MADC_{Ch1}$, $MADC_{Ch2}$ are the ADC codes of the two magnetic channels selected for the angle calculation.

Figure 6-18 shows the magnitude value stored in the MAGNITUDE_RESULT register. For on-axis angular measurement the magnitude value should remain constant across the full 360° measurement.



During the angle calculation, the MAGNITUDE_RESULT register stores the resultant vector magnitude. MAGNITUDE_RESULT is an unsigned 8-bit value with a LSB size that depends on the range of the device.

- 40 mT: 3.296875LSB/mT
- 80 mT: 1.66015625LSB/mT
- 133 mT: 1.02735375LSB/mT
- 266 mT: 0.515625LSB/mT

Table 6-9. 8-Bit Magnitude Data Format (Only Three Decimal Places Shown)

Magnitude (mT)				MAGNITUDE_RESULT[7:0]	
Range = 40 mT	Range = 80 mT	Range = 133 mT	Range = 266 mT	BINARY	HEX
0	0	0	0	0000 0000	00h

Table 6-9. 8-Bit Magnitude Data Format (Only Three Decimal Places Shown) (continued)

Magnitude (mT)				MAGNITUDE_RESULT[7:0]	
Range = 40 mT	Range = 80 mT	Range = 133 mT	Range = 266 mT	BINARY	HEX
0.303	0.602	0.973	1.939	0000 0001	01h
4.550	9.035	14.601	29.091	0000 1111	0Fh
32.152	63.849	103.179	205.576	1010 1010	6Ah
54.900	109.026	176.183	351.030	1011 0101	B5h

Figure 6-18. Magnitude Result Data Definition

6.5.2.4 Magnetic Sensor Offset Correction

The TMAG5173-Q1 enables offset correction for a pair of magnetic axes (see Figure 6-19). The MAG_OFFSET_CONFIG_1 and MAG_OFFSET_CONFIG_2 registers store the offset values to be corrected in 2's complement data format. As an example, if the uncorrected waveform for a particular axis has a value that is +2mT too high, enter the offset correction value of –2mT in the corresponding offset correction register. The selection and order of the sensors are defined in the ANGLE_EN register bits setting. The default value of these offset correction registers are set as zero.

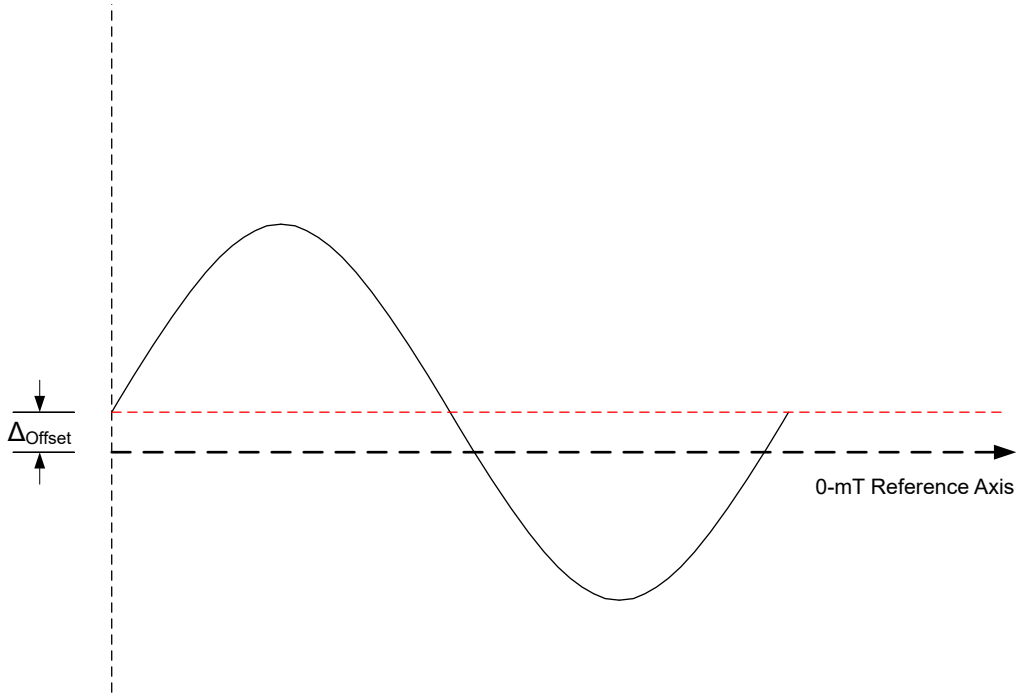


Figure 6-19. Magnetic Sensor Data Offset Correction

The offset correction is stored in 8-bit 2's complement format, with the LSB size defined by the magnetic range:

- 40mT: 52.75LSB/mT
- 80mT: 26.5625LSB/mT
- 133mT: 16.4375LSB/mT
- 266mT: 8.25LSB/mT

Table 6-10. 8-Bit Magnetic Sensor Offset Correction Data Format (Two Decimal Places Shown)

Magnetic Offset (mT)				MAG_OFFSET_CONFIG_x[7:0]	
Range = 40 mT	Range = 80 mT	Range = 133 mT	Range = 266 mT	BINARY	HEX
-2.43	-4.82	-7.79	-15.52	1000 0000	80h
-1.02	-2.03	-3.29	-6.55	1100 1010	4Ah
-0.02	-0.04	-0.06	-0.12	1111 1111	FFh
0	0	0	0	0000 0000	00h
0.02	0.04	0.06	0.12	0000 0001	01h
1.02	2.03	3.29	6.55	0011 0110	36h
2.41	4.78	7.73	15.39	0111 1111	7Fh

6.6 TMAG5173-Q1 Registers

Table 6-11 lists the memory-mapped registers for the TMAG5173-Q1 registers. All register offset addresses not listed in Table 6-11 should be considered as reserved locations and the register contents should not be modified.

Table 6-11. TMAG5173-Q1 Registers

Offset	Acronym	Register Name	Section
0h	DEVICE_CONFIG_1	Configure Device Operation Modes	Section 6.6.1
1h	DEVICE_CONFIG_2	Configure Device Operation Modes	Section 6.6.2
2h	SENSOR_CONFIG_1	Sensor Device Operation Modes	Section 6.6.3
3h	SENSOR_CONFIG_2	Sensor Device Operation Modes	Section 6.6.4
4h	X_THR_CONFIG	X Threshold Configuration	Section 6.6.5
5h	Y_THR_CONFIG	Y Threshold Configuration	Section 6.6.6
6h	Z_THR_CONFIG	Z Threshold Configuration	Section 6.6.7
7h	T_CONFIG	Temp Sensor Configuration	Section 6.6.8
8h	INT_CONFIG_1	Configure Device Operation Modes	Section 6.6.9
9h	MAG_GAIN_CONFIG	Configure Device Operation Modes	Section 6.6.10
Ah	MAG_OFFSET_CONFIG_1	Configure Device Operation Modes	Section 6.6.11
Bh	MAG_OFFSET_CONFIG_2	Configure Device Operation Modes	Section 6.6.12
Ch	I2C_ADDRESS	I2C Address Register	Section 6.6.13
Dh	DEVICE_ID	ID for the device die	Section 6.6.14
Eh	MANUFACTURER_ID_LSB	Manufacturer ID lower byte	Section 6.6.15
Fh	MANUFACTURER_ID_MSB	Manufacturer ID upper byte	Section 6.6.16
10h	T_MSB_RESULT	Conversion Result Register	Section 6.6.17
11h	T_LSB_RESULT	Conversion Result Register	Section 6.6.18
12h	X_MSB_RESULT	Conversion Result Register	Section 6.6.19
13h	X_LSB_RESULT	Conversion Result Register	Section 6.6.20
14h	Y_MSB_RESULT	Conversion Result Register	Section 6.6.21
15h	Y_LSB_RESULT	Conversion Result Register	Section 6.6.22
16h	Z_MSB_RESULT	Conversion Result Register	Section 6.6.23
17h	Z_LSB_RESULT	Conversion Result Register	Section 6.6.24
18h	CONV_STATUS	Conversion Satus Register	Section 6.6.25
19h	ANGLE_RESULT_MSB	Conversion Result Register	Section 6.6.26
1Ah	ANGLE_RESULT_LSB	Conversion Result Register	Section 6.6.27
1Bh	MAGNITUDE_RESULT	Conversion Result Register	Section 6.6.28

Table 6-11. TMAG5173-Q1 Registers (continued)

Offset	Acronym	Register Name	Section
1Ch	DEVICE_STATUS	Device_Diag Status Register	Section 6.6.29

Complex bit access types are encoded to fit into small table cells. Table 6-12 shows the codes that are used for access types in this section.

Table 6-12. TMAG5173-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1CP	W 1C P	Write 1 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

6.6.1 DEVICE_CONFIG_1 Register (Offset = 0h) [Reset = 00h]

DEVICE_CONFIG_1 is shown in Table 6-13.

Return to the Summary Table.

Table 6-13. DEVICE_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CRC_EN	R/W	0h	Enables I2C CRC byte to be sent. 0h = CRC disabled 1h = CRC enabled
6-5	MAG_TEMPCO	R/W	0h	Temperature coefficient of the magnet. 0h = 0 %/°C (No temperature compensation) 1h = 0.12 %/°C (NdBFe) 2h = 0.03 %/°C (SmCo) 3h = 0.20 %/°C (Ceramic)
4-2	CONV_AVG	R/W	0h	Enables additional sampling of the sensor data to reduce the noise effect (or to increase resolution). 0h = 1x average, 10.0-kSPS (3-axes) or 20-kSPS (1 axis) 1h = 2x average, 5.7-kSPS (3-axes) or 13.3-kSPS (1 axis) 2h = 4x average, 3.1-kSPS (3-axes) or 8.0-kSPS (1 axis) 3h = 8x average, 1.6-kSPS (3-axes) or 4.4-kSPS (1 axis) 4h = 16x average, 0.8-kSPS (3-axes) or 2.4-kSPS (1 axis) 5h = 32x average, 0.4-kSPS (3-axes) or 1.2-kSPS (1 axis)
1-0	I2C_RD	R/W	0h	Defines the I2C read mode. 0h = Standard I2C 3-byte read command 1h = 1-byte I2C read command for 16bit sensor data and conversion status 2h = 1-byte I2C read command for 8 bit sensor MSB data and conversion status 3h = Reserved

6.6.2 DEVICE_CONFIG_2 Register (Offset = 1h) [Reset = 00h]

DEVICE_CONFIG_2 is shown in Table 6-14.

Return to the Summary Table.

Table 6-14. DEVICE_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	THR_HYST	R/W	0h	Select threshold band for the interrupt function, or hysteresis for the switch function. As an example, with 40-mT range the threshold band or hysteresis value, when THR_HYST set at 2h, ((40/(2^{11}))*8 = 0.156 mT. 0h = Takes the 2's complement value of each x_THR_CONFIG register to create a magnetic threshold of the corresponding axis 1h = Takes the 7 LSB bits of the x_THR_CONFIG register to create two opposite magnetic thresholds (one north, and another south) of equal magnitude. 2h = 8 LSB threshold band, 12 bit resolution 3h = 16 LSB threshold band, 12 bit resolution 4h = 32 LSB threshold, band 12 bit resolution 5h = 64 LSB threshold band, 12 bit resolution 6h = 128 LSB threshold band, 12 bit resolution 7h = 256 LSB threshold band, 12 bit resolution
4	LP_LN	R/W	0h	Selects the modes between low active current or low-noise modes. 0h = Low active current mode 1h = Low noise mode
3	I2C_GLITCH_FILTER	R/W	0h	I2C glitch filter. 0h = Glitch filter on 1h = Glitch filter off
2	TRIGGER_MODE	R/W	0h	Selects a condition which initiates a single conversion based off already configured registers. A running conversion completes before executing a trigger. Redundant triggers are ignored. TRIGGER_MODE is available only during the mode explicitly mentioned in OPERATING_MODE. 0h = Conversion starts at I2C command bits, default 1h = Conversion starts through a trigger signal at the $\overline{\text{INT}}$ pin
1-0	OPERATING_MODE	R/W	0h	Selects the device operating mode. 0h = Standby mode (starts new conversion at trigger event) 1h = Sleep mode 2h = Continuous measure mode 3h = Wake-up and sleep mode (W&S mode)

6.6.3 SENSOR_CONFIG_1 Register (Offset = 2h) [Reset = 00h]

SENSOR_CONFIG_1 is shown in Table 6-15.

Return to the Summary Table.

Table 6-15. SENSOR_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MAG_CH_EN	R/W	0h	Enables data acquisition of the magnetic channel(s). 0h = All magnetic channels of off, default 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channel enabled 4h = Z channel enabled 5h = Z, X channel enabled 6h = Y, Z channel enabled 7h = X, Y, Z channel enabled 8h = XYX channel enabled 9h = YXY channel enabled Ah = YZY channel enabled Bh = XZX channel enabled Ch = X, Y, Z with positive AFE diagnostic check Dh = X, Y, Z with negative AFE diagnostic check Eh = Hall resistance check + ADC check Fh = Hall offset check +ADC check

Table 6-15. SENSOR_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	SLEEPTIME	R/W	0h	Selects the time spent in low power mode between conversions when OPERATING_MODE=11b 0h = 1ms 1h = 5ms 2h = 10ms 3h = 15ms 4h = 20ms 5h = 30ms 6h = 50ms 7h = 100ms 8h = 500ms 9h = 1000ms Ah = 2000ms Bh = 5000ms Ch = 20000ms

6.6.4 SENSOR_CONFIG_2 Register (Offset = 3h) [Reset = 00h]

SENSOR_CONFIG_2 is shown in Table 6-16.

Return to the Summary Table.

Table 6-16. SENSOR_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	THRX_COUNT	R/W	0h	Number of threshold crossings before the interrupt is asserted. 0h = 1 threshold crossing 1h = 4 threshold crossing
5	MAG_THR_DIR	R/W	0h	Selects the direction of threshold check. This bit is ignored when THR_HYST > 001b. 0h = sets interrupt for field above the threshold 1h = sets interrupt for field below the threshold
4	MAG_GAIN_CH	R/W	0h	Selects the axis for magnitude gain correction value entered in MAG_GAIN_CONFIG register. 0h = 1st channel is selected for gain adjustment 1h = 2nd channel is selected for gain adjustment
3-2	ANGLE_EN	R/W	0h	Enables angle calculation, magnetic gain, and offset corrections between two selected magnetic channels. 0h = No angle calculation, magnitude gain, and offset correction enabled 1h = X 1st, Y 2nd 2h = Y 1st, Z 2nd 3h = X 1st, Z 2nd
1	X_Y_RANGE	R/W	0h	Select the X and Y axes magnetic range from 2 different options. 0h = ±40mT (TMAG5173A1) or ±133mT (TMAG5173A2), default 1h = ±80mT (TMAG5173A1) or ±266mT (TMAG5173A2)
0	Z_RANGE	R/W	0h	Select the Z axis magnetic range from 2 different options. 0h = ±40mT (TMAG5173A1) or ±133mT (TMAG5173A2), default 1h = ±80mT (TMAG5173A1) or ±266mT (TMAG5173A2)

6.6.5 X_THR_CONFIG Register (Offset = 4h) [Reset = 00h]

X_THR_CONFIG is shown in Table 6-17.

Return to the Summary Table.

Table 6-17. X_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_THR_CONFIG	R/W	0h	8-bit, 2's complement X axis threshold code for limit check. The range of possible threshold entrees can be from -128 to 127. The threshold value in mT is calculated for A1 as (40(1+X_Y_RANGE)/128)*X_THR_CONFIG, for A2 as (133(1+X_Y_RANGE)/128)*X_THR_CONFIG. Default 0h means no threshold comparison.

6.6.6 Y_THR_CONFIG Register (Offset = 5h) [Reset = 00h]

Y_THR_CONFIG is shown in Table 6-18.

Return to the Summary Table.

Table 6-18. Y_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_THR_CONFIG	R/W	0h	8-bit, 2's complement Y axis threshold code for limit check. The range of possible threshold entrees can be from -128 to 127. The threshold value in mT is calculated for A1 as (40(1+X_Y_RANGE)/128)*Y_THR_CONFIG, for A2 as (133(1+X_Y_RANGE)/128)*Y_THR_CONFIG. Default 0h means no threshold comparison.

6.6.7 Z_THR_CONFIG Register (Offset = 6h) [Reset = 00h]

Z_THR_CONFIG is shown in Table 6-19.

Return to the Summary Table.

Table 6-19. Z_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_THR_CONFIG	R/W	0h	8-bit, 2's complement Z axis threshold code for limit check. The range of possible threshold entrees can be from -128 to 127. The threshold value in mT is calculated for A1 as (40(1+Z_RANGE)/128)*Z_THR_CONFIG, for A2 as (133(1+Z_RANGE)/128)*Z_THR_CONFIG. Default 0h means no threshold comparison.

6.6.8 T_CONFIG Register (Offset = 7h) [Reset = 00h]

T_CONFIG is shown in Table 6-20.

Return to the Summary Table.

Table 6-20. T_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	T_THR_CONFIG	R/W	0h	Temperature threshold code entered by user. The valid temperature threshold ranges are -41C to 170C with the threshold codes for -41C = 1Ah, and 170C = 34h. Resolution is 8-degree C/ LSB. Default 0h means no threshold comparison.
0	T_CH_EN	R/W	0h	Enables data acquisition of the temperature channel. 0h = Temp channel disabled 1h = Temp channel enabled

6.6.9 INT_CONFIG_1 Register (Offset = 8h) [Reset = 00h]

INT_CONFIG_1 is shown in Table 6-21.

Return to the Summary Table.

Table 6-21. INT_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSLT_INT	R/W	0h	Enable interrupt response when conversion result is complete. 0h = Interrupt is not asserted when the configured set of conversions are complete 1h = Interrupt is asserted when the configured set of conversions are complete
6	THRSLD_INT	R/W	0h	Enable interrupt response on a predefined threshold cross. 0h = Interrupt is not asserted when a threshold is crossed 1h = Interrupt is asserted when a threshold is crossed
5	INT_STATE	R/W	0h	$\overline{\text{INT}}$ interrupt latched or pulsed. 0h = $\overline{\text{INT}}$ interrupt latched until clear by a primary addressing the device 1h = $\overline{\text{INT}}$ interrupt pulse for 10 us

Table 6-21. INT_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-2	INT_MODE	R/W	0h	Interrupt mode select. 0h = No interrupt 1h = Interrupt through $\overline{\text{INT}}$ 2h = Interrupt through $\overline{\text{INT}}$ except when I2C bus is busy. 3h = Interrupt through SCL 4h = Interrupt through SCL except when I2C bus is busy. 5h = Unipolar switch function during continuous measure mode (only one magnetic field conversion support, selects the first magnetic field in X, Y, Z order if multiple thresholds are enabled). This mode overrides any interrupt function (INT trigger is also disabled), and only implements a Hall switch function based off the x_THRX_CONFIG and THR_HYST settings. Select THR_HYST >001b for this mode. 6h = Omnipolar switch function during continuous measure mode (only one magnetic field conversion support, selects the first magnetic field in X, Y, Z order if multiple thresholds are enabled). This mode overrides any interrupt function (INT trigger is also disabled), and only implements a Hall switch function based off the x_THRX_CONFIG and THR_HYST settings. Select THR_HYST >001b for this mode. 7h = Not valid- defaults to 000b mode
1	RESERVED	R	0h	Reserved
0	MASK_INTB	R/W	0h	Mask $\overline{\text{INT}}$ pin when $\overline{\text{INT}}$ connected to GND. 0h = $\overline{\text{INT}}$ pin is enabled 1h = $\overline{\text{INT}}$ pin is disabled (for wake-up and trigger functions)

6.6.10 MAG_GAIN_CONFIG Register (Offset = 9h) [Reset = 00h]

MAG_GAIN_CONFIG is shown in Table 6-22.

Return to the Summary Table.

Table 6-22. MAG_GAIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_VALUE	R/W	0h	8-bit gain value determined by a primary to adjust a Hall axis gain. The particular axis is selected based off the settings of MAG_GAIN_CH and ANGLE_EN register bits. The binary 8-bit input is interpreted as a fractional value in between 0 and 1 based off the formula, 'user entered value in decimal/256'. Gain value of 0 is interpreted by the device as 1.

6.6.11 MAG_OFFSET_CONFIG_1 Register (Offset = Ah) [Reset = 00h]

MAG_OFFSET_CONFIG_1 is shown in Table 6-23.

Return to the Summary Table.

Table 6-23. MAG_OFFSET_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OFFSET_VALUE_1ST	R/W	0h	8-bit, 2's complement number entered by a primary to adjust the 1st axis offset during angle calculation. The 1st axis is defined in ANGLE_EN register bits. The range of possible valid entrees in decimal numbers can be -128 to 127. The offset value is calculated by multiplying bit resolution (uT/ LSB) with the entered value.

6.6.12 MAG_OFFSET_CONFIG_2 Register (Offset = Bh) [Reset = 00h]

MAG_OFFSET_CONFIG_2 is shown in Table 6-24.

Return to the Summary Table.

Table 6-24. MAG_OFFSET_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OFFSET_VALUE_2ND	R/W	0h	8-bit, 2's complement number entered by a primary to adjust the 2nd axis offset during angle calculation. The 2nd axis is defined in ANGLE_EN register bits. The range of possible valid entrees in decimal numbers can be -128 to 127. The offset value is calculated by multiplying bit resolution (uT/ LSB) with the entered value.

6.6.13 I2C_ADDRESS Register (Offset = Ch) [Reset = 6Ah]

I2C_ADDRESS is shown in Table 6-25.

Return to the Summary Table.

Table 6-25. I2C_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	I2C_ADDRESS	R/W	35h	7-bit default factory I2C address is loaded from OTP during first power up. Change these bits to a new setting if a new I2C address is required (at each power cycle these bits need to be written again to avoid going back to default factory address).
0	I2C_ADDRESS_UPDATE_EN	R/W	0h	Enable a new user defined I2C address. 0h = Disable update of I2C address 1h = Enable update of I2C address with bits (7:1)

6.6.14 DEVICE_ID Register (Offset = Dh) [Reset = 04h]

DEVICE_ID is shown in Table 6-26.

Return to the Summary Table.

Table 6-26. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	1h	Reserved
1-0	VER	R	0h	Device version indicator. Reset value of DEVICE_ID depends on the orderable part number. 0h = ±40-mT and ±80-mT range 1h = Reserved 2h = ±133-mT and ±266-mT range 3h = Reserved

6.6.15 MANUFACTURER_ID_LSB Register (Offset = Eh) [Reset = 49h]

MANUFACTURER_ID_LSB is shown in Table 6-27.

Return to the Summary Table.

Table 6-27. MANUFACTURER_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[7:0]	R	49h	Unique manufacturer ID LSB bits.

6.6.16 MANUFACTURER_ID_MSB Register (Offset = Fh) [Reset = 54h]

MANUFACTURER_ID_MSB is shown in Table 6-28.

Return to the Summary Table.

Table 6-28. MANUFACTURER_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[15:8]	R	54h	Unique manufacturer ID MSB bits.

6.6.17 T_MSB_RESULT Register (Offset = 10h) [Reset = 00h]

T_MSB_RESULT is shown in Table 6-29.

Return to the Summary Table.

Table 6-29. T_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	T_CH_RESULT [15:8]	R	0h	T-channel data conversion results, MSB 8 bits.

6.6.18 T_LSB_RESULT Register (Offset = 11h) [Reset = 00h]

T_LSB_RESULT is shown in Table 6-30.

Return to the Summary Table.

Table 6-30. T_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	T_CH_RESULT [7:0]	R	0h	T-channel data conversion results, LSB 8 bits.

6.6.19 X_MSB_RESULT Register (Offset = 12h) [Reset = 00h]

X_MSB_RESULT is shown in Table 6-31.

Return to the Summary Table.

Table 6-31. X_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_CH_RESULT [15:8]	R	0h	X-channel data conversion results, MSB 8 bits.

6.6.20 X_LSB_RESULT Register (Offset = 13h) [Reset = 00h]

X_LSB_RESULT is shown in Table 6-32.

Return to the Summary Table.

Table 6-32. X_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_CH_RESULT [7:0]	R	0h	X-channel data conversion results, LSB 8 bits.

6.6.21 Y_MSB_RESULT Register (Offset = 14h) [Reset = 00h]

Y_MSB_RESULT is shown in Table 6-33.

Return to the Summary Table.

Table 6-33. Y_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_CH_RESULT [15:8]	R	0h	Y-channel data conversion results, MSB 8 bits.

6.6.22 Y_LSB_RESULT Register (Offset = 15h) [Reset = 00h]

Y_LSB_RESULT is shown in Table 6-34.

Return to the Summary Table.

Table 6-34. Y_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_CH_RESULT [7:0]	R	0h	Y-channel data conversion results, LSB 8 bits.

6.6.23 Z_MSB_RESULT Register (Offset = 16h) [Reset = 00h]

Z_MSB_RESULT is shown in Table 6-35.

Return to the Summary Table.

Table 6-35. Z_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_CH_RESULT [15:8]	R	0h	Z-channel data conversion results, MSB 8 bits.

6.6.24 Z_LSB_RESULT Register (Offset = 17h) [Reset = 00h]

Z_LSB_RESULT is shown in Table 6-36.

Return to the Summary Table.

Table 6-36. Z_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_CH_RESULT [7:0]	R	0h	Z-channel data conversion results, LSB 8 bits.

6.6.25 CONV_STATUS Register (Offset = 18h) [Reset = 10h]

CONV_STATUS is shown in Table 6-37.

Return to the Summary Table.

Table 6-37. CONV_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SET_COUNT	R	0h	Rolling count of conversion data sets.
4	POR	R/W1CP	1h	Device powered up, or experienced power-on-reset. Bit is clear when host writes back '1'. 0h = No POR 1h = POR occurred
3-2	RESERVED	R	0h	Reserved

Table 6-37. CONV_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DIAG_STATUS	R	0h	Detect any internal diagnostics fail which include V_{CC} UV, internal memory CRC error, $\overline{INT}$ pin error and internal clock error. 0h = No diagnostic fail 1h = Diagnostic fail detected
0	RESULT_STATUS	R	0h	Conversion data buffer is ready to be read. 0h = Conversion data not complete 1h = Conversion data complete

6.6.26 ANGLE_RESULT_MSB Register (Offset = 19h) [Reset = 00h]

ANGLE_RESULT_MSB is shown in Table 6-38.

Return to the Summary Table.

Table 6-38. ANGLE_RESULT_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANGLE_RESULT_MSB	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits after combining the ANGLE_RESULT_MSB and _LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

6.6.27 ANGLE_RESULT_LSB Register (Offset = 1Ah) [Reset = 00h]

ANGLE_RESULT_LSB is shown in Table 6-39.

Return to the Summary Table.

Table 6-39. ANGLE_RESULT_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANGLE_RESULT_LSB	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits after combining the ANGLE_RESULT_MSB and _LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

6.6.28 MAGNITUDE_RESULT Register (Offset = 1Bh) [Reset = 00h]

MAGNITUDE_RESULT is shown in Table 6-40.

Return to the Summary Table.

Table 6-40. MAGNITUDE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAGNITUDE_RESULT	R	0h	Resultant vector magnitude during angle measurement. This value should be constant during 360-degree on-axis angle measurement. The magnitude in mT can be calculated as (MAGNITUDE_RESULT*256)/(LSB/mT) where the LSB/mT is calculated in 16-bit format as specified in the magnetic characteristics table.

6.6.29 DEVICE_STATUS Register (Offset = 1Ch) [Reset = 10h]

DEVICE_STATUS is shown in Table 6-41.

Return to the Summary Table.

Table 6-41. DEVICE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	INTB_RB	R	1h	Indicates the level that the device is reading back from $\overline{\text{INT}}$ pin. The reset value of DEVICE_STATUS depends on the status of the $\overline{\text{INT}}$ pin at power-up. 0h = $\overline{\text{INT}}$ pin driven low 1h = $\overline{\text{INT}}$ pin status high
3	OSC_ER	R/W1CP	0h	Indicates if Oscillator error is detected. Bit is clear when host writes back '1'. 0h = No oscillator error detected 1h = Oscillator error detected

Table 6-41. DEVICE_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	INT_ER	R/W1CP	0h	Indicates if $\overline{INT}$ pin error is detected. Bit is clear when host writes back '1'. 0h = No $\overline{INT}$ error detected 1h = $\overline{INT}$ error detected
1	OTP_CRC_ER	R/W1CP	0h	Indicates if OTP CRC error is detected. Bit is clear when host writes back '1'. 0h = No OTP CRC error detected 1h = OTP CRC error detected
0	VCC_UV_ER	R/W1CP	0h	Indicates if V_{CC} undervoltage was detected. Bit is clear when host writes back '1'. 0h = No V_{CC} UV detected 1h = V_{CC} UV detected

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Select the Sensitivity Option

Select the highest TMAG5173-Q1 sensitivity option that can measure the required range of magnetic flux density so that the ADC input range is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations under the TMAG5173-Q1 product folder on ti.com.

7.1.2 Temperature Compensation for Magnets

The TMAG5173-Q1 temperature compensation is designed to directly compensate the average temperature drift of several magnets as specified in the MAG_TEMPCO register bits. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite magnets as the temperature increases. Set the MAG_TEMPCO bit to default 00b if the device temperature compensation is not needed.

7.1.3 Sensor Conversion

Multiple conversion schemes can be adopted based off the MAG_CH_EN and CONV_AVG register bits settings.

7.1.3.1 Continuous Conversion

The TMAG5173-Q1 can be set in continuous conversion mode when OPERATING_MODE is set to 10b. Figure 7-1 shows a few examples of continuous conversion. The input magnetic field is processed in two steps. In the first step, the device spins the Hall sensor elements and integrates the sampled data. In the second step, the ADC block converts the analog signal into digital bits and stores in the corresponding result register. While the ADC starts processing the first magnetic sample, the spin block can start processing another magnetic sample. In this mode, the temperature data is taken at the beginning of each new conversion. This temperature data is used to compensate for the magnetic thermal drift.

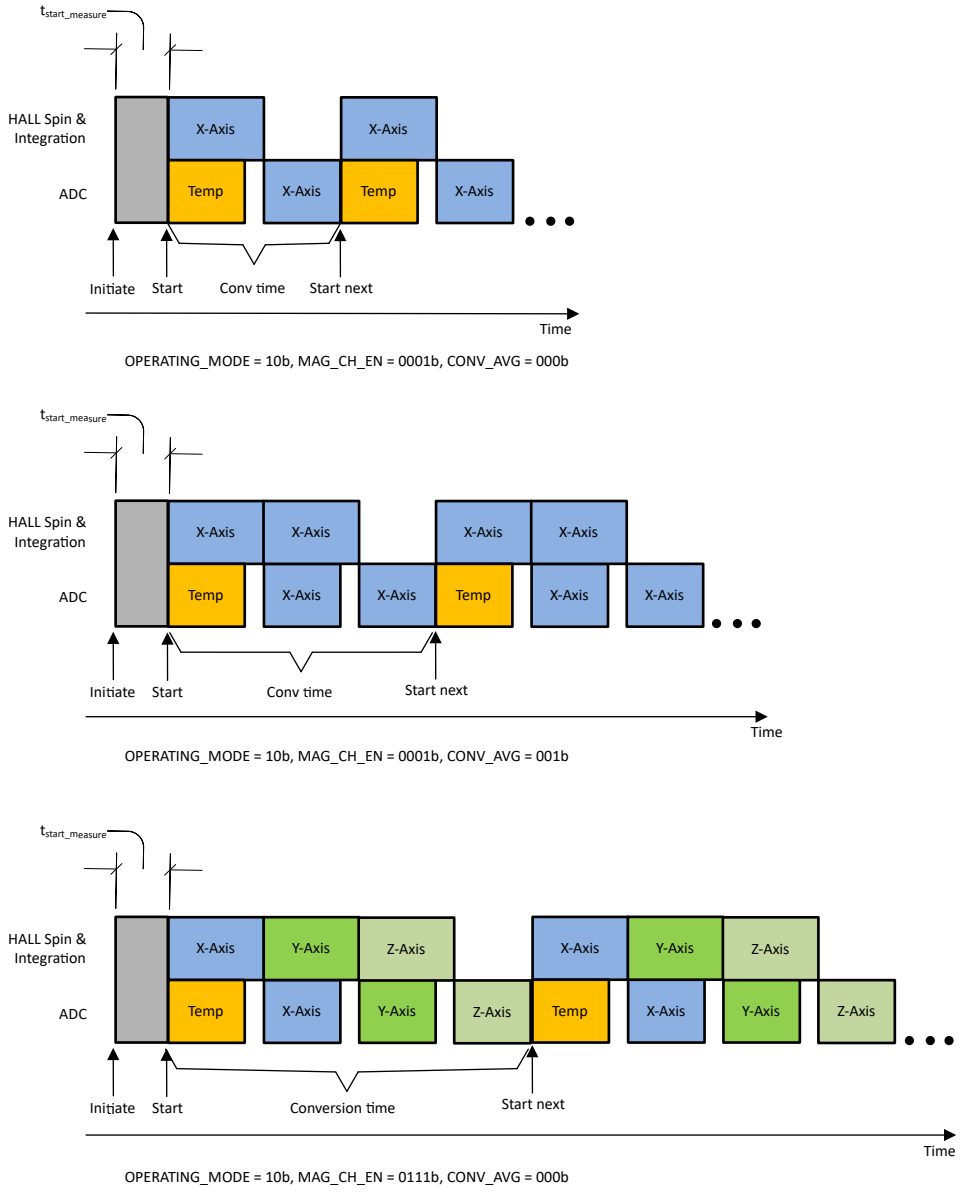


Figure 7-1. Continuous Conversion Examples

7.1.3.2 Trigger Conversion

The TMAG5173-Q1 supports trigger conversion with OPERATING_MODE set to 00b. The trigger event can be initiated through I^2C command or $\overline{INT}$ signal. Figure 7-2 shows an example of trigger conversion with temperature, X, Y, and Z sensors activated.

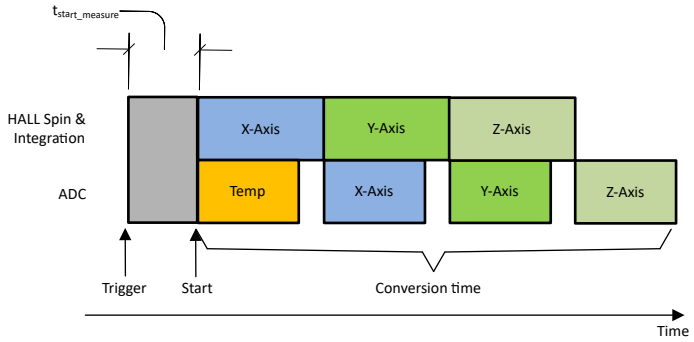


Figure 7-2. Trigger Conversion for Temperature, X, Y, & Z Sensors

7.1.3.3 Pseudo-Simultaneous Sampling

In absolute angle measurement, application sensor data from multiple axes are required to calculate an accurate angle. The magnetic field data collected at different times through the same signal chain introduces error in angle calculation. The TMAG5173-Q1 offers pseudo-simultaneous sampling data collection modes to eliminate this error. Figure 7-3 shows an example where MAG_CH_EN is set at 1011b to collect XZX data. Equation 13 shows that the time stamps for the X and Z sensor data are the same.

$$t_Z = \frac{t_{X1} + t_{X2}}{2} \tag{13}$$

where

- t_{X1}, t_Z, t_{X2} are time stamps for X, Z, X sensor data completion as defined in Figure 7-3.

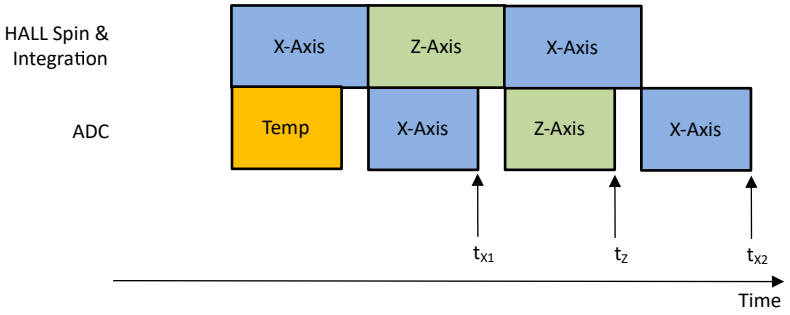


Figure 7-3. XZX Magnetic Field Conversion

The vertical X, Y sensors of the TMAG5173-Q1 exhibit more noise than the horizontal Z sensor. The pseudo-simultaneous sampling can be used to equalize the noise floor when two set of vertical sensor data are collected against one set of horizontal sensor data, as in examples of XZX or YZY modes.

7.1.4 Magnetic Limit Check

The TMAG5173-Q1 enables magnetic limit checks for single or multiple axes at the same time. Figure 7-4 to Figure 7-7 show examples of magnetic limit cross detection events while the field going above, below, exiting a magnetic band, and entering a magnetic band. The device keeps generating interrupt with each new conversion if the magnetic fields remain in the shaded regions in the figures. The MAG_THR_DIR and THR_HYST register bits help select different limit cross modes.

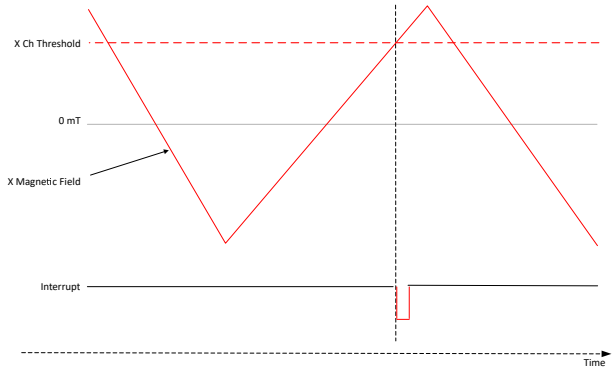


Figure 7-4. Magnetic Upper Limit Cross Check With MAG_THR_DIR =0b, THR_HYST = 000b

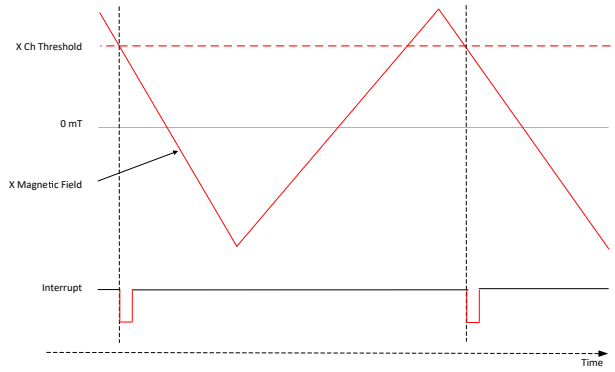


Figure 7-5. Magnetic Lower Limit Cross Check With MAG_THR_DIR =1b, THR_HYST = 000b

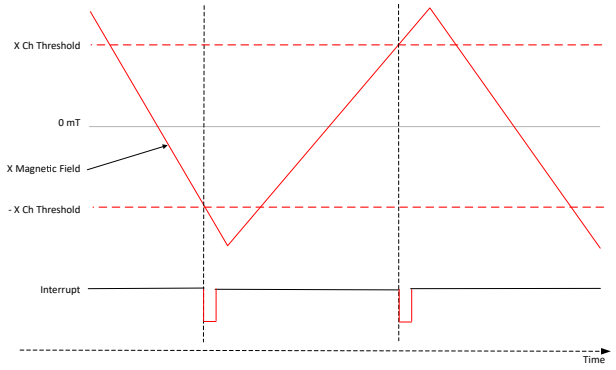


Figure 7-6. Magnetic Field Going Out of Band Check With MAG_THR_DIR =0b, THR_HYST = 001b

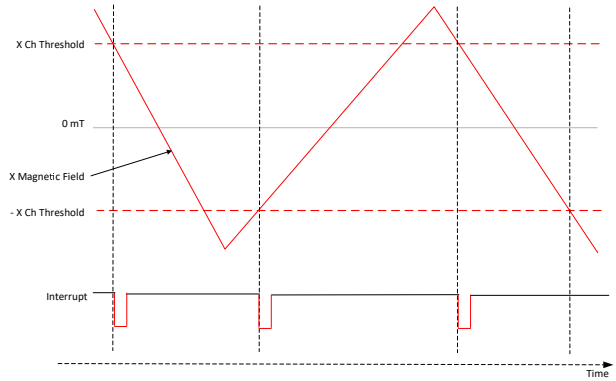


Figure 7-7. Magnetic Field Entering a Band Check With MAG_THR_DIR =1b, THR_HYST = 001b

7.1.5 Magnetic Threshold Band Cross Detection

Table 7-1 shows different threshold band width options supported by the TMAG5173-Q1. For larger threshold band use the A2 orderable. The magnetic threshold band is useful to create programmable magnetic switch and latch hysteresis.

Table 7-1. Threshold Band Width (Upper Threshold- Lower Threshold) in mT

THR_HYST Codes	±40-mT Option	±80-mT Option	±133-mT Option	±266-mT Option
	A1/ B1/ C1/ D1 Orderable		A2/ B2/ C2/ D2 Orderable	
010b	0.156	0.312	0.52	1.04
011b	0.312	0.625	1.04	2.08
100b	0.625	1.25	2.08	4.15
101b	1.25	2.5	4.16	8.30
110b	2.5	5.0	8.30	16.63
111b	5.0	10.0	16.63	33.25

7.1.6 Error Calculation During Linear Measurement

The TMAG5173-Q1 offers independent configurations to perform linear position measurements in X, Y, and Z axes. To calculate the expected error during linear measurement, the contributions from each of the individual error sources must be understood. The relevant error sources include sensitivity error, offset, noise, cross axis sensitivity, hysteresis, nonlinearity, drift across temperature, drift across life time, and so forth. For a 3-axis Hall solution like the TMAG5173-Q1, the cross-axis sensitivity and hysteresis error sources are insignificant. Use Equation 14 to estimate the linear measurement error calculation at room temperature.

$$\text{Error}_{\text{LM\_25C}} = \frac{\sqrt{(\text{B} \times \text{SENS}_{\text{ER}})^2 + \text{B}_{\text{off}}^2 + \text{N}_{\text{RMS\_25}}^2}}{\text{B}} \times 100\% \quad (14)$$

where

- $\text{Error}_{\text{LM\_25C}}$ is total error in % during linear measurement at 25°C.
- B is input magnetic field.
- SENS_{ER} is sensitivity error in decimal number at 25°C. As an example, enter 0.05 for sensitivity error of 5%.
- B_{off} is offset error at 25°C.
- $\text{N}_{\text{RMS\_25}}$ is RMS noise at 25°C.

In many applications, system level calibration at room temperature can nullify the offset and sensitivity errors at 25°C. The noise errors can be reduced by internally averaging by up to 32x on the device in addition to the averaging that can be done in the microcontroller. Use Equation 15 to estimate the linear measurement error across temperature after calibration at room temperature.

$$\text{Error}_{\text{LM\_Temp}} = \frac{\sqrt{(\text{B} \times \text{SENS}_{\text{DR}})^2 + \text{B}_{\text{off\_DR}}^2 + \text{N}_{\text{RMS\_Temp}}^2}}{\text{B}} \times 100\% \quad (15)$$

where

- $\text{Error}_{\text{LM\_Temp}}$ is total error in % during linear measurement across temperature after room temperature calibration.
- B is input magnetic field.
- SENS_{DR} is sensitivity drift in decimal number from value at 25°C. As an example, enter 0.05 for sensitivity drift of 5%.
- $\text{B}_{\text{off\_DR}}$ is offset drift from value at 25°C.
- $\text{N}_{\text{RMS\_Temp}}$ is RMS noise across temperature.

If room temperature calibration is not performed, sensitivity and offset errors at room temperature must also account for total error calculation across temperature (see Equation 16).

$$\text{Error}_{\text{LM\_Temp\_NCal}} = \frac{\sqrt{(\text{B} \times \text{SENS}_{\text{ER}})^2 + (\text{B} \times \text{SENS}_{\text{DR}})^2 + \text{B}_{\text{off}}^2 + \text{B}_{\text{off\_DR}}^2 + \text{N}_{\text{RMS\_Temp}}^2}}{\text{B}} \times 100\% \quad (16)$$

where

- $\text{Error}_{\text{LM\_Temp\_NCal}}$ is total error in % during linear measurement across temperature without room temperature calibration.

Note

In this section, error sources such as system mechanical vibration, magnet temperature gradient, earth magnetic field, nonlinearity, lifetime drift, and so forth, are not considered. The user must take these additional error sources into account while calculating overall system error budgets.

7.1.7 Error Calculation During Angular Measurement

The TMAG5173-Q1 offers on-chip CORDIC to measure angle data from any of the two magnetic axes. The linear magnetic axis data can be used to calculate the angle using an external CORDIC as well. To calculate the expected error during angular measurement, the contributions from each individual error source must be understood. The relevant error sources include sensitivity error, offset, noise, axis-axis mismatch, nonlinearity, drift across temperature, drift across life time, and so forth. Use the Angle Error Calculation Tool to estimate the total error during angular measurement.

7.2 Typical Applications

Magnetic 3D sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5173-Q1 offers design flexibility in wide

range of industrial and personal electronics applications. In this section three common application examples are discussed in details.

7.2.1 Angle Measurement

Magnetic angle sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5173-Q1 offers an on-chip angle calculator providing angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE_EN register bits. The device offers angle output in complete 360 degree scale. Take several error sources into account for angle calculation, including sensitivity error, offset error, linearity error, noise, mechanical vibration, temperature drift, and so forth.

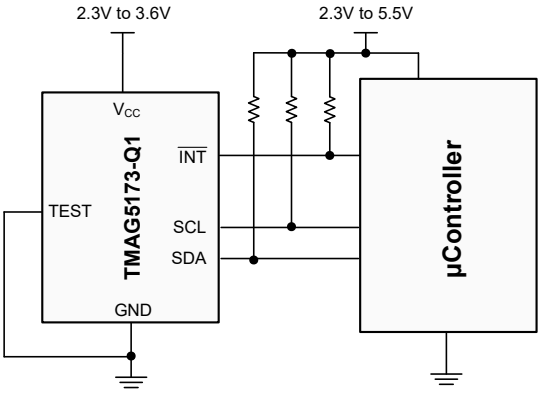


Figure 7-8. TMAG5173-Q1 Application Diagram for Angle Measurement

7.2.1.1 Design Requirements

Use the parameters listed in Table 7-2 for this design example.

Table 7-2. Design Parameters

DESIGN PARAMETERS	ON-AXIS MEASUREMENT	OFF-AXIS MEASUREMENT
Device	TMAG5173A1-Q1	TMAG5173A1-Q1
V_{CC}	3.3V	3.3V
Device Position	Directly under the magnet	At the adjacent side of the magnet
Magnet	Cylinder: 4.7625mm diameter, 12.7mm thick, neodymium N52, Br = 1480	Cylinder: 4.7625mm diameter, 12.7mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<600	<600
Desired Accuracy	<2° for 360° rotation	<2° for 360° rotation

7.2.1.2 Detailed Design Procedure

For accurate angle measurement, the two axes amplitudes must be normalized by selecting the proper gain adjustment value in the MAG_GAIN_CONFIG register. The gain adjustment value is a fractional decimal number between 0 and 1. The following steps must be followed to calculate this fractional value:

- Set the device at 32x average mode and rotate the shaft full 360 degree.
- Record the two axes sensor ADC codes for the full 360 degree rotation.
- A normalized plot for the full 360 degree rotations are represented in Figure 7-10 or Figure 7-11.
- Measure the maximum peak-peak ADC code delta for each axis, A_X and A_Y.
- If $A_X > A_Y$, set the MAG_GAIN_CH register bit to 0b. Calculate the gain adjustment value for X axis: $G_X = \frac{A_Y}{A_X}$

- If A_X<A_Y, set the MAG_GAIN_CH register bit to 1b. Calculate the gain adjustment value for Y axis: $G_Y = \frac{1}{G_X}$
- The target binary gain setting at the GAIN VALUE register bits are calculated from the equation, G_X or G_Y = $GAIN\_VALUE_{decimal}$/ 256.

Example 1: If $A_X = A_Y$ = 60,000, the GAIN_VALUE register bits are set at default 0000 0000b.

Example 2: If A_X= 60,000, A_Y = 45,000, the G_X = 45,000/60,000 =0.75. Set MAG_GAIN_CH to 0b and GAIN_VALUE to 1100 0000b.

Example 3: If A_X= 45,000, A_Y = 60,000, the G_X = (60,000/45,000) =1.33. Since G_X >1, the gain adjustment needs to be applied to Y axis with G_Y =1/G_X. Set MAG_GAIN_CH to 1b and GAIN_VALUE to 1100 0000b.

7.2.1.2.1 Gain Adjustment for Angle Measurement

Common measurement topology include angular position measurements in on-axis or off-axis angular measurements shown in Figure 7-9. Select the on-axis measurement topology whenever possible as this offers the best optimization of magnetic field and the device measurement ranges. The TMAG5173-Q1 offers on-chip gain adjustment option to account for mechanical position misalignments.

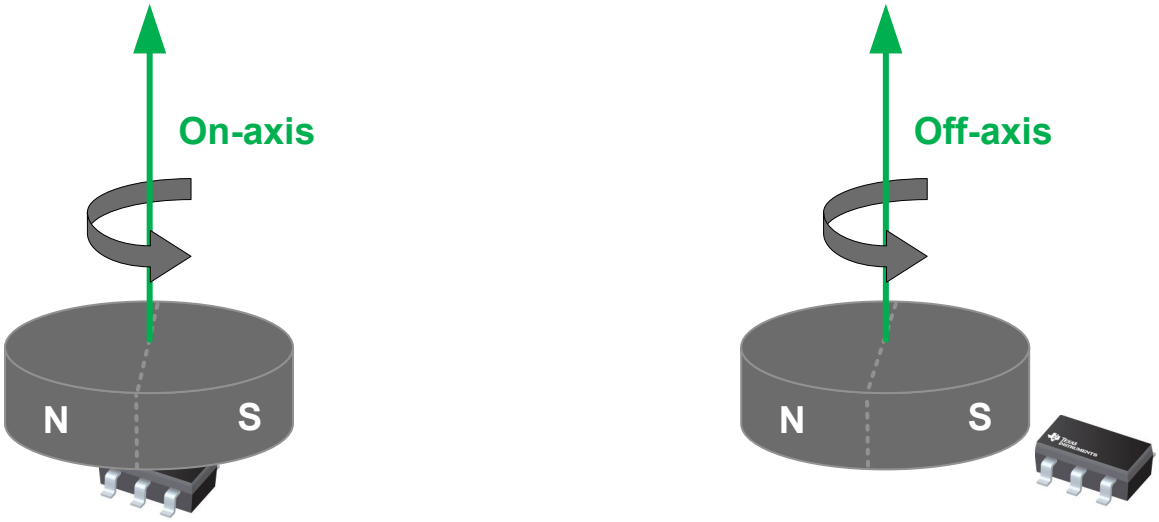


Figure 7-9. On-Axis vs Off-Axis Angle Measurements

7.2.1.3 Application Curves

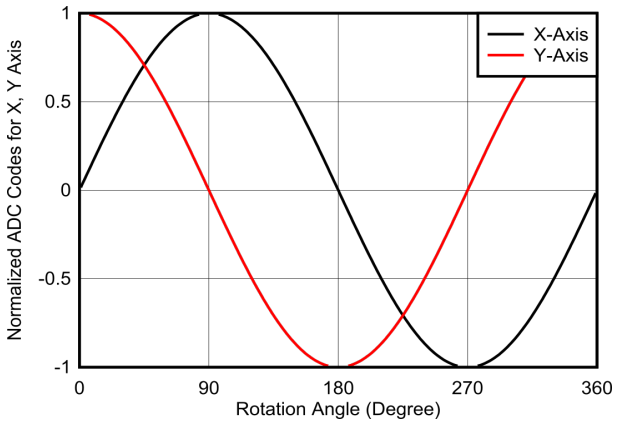


Figure 7-10. X and Y Sensor Data for Full 360 Degree Rotation for On-Axis Measurement

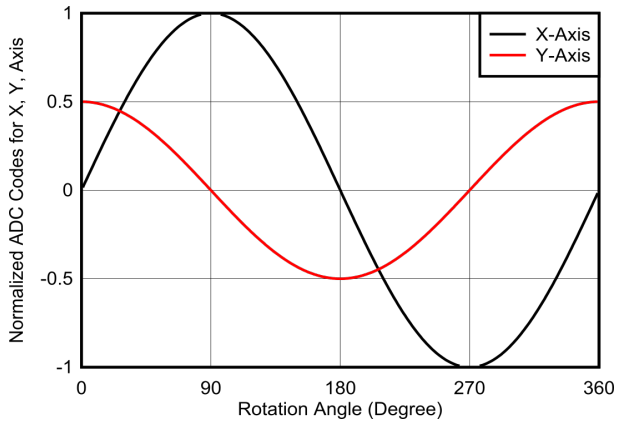


Figure 7-11. X and Y Sensor Data for Full 360 Degree Rotation for Off-Axis Measurement

7.2.2 I²C Address Expansion

The TMAG5173-Q1 is offered in four different factory-programmed I²C addresses. The device also supports additional I²C addresses through the configuration of the I2C_ADDRESS register. There are seven bits to select 128 different addresses. Take system limitations like bus loading, maximum clock frequency, available GPIOs from a microcontroller, and so forth, in account before selecting maximum number of sensors in a single I²C bus.

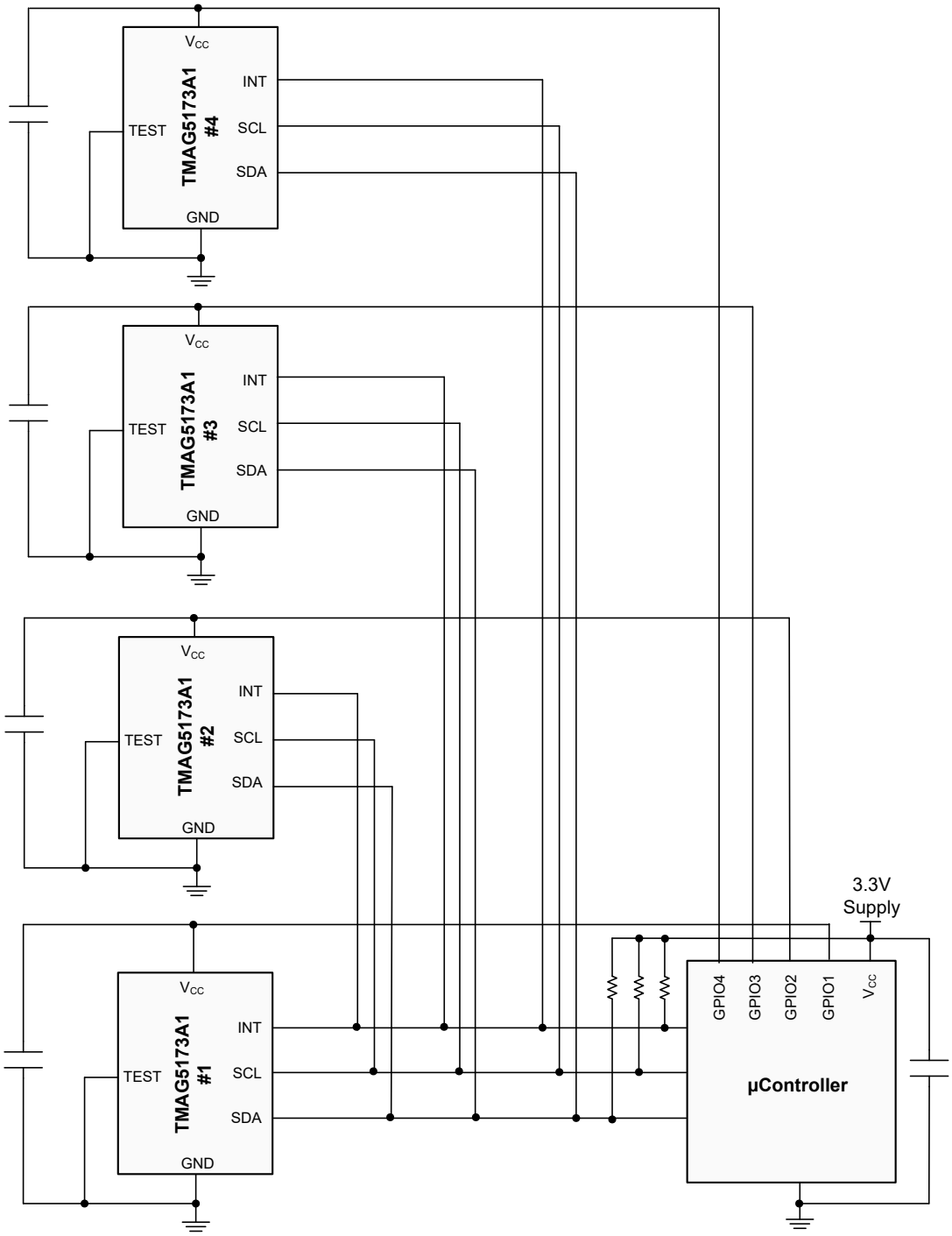


Figure 7-12. TMAG5173-Q1 Application Diagram for I²C Address Expansion

7.2.2.1 Design Requirements

Use the parameters listed in Table 7-2 for this design example.

Table 7-3. Design Parameters

PARAMETERS	DESIGN TARGET
Device orderable	TMAG5173A1-Q1
V_{CC}	3.3V
# of Devices in same bus	4 (same method can be used to expand the number of sensors in the I^2C bus)
Design objective	Optimize the # GPIO and component count
Current supply per sensor	5mA, supplied by a microcontroller GPIO

7.2.2.2 Detailed Design Procedure

Select GPIO with current supply capability of 5 mA. Figure 7-12 shows that the SCL, SDA lines and $\overline{INT}$ pin can be shared. However, the function of the $\overline{INT}$ pin must be analyzed when shared by multiple sensors. As an example, if the sensors are configured to generate interrupt through the $\overline{INT}$ pin, the microcontroller needs to read all the sensors to determine which specific one sending the interrupt. Take the following steps sequentially to assign new I^2C addresses to the four TMAG5173-Q1 shown in Figure 7-13:

- Turn on the GPIO#1 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#1 with factory programmed address. Write to the I2C_ADDRESS register to assign a new address.
- Turn on the GPIO#2 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#2 with factory programmed address. Write to the I2C_ADDRESS register to assign a new unique address.
- Turn on the GPIO#3 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#3 with factory programmed address. Write to the I2C_ADDRESS register to assign a new unique address.
- Turn on the GPIO#4 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#4 with factory programmed address. Write to the I2C_ADDRESS register to assign a new unique address.

Repeat the above steps if there is a power outage or power-up reset condition.

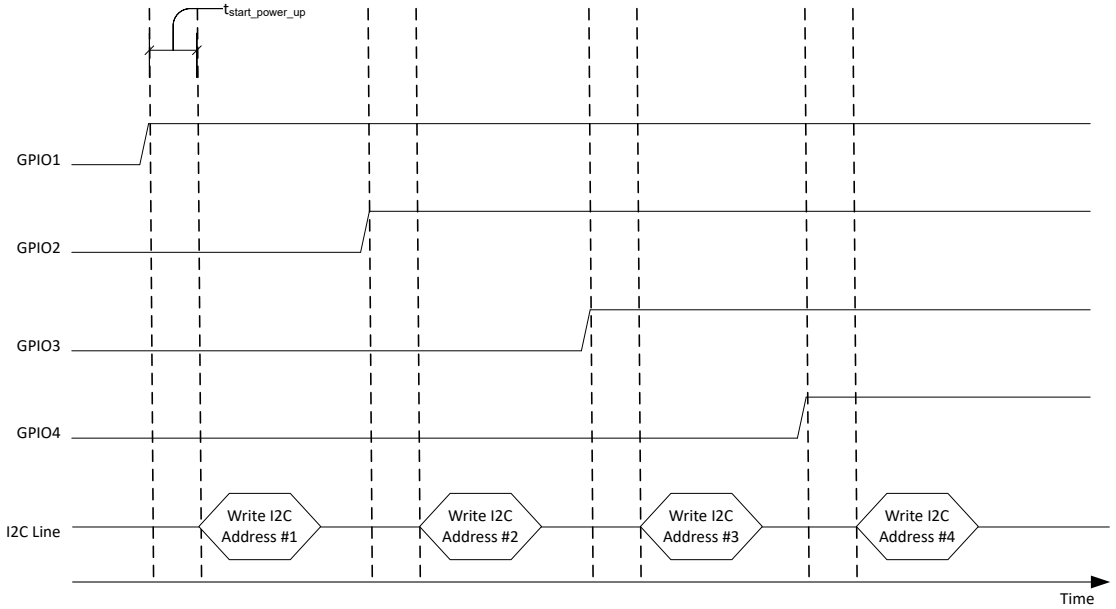


Figure 7-13. Power-Up Timing and I^2C Address Allocation for the Four Sensors

7.3 Best Design Practices

The TMAG5173-Q1 updates the result registers at the end of a conversion. I^2C read of the result register must be synchronized with the conversion update time to avoid reading a result data while the result register is being updated. For applications with a tight timing budget, use the $\overline{INT}$ signal to notify the primary when a conversion is complete.

7.4 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF. Connect the TEST pin to ground.

7.5 Layout

7.5.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

7.5.2 Layout Example

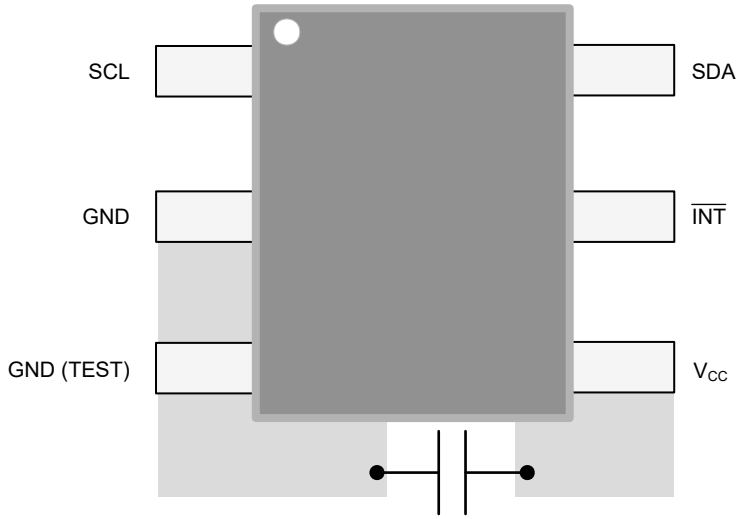


Figure 7-14. Layout Example With TMAG5173-Q1

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HALL-ADAPTER-EVM User's Guide* (SLYU043)
- Texas Instruments, *TMAG5173 Evaluation Manual user's guide* (SLYU058)
- Texas Instruments, *Angle Measurement With Multi-Axis Linear Hall-Effect Sensors* application note (SBAA463)
- Texas Instruments, *Absolute Angle Measurements for Rotational Motion Using Hall-Effect Sensors* application brief (SBAA503)
- Texas Instruments, *Limit Detection for Tamper and End-of-Travel Detection Using Hall-Effect Sensors* application brief (SBOA514)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision A (September 2023) to Revision B (July 2025)	Page
• Added wake-up and sleep mode to description	1
• Updated *Electrical Characteristics* table formatting	6
• Added Wake and Sleep Mode currrent consumption to *Electrical Characteristics* Table	6
• Updated *Temperature Sensor* table formatting	6
• Updated *Magnetic Characteristics For A1, B1, C1, D1* table formatting	8
• Updated *Magnetic Characteristics for A2, B2, C2, D2* table formatting	9
• Updated *Magnetic Temp Compensation Characteristics* table formatting	10
• Updated *Power up Timing* table formatting	11
• Added Wake-up and Sleep functional mode	19
• Added wake-up and sleep mode in figure showing TMAG5173-Q1 operating modes	20

- Added table of examples for magnetic sensor data calculation..... 26
- Added table of examples for temperature sensor data calculation.....26
- Added table of examples for angle and magnitude data calculation..... 27
- Added table of examples for magnetic sensor offset calculation.....29
- Added wake-up and sleep mode to OPERATING_MODE and added SLEEPTIME register..... 30
- Changed *TMAG5173-Q1 Application Diagram for Angle Measurement* image..... 48

Changes from Revision * (September 2022) to Revision A (September 2023)	Page
• Changed data sheet status from Advanced Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

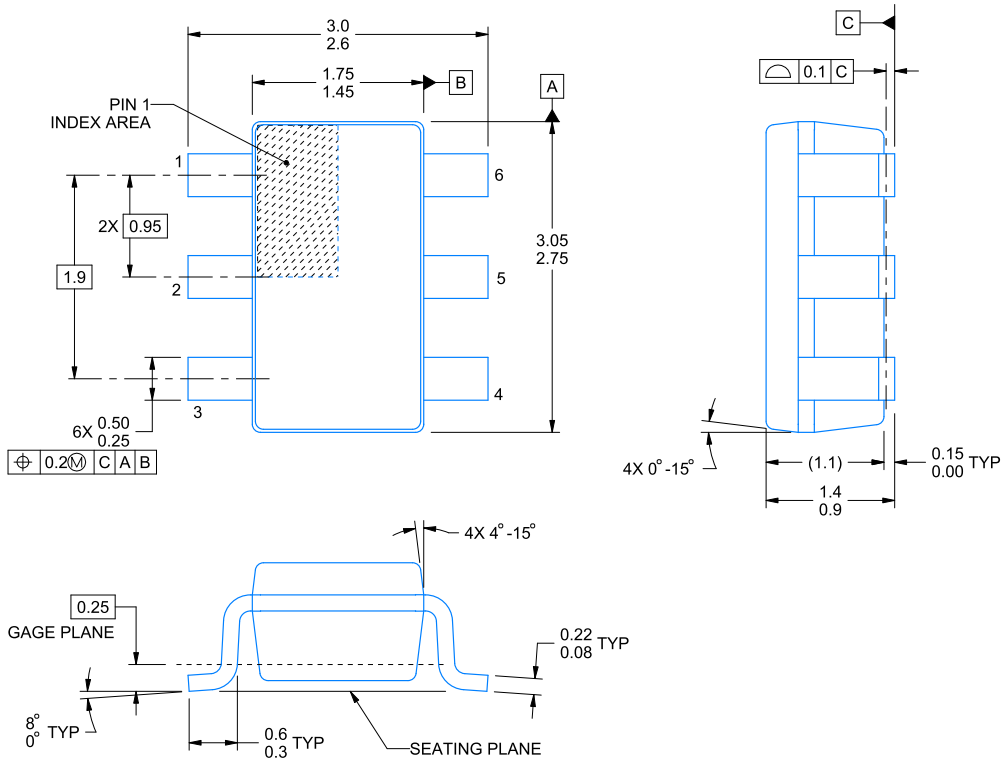
TMAG5173xxx/TMAG5273xxx

DBV0006A-C02

PACKAGE OUTLINE

SOT-23 - 1.4 mm max height

SMALL OUTLINE TRANSISTOR



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

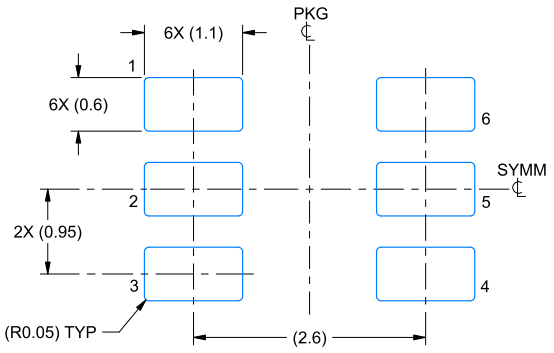
TMAG5173xxx/TMAG5273xxx

DBV0006A-C02

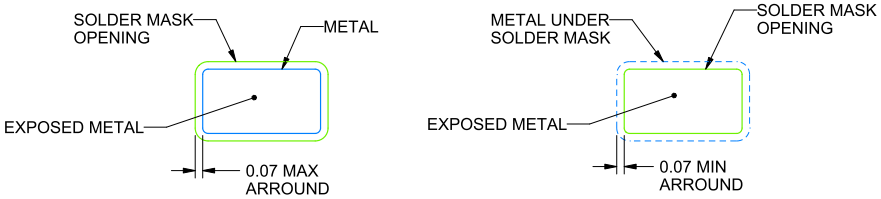
EXAMPLE BOARD LAYOUT

SOT-23 - 1.4 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4231316/A 10/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

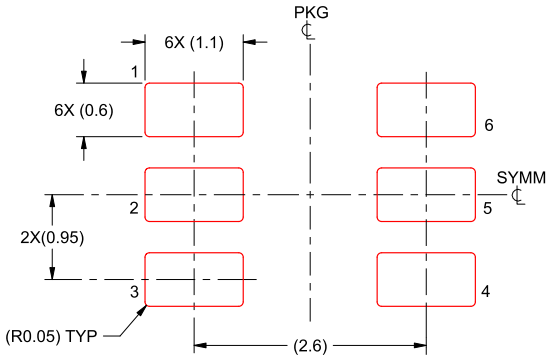
TMAG5173xxx/TMAG5273xxx

DBV0006A-C02

EXAMPLE STENCIL DESIGN

SOT-23 - 1.4 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4231316/A 10/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMAG5173A1QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3A1Q
TMAG5173A1QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173A1QDBVRQ1	3A1Q
TMAG5173A2QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	73A2
TMAG5173A2QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173A2QDBVRQ1	73A2
TMAG5173B1QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	73B1
TMAG5173B1QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173B1QDBVRQ1	73B1
TMAG5173B2QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	73B2
TMAG5173B2QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173B2QDBVRQ1	73B2
TMAG5173C1QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	73C1
TMAG5173C1QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173C1QDBVRQ1	73C1
TMAG5173C2QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	73C2
TMAG5173C2QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173C2QDBVRQ1	73C2
TMAG5173D1QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	73D1
TMAG5173D1QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173D1QDBVRQ1	73D1
TMAG5173D2QDBVRQ1	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	73D2
TMAG5173D2QDBVRQ1.A	Active	Production	null (null) |	3000 | LARGE T&R	-	SN	Level-1-260C-UNLIM	See TMAG5173D2QDBVRQ1	73D2

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

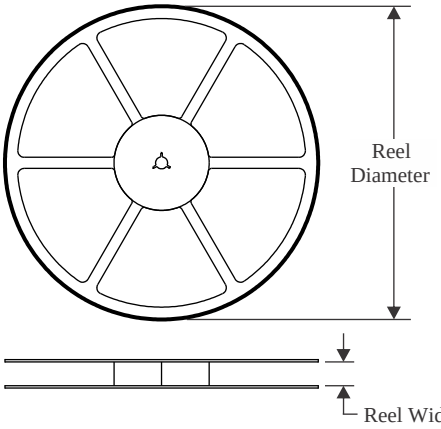
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

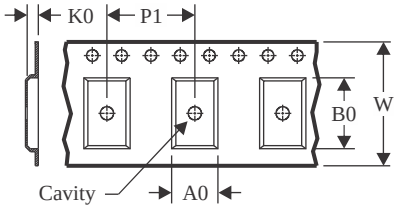
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

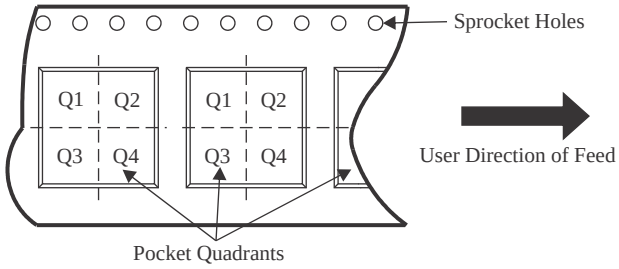


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

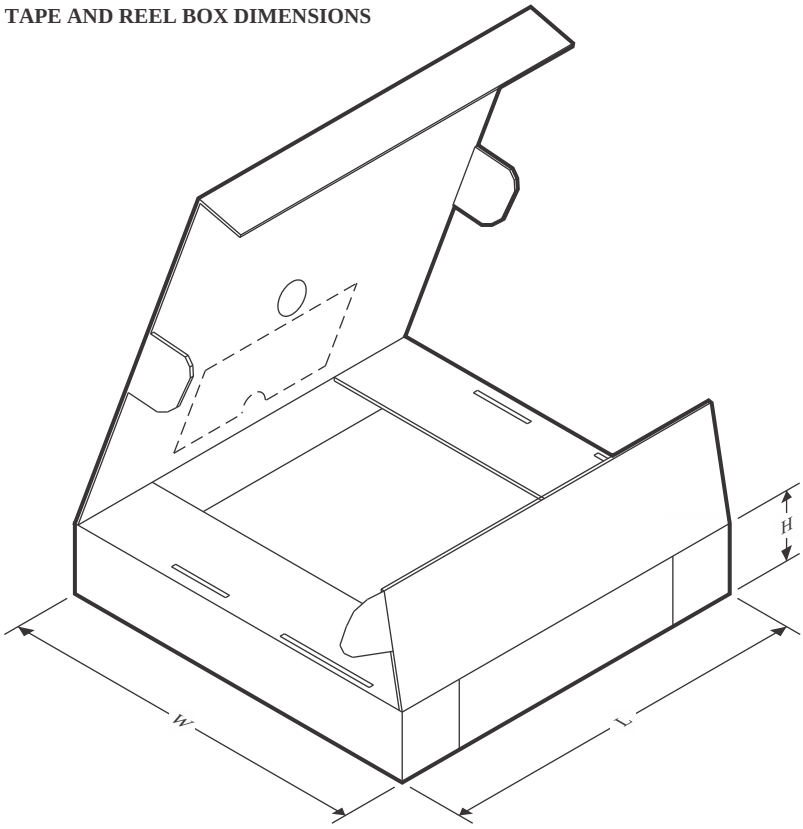
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMAG5173A1QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173A2QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173B1QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173B2QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173C1QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173C2QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173D1QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173D2QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

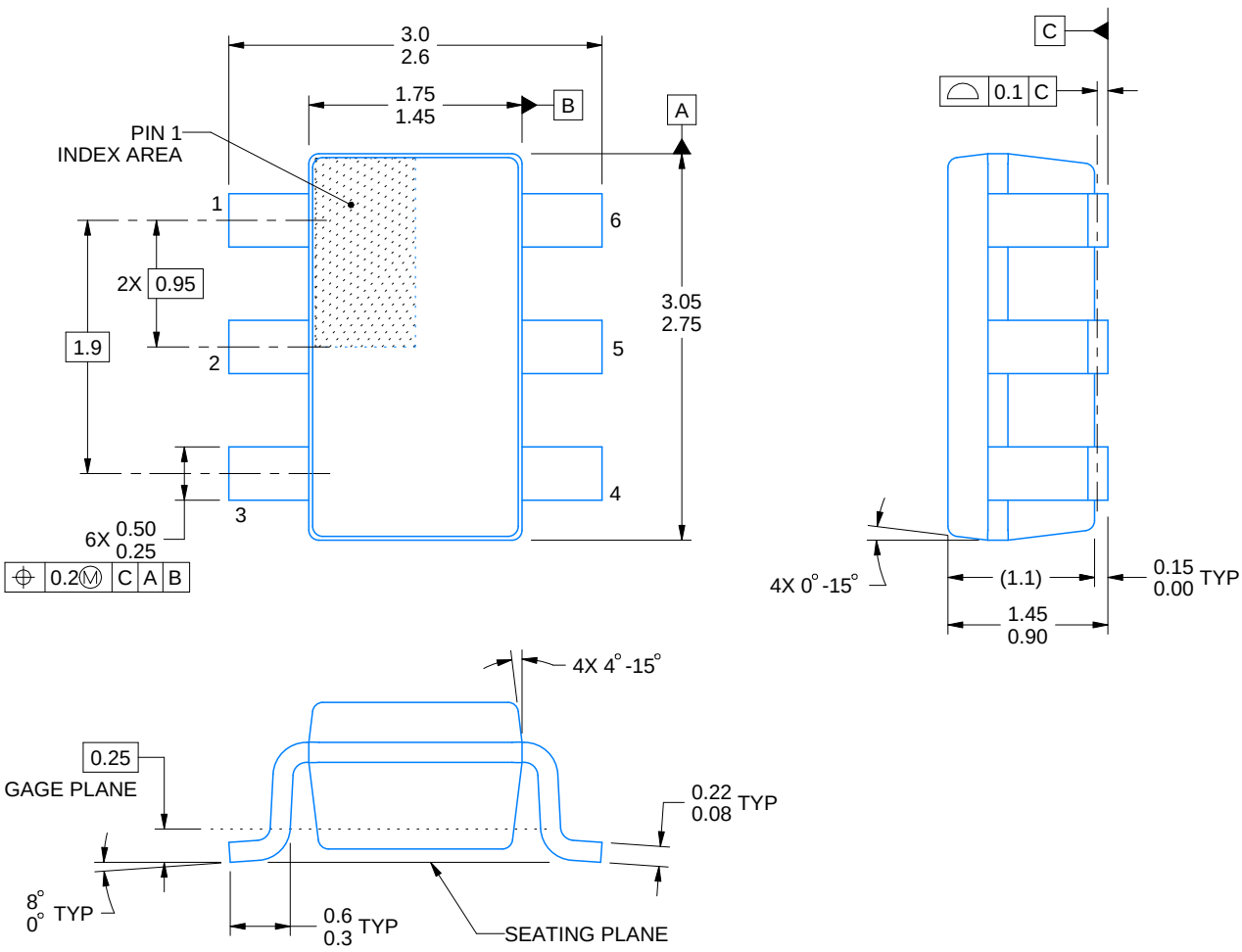
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMAG5173A1QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173A2QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173B1QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173B2QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173C1QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173C2QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173D1QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173D2QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

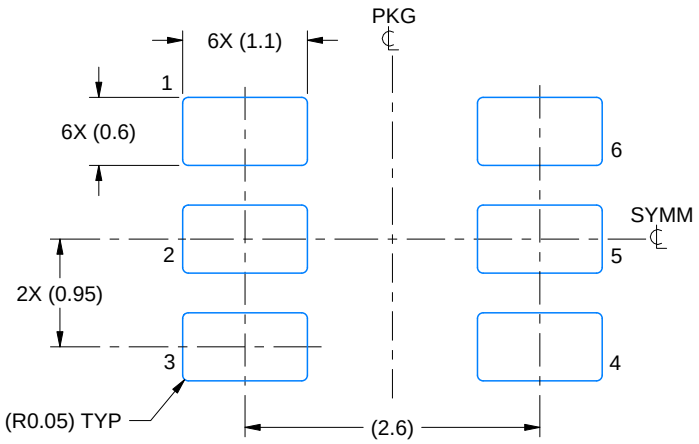
SMALL OUTLINE TRANSISTOR



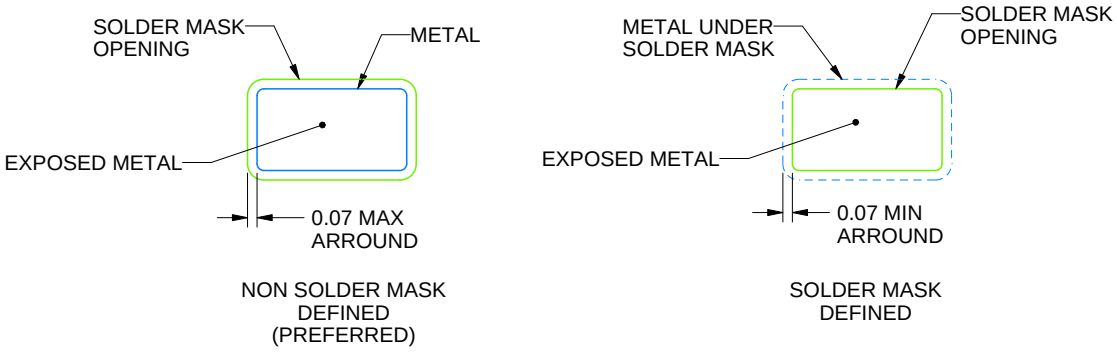
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

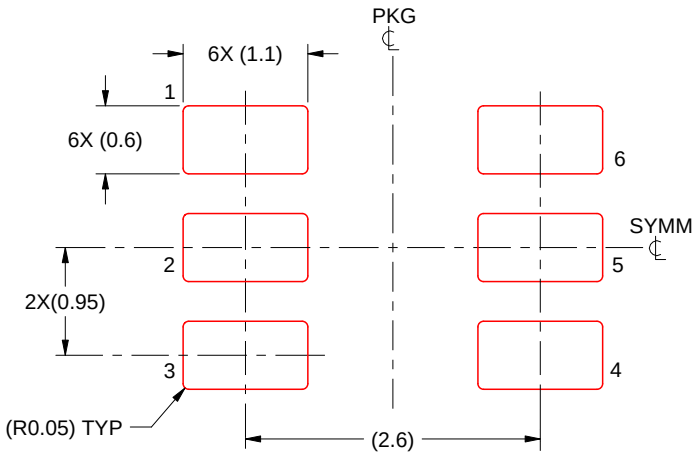


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265