TLV916x-Q1 Automotive 16V, 11MHz, Rail-to-Rail Input or Output, Low Offset Voltage, Low Noise Automotive Op Amp

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level 3A (≥2500V)
  - Device CDM ESD classification level C3 (≥1500V)
- Low offset voltage: ±210µV
- Low offset voltage drift: ±0.25µV/°C
- Low noise: 6.8nV/√Hz at 1kHz, 4.2nV/√Hz broadband
- High common-mode rejection: 110dB
- Low bias current: ±10pA
- Rail-to-rail input and output
- Wide bandwidth: 11MHz GBW, unity-gain stable
- High slew rate: 33V/µs
- Low quiescent current: 2.4mA per amplifier
- Wide supply: ±1.35V to ±8V, 2.7V to 16V
- Robust EMIRR performance

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment and cluster
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- On-board (OBC) and wireless charger
- Powertrain current sensor
- Advanced driver assistance systems (ADAS)
- High-side and low-side current sensing

3 Description

The TLV916x-Q1 family (TLV9161-Q1, TLV9162-Q1, and TLV9164-Q1) is a family of 16V, general-purpose automotive operational amplifiers. These devices offer exceptional DC precision and AC performance, including rail-to-rail input or output, low offset (±210µV, typical), low-offset drift (±0.25µV/°C, typical), and low noise (6.8nV/√Hz at 1kHz, 4.2nV/√Hz at 10kHz).

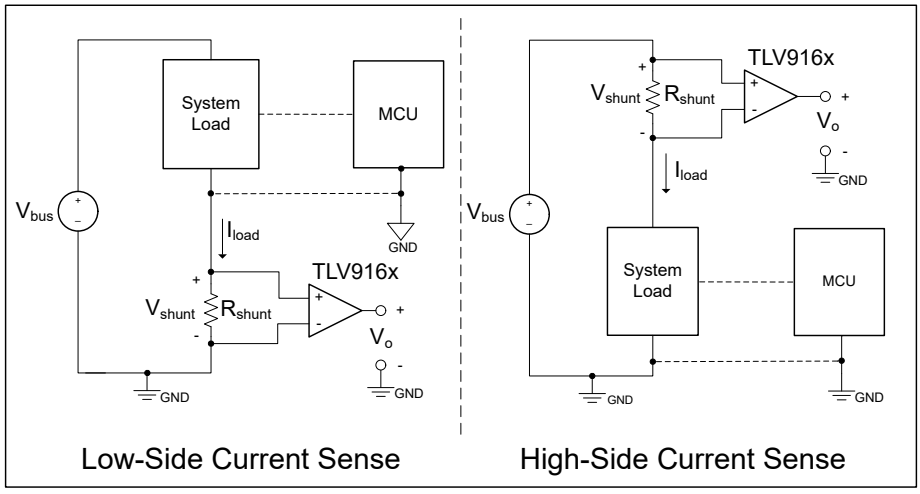
Features such as wide differential input voltage range, high short-circuit current (±73mA), and high slew rate (33V/µs) make the TLV916x-Q1 a flexible, robust, and high-performance op amp for automotive applications.

The TLV916x-Q1 family of op amps is available in standard packages and is specified from –40°C to 125°C.

Package Information

PART NUMBER(1)	CHANNEL COUNT	PACKAGE	PACKAGE SIZE(2)
TLV9161-Q1	Single	DBV (SOT-23, 5)	2.9mm × 2.8mm
		DCK (SC70, 5)	2mm × 2.1mm
TLV9162-Q1	Dual	D (SOIC, 8)	4.9mm × 6mm
		DGK (VSSOP, 8)	3mm × 4.9mm
		PW (TSSOP, 8)	3mm × 6.4mm
TLV9164-Q1	Quad	D (SOIC, 14)	8.65mm × 6mm
		PW (TSSOP, 14)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TLV916x-Q1 in Current-Sensing Applications

Table of Contents

4 Pin Configuration and Functions

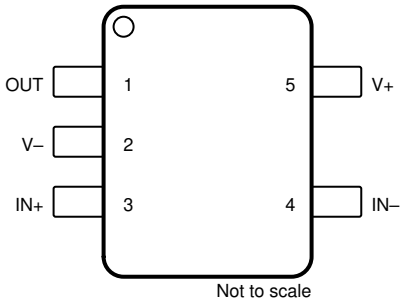


Figure 4-1. TLV9161-Q1 DBV Package, 5-Pin SOT-23 (Top View)

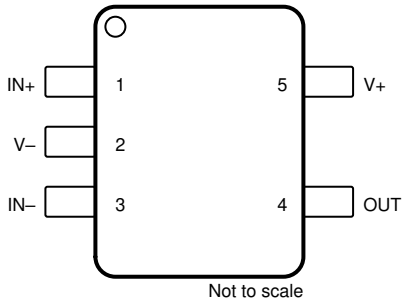


Figure 4-2. TLV9161-Q1 DCK Package, 5-Pin SC70 (Top View)

Table 4-1. Pin Functions: TLV9161-Q1

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23 (DBV)	SC70 (DCK)		
IN+	3	1	I	Noninverting input
IN–	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

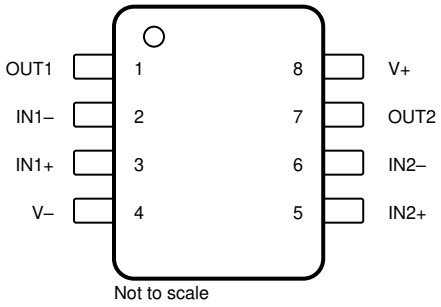


Figure 4-3. TLV9162-Q1 D, PW, and DGK Package, 8-Pin SOIC, TSSOP, and VSSOP (Top View)

Table 4-2. Pin Functions: TLV9162-Q1

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) I = input, O = output

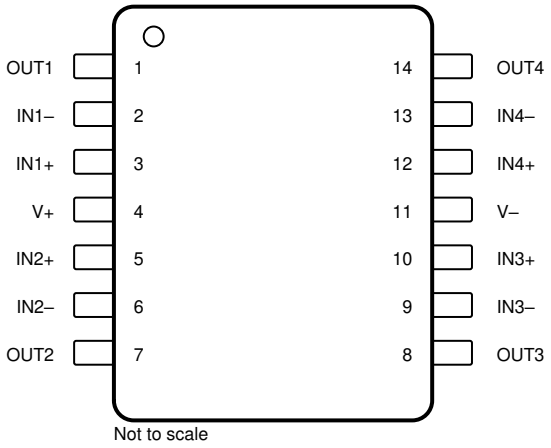


Figure 4-4. TLV9164-Q1 D and PW Package, 14-Pin SOIC and TSSOP (Top View)

Table 4-3. Pin Functions: TLV9164-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	20	V
Signal input pins	Common-mode voltage(3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current(3)	–10	10	mA
Shutdown pin voltage		V–	V+	
Output short-circuit(2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
TLV9161-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	
TLV9162-Q1 and TLV9164-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	16	V
V_I	Common mode voltage range	V–	V+	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Single Channel

THERMAL METRIC[1]		TLV9161-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.3	202.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.8	111.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	51.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.6	25.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.5	51.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Thermal Information for Dual Channel

THERMAL METRIC[1]		TLV9162-Q1			Unit
		D (SOIC)	PW (TSSOP)	DGK (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	130.8	159.1	173.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.0	67.9	65.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.3	98.1	95.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.8	9.1	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	73.5	96.7	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Thermal Information for Quad Channel

THERMAL METRIC[1]		TLV9164-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.9	120.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.1	50.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.4	63.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.3	8.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.0	62.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7V to 16V (±1.35V to ±8V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.21	±1.03	mV
			T_A = –40°C to 125°C			±1.2	
dV_{OS}/dT	Input offset voltage drift	V_{CM} = V–	T_A = –40°C to 125°C		±0.25		µV/°C
PSRR	Input offset voltage versus power supply	TLV9161-Q1, TLV9162-Q1, V_{CM} = V–, V_S = 5V to 16V			±0.45	±2	µV/V
		TLV9161-Q1, TLV9162-Q1 D and DGK packages V_{CM} = V–, V_S = 5V to 16V	T_A = –40°C to 125°C		±0.45	±3	
		TLV9162-Q1 PW package V_{CM} = V–, V_S = 5V to 16V	T_A = –40°C to 125°C		±0.45	±3.8	
		TLV9164-Q1, V_{CM} = V–, V_S = 5V to 16V			±0.45	±2.2	
			T_A = –40°C to 125°C		±0.45	±3.8	
		TLV9161-Q1, TLV9162-Q1, TLV9164-Q1, V_{CM} = V–, V_S = 2.7V to 16V[1]	T_A = –40°C to 125°C		±2	±12	
	DC channel separation				0.4		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			2.7		μV_{PP}
					0.49		μV_{RMS}
e_N	Input voltage noise density	f = 1kHz			6.8		$nV/\sqrt{Hz}$
		f = 10kHz			4.2		
i_N	Input current noise density	f = 1kHz			55		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	V_S = 16V, V– < V_{CM} < (V+) – 2V (PMOS pair)	T_A = –40°C to 125°C	85	110		dB
		V_S = 5V, V– < V_{CM} < (V+) – 2V (PMOS pair)[1]		75	98		
		V_S = 2.7V, V– < V_{CM} < (V+) – 2V (PMOS pair)			90		
		V_S = 2.7 – 16V, (V+) – 1V < V_{CM} < V+ (NMOS pair)			78		
		(V+) – 2V < V_{CM} < (V+) – 1V		See Figure 5-6			
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 9		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 16V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V		120	136		dB
			T_A = –40°C to 125°C		136		
		V_S = 5V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V[1]		104	125		
			T_A = –40°C to 125°C		125		
		V_S = 2.7V, V_{CM} = V_S / 2, (V–) + 0.1V < V_O < (V+) – 0.1V[1]		90	105		
			T_A = –40°C to 125°C		105		

5.7 Electrical Characteristics (continued)

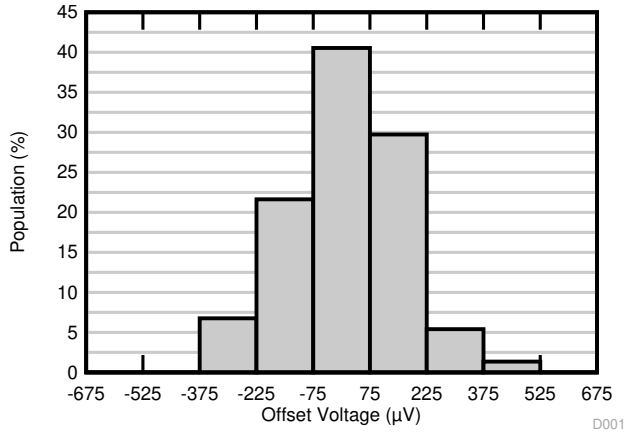
For V_S = (V+) – (V–) = 2.7V to 16V (±1.35V to ±8V) at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				11		MHz
SR	Slew rate	V_S = 16V, G = +1, V_{STEP} = 10V, C_L = 20pF(2)			33		V/µs
t_S	Settling time	To 0.1%, V_S = 16V, V_{STEP} = 10V, G = +1, C_L = 20pF			0.70		µs
		To 0.1%, V_S = 16V, V_{STEP} = 2V, G = +1, C_L = 20pF			0.22		
		To 0.01%, V_S = 16V, V_{STEP} = 10V, G = +1, C_L = 20pF			0.89		
		To 0.01%, V_S = 16V, V_{STEP} = 2V, G = +1, C_L = 20pF			0.42		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			64		°
	Overload recovery time	V_{IN} × gain > V_S			120		ns
THD+N	Total harmonic distortion + noise	V_S = 16V, V_O = 3V_{RMS}, G = 1, f = 1kHz			0.00005%		
					126		dB
		V_S = 10V, V_O = 3V_{RMS}, G = 1, f = 1kHz, R_L = 128Ω			0.0032%		
					90		dB
		V_S = 10V, V_O = 0.4V_{RMS}, G = 1, f = 1kHz, R_L = 32Ω			0.00032%		
					110		dB
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 16V, R_L = no load		6		mV
			V_S = 16V, R_L = 10kΩ		25	60	
			V_S = 16V, R_L = 2kΩ		85	300	
			V_S = 2.7V, R_L = no load		0.5		
			V_S = 2.7V, R_L = 10kΩ		5	20	
			V_S = 2.7V, R_L = 2kΩ		20	50	
I_{SC}	Short-circuit current				±73		mA
C_{LOAD}	Capacitive load drive				See Figure 5-33		pF
Z_O	Open-loop output impedance	I_O = 0A			See Figure 5-30		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	TLV9162-Q1, TLV9164-Q1, I_O = 0A			2.4	2.8	mA
			T_A = –40°C to 125°C			2.84	
		TLV9161-Q1, I_O = 0A			2.48	2.92	
			T_A = –40°C to 125°C			2.98	

(1) Specified by characterization only.
(2) See Figure 5-15 for more information.

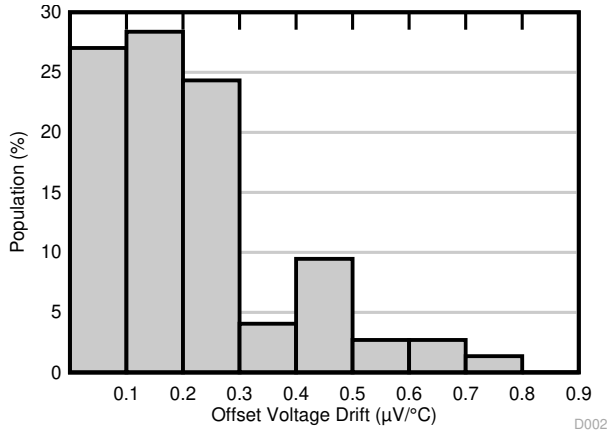
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



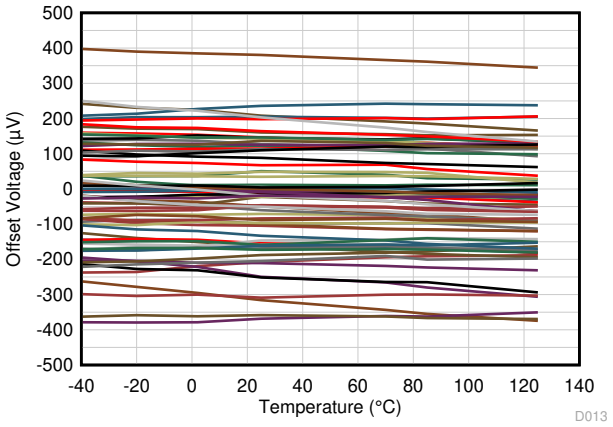
Distribution from 74 amplifiers, T_A = 25°C

Figure 5-1. Offset Voltage Production Distribution



Distribution from 74 amplifiers

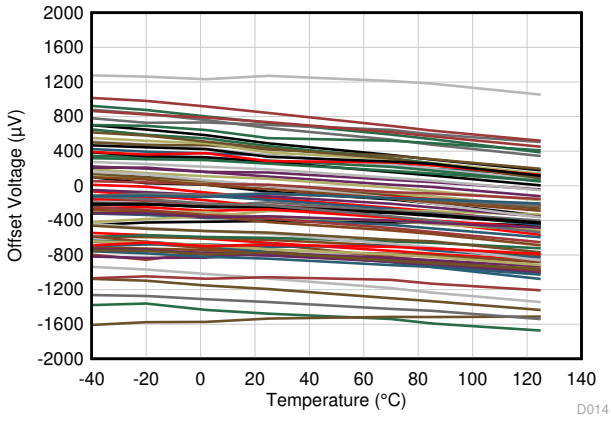
Figure 5-2. Offset Voltage Drift Distribution



V_{CM} = V–

Data from 74 amplifiers

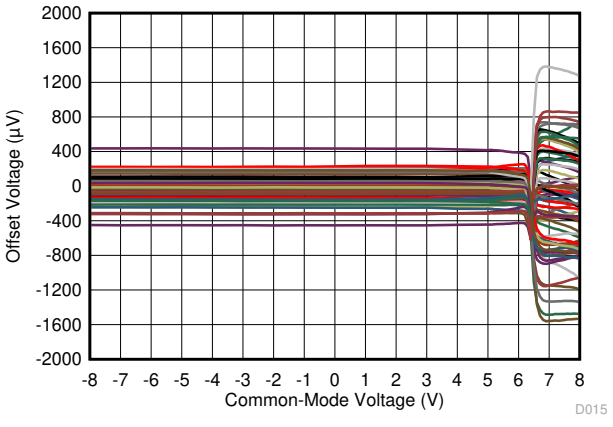
Figure 5-3. Offset Voltage vs Temperature



V_{CM} = V+

Data from 74 amplifiers

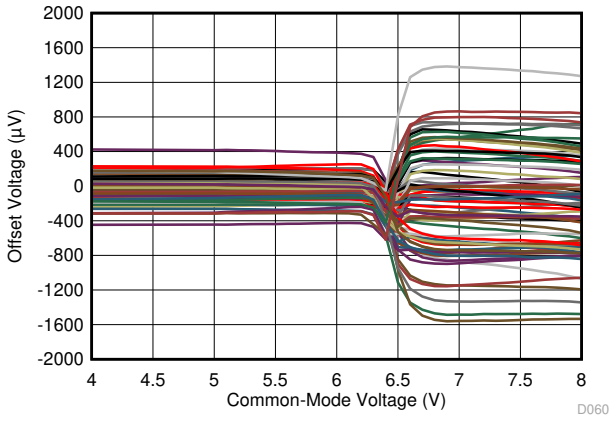
Figure 5-4. Offset Voltage vs Temperature



T_A = 25°C

Data from 74 amplifiers

Figure 5-5. Offset Voltage vs Common-Mode Voltage



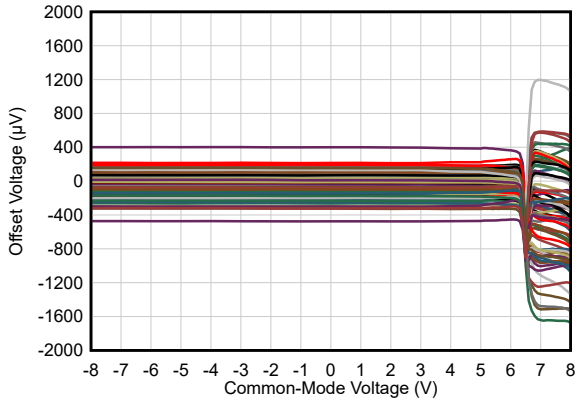
T_A = 25°C

Data from 74 amplifiers

Figure 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

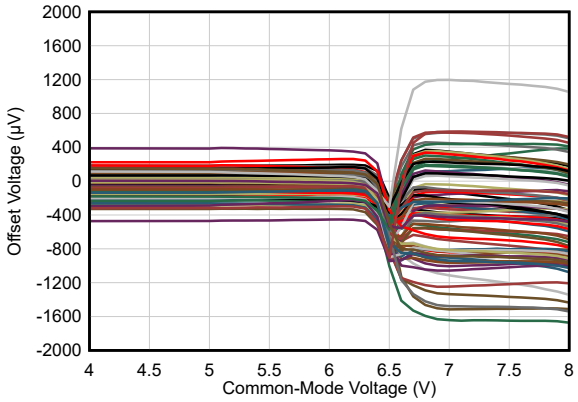
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



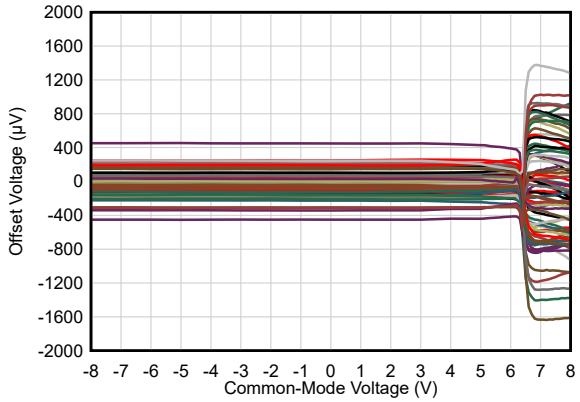
T_A = 125°C
Data from 74 amplifiers

Figure 5-7. Offset Voltage vs Common-Mode Voltage



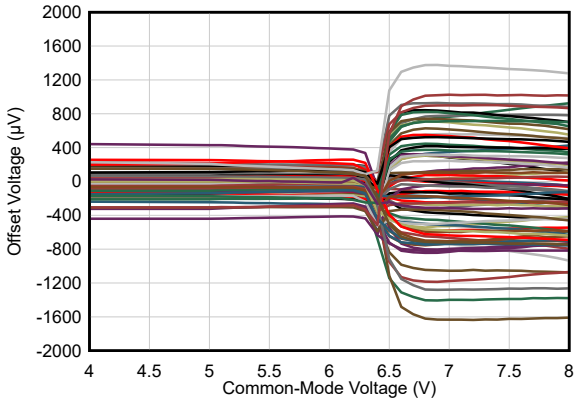
T_A = 125°C
Data from 74 amplifiers

Figure 5-8. Offset Voltage vs Common-Mode Voltage (Transition Region)



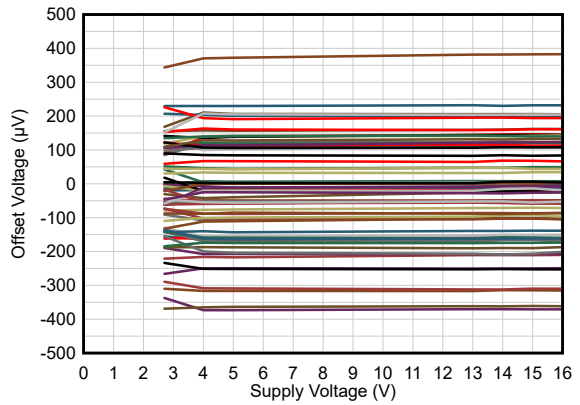
T_A = –40°C
Data from 74 amplifiers

Figure 5-9. Offset Voltage vs Common-Mode Voltage



T_A = –40°C
Data from 74 amplifiers

Figure 5-10. Offset Voltage vs Common-Mode Voltage (Transition Region)



V_{CM} = V–
Data from 74 amplifiers

Figure 5-11. Offset Voltage vs Power Supply

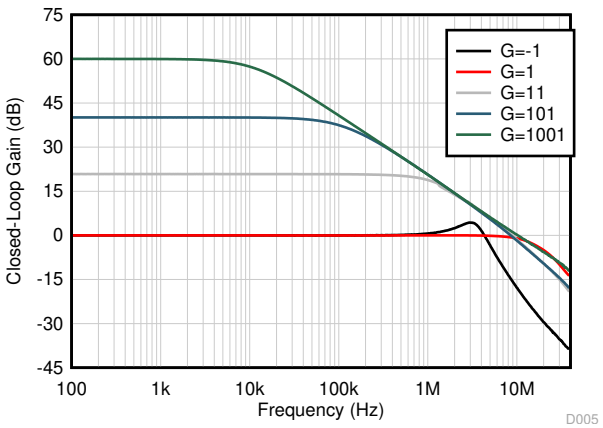
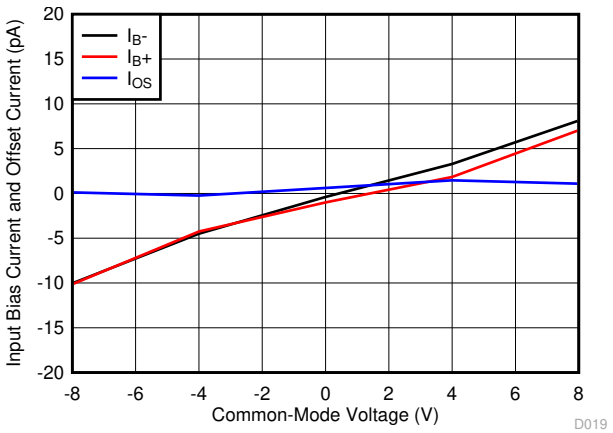


Figure 5-12. Closed-Loop Gain vs Frequency

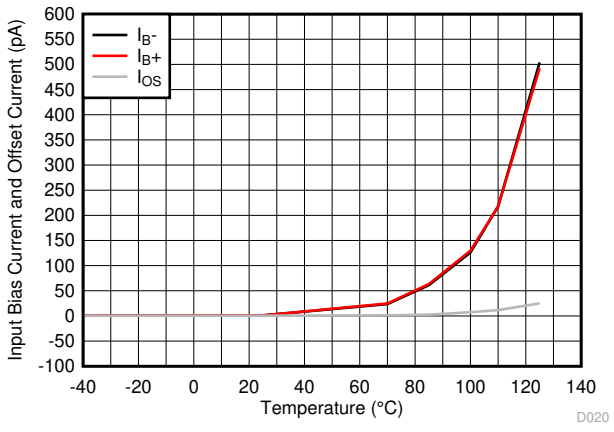
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



No Load

Figure 5-13. Input Bias Current and Offset Current vs Common-Mode Voltage



No Load

Figure 5-14. Input Bias Current and Offset Current vs Temperature

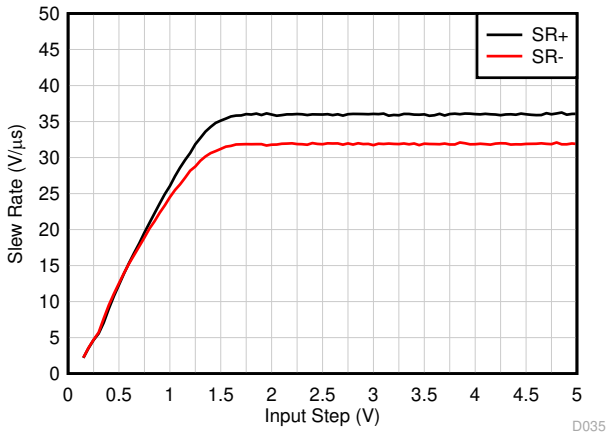
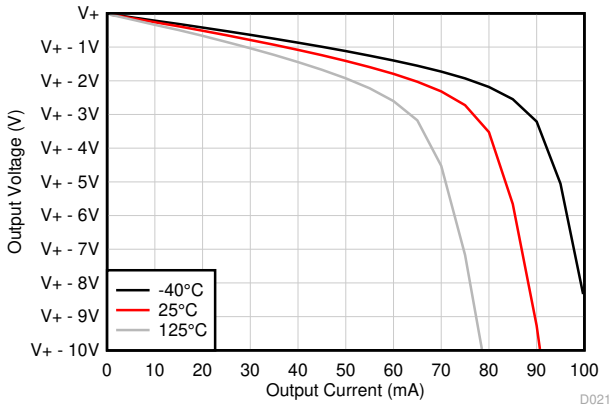
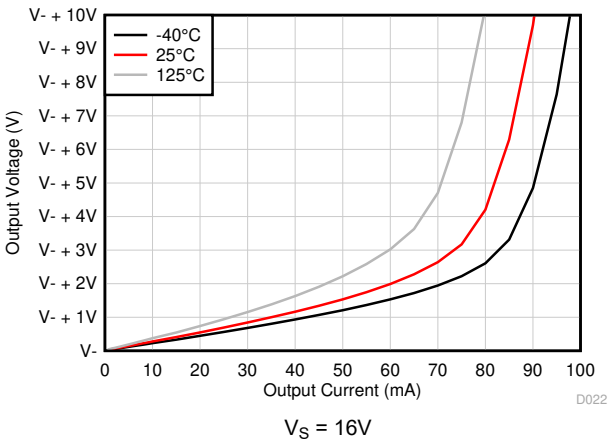


Figure 5-15. Slew Rate vs Input Step Voltage



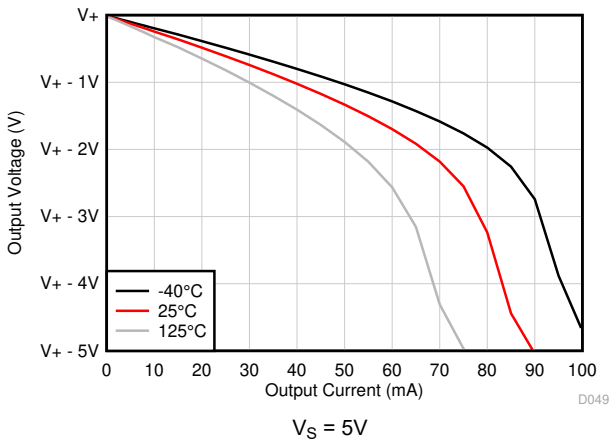
V_S = 16V

Figure 5-16. Output Voltage Swing vs Output Current (Sourcing)



V_S = 16V

Figure 5-17. Output Voltage Swing vs Output Current (Sinking)

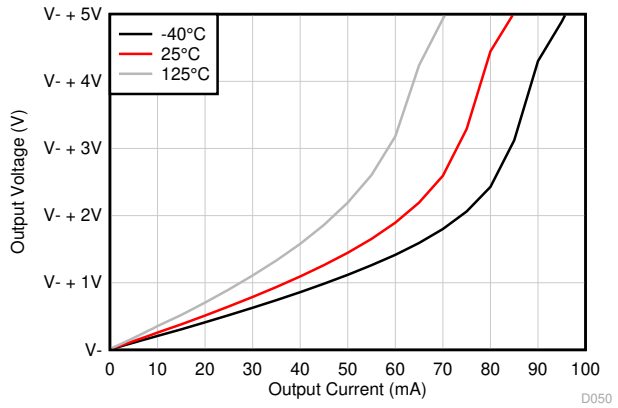


V_S = 5V

Figure 5-18. Output Voltage Swing vs Output Current (Sourcing)

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



V_S = 5V

Figure 5-19. Output Voltage Swing vs Output Current (Sinking)

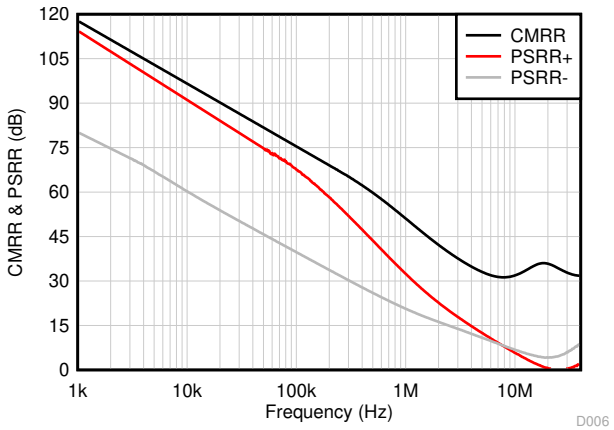
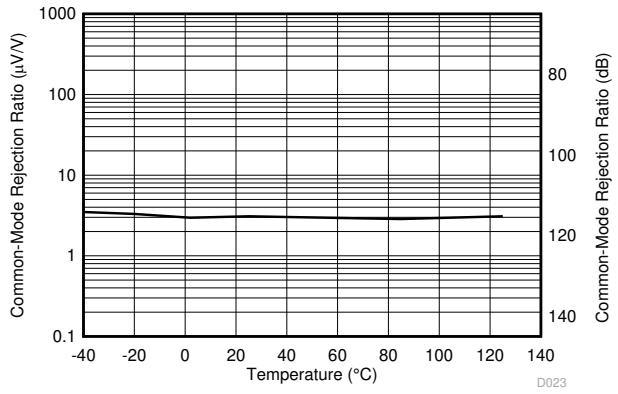
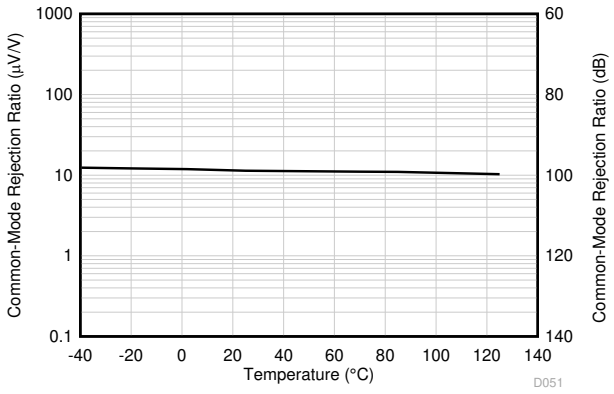


Figure 5-20. CMRR and PSRR vs Frequency



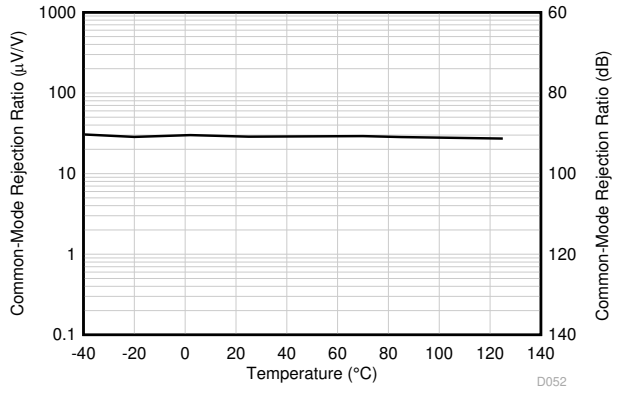
V_S = 16V, V_{CM} = V–

Figure 5-21. CMRR vs Temperature



V_S = 5V, V_{CM} = V–

Figure 5-22. CMRR vs Temperature



V_S = 2.7V, V_{CM} = V–

Figure 5-23. CMRR vs Temperature

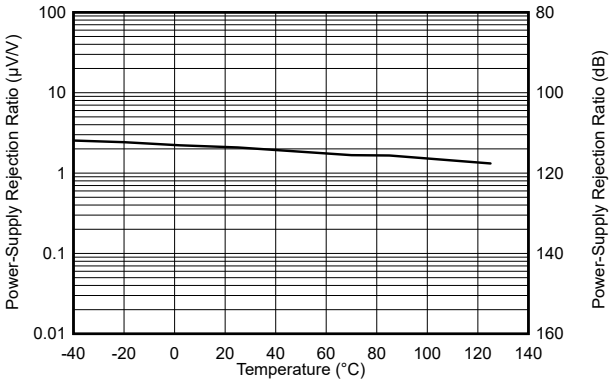


Figure 5-24. PSRR vs Temperature

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)

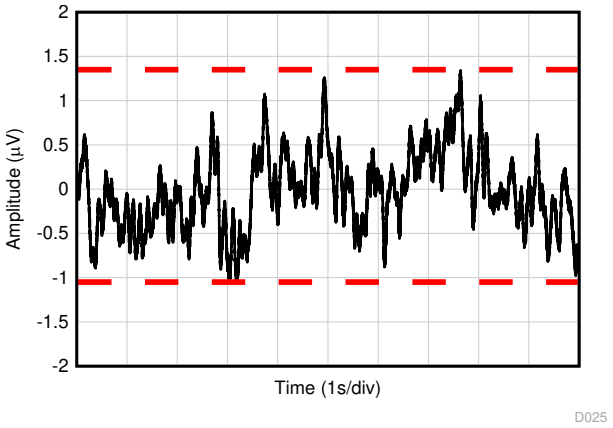


Figure 5-25. 0.1Hz to 10Hz Noise

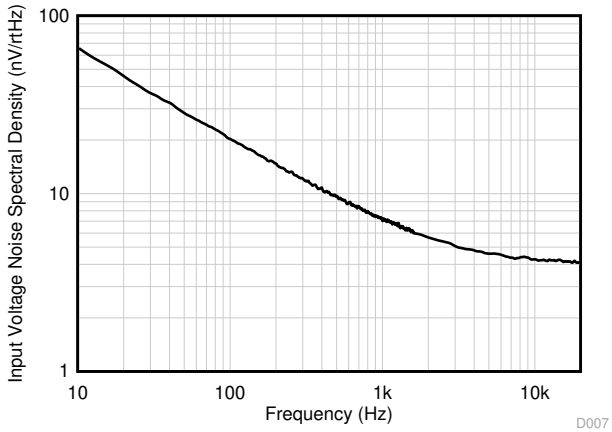
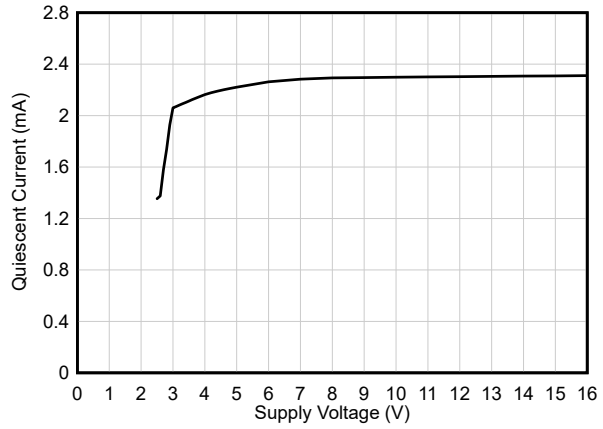
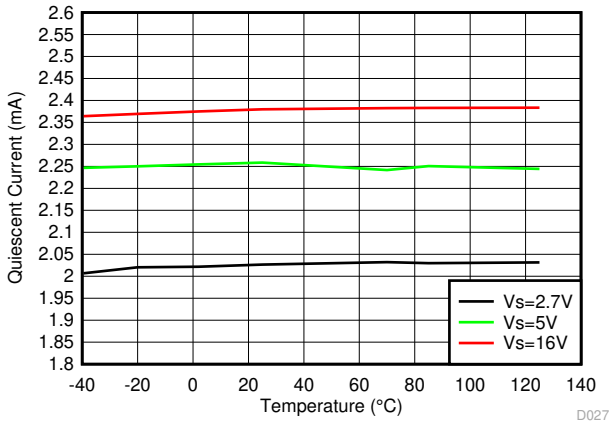


Figure 5-26. Input Voltage Noise Spectral Density vs Frequency



V_{CM} = V–

Figure 5-27. Quiescent Current vs Supply Voltage



V_{CM} = V–

Figure 5-28. Quiescent Current vs Temperature

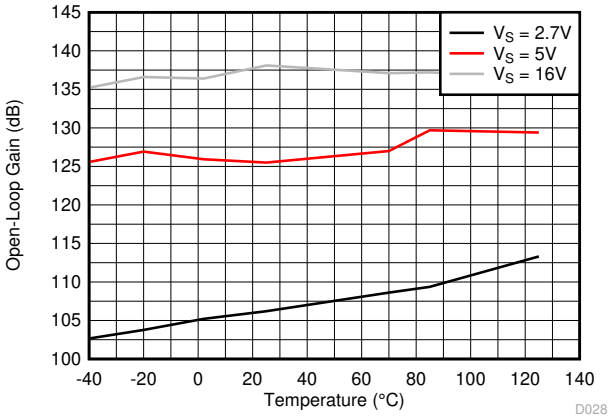


Figure 5-29. Open-Loop Voltage Gain vs Temperature (dB)

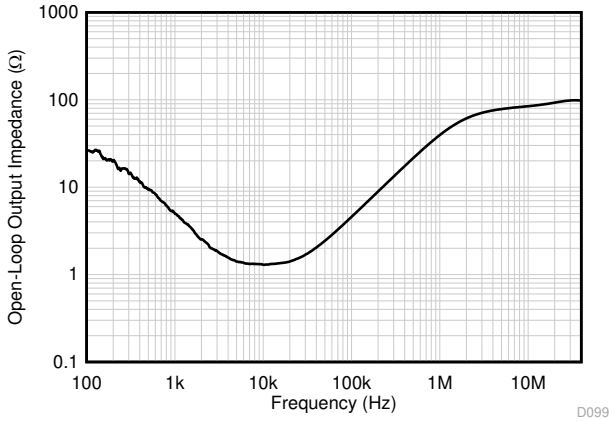
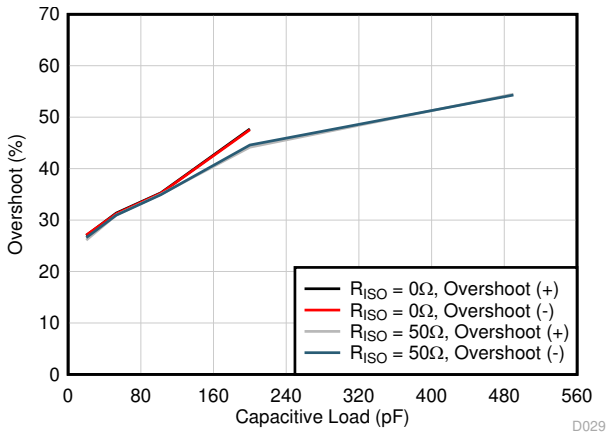


Figure 5-30. Open-Loop Output Impedance vs Frequency

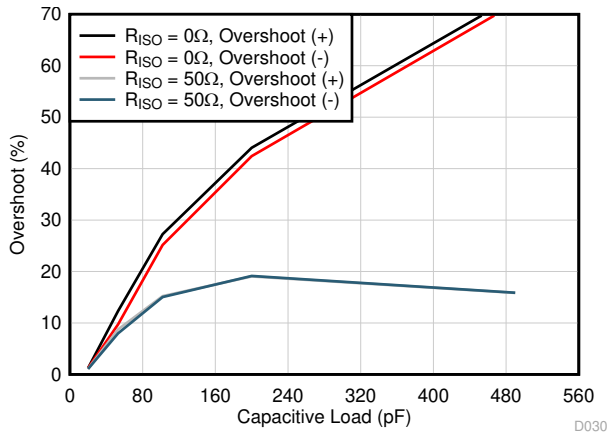
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



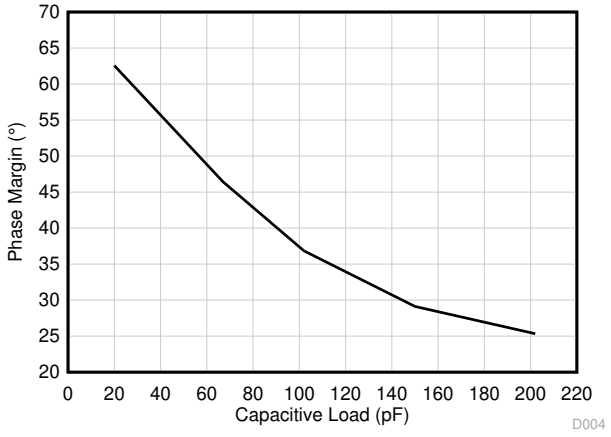
20mV$_{pp}$ output step, G = –1

Figure 5-31. Small-Signal Overshoot vs Capacitive Load



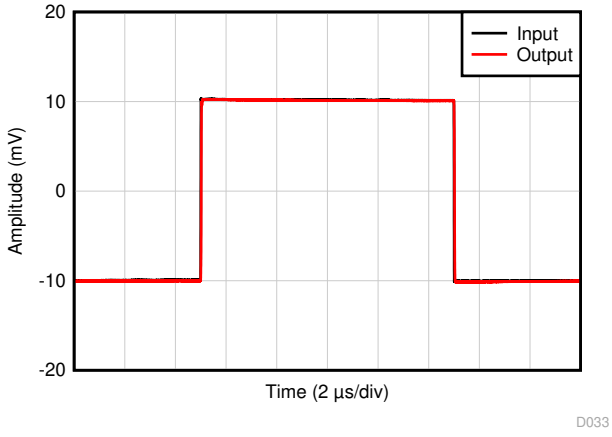
20mV$_{pp}$ output step, G = +1

Figure 5-32. Small-Signal Overshoot vs Capacitive Load



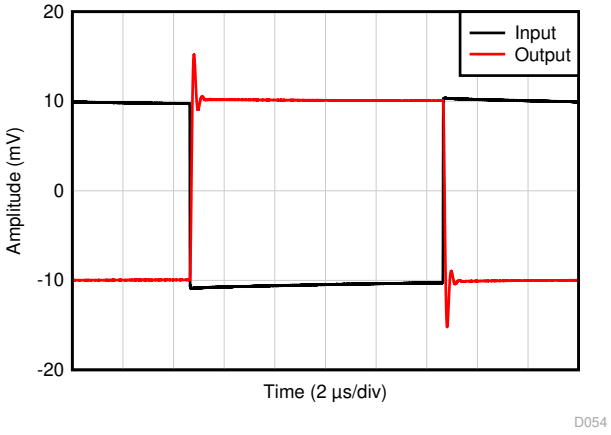
G = +1

Figure 5-33. Phase Margin vs Capacitive Load



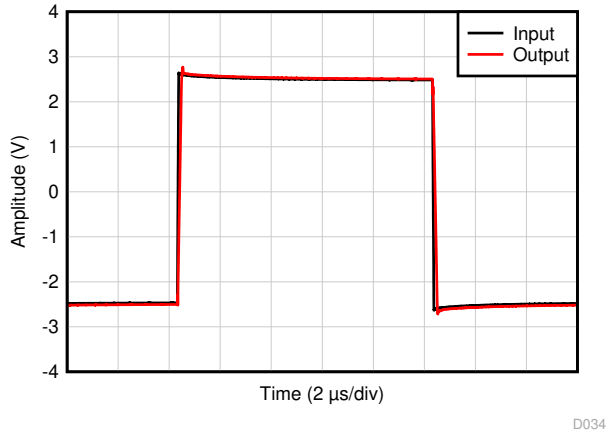
C_L = 20pF, G = 1, 20mV$_{pp}$ step response

Figure 5-34. Small-Signal Step Response



C_L = 20pF, G = –1, 20mV$_{pp}$ step response

Figure 5-35. Small-Signal Step Response

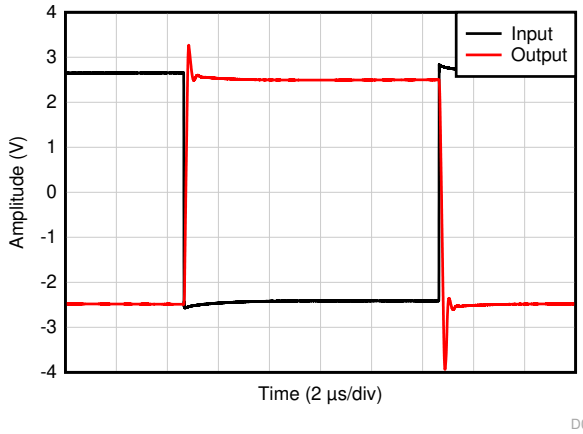


C_L = 20pF, G = 1, 5V$_{pp}$ step response

Figure 5-36. Large-Signal Step Response

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ (unless otherwise noted)



C_L = 20pF, G = –1, $5V_{pp}$ step response

Figure 5-37. Large-Signal Step Response

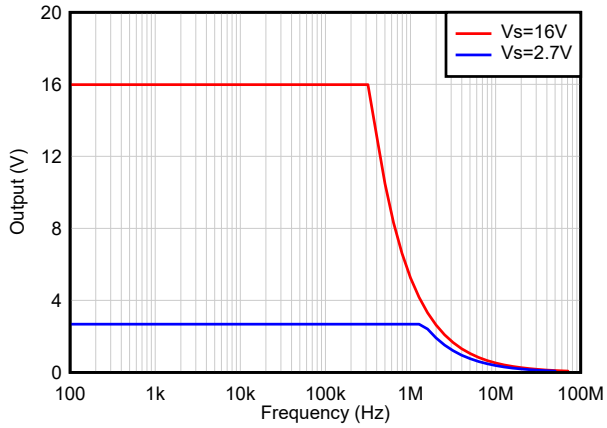


Figure 5-38. Maximum Output Voltage vs Frequency

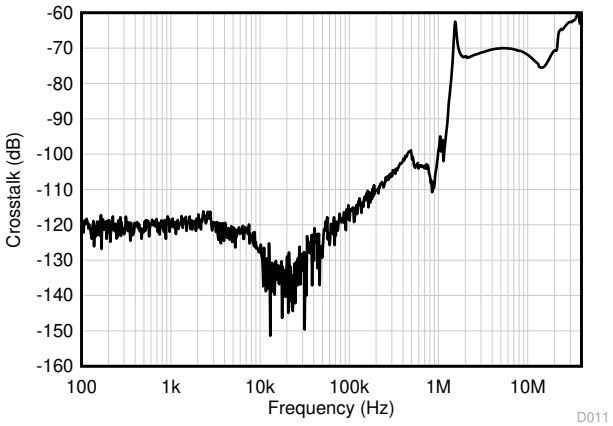


Figure 5-39. Channel Separation vs Frequency

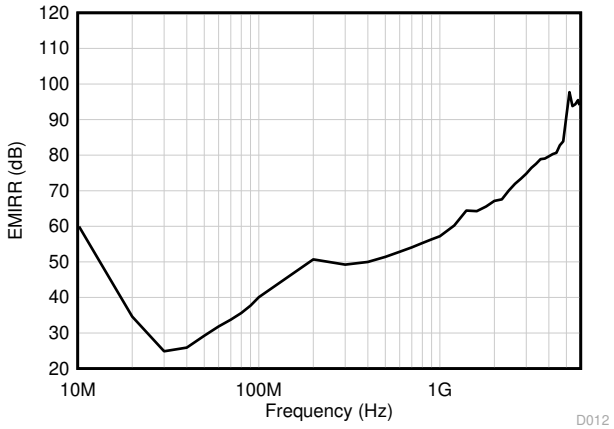


Figure 5-40. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Detailed Description

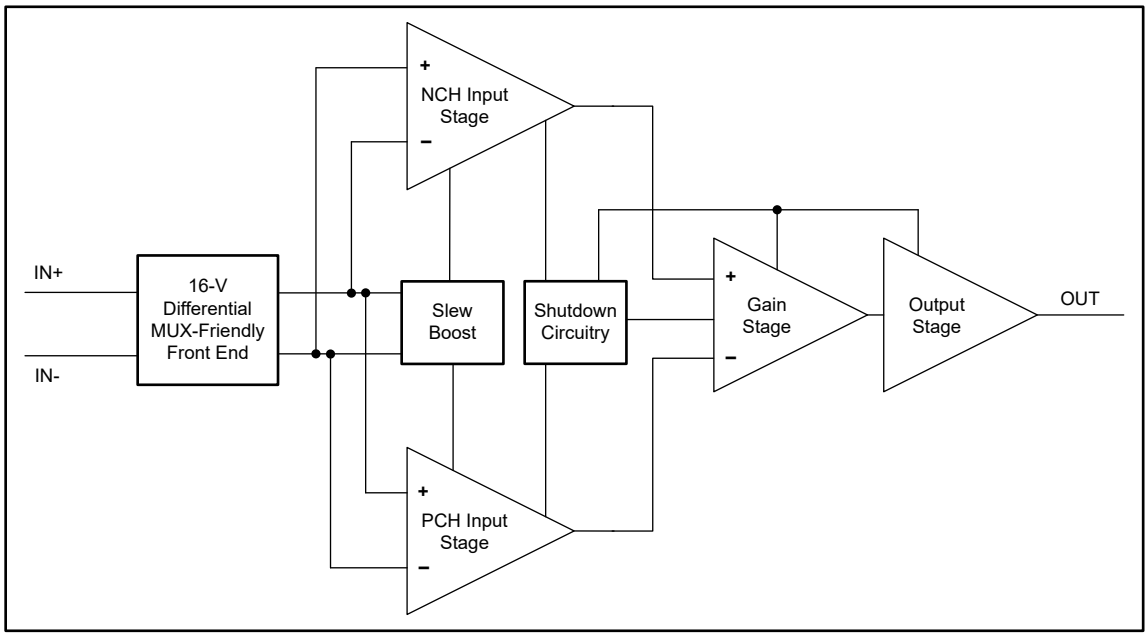
6.1 Overview

The TLV916x-Q1 family (TLV9161-Q1, TLV9162-Q1, and TLV9164-Q1) is a family of 16V, general-purpose, automotive operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input or output, low offset (±210µV, typical), low offset drift (±0.25µV/°C, typical), and 11MHz bandwidth.

Features such as wide differential input range, high short-circuit current (±73mA), and high slew rate (33V/µs) make the TLV916x-Q1 a flexible, robust, and high-performance operational amplifier for 16V automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Protection Circuitry

The TLV916x-Q1 uses a special input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

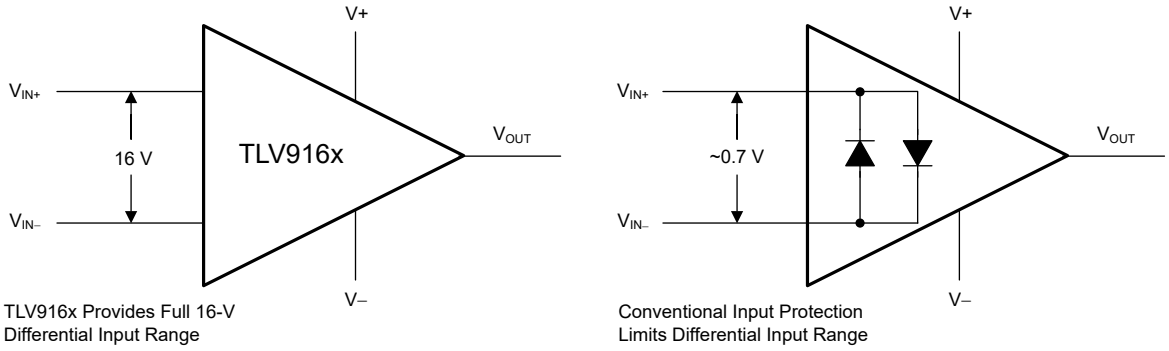


Figure 6-1. TLV916x-Q1 Input Protection Does Not Limit Differential Input Capability

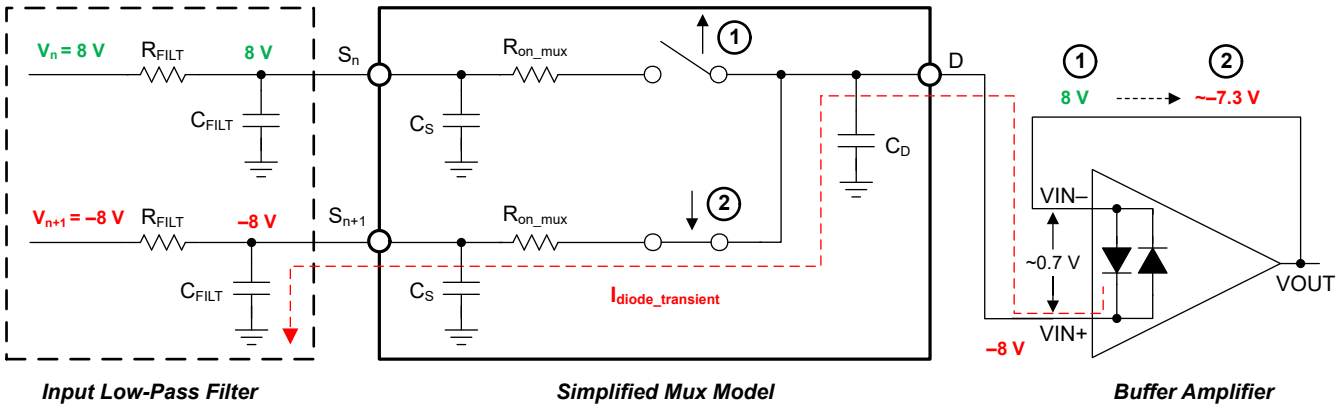


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The TLV916x-Q1 family of operational amplifiers provides a true high-impedance differential input capability using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The TLV916x-Q1 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 16V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

6.3.2 EMI Rejection

The TLV916x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV916x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-3 shows the results of this testing on the TLV916x-Q1. Table 6-1 provides the EMIRR IN+ values for the TLV916x-Q1 at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

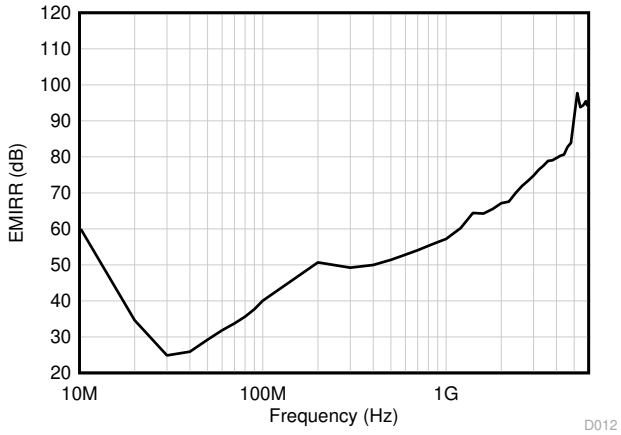


Figure 6-3. EMIRR Testing

Table 6-1. TLV9161-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	50.0dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	56.3dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	65.6dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	70.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	78.9dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	91.0dB

6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV916x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV916x-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. Figure 6-4 shows an application example for the TLV9162-Q1 that has significant self heating because of its power dissipation (0.627W). In this example, both channels have a quiescent power dissipation while one of the channels has a significant load. Thermal calculations indicate that for an ambient temperature of 60°C, the device junction temperature reaches 175°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. Figure 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 5V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor R_L. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected. Please note that thermal performance can vary greatly depending on the package selected and the PCB layout design. This example uses the thermal performance of the TSSOP (8) package.

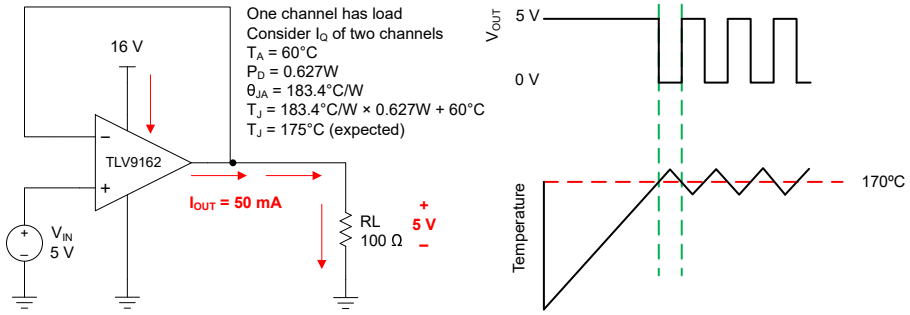


Figure 6-4. Thermal Protection

6.3.4 Capacitive Load and Stability

The TLV916x-Q1 features an output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive larger capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 6-5 and Figure 6-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

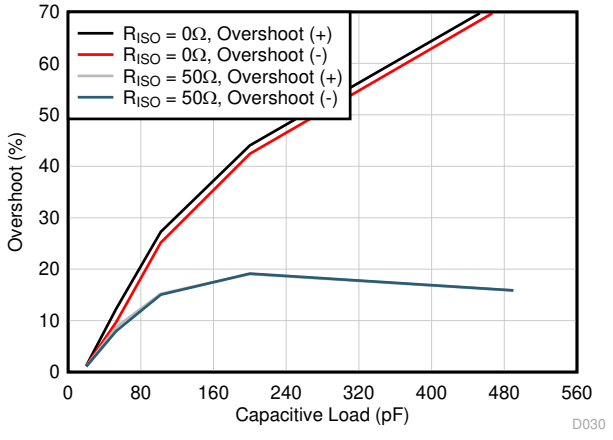


Figure 6-5. Small-Signal Overshoot vs Capacitive Load (20mV$_{pp}$ Output Step, G = +1)

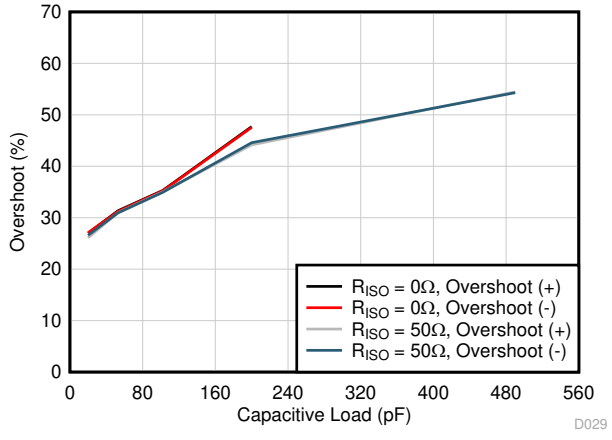


Figure 6-6. Small-Signal Overshoot vs Capacitive Load (20mV$_{pp}$ Output Step, G = -1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, R_{ISO}, in series with the output, as shown in Figure 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the TLV916x-Q1 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 6-7 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

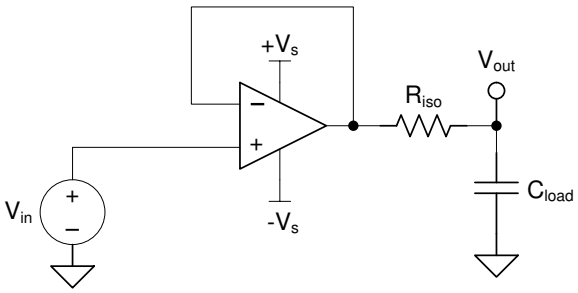


Figure 6-7. Extending Capacitive Load Drive With the TLV9161-Q1

6.3.5 Common-Mode Voltage Range

The TLV916x-Q1 is a 16V, rail-to-rail input operational amplifier with an input common-mode range that extends to both supply rails. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6-8. The N-channel pair is active for input voltages close to the positive rail, typically from (V+) – 1V to the positive supply. The P-channel pair is active for inputs from the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) – 2V to (V+) – 1V in which both input pairs are on. This transition region can vary modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

Figure 5-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.

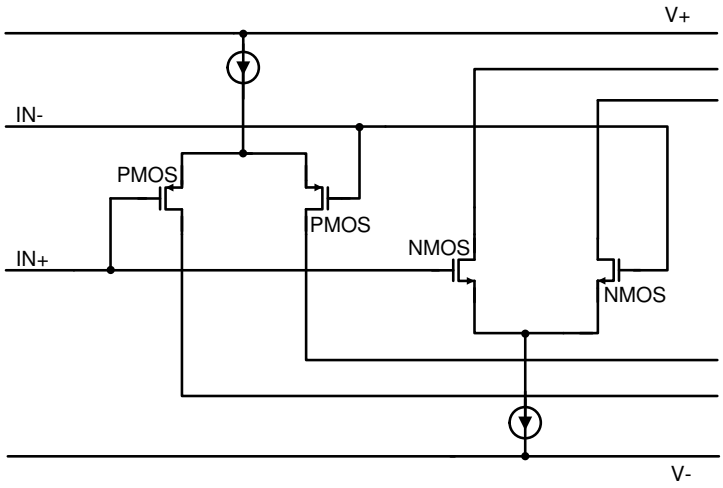


Figure 6-8. Rail-to-Rail Input Stage

6.3.6 Phase Reversal Protection

The TLV916x-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV916x-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-9 shows an illustration of the ESD circuits contained in the TLV916x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

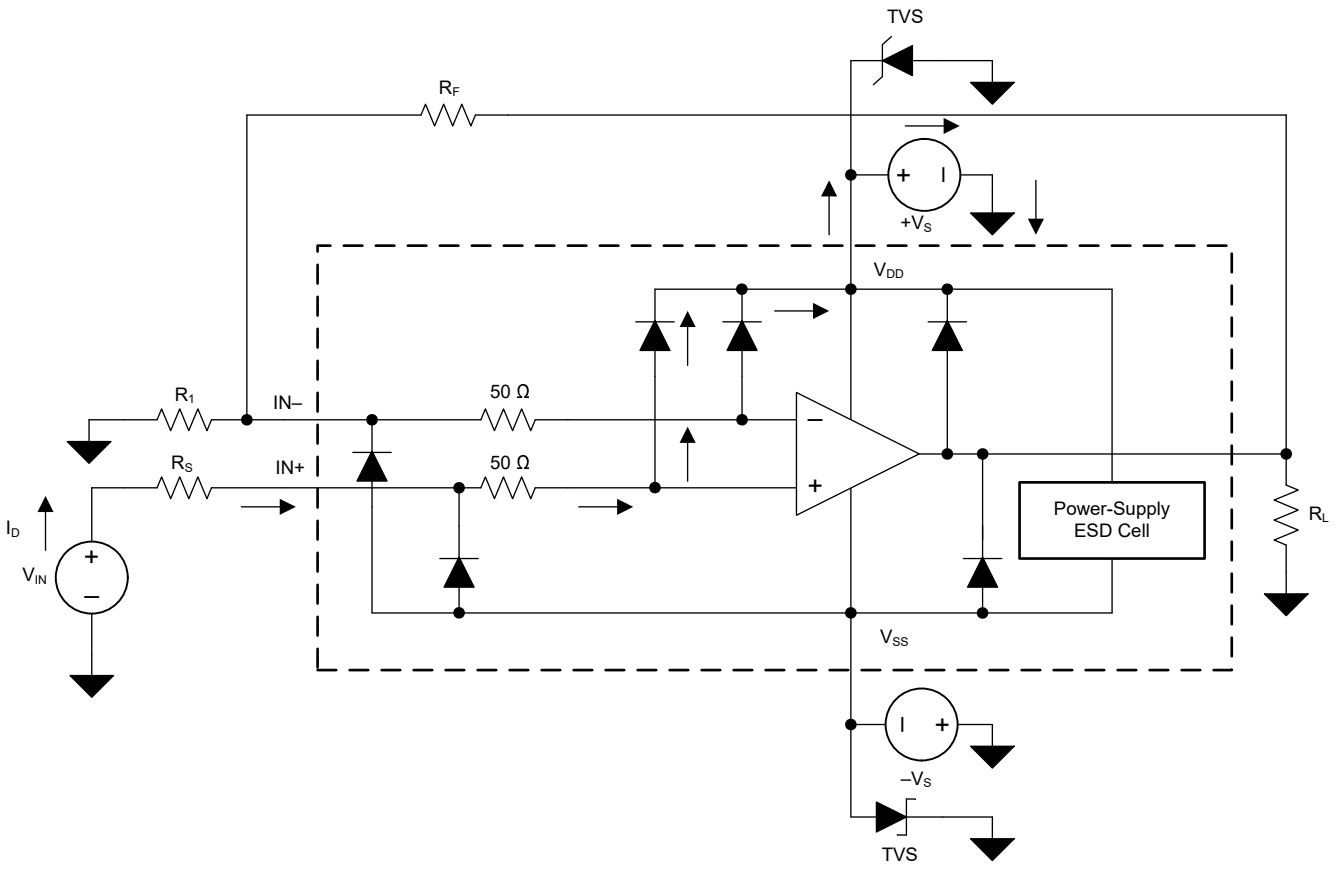


Figure 6-9. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example; 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV916x-Q1 is approximately 120ns.

6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.

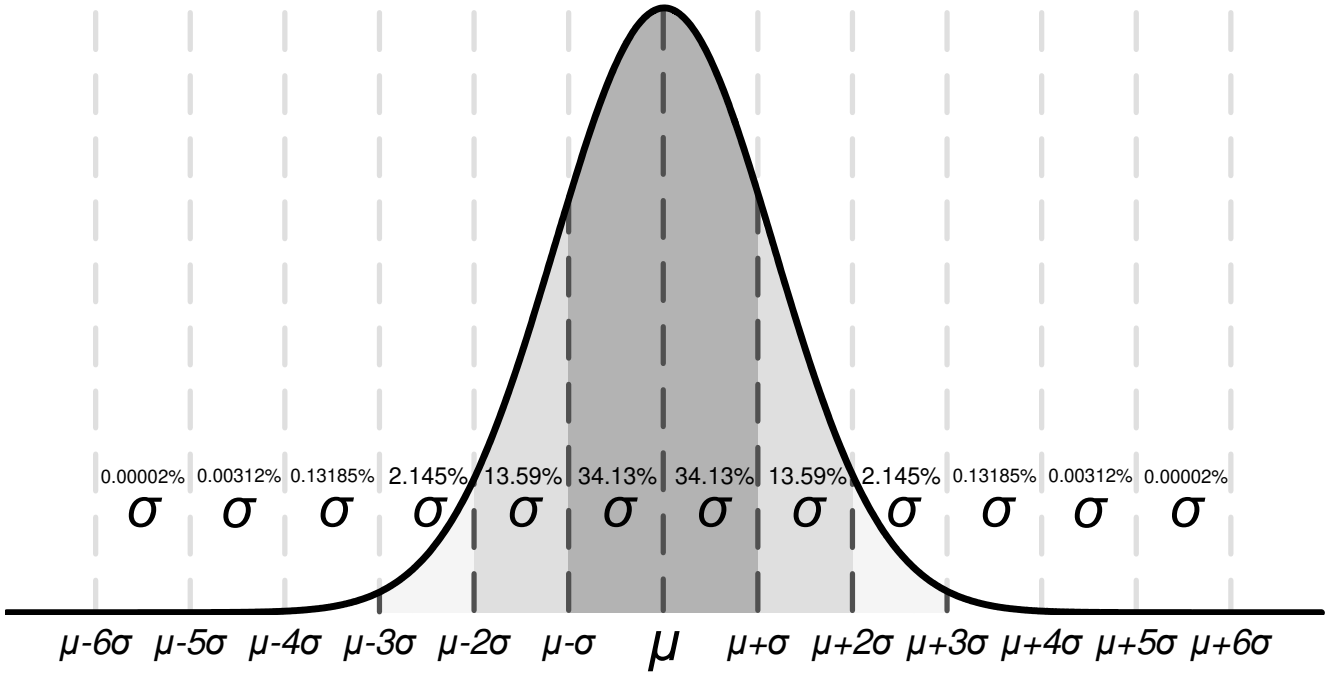


Figure 6-10. Ideal Gaussian Distribution

Figure 6-10 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

This chart can be used to calculate approximate probability of a specification in a unit; for example, for TLV916x-Q1, the typical input voltage offset is 210µV, so 68.2% of all TLV916x-Q1 devices are expected to have an offset from –210µV to 210µV. At 4 σ (±840µV), 99.9937% of the distribution has an offset voltage less than ±840µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV916x-Q1 family has a maximum offset voltage of 1mV at 25°C, and even though this corresponds to about 5σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV916x-Q1 family does not have a maximum or minimum for offset voltage drift, but based on the typical value of 0.25µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6σ value for offset voltage drift is about 1.5µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

6.4 Device Functional Modes

The TLV916x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7V (±1.35V). The maximum power supply voltage for the TLV916x-Q1 is 16V (±8V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV916x-Q1 family offers excellent DC precision and AC performance. These devices operate up to 16V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 11MHz bandwidth and high output drive. These features make the TLV916x-Q1 a robust, high-performance operational amplifier for 16V industrial applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-1 shows the TLV9161-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution* .

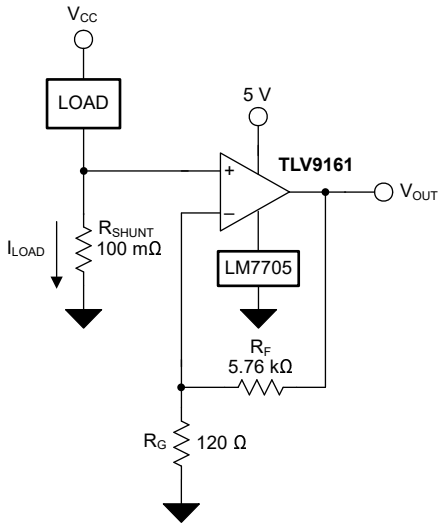


Figure 7-1. TLV9161-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV916x-Q1 to produce an output voltage of 0V to 4.9V. The gain needed by the TLV916x-Q1 to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the TLV916x-Q1 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Choosing R_F as 5.76kΩ, R_G is calculated to be 120Ω. R_F and R_G were chosen as 5.76kΩ and 120Ω because the values are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. However, excessively large resistors generate thermal noise that exceeds the intrinsic noise of the op amp. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

7.2.1.3 Application Curves

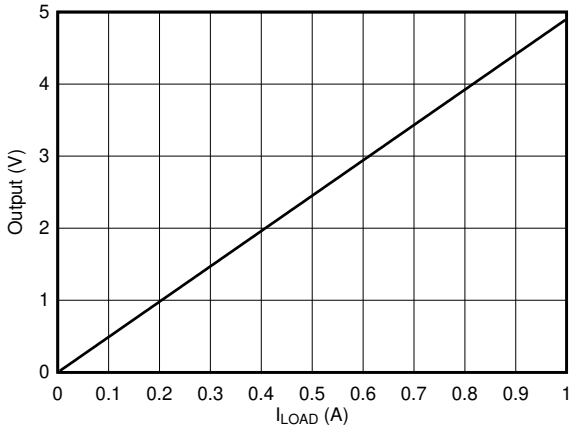


Figure 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV916x-Q1 is specified for operation from 2.7V to 16V (±1.35V to ±8V); many specifications apply from –40°C to 125°C or with specific supply voltage and test conditions.

CAUTION

Supply voltages larger than 20V can permanently damage the device; see the *Absolute Maximum Ratings* section.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout* section.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

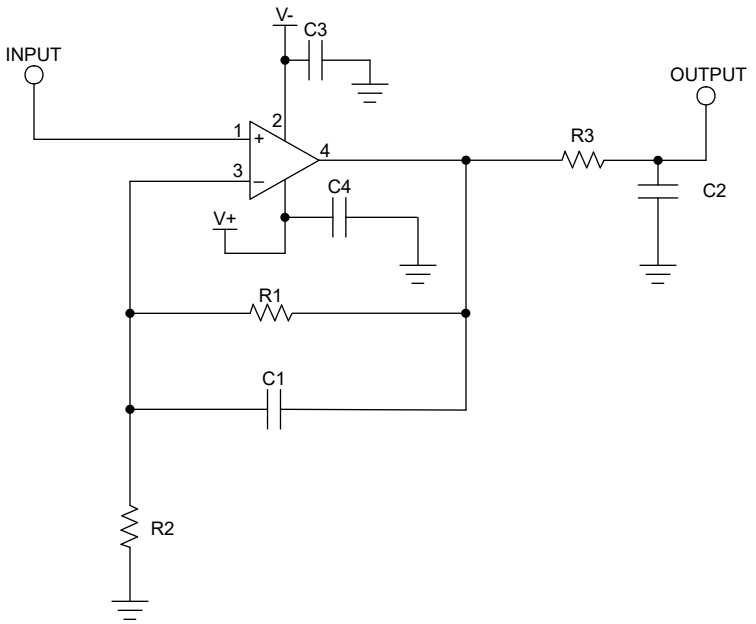


Figure 7-3. Schematic for Non-inverting Configuration Layout Example

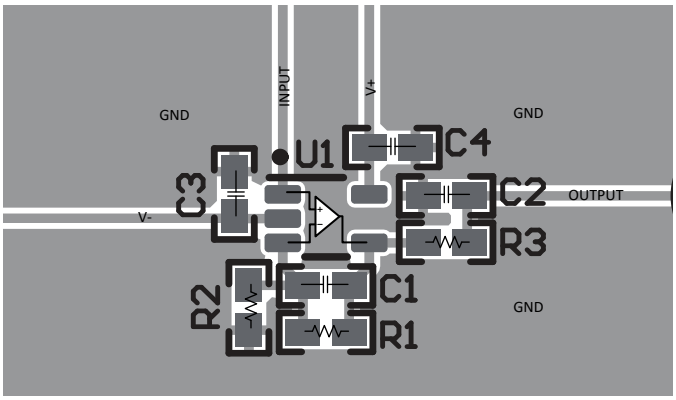


Figure 7-4. Operational Amplifier Board Layout for Non-inverting Configuration - SC70 (DCK) Package

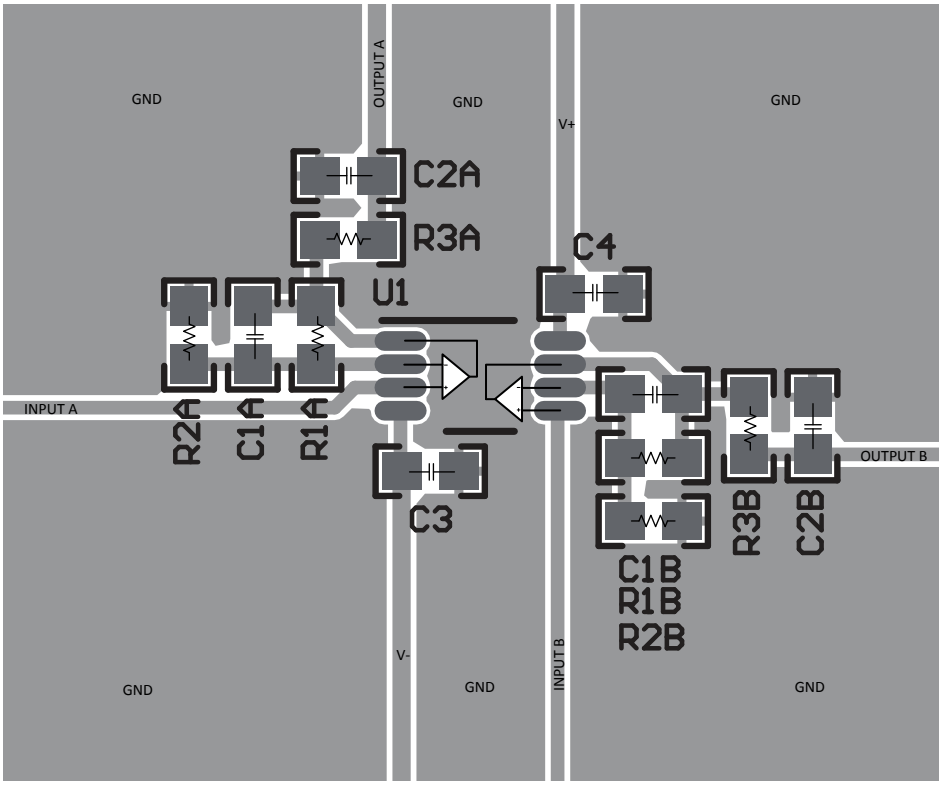


Figure 7-5. Example Layout for VSSOP-8 (DGK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

1. Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers*
2. Texas Instruments, *AN31 amplifier circuit collection* application note
3. Texas Instruments, *MUX-Friendly, Precision Operational Amplifiers* application brief
4. Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
5. Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TINA-TI™ is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
TINA™ and DesignSoft™ are trademarks of DesignSoft, Inc.
TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision * (April 2023) to Revision A (August 2024)	Page
• Changed *Device Information* table to *Package Information*	1
• Added the PW package to the *Package Information* table	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9161QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2W2H
TLV9161QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2W2H
TLV9161QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NJ
TLV9161QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NJ
TLV9162QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S5T
TLV9162QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2S5T
TLV9162QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9162Q
TLV9162QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9162Q
TLV9162QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9162PW
TLV9162QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9162PW
TLV9164QDRQ1	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9164QD
TLV9164QDRQ1.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9164QD
TLV9164QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9164PW
TLV9164QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9164PW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV9161-Q1, TLV9162-Q1, TLV9164-Q1 :

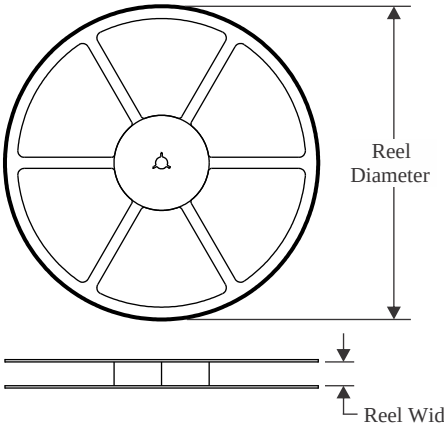
- Catalog : TLV9161, TLV9162, TLV9164

NOTE: Qualified Version Definitions:

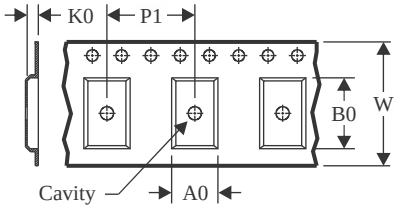
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

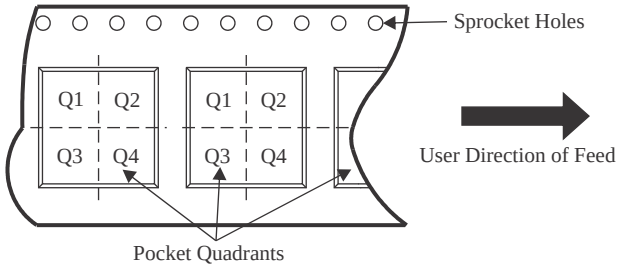


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

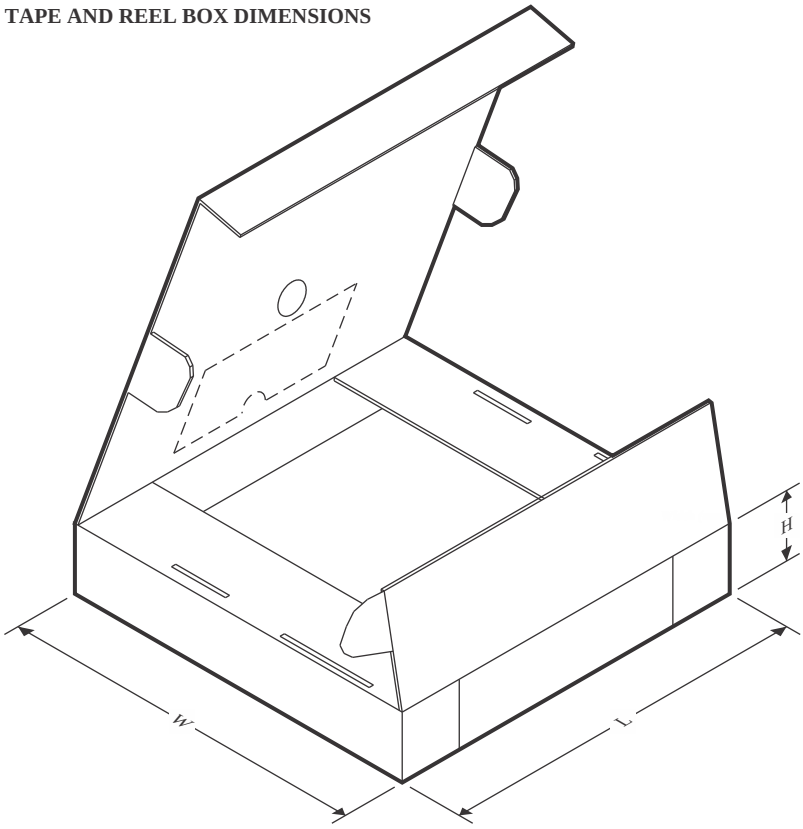
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9161QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9161QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9162QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV9162QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9162QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9164QDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9164QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

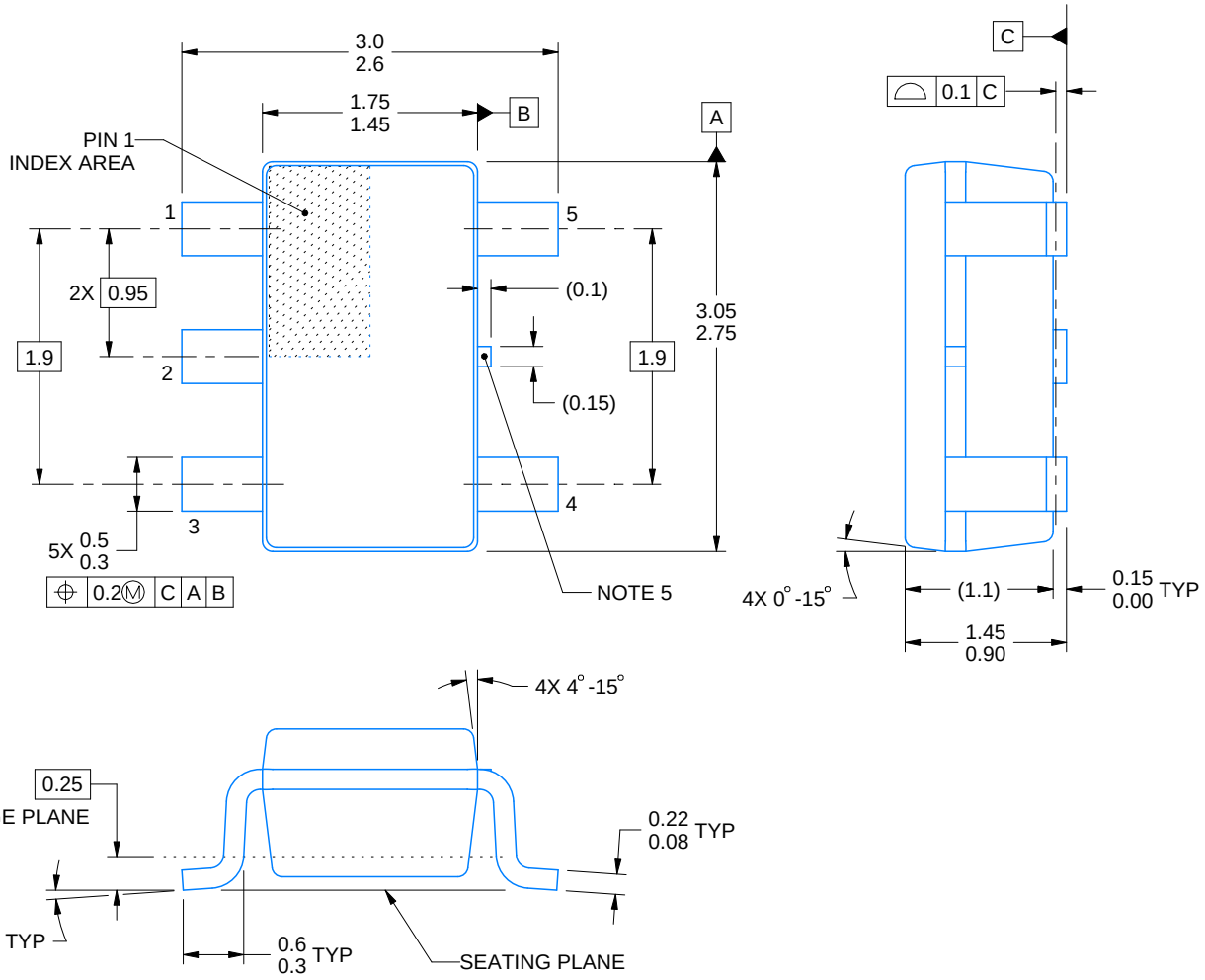
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9161QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9161QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TLV9162QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9162QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
TLV9162QPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV9164QDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
TLV9164QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

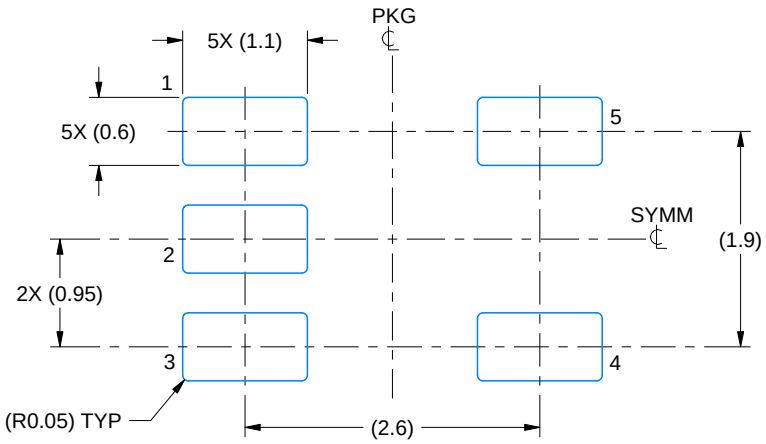
SMALL OUTLINE TRANSISTOR



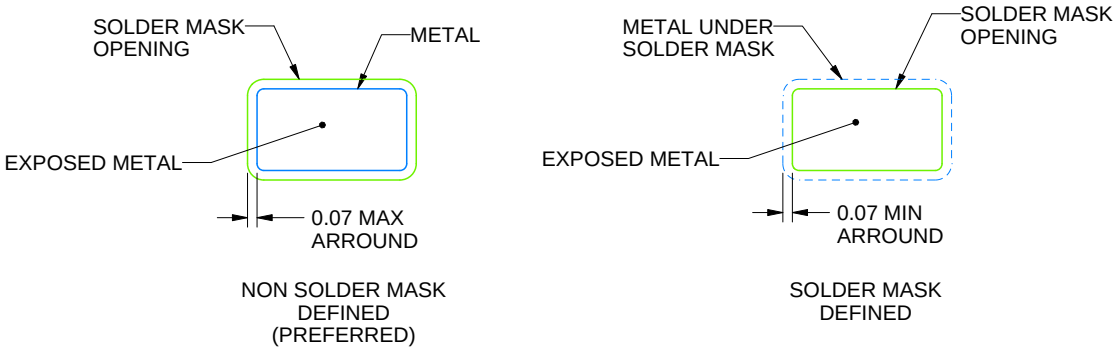
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

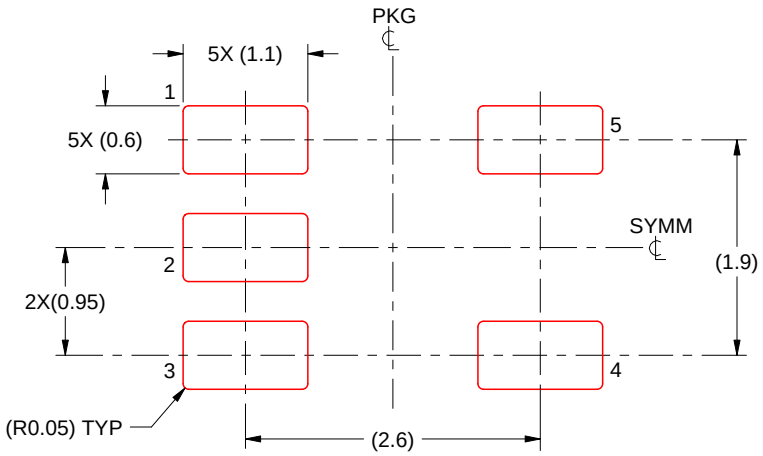


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

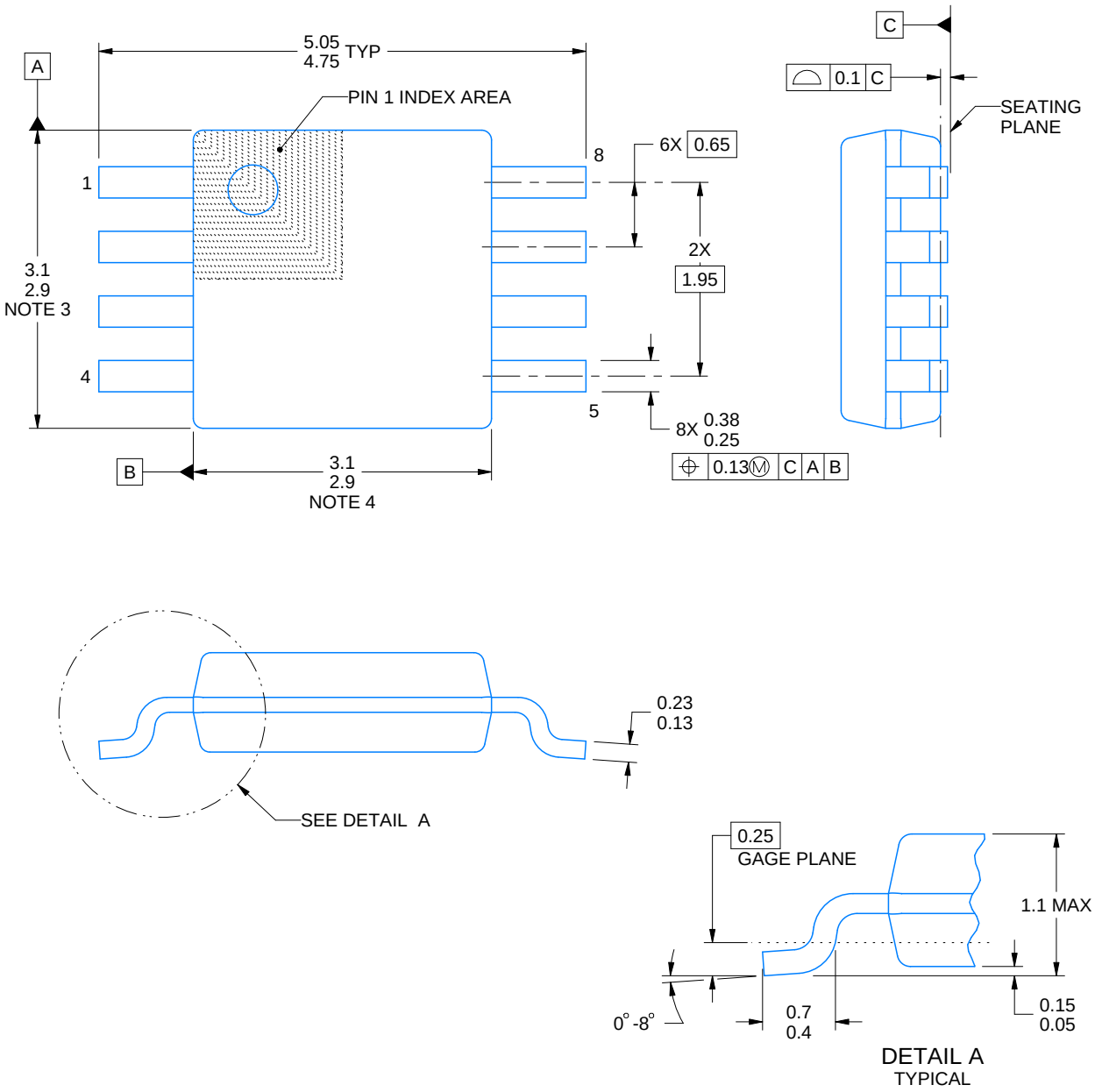
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

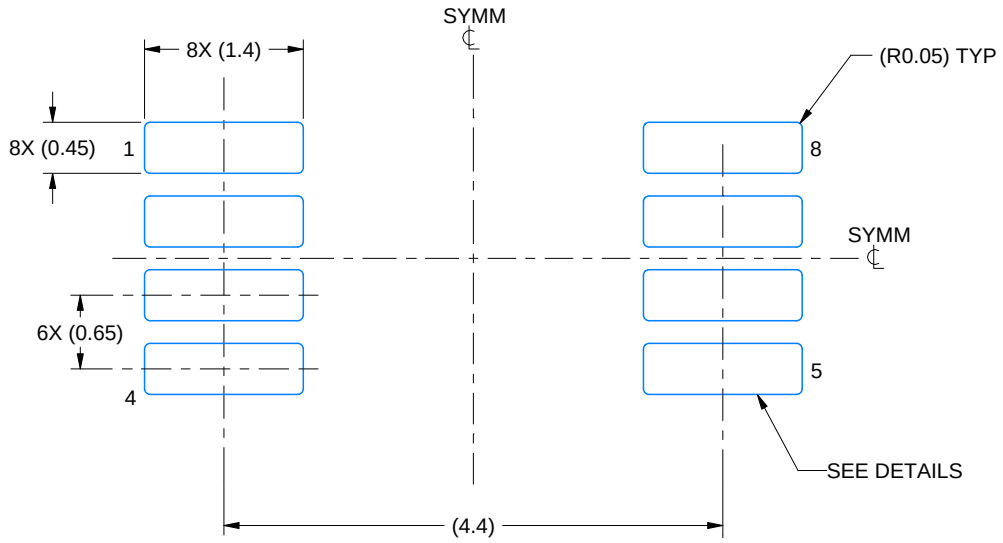
SMALL OUTLINE PACKAGE



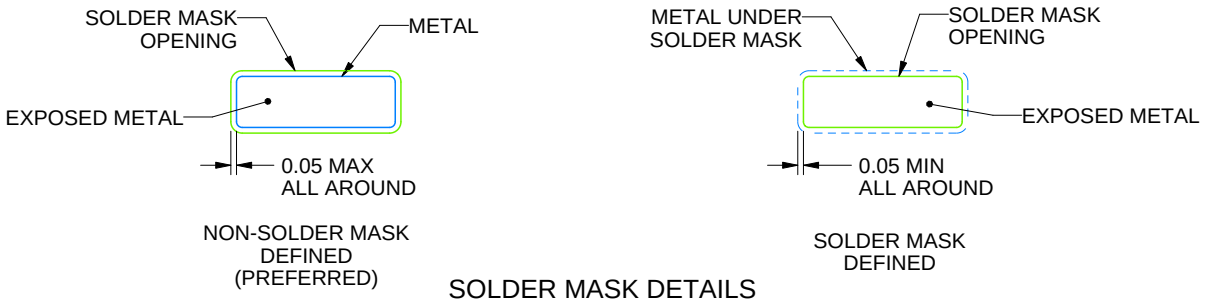
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

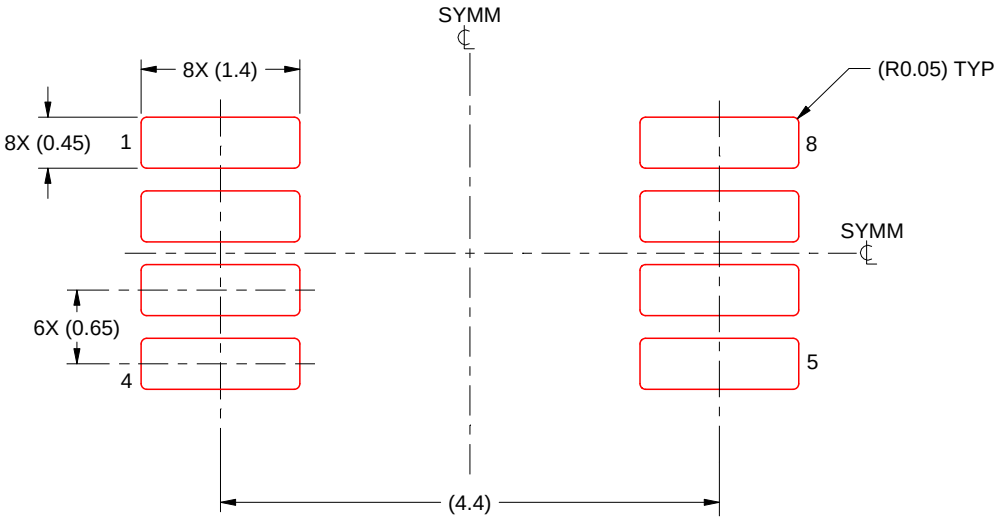


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

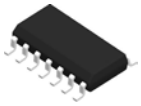


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

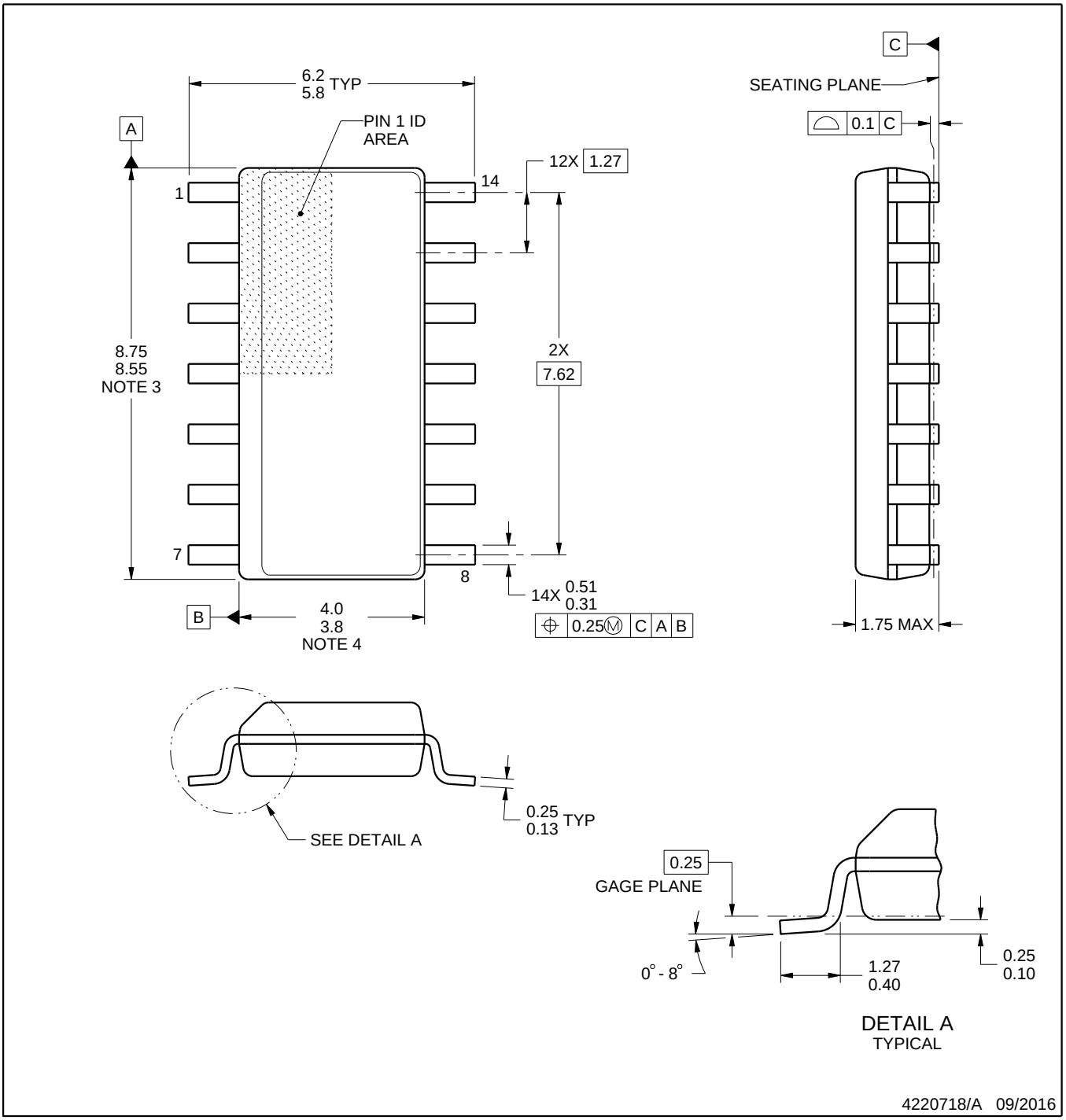


PACKAGE OUTLINE

D0014A

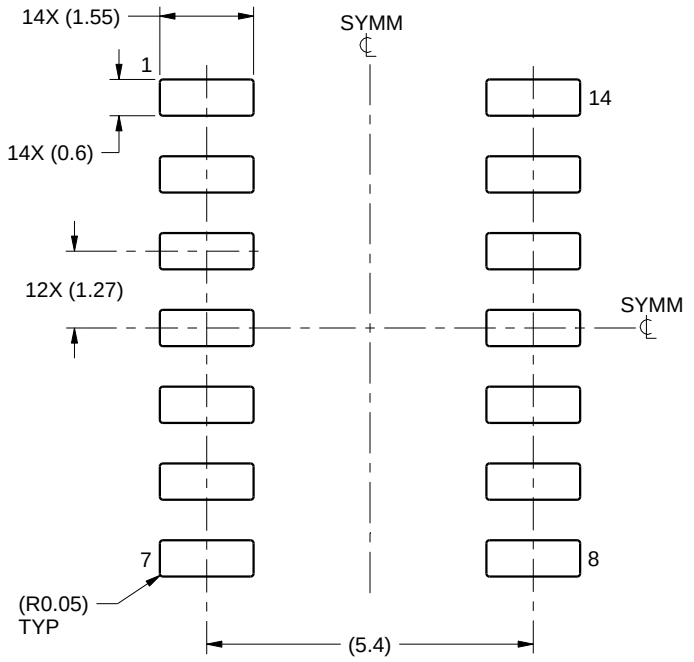
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

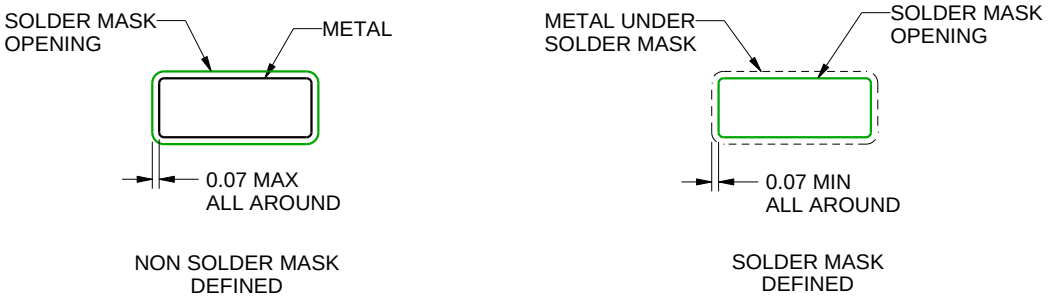


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

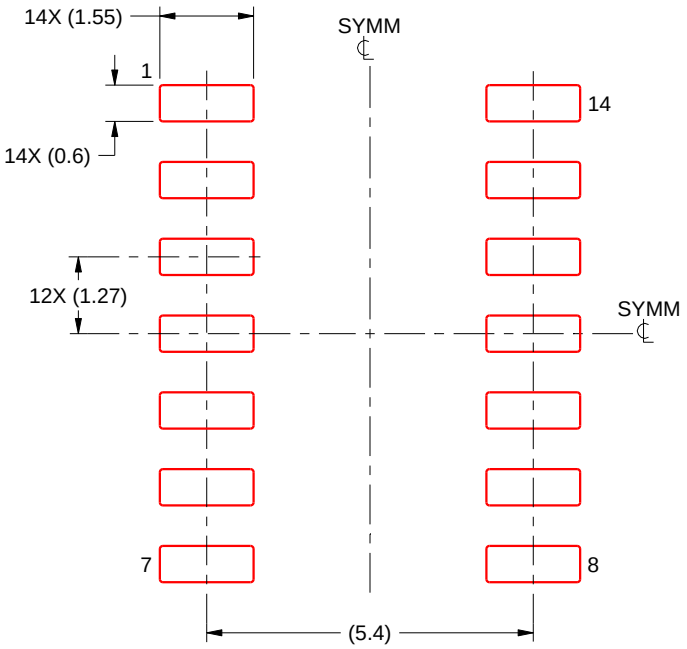
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

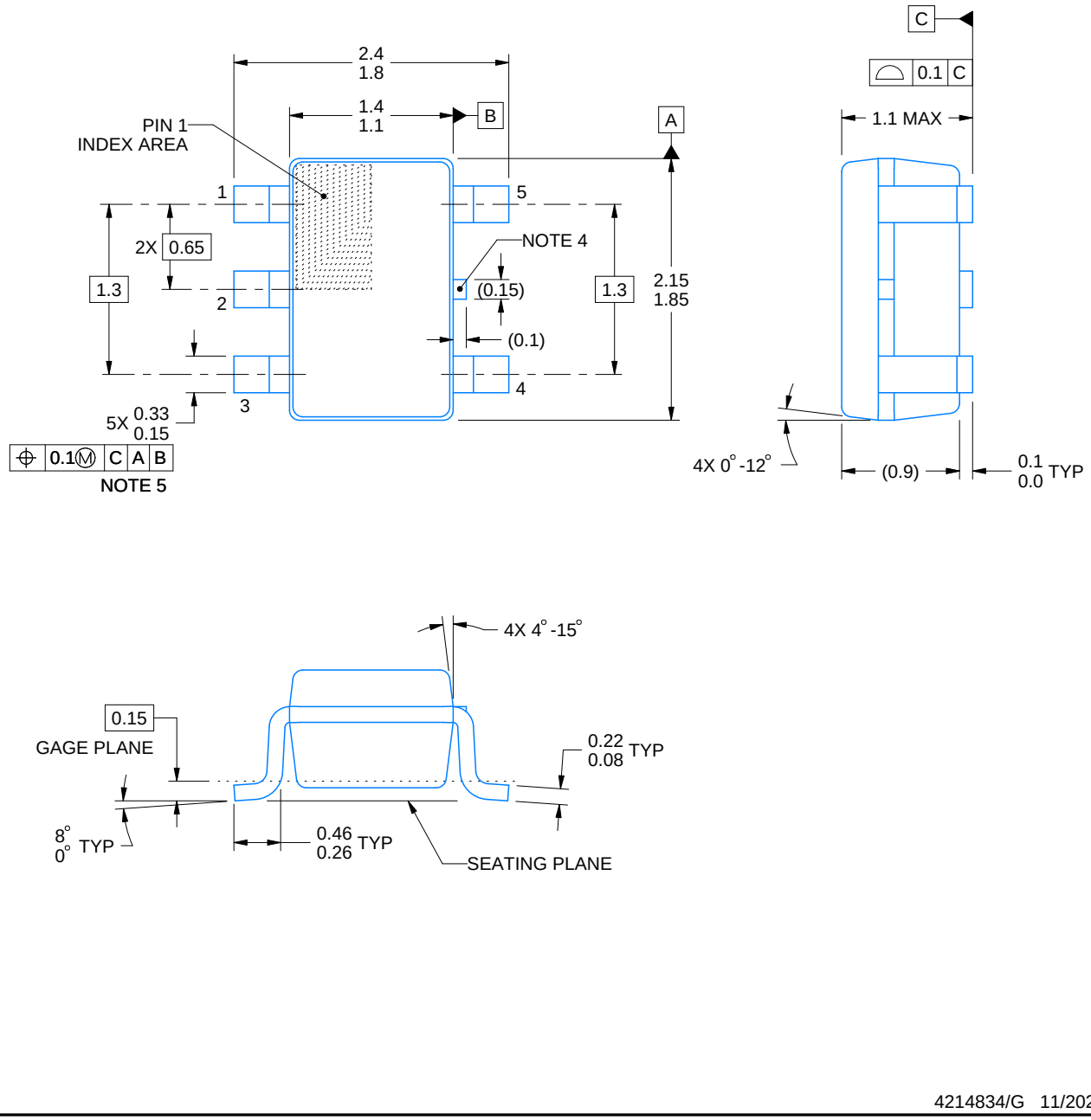
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

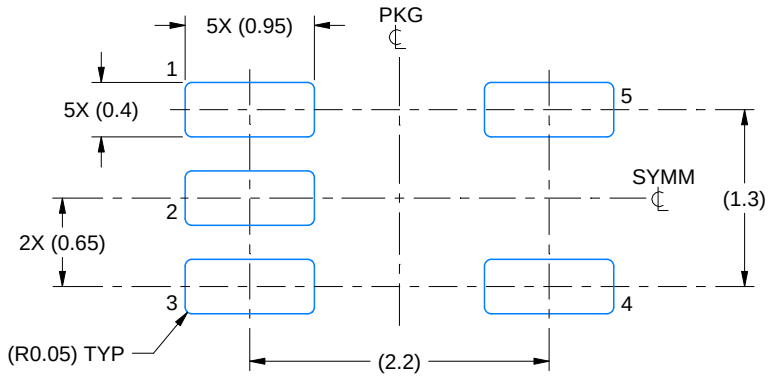
SMALL OUTLINE TRANSISTOR



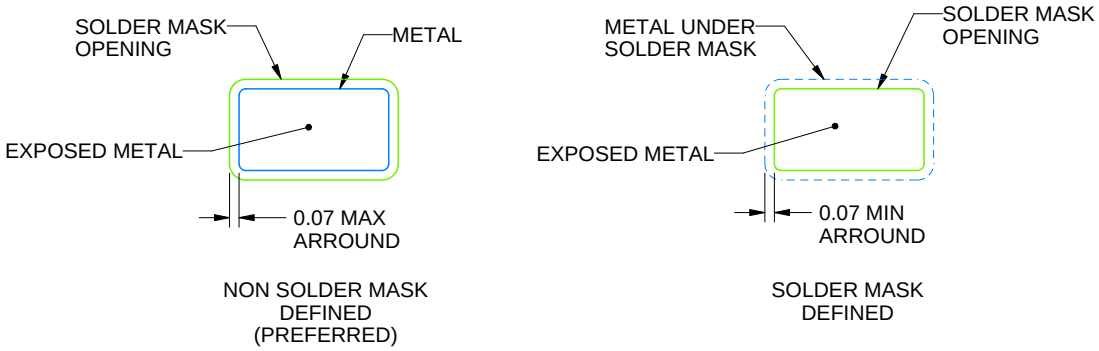
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

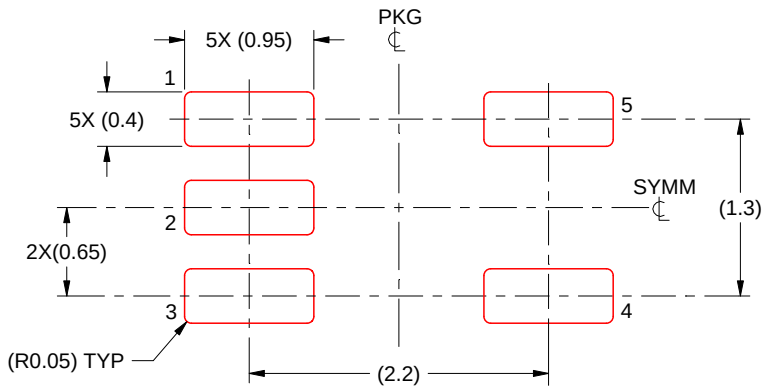


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

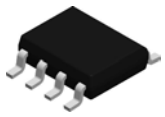


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

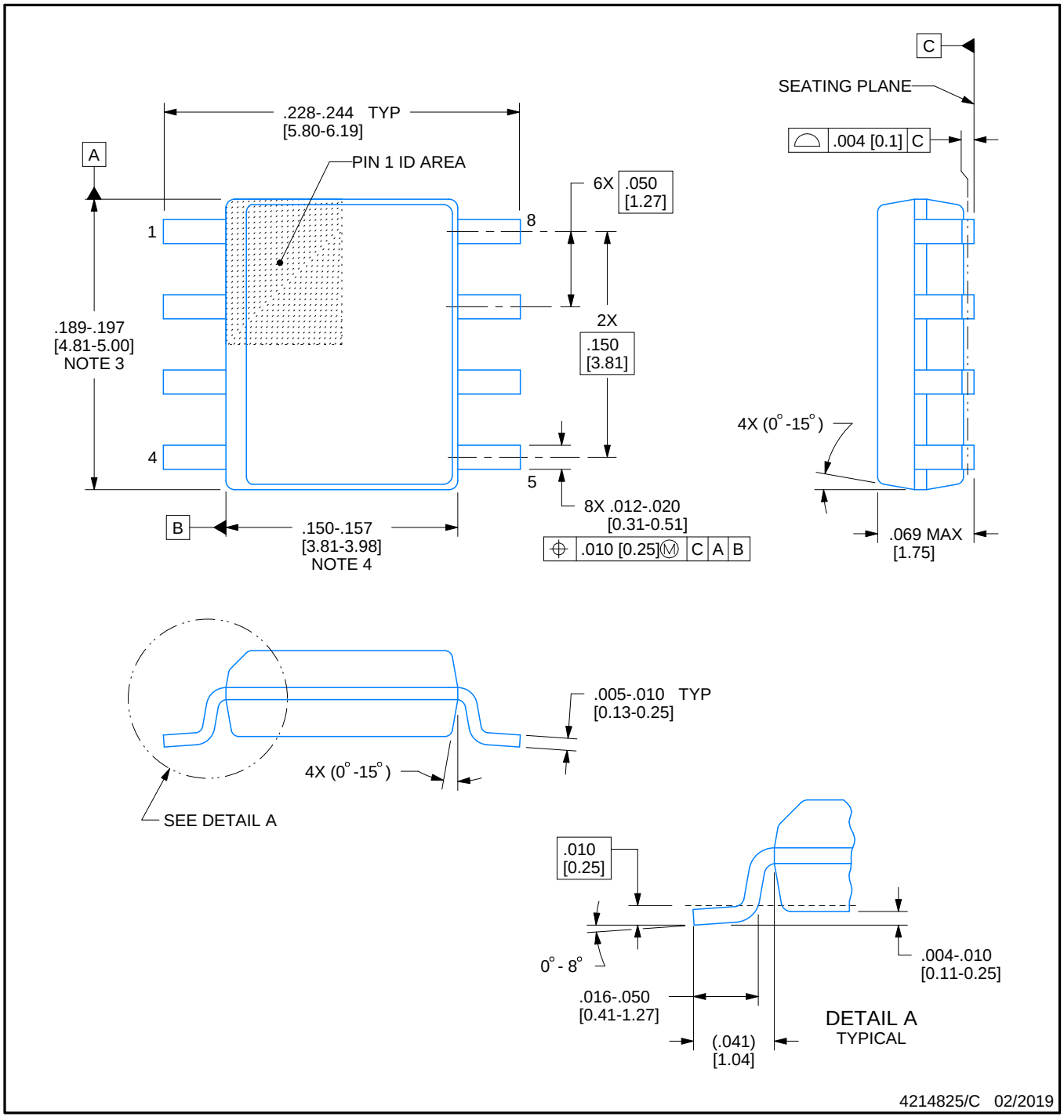


PACKAGE OUTLINE

D0008A

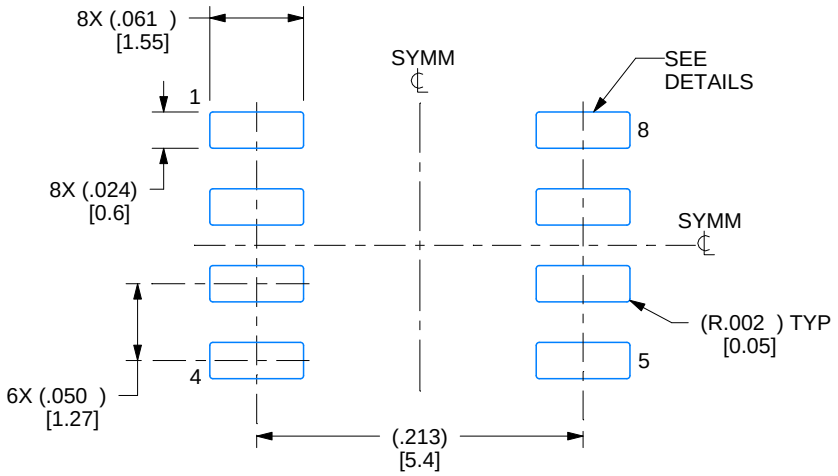
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

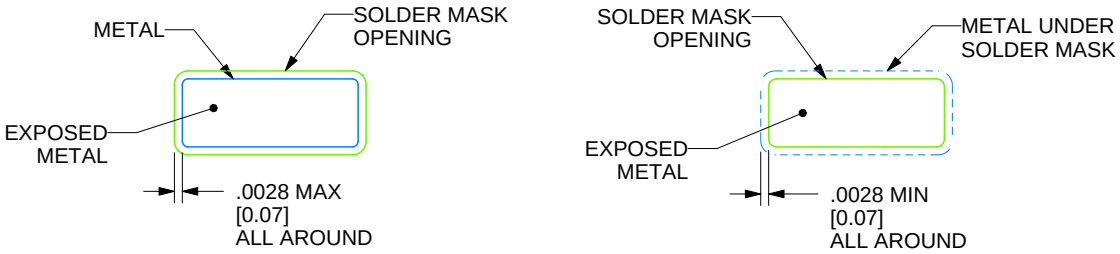


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

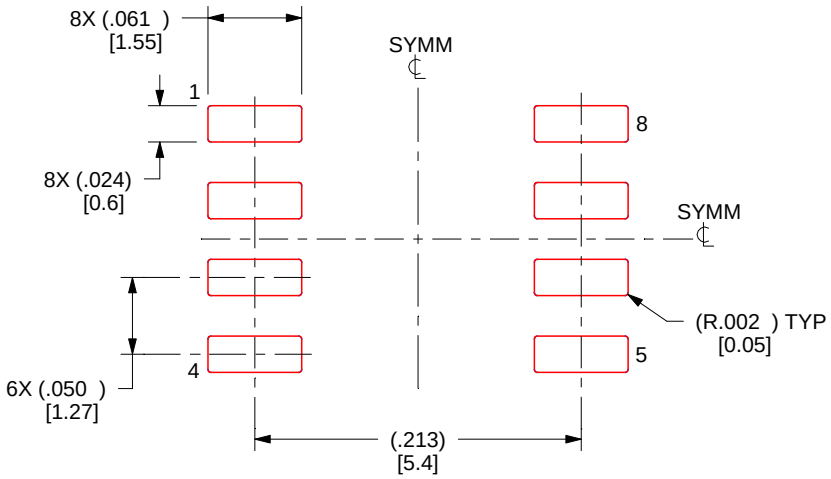
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

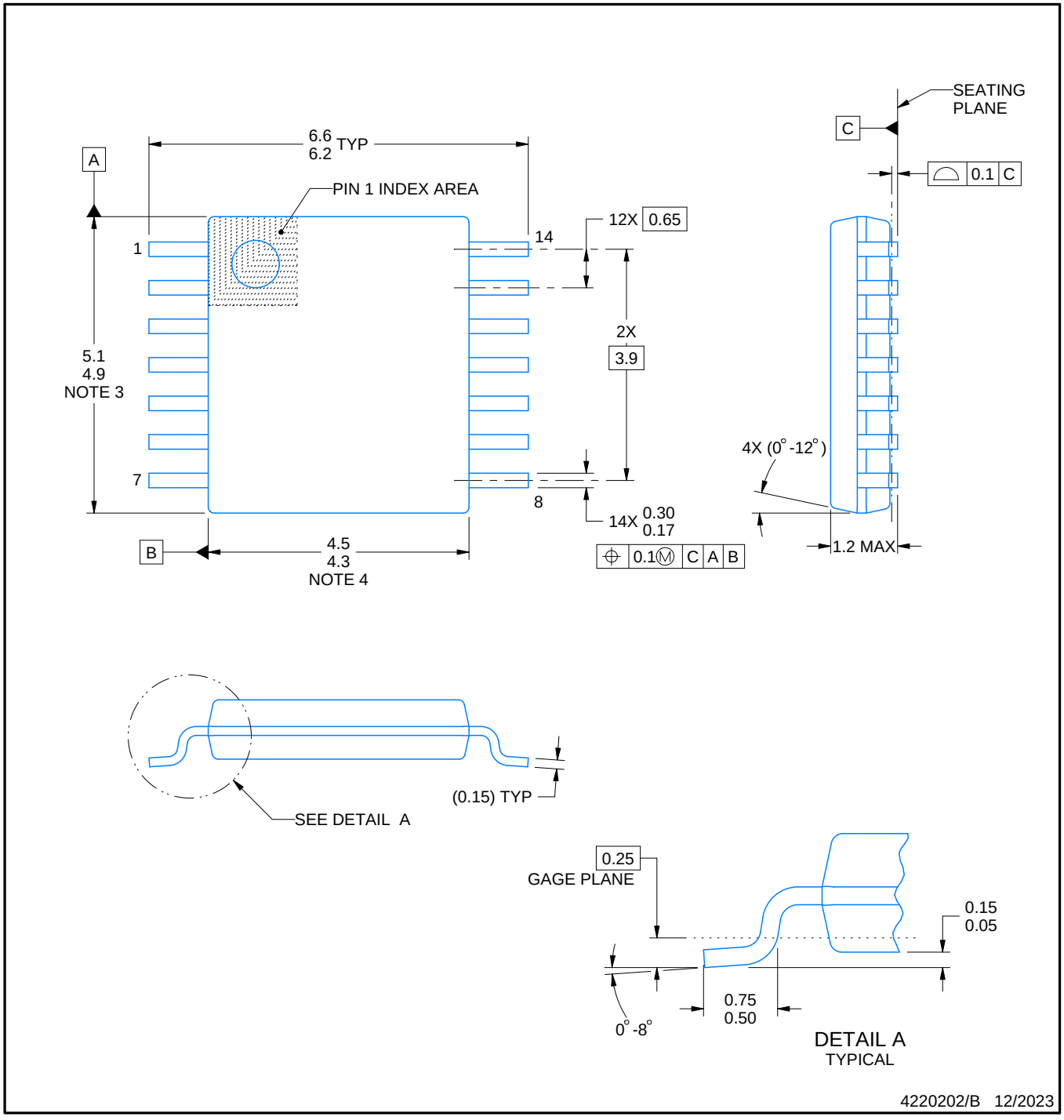
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

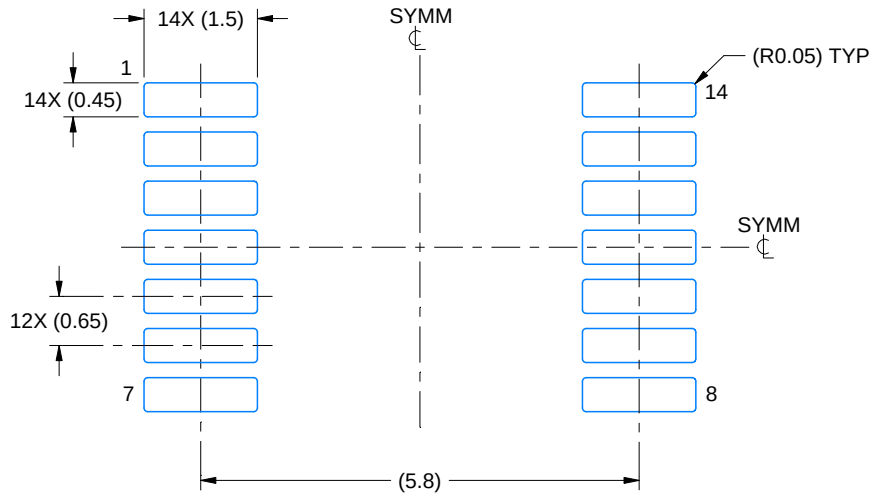
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

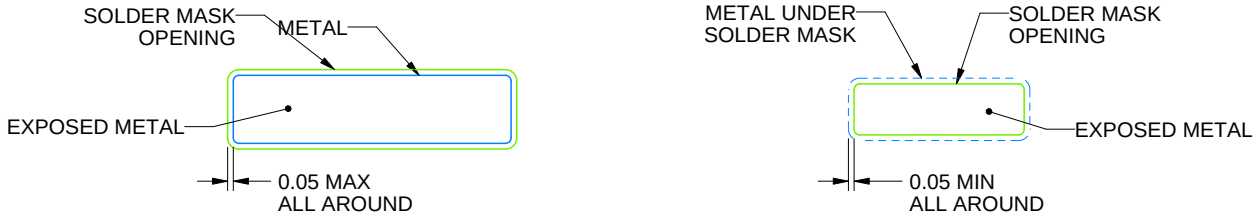


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

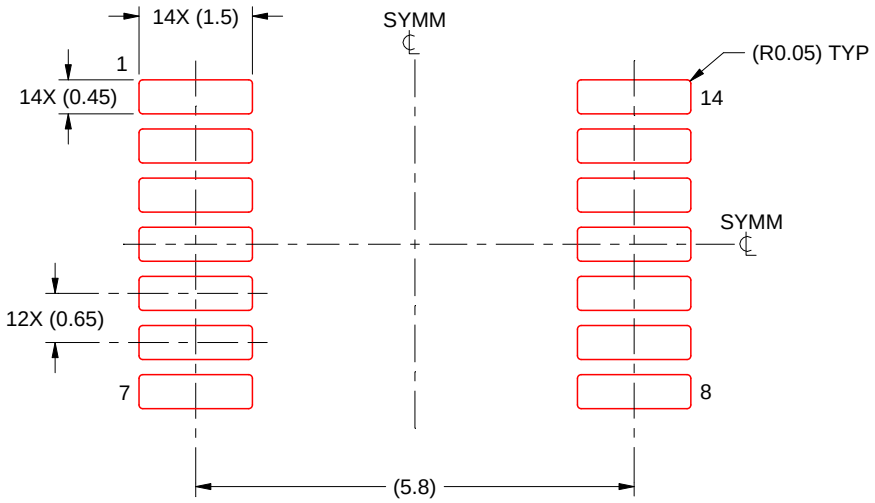


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

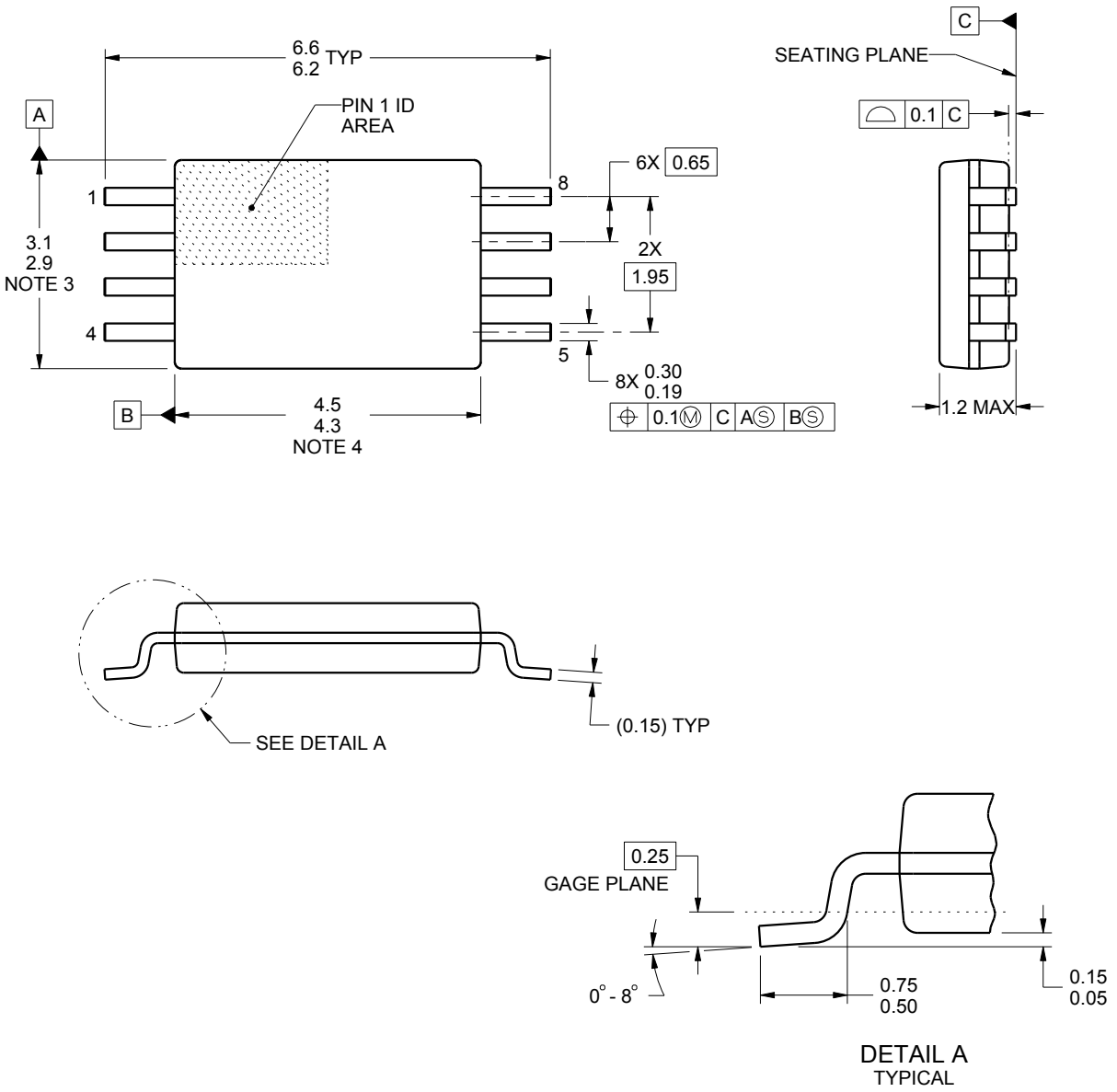
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

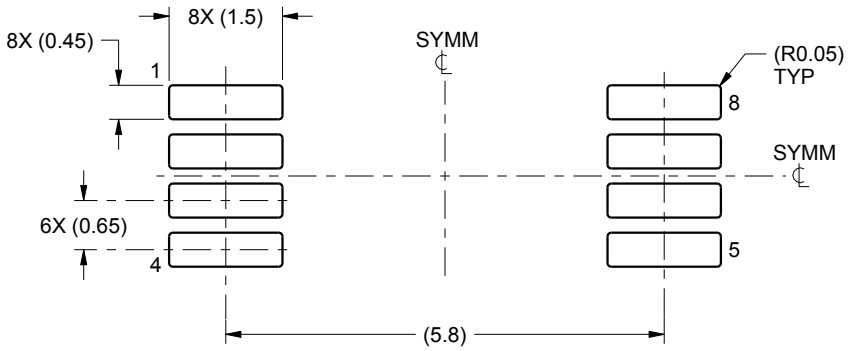
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

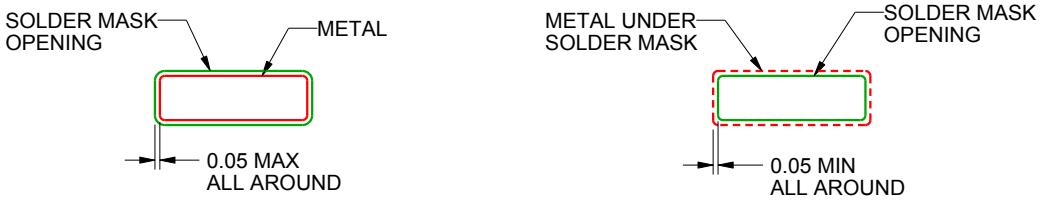


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

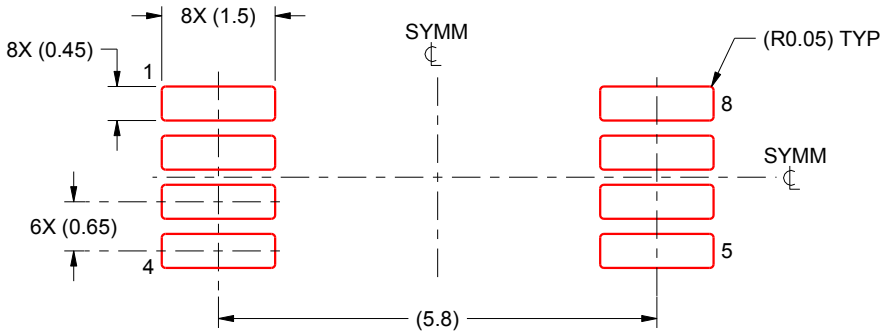


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265