

TLV906xS 10MHz, RRIO, CMOS Operational Amplifiers for Cost-Sensitive Systems

1 Features

- Rail-to-rail input and output
- Low input offset voltage: $\pm 0.3\text{mV}$
- Unity-gain bandwidth: 10MHz
- Low broadband noise: $10\text{nV}/\sqrt{\text{Hz}}$
- Low input bias current: 0.5pA
- Low quiescent current: 538 μA
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Shutdown version: TLV906xS
- Extended temperature range: -40°C to 125°C

2 Applications

- [E-bikes](#)
- [Smoke detectors](#)
- [HVAC: heating, ventilating, and air conditioning](#)
- [Motor control: AC induction](#)
- [Refrigerators](#)
- [Wearable devices](#)
- [Laptop computers](#)
- [Washing machines](#)
- [Sensor signal conditioning](#)
- [Power modules](#)
- [Barcode scanners](#)
- [Active Filters](#)
- [Low-side current sensing](#)

3 Description

The TLV9061 (single), TLV9062 (dual), and TLV9064 (quad) are single-, dual-, and quad- low-voltage, 1.8V to 5.5V operational amplifiers, op amps) with rail-to-rail input and output swing capabilities.

These devices are highly cost-effective options for applications where low-voltage operation, a small footprint, and high capacitive load drive are required.

Although the capacitive load drive of the TLV906x is 100pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. These op amps are designed specifically for low-voltage operation (1.8V to 5.5V), with performance specifications similar to the OPAx316 and TLVx316 devices.

The TLV906xS devices include a shutdown mode that allow the amplifiers to switch into standby mode with typical current consumption less than 1 μA .

The TLV906xS family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

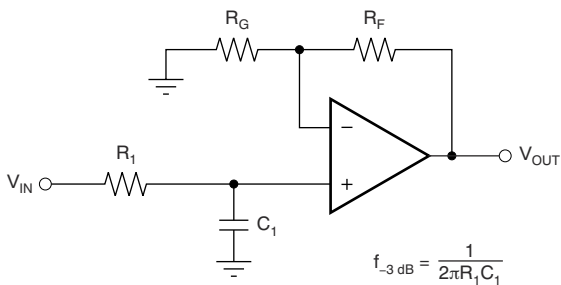
Micro size packages, such as X2SON and X2QFN, are offered for all the channel variants (single, dual and quad), along with industry-standard packages, such as SOIC, MSOP, SOT-23, and TSSOP.

Device Information

| PART NUMBER ⁽³⁾ | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) ⁽⁴⁾ |
|----------------------------|---------------------------------|--------------------------------|
| TLV9061 | DBV (SOT-23, 5) | 2.90mm × 1.60 mm |
| | DCK (SC70, 5) | 2.00mm × 1.25 mm |
| | DRL (SOT-553, 5) ⁽²⁾ | 1.60mm × 1.20 mm |
| | DPW (X2SON, 5) | 0.80mm × 0.80mm |
| TLV9061S | DBV (SOT-23, 6) | 2.90mm × 1.60 mm |
| | DRY (USON, 6) | 1.45mm × 1.00 mm |
| TLV9062 | D (SOIC, 8) | 4.90mm × 3.90 mm |
| | PW (TSSOP, 8) | 3.00mm × 4.40 mm |
| | DGK (VSSOP, 8) | 3.00mm × 3.00 mm |
| | DDF (SOT-23, 8) | 2.90mm × 1.60 mm |
| | DSG (WSON, 8) | 2.00mm × 2.00 mm |
| TLV9062S | DGS (VSSOP, 10) | 3.00mm × 3.00 mm |
| | RUG (X2QFN, 10) | 2.00mm × 1.50mm |
| | YCK (DSBGA, 9) | 1.00mm × 1.00mm |
| TLV9064 | D (SOIC, 14) | 8.65mm × 3.90 mm |
| | PW (TSSOP, 14) | 5.00mm × 4.40 mm |
| | RTE (WQFN, 16) | 3.00mm × 3.00mm |
| | RUC (X2QFN, 14) | 2.00mm × 2.00mm |
| TLV9064S | RTE (WQFN, 16) | 3.00mm × 3.00mm |

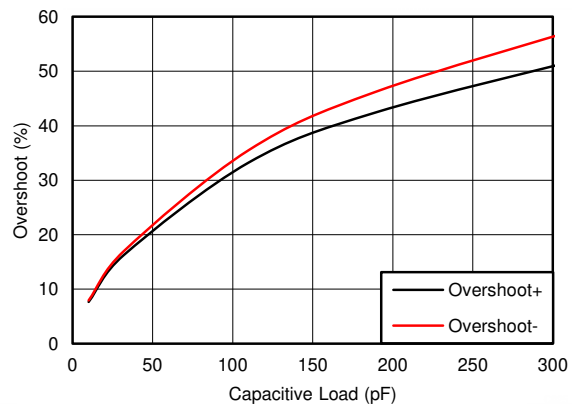
- (1) For all available packages, see [Section 10](#).
- (2) Package is preview only.
- (3) See [Device Comparison](#).
- (4) The body size (length × width) is a nominal value and does not include pins.





$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

Single-Pole, Low-Pass Filter



Small-Signal Overshoot vs Load Capacitance

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Device Comparison Table

| DEVICE | NO. OF CHANNELS | PACKAGE LEADS | | | | | | | | | | | | | | |
|----------|-----------------|---------------|----------|------------|-----------|-----------|-----------|-----------|-----------|--------------|----------|----------|------------|----------|-----------|-----------|
| | | SOIC D | USON DRY | SOT-23 DBV | SC-70 DCK | VSSOP DGK | VSSOP DGS | DSBGA YCK | X2SON DPW | SOT-55 3 DRL | WSOP DSG | TSSOP PW | SOT-23 DDF | WQFN RTE | X2QFN RUC | X2QFN RUG |
| TLV9061 | 1 | 8 | — | 5 | 5 | — | — | — | 5 | 5 | — | — | — | — | — | — |
| TLV9061S | | — | 6 | 6 | — | — | — | — | — | — | — | — | — | — | — | — |
| TLV9062 | 2 | 8 | — | — | — | 8 | 10 | — | — | — | 8 | 8 | 8 | — | — | — |
| TLV9062S | | — | — | — | — | — | 10 | 9 | — | — | — | — | — | — | — | 10 |
| TLV9064 | 4 | 14 | — | — | — | — | — | — | — | — | — | 14 | — | 16 | 14 | — |
| TLV9064S | | — | — | — | — | — | — | — | — | — | — | — | — | 16 | — | — |

4 Pin Configuration and Functions

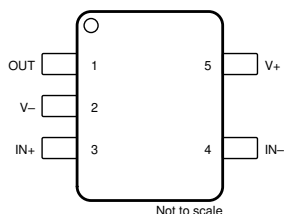


Figure 4-1. TLV9061 DBV or DRL Package, 5-Pin SOT-23 or SOT-553 (Top View)

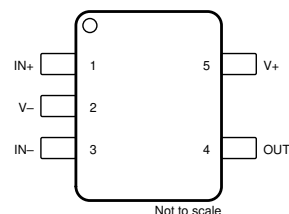


Figure 4-2. TLV9061 DCK Package, 5-Pin SC70 (Top View)

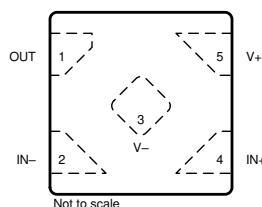


Figure 4-3. TLV9061 DPW Package, 5-Pin X2SON (Top View)

Table 4-1. Pin Functions: TLV9061

| NAME | PIN | | | TYPE ⁽¹⁾ | DESCRIPTION |
|------|--------------------|------|-------|---------------------|---|
| | SOT-23, SOT-553 | SC70 | X2SON | | |
| IN– | 4 | 3 | 2 | I | Inverting input |
| IN+ | 3 | 1 | 4 | I | Noninverting input |
| OUT | 1 | 4 | 1 | O | Output |
| V– | 2 | 2 | 3 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 5 | 5 | 5 | I | Positive (high) supply |

(1) I = input, O = output

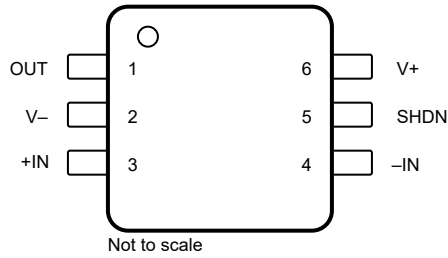


Figure 4-4. TLV9061S DBV Package, 6-Pin SOT-23 (Top View)

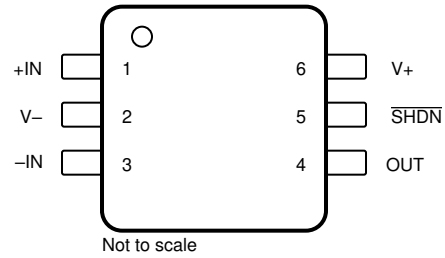


Figure 4-5. TLV9061S DRY Package, 6-Pin USON (Top View)

Table 4-2. Pin Functions: TLV9061S

| NAME | PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|------|--------|------|---------------------|---|
| | SOT-23 | USON | | |
| IN– | 4 | 3 | I | Inverting input |
| IN+ | 3 | 1 | I | Noninverting input |
| OUT | 1 | 4 | O | Output |
| SHDN | 5 | 5 | I | Shutdown: low = amp disabled, high = amp enabled. See Shutdown Function section for more information. |
| V– | 2 | 2 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 6 | 6 | I | Positive (high) supply |

(1) I = input, O = output

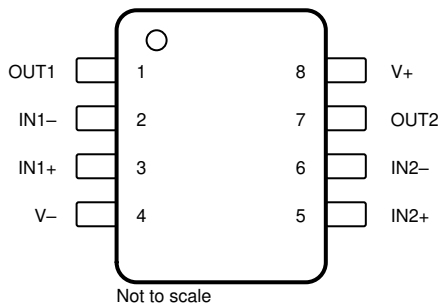


Figure 4-6. TLV9062 D, DGK, PW, or DDF Package, 8-Pin SOIC, VSSOP, TSSOP, or SOT-23 (Top View)

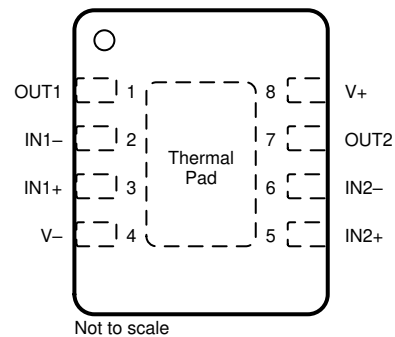


Figure 4-7. TLV9062 DSG Package, 8-Pin WSON With Exposed Thermal Pad (Top View)

Table 4-3. Pin Functions: TLV9062

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|------|-----|---------------------|--|
| NAME | NO. | | |
| IN1– | 2 | I | Inverting input, channel 1 |
| IN1+ | 3 | I | Noninverting input, channel 1 |
| IN2– | 6 | I | Inverting input, channel 2 |
| IN2+ | 5 | I | Noninverting input, channel 2 |
| OUT1 | 1 | O | Output, channel 1 |
| OUT2 | 7 | O | Output, channel 2 |
| V– | 4 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 8 | — | Positive (highest) supply |

(1) I = input, O = output

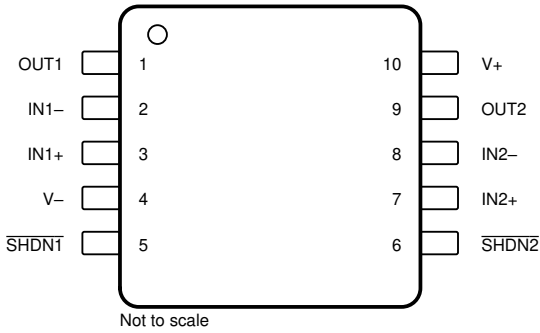


Figure 4-8. TLV9062S DGS Package, 10-Pin VSSOP (Top View)

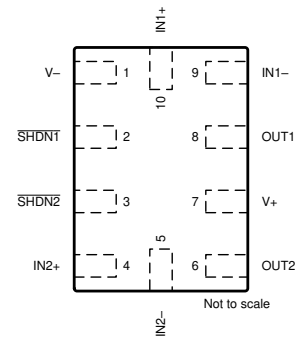


Figure 4-9. TLV9062S RUG Package, 10-Pin X2QFN (Top View)

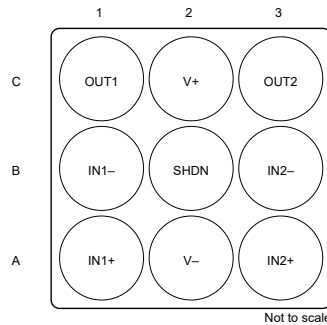


Figure 4-10. TLV9062S YCK Package 9-Pin DSBGA (WCSP) Bottom View

Table 4-4. Pin Functions: TLV9062S

| NAME | PIN | | | I/O | DESCRIPTION |
|-------|-------|-------|--------------|--------|--|
| | VSSOP | X2QFN | DSBGA (WCSP) | | |
| IN1- | 2 | 9 | B1 | I | Inverting input, channel 1 |
| IN1+ | 3 | 10 | A1 | I | Noninverting input, channel 1 |
| IN2- | 8 | 5 | B3 | I | Inverting input, channel 2 |
| IN2+ | 7 | 4 | A3 | I | Noninverting input, channel 2 |
| OUT1 | 1 | 8 | C1 | O | Output, channel 1 |
| OUT2 | 9 | 6 | C3 | O | Output, channel 2 |
| SHDN1 | 5 | 2 | — | I | Shutdown: low = amp disabled, high = amp enabled, channel 1. See Shutdown Function for more information. |
| SHDN2 | 6 | 3 | — | I | Shutdown: low = amp disabled, high = amp enabled, channel 1. See Shutdown Function for more information. |
| SHDN | — | — | B2 | | Shutdown: low = both amplifiers disabled, high = both amplifiers enabled |
| V- | 4 | 1 | A2 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 10 | 7 | C2 | I | Positive (high) supply |

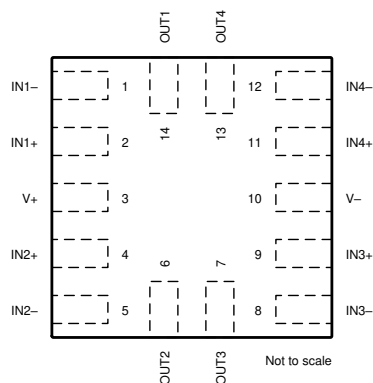


Figure 4-11. TLV9064 RUC Package, 14-Pin X2QFN (Top View)

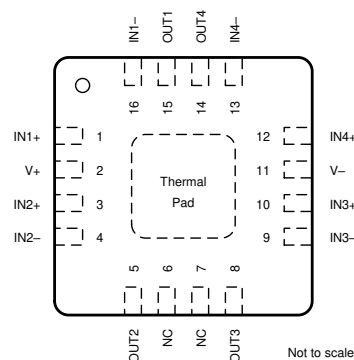


Figure 4-12. TLV9064 RTE Package, 16-Pin WQFN With Exposed Thermal Pad (Top View)

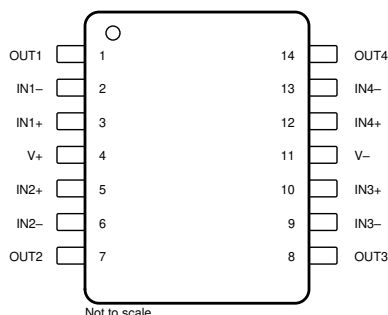
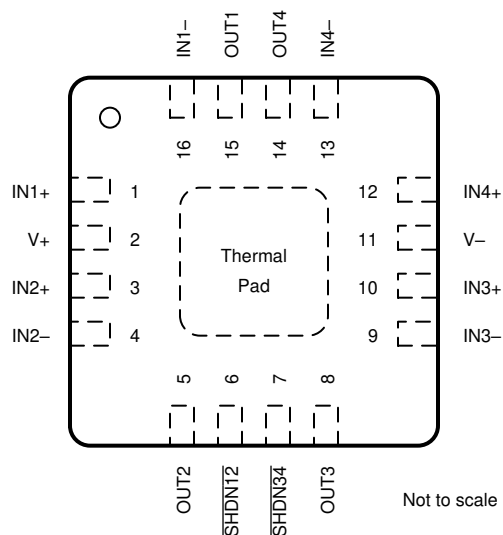


Figure 4-13. TLV9064 D or PW Package, 14-Pin SOIC or TSSOP (Top View)

Table 4-5. Pin Functions: TLV9064

| NAME | PIN | | | TYPE ⁽¹⁾ | DESCRIPTION |
|------|-------------|------|-------|---------------------|---|
| | SOIC, TSSOP | WQFN | X2QFN | | |
| IN1– | 2 | 16 | 1 | I | Inverting input, channel 1 |
| IN1+ | 3 | 1 | 2 | I | Noninverting input, channel 1 |
| IN2– | 6 | 4 | 5 | I | Inverting input, channel 2 |
| IN2+ | 5 | 3 | 4 | I | Noninverting input, channel 2 |
| IN3– | 9 | 9 | 8 | I | Inverting input, channel 3 |
| IN3+ | 10 | 10 | 9 | I | Noninverting input, channel 3 |
| IN4– | 13 | 13 | 12 | I | Inverting input, channel 4 |
| IN4+ | 12 | 12 | 11 | I | Noninverting input, channel 4 |
| NC | — | 6, 7 | — | — | No internal connection |
| OUT1 | 1 | 15 | 14 | O | Output, channel 1 |
| OUT2 | 7 | 5 | 6 | O | Output, channel 2 |
| OUT3 | 8 | 8 | 7 | O | Output, channel 3 |
| OUT4 | 14 | 14 | 13 | O | Output, channel 4 |
| V– | 11 | 11 | 10 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 4 | 2 | 3 | I | Positive (high) supply |

(1) I = input, O = output



A. Connect thermal pad to V–

Figure 4-14. TLV9064S RTE Package, 16-Pin WQFN With Exposed Thermal Pad (Top View)

Table 4-6. Pin Functions: TLV9064S

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|--------|-----|---------------------|--|
| NAME | NO. | | |
| IN1– | 16 | I | Inverting input, channel 1 |
| IN1+ | 1 | I | Noninverting input, channel 1 |
| IN2– | 4 | I | Inverting input, channel 2 |
| IN2+ | 3 | I | Noninverting input, channel 2 |
| IN3– | 9 | I | Inverting input, channel 3 |
| IN3+ | 10 | I | Noninverting input, channel 3 |
| IN4– | 13 | I | Inverting input, channel 4 |
| IN4+ | 12 | I | Noninverting input, channel 4 |
| OUT1 | 15 | O | Output, channel 1 |
| OUT2 | 5 | O | Output, channel 2 |
| OUT3 | 8 | O | Output, channel 3 |
| OUT4 | 14 | O | Output, channel 4 |
| SHDN12 | 6 | I | Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Shutdown Function section for more information. |
| SHDN34 | 7 | I | Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Shutdown Function section for more information. |
| V– | 11 | I or — | Negative (low) supply or ground (for single-supply operation) |
| V+ | 2 | I | Positive (high) supply |

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)⁽¹⁾

| | | | MIN | MAX | UNIT |
|-------------------------------------|---------------------------|--------------|-------------------|------------|------|
| Supply voltage [(V+) – (V–)] | | | 0 | 6 | V |
| Signal input pins | Voltage ⁽²⁾ | Common-mode | (V–) – 0.5 | (V+) + 0.5 | V |
| | | Differential | (V+) – (V–) + 0.2 | | V |
| | Current ⁽²⁾ | | –10 | 10 | mA |
| Output short-circuit ⁽³⁾ | | | Continuous | | mA |
| Temperature | Specified, T _A | | –40 | 125 | °C |
| | Junction, T _J | | | 150 | |
| | Storage, T _{stg} | | –65 | 150 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|-------|------|
| TLV9061 PACKAGES | | | |
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2500 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |
| ALL OTHER PACKAGES | | | |
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±4000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|----------------------|--|------------|------------|------|
| V _S | Supply voltage (V _S = [V+] – [V–]) | 1.8 | 5.5 | V |
| V _I | Input voltage range | (V–) – 0.1 | (V+) + 0.1 | V |
| V _O | Output voltage range | V– | V+ | V |
| V _{SHDN_IH} | High level input voltage at shutdown pin (amplifier enabled) | 1.1 | V+ | V |
| V _{SHDN_IL} | Low level input voltage at shutdown pin (amplifier disabled) | V– | 0.2 | V |
| T _A | Specified temperature | –40 | 125 | °C |

5.4 Thermal Information: TLV9061

| THERMAL METRIC ⁽¹⁾ | | TLV9061 | | | UNIT |
|-------------------------------|--|--------------|------------|-------------|------|
| | | DBV (SOT-23) | DCK (SC70) | DPW (X2SON) | |
| | | 5 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 221.7 | 263.3 | 467 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 144.7 | 75.5 | 211.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 49.7 | 51 | 332.2 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 26.1 | 1 | 29.3 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 49 | 50.3 | 330.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | 125 | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.5 Thermal Information: TLV9061S

| THERMAL METRIC ⁽¹⁾ | | TLV9061S | | UNIT |
|-------------------------------|--|--------------|------------|------|
| | | DBV (SOT-23) | DRY (USON) | |
| | | 6 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 216.5 | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 155.1 | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 96.2 | TBD | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 80.3 | TBD | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 95.9 | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#).

5.6 Thermal Information: TLV9062

| THERMAL METRIC ⁽¹⁾ | | TLV9062 | | | | | UNIT |
|-------------------------------|--|----------|-------------|-----------|------------|--------------|------|
| | | D (SOIC) | DGK (VSSOP) | DSG (WSN) | PW (TSSOP) | DDF (SOT-23) | |
| | | 8 PINS | 8 PINS | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 157.6 | 201.2 | 94.4 | 205.1 | 184.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 104.6 | 85.7 | 116.5 | 93.7 | 112.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 99.7 | 122.9 | 61.3 | 135.7 | 99.9 | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter | 55.6 | 21.2 | 13 | 25.0 | 18.7 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter | 99.2 | 121.4 | 61.7 | 134.0 | 99.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | 34.4 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.7 Thermal Information: TLV9062S

| THERMAL METRIC ⁽¹⁾ | | TLV9002S | | | UNIT |
|-------------------------------|--|-------------|-------------|-------------|------|
| | | YCK (DSBGA) | RUG (X2QFN) | DGS (VSSOP) | |
| | | 9 PINS | 10 PINS | 10 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 129.8 | 197.2 | 170.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 0.9 | 93.3 | 84.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 37.5 | 123.8 | 113.5 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.5 | 3.7 | 16.4 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 37.1 | 120.2 | 112.3 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.8 Thermal Information: TLV9064

| THERMAL METRIC ⁽¹⁾ | | TLV9064 | | | | UNIT |
|-------------------------------|--|------------|----------|------------|-------------|------|
| | | PW (TSSOP) | D (SOIC) | RTE (WQFN) | RUC (X2QFN) | |
| | | 14 PINS | 14 PINS | 16 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 135.8 | 106.9 | 65.1 | 205.5 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 64 | 64 | 67.9 | 72.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 79 | 63 | 40.4 | 150.2 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 15.7 | 25.9 | 5.5 | 3.0 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 78.4 | 62.7 | 40.2 | 149.6 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | 23.8 | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.9 Thermal Information: TLV9064S

| THERMAL METRIC ⁽¹⁾ | | TLV9064S | UNIT |
|-------------------------------|--|------------|------|
| | | RTE (WQFN) | |
| | | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 65.1 | °C/W |
| R _{θJC(top)} | Junction-to-case(top) thermal resistance | 67.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 40.4 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 5.5 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 40.2 | °C/W |
| R _{θJC(bot)} | Junction-to-case(bottom) thermal resistance | 23.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

5.10 Electrical Characteristics

For V_S (Total Supply Voltage) = $(V+) - (V-) = 1.8V$ to $5.5V$ at $T_A = 25^\circ C$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|--|--|------------|---------|------------|------------------|
| OFFSET VOLTAGE | | | | | | |
| V _{OS} | Input offset voltage | V _S = 5V | | ±0.3 | ±1.6 | mV |
| | | V _S = 5V, T _A = −40°C to 125°C | | | ±2 | |
| dV _{OS} /dT | Drift | V _S = 5V, T _A = −40°C to 125°C | | ±0.53 | | µV/°C |
| PSRR | Power-supply rejection ratio | V _S = 1.8V – 5.5V, V _{CM} = (V−) | | ±7 | ±80 | µV/V |
| | Channel separation, DC | At DC | | 100 | | dB |
| INPUT VOLTAGE RANGE | | | | | | |
| V _{CM} | Common-mode voltage range | V _S = 1.8V to 5.5V | (V−) − 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | V _S = 5.5V, (V−) − 0.1V < V _{CM} < (V+) − 1.4V, T _A = −40°C to 125°C | 80 | 103 | | dB |
| | | V _S = 5.5V, V _{CM} = −0.1V to 5.6V, T _A = −40°C to 125°C | 57 | 87 | | |
| | | V _S = 1.8V, (V−) − 0.1V < V _{CM} < (V+) − 1.4V, T _A = −40°C to 125°C | | 88 | | |
| | | V _S = 1.8V, V _{CM} = −0.1V to 1.9V, T _A = −40°C to 125°C | | 81 | | |
| INPUT BIAS CURRENT | | | | | | |
| I _B | Input bias current | | | ±0.5 | | pA |
| I _{OS} | Input offset current | | | ±0.05 | | pA |
| NOISE | | | | | | |
| E _n | Input voltage noise (peak-to-peak) | V _S = 5V, f = 0.1Hz to 10Hz | | 4.77 | | µV _{PP} |
| e _n | Input voltage noise density | V _S = 5V, f = 10kHz | | 10 | | nV/√Hz |
| | | V _S = 5V, f = 1kHz | | 16 | | |
| i _n | Input current noise density | f = 1kHz | | 23 | | fA/√Hz |
| INPUT CAPACITANCE | | | | | | |
| C _{ID} | Differential | | | 2 | | pF |
| C _{IC} | Common-mode | | | 4 | | pF |
| OPEN-LOOP GAIN | | | | | | |
| A _{OL} | Open-loop voltage gain | V _S = 1.8V, (V−) + 0.04V < V _O < (V+) − 0.04V, R _L = 10kΩ | | 100 | | dB |
| | | V _S = 5.5V, (V−) + 0.05V < V _O < (V+) − 0.05V, R _L = 10kΩ | 104 | 130 | | |
| | | V _S = 1.8V, (V−) + 0.06V < V _O < (V+) − 0.06V, R _L = 2kΩ | | 100 | | |
| | | V _S = 5.5V, (V−) + 0.15V < V _O < (V+) − 0.15V, R _L = 2kΩ | | 130 | | |
| FREQUENCY RESPONSE | | | | | | |
| GBP | Gain bandwidth product | V _S = 5V, G = +1 | | 10 | | MHz |
| φ _m | Phase margin | V _S = 5V, G = +1 | | 55 | | ° |
| SR | Slew rate | V _S = 5V, G = +1 | | 6.5 | | V/µs |
| t _S | Settling time | To 0.1%, V _S = 5V, 2V step , G = +1, C _L = 100pF | | 0.5 | | µs |
| | | To 0.01%, V _S = 5V, 2V step, G = +1, C _L = 100pF | | 1 | | |
| t _{OR} | Overload recovery time | V _S = 5V, V _{IN} × gain > V _S | | 0.2 | | µs |
| THD + N | Total harmonic distortion + noise ⁽¹⁾ | V _S = 5.5V, V _{CM} = 2.5V, V _O = 1V _{RMS} , G = +1, f = 1kHz | | 0.0008% | | |
| OUTPUT | | | | | | |
| V _O | Voltage output swing from supply rails | V _S = 5.5V, R _L = 10kΩ | | | 20 | mV |
| | | V _S = 5.5V, R _L = 2kΩ | | | 60 | |
| I _{SC} | Short-circuit current | V _S = 5V | | ±50 | | mA |

5.10 Electrical Characteristics (continued)

For V_S (Total Supply Voltage) = $(V+) - (V-) = 1.8V$ to $5.5V$ at $T_A = 25^\circ C$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------------------|---|--|--|-----|-------------|-------------|----------|
| Z _O | Open-loop output impedance | V _S = 5V, f = 10MHz | | | 100 | | Ω |
| POWER SUPPLY | | | | | | | |
| I _Q | Quiescent current per amplifier | V _S = 5.5V, I _O = 0mA | | | 538 | 750 | μA |
| | | V _S = 5.5V, I _O = 0mA, T _A = −40°C to 125°C | | | | 800 | |
| SHUTDOWN | | | | | | | |
| I _{QSD} | Quiescent current per amplifier | V _S = 1.8V to 5.5V, all amplifiers disabled, $\overline{\text{SHDN}}$ = Low | | | 0.5 | 1.5 | μA |
| Z _{SHDN} | Output impedance during shutdown | V _S = 1.8V to 5.5V, amplifier disabled | | | 10 8 | | GΩ pF |
| V _{SHDN_THR_HI} | High level voltage shutdown threshold (amplifier enabled) | V _S = 1.8V to 5.5V | | | (V−) + 0.9V | (V−) + 1.1V | V |
| V _{SDHN_THR_LO} | Low level voltage shutdown threshold (amplifier disabled) | V _S = 1.8V to 5.5V | | | (V−) + 0.2V | (V−) + 0.7V | V |
| t _{ON} | Amplifier enable time (shutdown) (2) | V _S = 1.8V to 5.5V, full shutdown; G = 1, V _{OUT} = 0.9 × V _S / 2, R _L connected to V− | | | 10 | | μs |
| t _{OFF} | Amplifier disable time ⁽²⁾ | V _S = 1.8V to 5.5V, G = 1, V _{OUT} = 0.1 × V _S / 2, R _L connected to V− | | | 0.6 | | μs |
| | $\overline{\text{SHDN}}$ pin input bias current (per pin) | V _S = 1.8V to 5.5V, V+ ≥ $\overline{\text{SHDN}}$ ≥ (V+) − 0.8V | | | 130 | | pA |
| | | V _S = 1.8V to 5.5V, V− ≤ $\overline{\text{SHDN}}$ ≤ V− + 0.8V | | | 40 | | |

(1) Third-order filter; bandwidth = 80kHz at -3dB .

(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the \overline{SHDN} pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

5.11 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

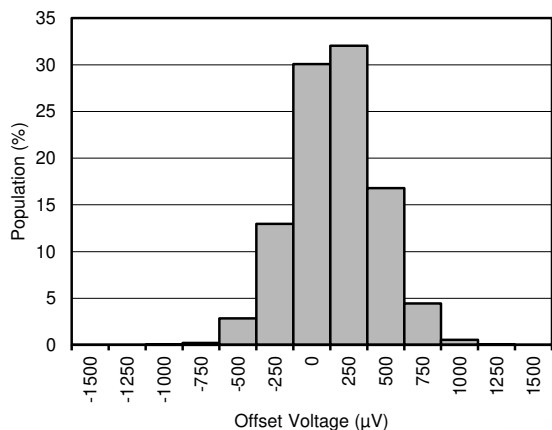
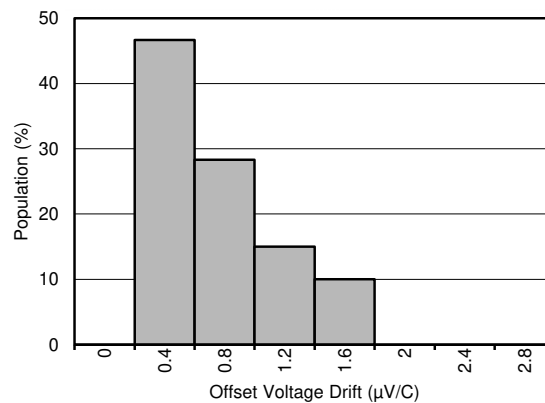


Figure 5-1. Offset Voltage Production Distribution



$T_A = -40^\circ\text{C}$ to 125°C

Figure 5-2. Offset Voltage Drift Distribution

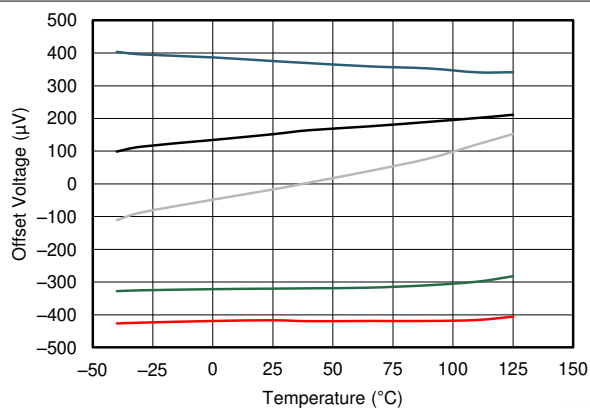
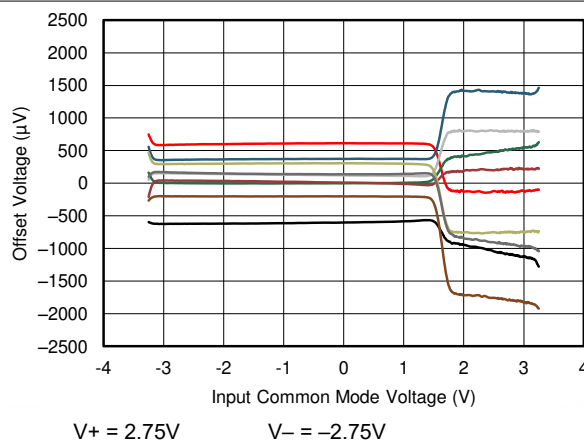


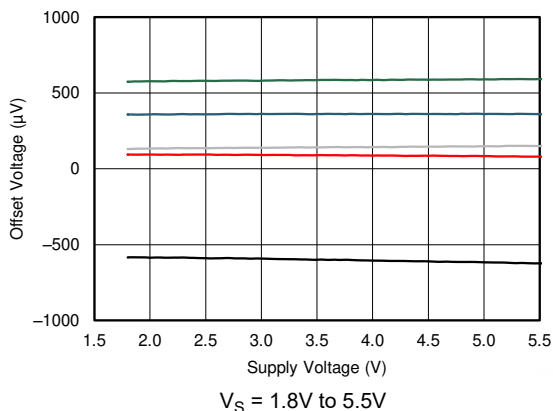
Figure 5-3. Offset Voltage vs Temperature



$V_+ = 2.75\text{V}$

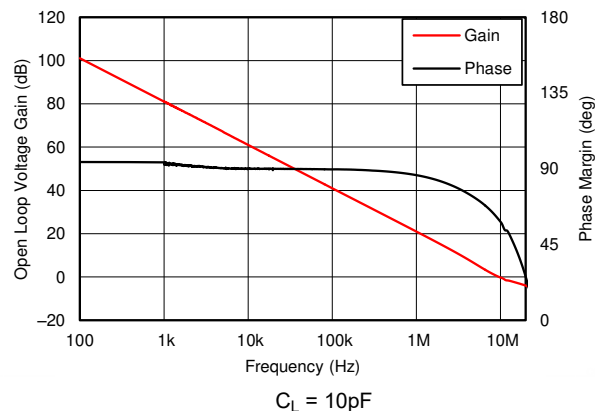
$V_- = -2.75\text{V}$

Figure 5-4. Offset Voltage vs Common-Mode Voltage



$V_S = 1.8\text{V}$ to 5.5V

Figure 5-5. Offset Voltage vs Power Supply



$C_L = 10\text{pF}$

Figure 5-6. Open-Loop Gain and Phase vs Frequency

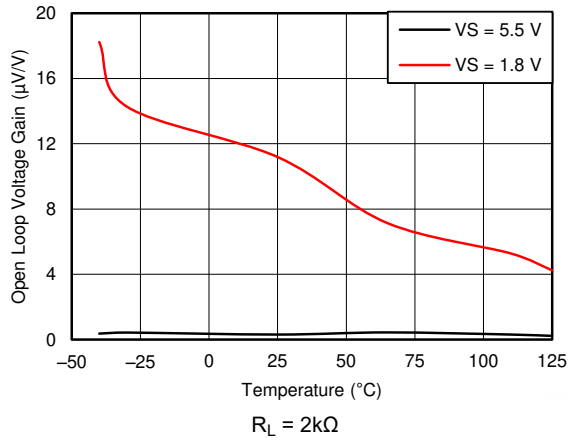


Figure 5-7. Open-Loop Gain vs Temperature

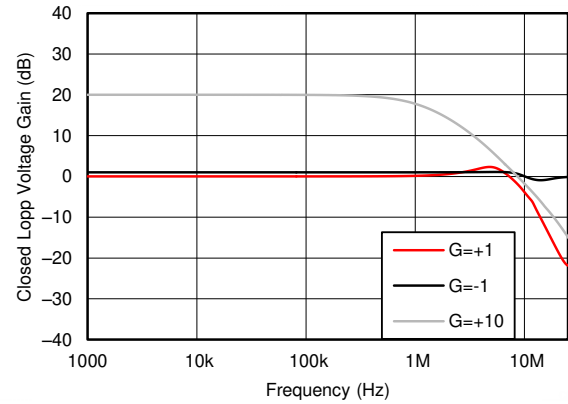


Figure 5-8. Closed-Loop Gain vs Frequency

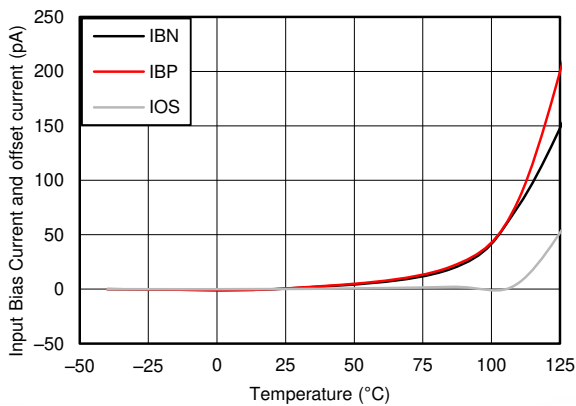


Figure 5-9. Input Bias Current vs Temperature

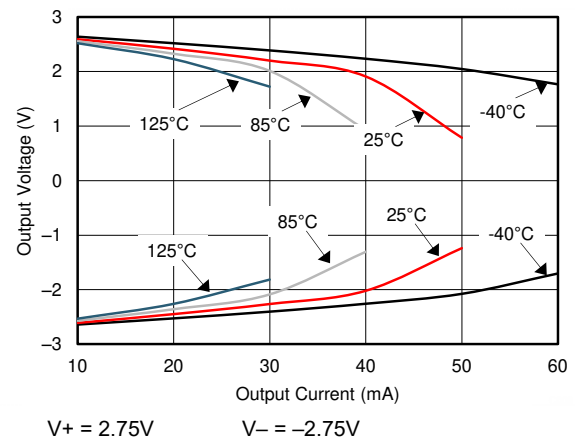


Figure 5-10. Output Voltage Swing vs Output Current

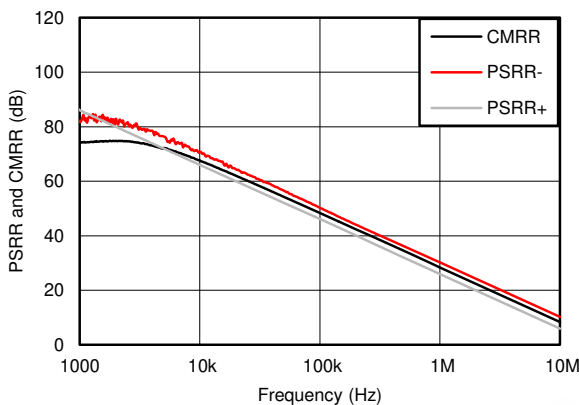


Figure 5-11. CMRR and PSRR vs Frequency (Referred to Input)

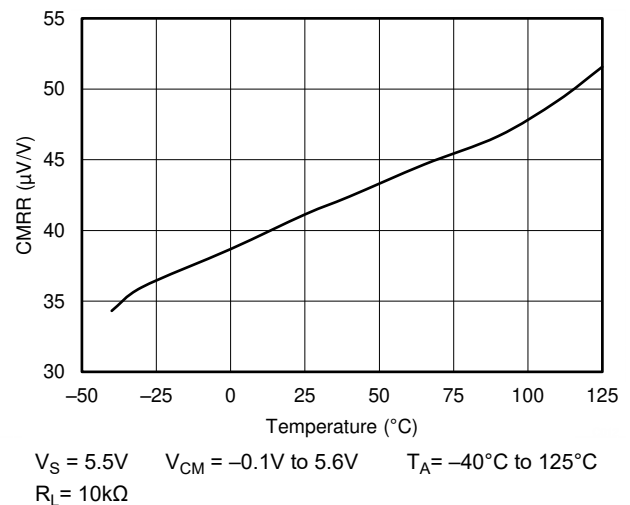
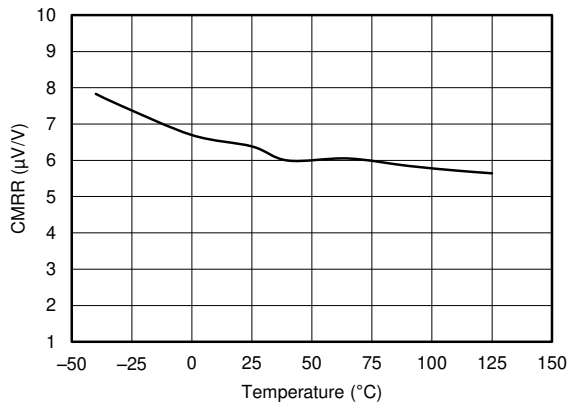
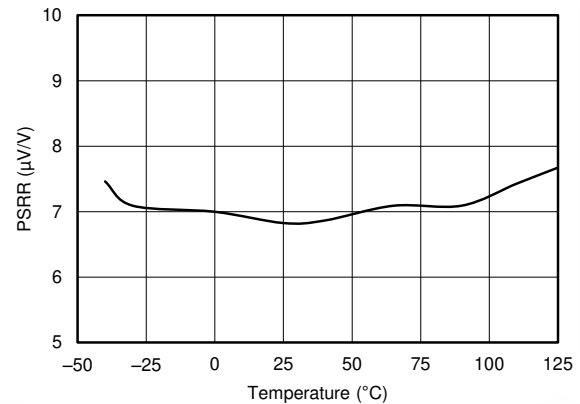


Figure 5-12. CMRR vs Temperature



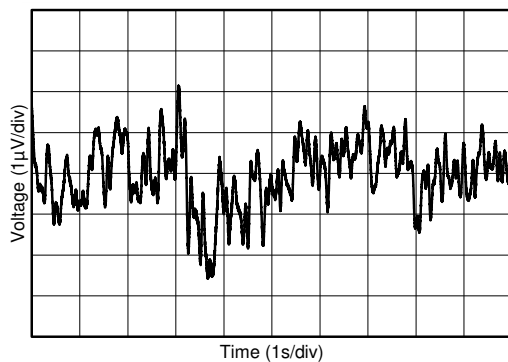
$V_{CM} = (V-) - 0.1V \text{ to } (V+) - 1.4V$
 $T_A = -40^\circ\text{C to } 125^\circ\text{C}$ $R_L = 10k\Omega$ $V_S = 5.5V$

Figure 5-13. CMRR vs Temperature



$V_S = 1.8V \text{ to } 5.5V$

Figure 5-14. PSRR vs Temperature



$V_S = 1.8V \text{ to } 5.5V$

Figure 5-15. 0.1Hz to 10Hz Input Voltage Noise

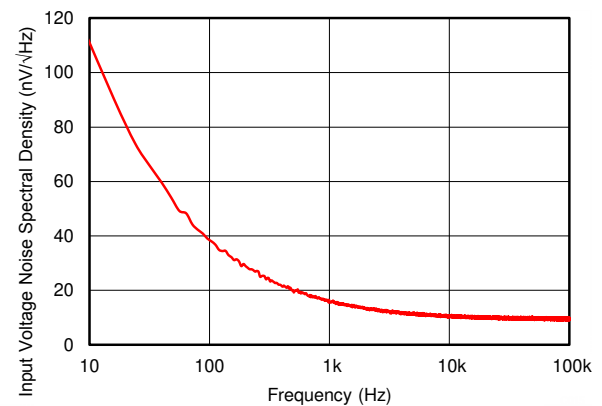
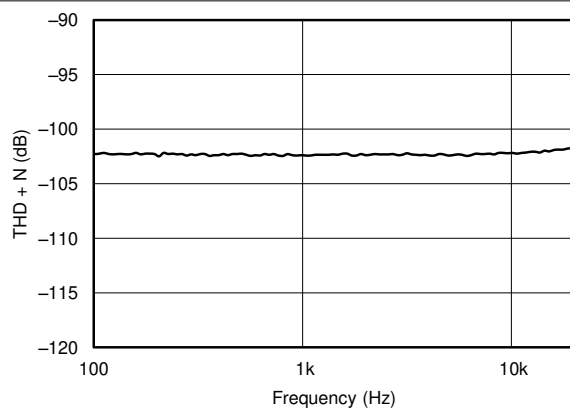
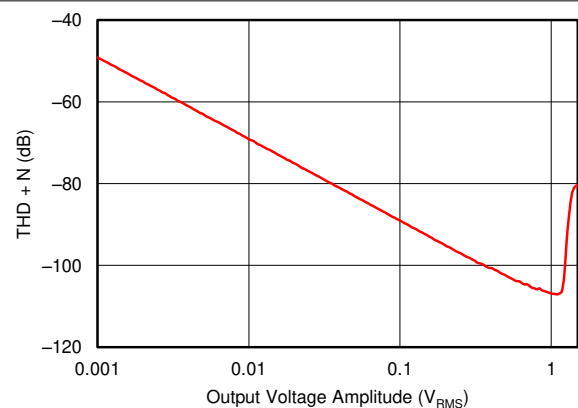


Figure 5-16. Input Voltage Noise Spectral Density vs Frequency



$V_S = 5.5V$ $V_{CM} = 2.5V$ $R_L = 2k\Omega$
 $V_{OUT} = 0.5V_{RMS}$ $BW = 80kHz$ $G = +1$

Figure 5-17. THD + N vs Frequency



$V_S = 5.5V$ $R_L = 2k\Omega$ $G = +1$
 $V_{CM} = 2.5V$ $BW = 80kHz$ $f = 1kHz$

Figure 5-18. THD + N vs Amplitude

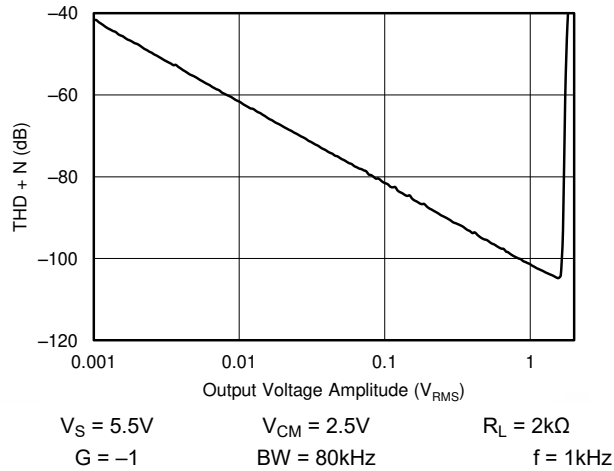


Figure 5-19. THD + N vs Amplitude

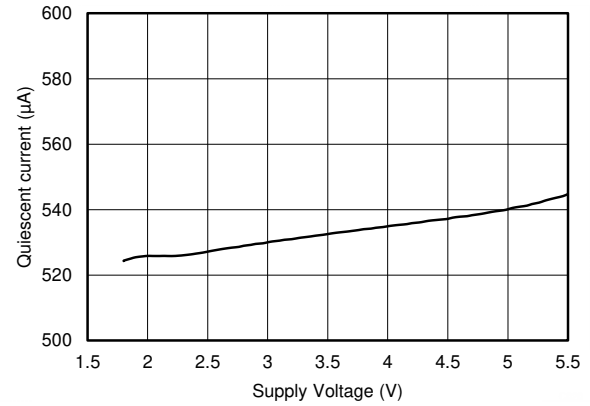


Figure 5-20. Quiescent Current vs Supply Voltage

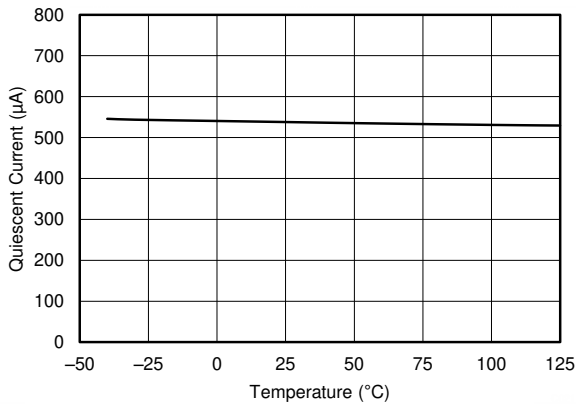


Figure 5-21. Quiescent Current vs Temperature

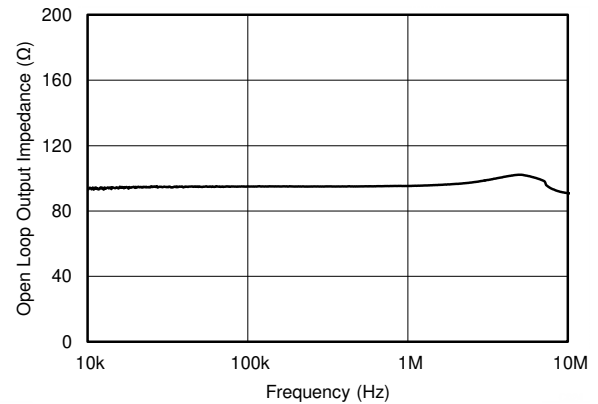


Figure 5-22. Open-Loop Output Impedance vs Frequency

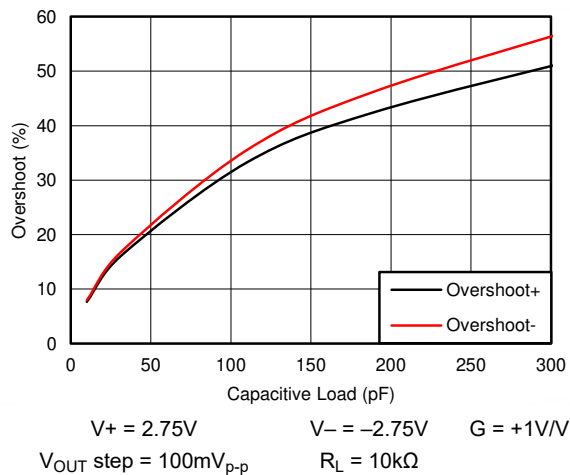


Figure 5-23. Small-Signal Overshoot vs Load Capacitance

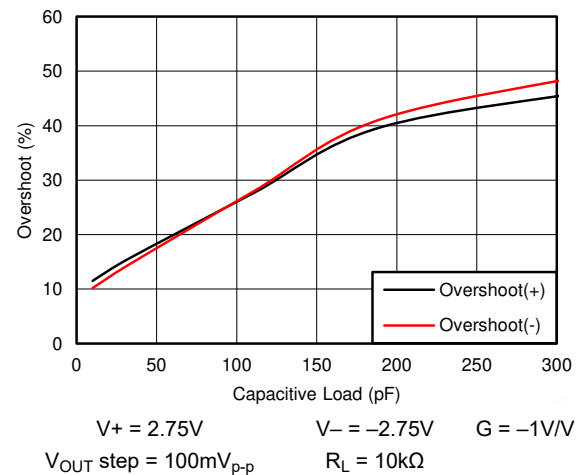
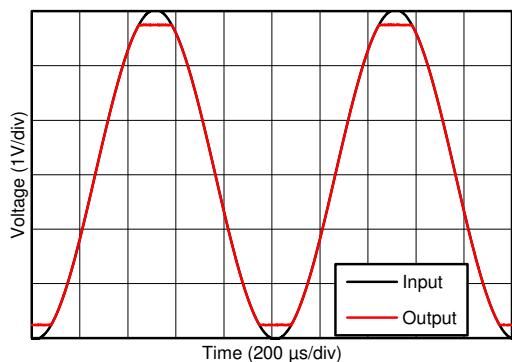
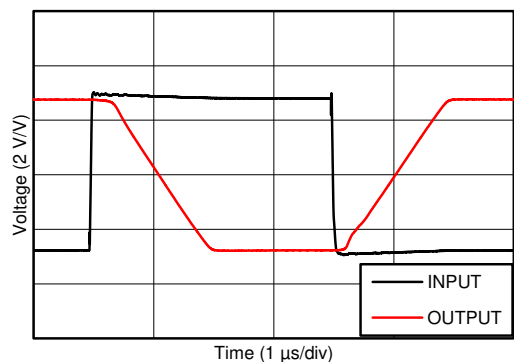


Figure 5-24. Small-Signal Overshoot vs Load Capacitance



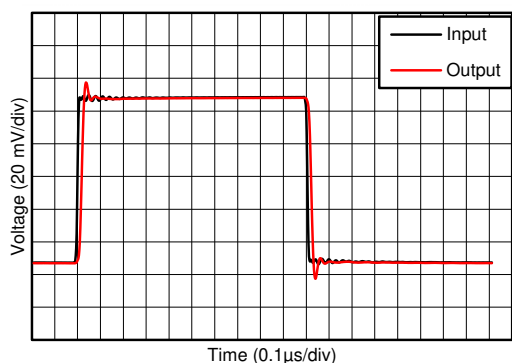
$V_+ = 2.75V$ $V_- = -2.75V$

Figure 5-25. No Phase Reversal



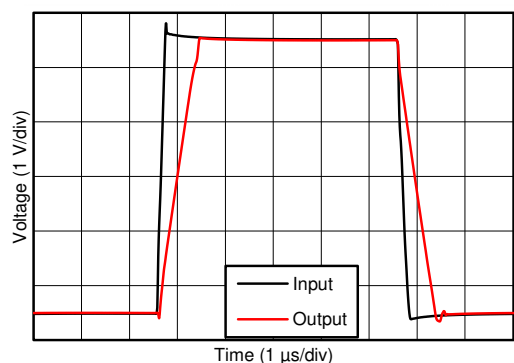
$V_+ = 2.75V$ $V_- = -2.75V$ $G = -10V/V$

Figure 5-26. Overload Recovery



$V_+ = 2.75V$ $V_- = -2.75V$ $G = 1V/V$

Figure 5-27. Small-Signal Step Response



$V_+ = 2.75V$ $V_- = -2.75V$ $C_L = 100pF$
 $G = 1V/V$

Figure 5-28. Large-Signal Step Response

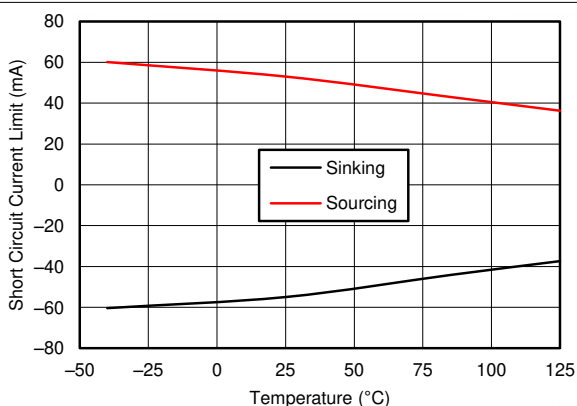
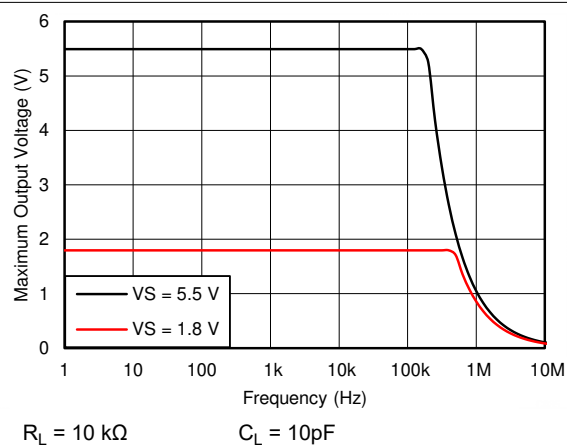


Figure 5-29. Short-Circuit Current vs Temperature



$R_L = 10\text{ k}\Omega$ $C_L = 10pF$

Figure 5-30. Maximum Output Voltage vs Frequency and Supply Voltage

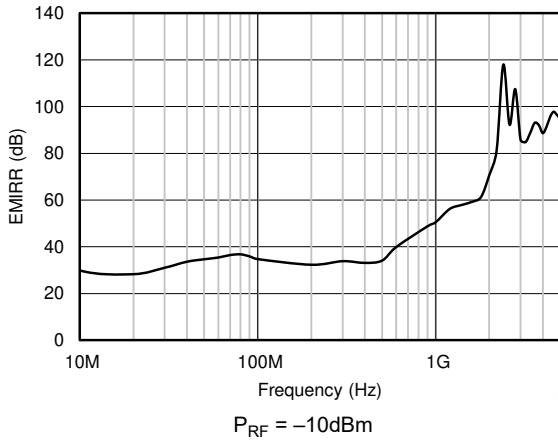


Figure 5-31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

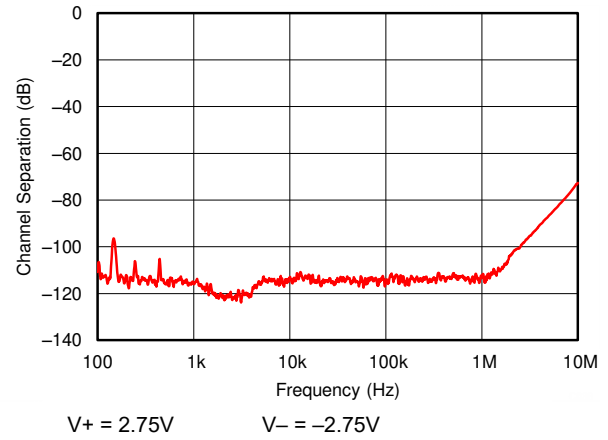


Figure 5-32. Channel Separation vs Frequency

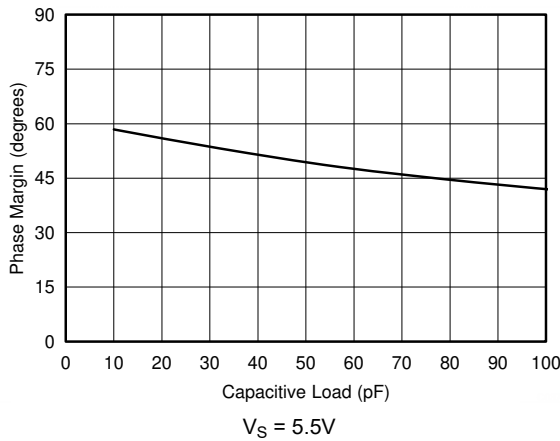


Figure 5-33. Phase Margin vs Capacitive Load

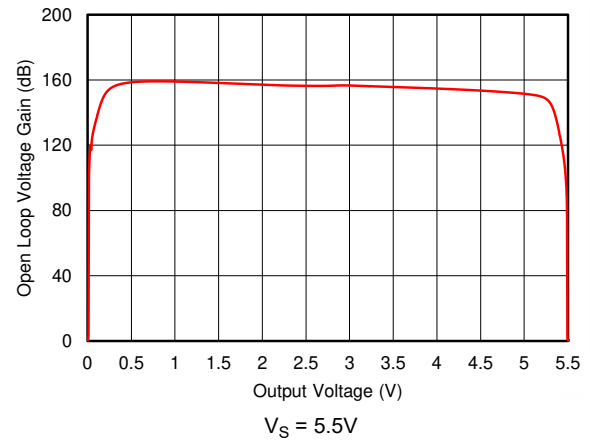


Figure 5-34. Open Loop Voltage Gain vs Output Voltage

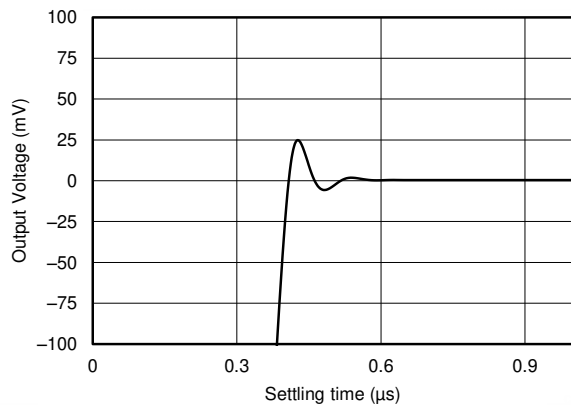


Figure 5-35. Large Signal Settling Time (Positive)

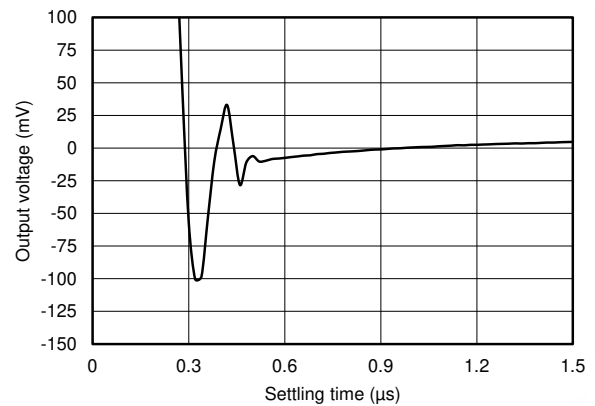


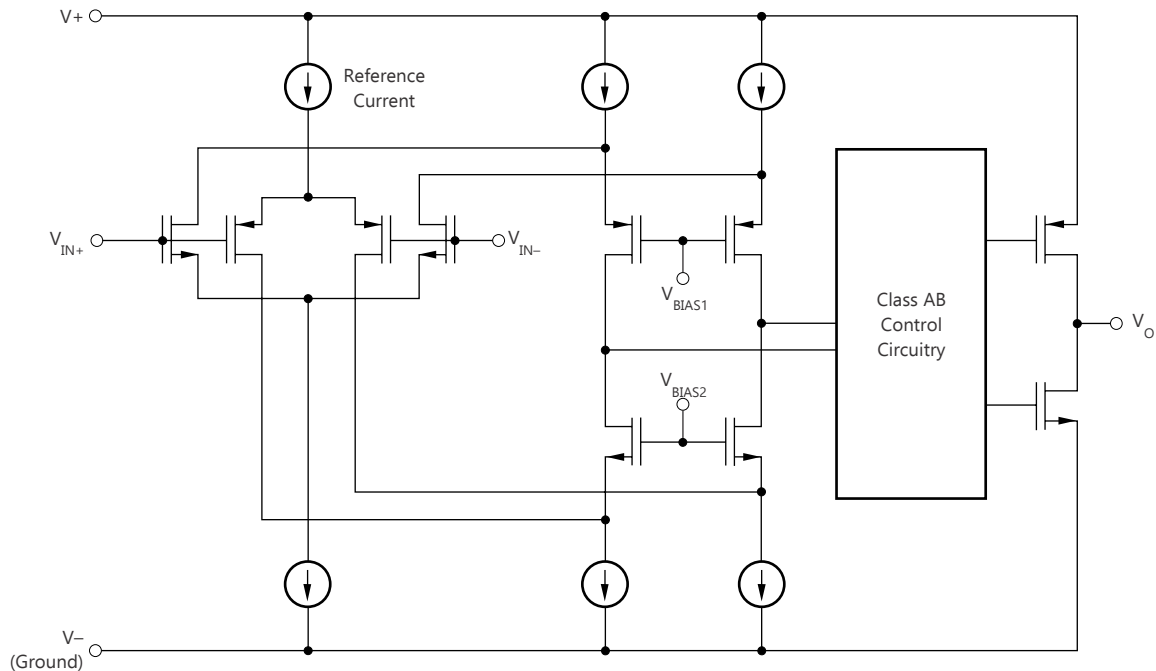
Figure 5-36. Large Signal Settling Time (Negative)

6 Detailed Description

6.1 Overview

The TLV906x devices are a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8V to 5.5V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. The high bandwidth enables this family to drive the sample-and-hold circuitry of analog-to-digital converters (ADCs).

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x family extends 100mV beyond the supply rails for the full supply voltage range of 1.8V to 5.5V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.4V$ to 200mV above the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately $(V+) - 1.4V$. There is a small transition region, typically $(V+) - 1.2V$ to $(V+) - 1V$, in which both pairs are on. This 200-mV transition region can vary up to 200mV with process variation. Thus, the transition region (with both stages on) can range from $(V+) - 1.4V$ to $(V+) - 1.2V$ on the low end, and up to $(V+) - 1V$ to $(V+) - 0.8V$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

6.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10k Ω , the output swings to within 15mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

6.3.3 EMI Rejection

The TLV906x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV906x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. [Figure 6-1](#) shows the results of this testing on the TLV906x. [Table 6-1](#) lists the EMIRR IN+ values for the TLV906x at particular frequencies commonly encountered in real-world applications. See [EMI Rejection Ratio of Operational Amplifiers application note](#) for more information.

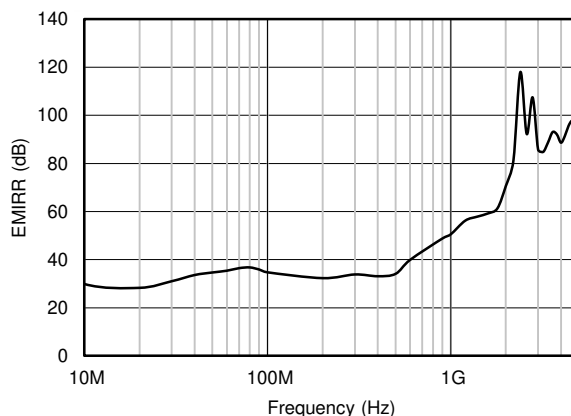


Figure 6-1. EMIRR Testing

Table 6-1. TLV906x EMIRR IN+ For Frequencies of Interest

| FREQUENCY | APPLICATION or ALLOCATION | EMIRR IN+ |
|-----------|--|-----------|
| 400MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 59.5dB |
| 900MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications | 68.9dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz) | 77.8dB |
| 2.4GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz) | 78.0dB |

Table 6-1. TLV906x EMIRR IN+ For Frequencies of Interest (continued)

| FREQUENCY | APPLICATION or ALLOCATION | EMIRR IN+ |
|-----------|---|-----------|
| 3.6GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 88.8dB |
| 5GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz) | 87.6dB |

6.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x family is approximately 200ns.

6.3.5 Shutdown Function

The TLV906xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the op amp into a low-power standby mode. In this mode, the op amp typically consumes less than 1 μ A. The $\overline{\text{SHDN}}$ pins are active-low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V_- and $V_- + 0.2V$. A valid logic high is defined as a voltage between $V_- + 1.2V$ and V_+ . The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit. There is **no** internal pull-up to enable the amplifier.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 μ s for full shutdown of all channels; disable time is 6 μ s. When disabled, the output assumes a high-impedance state. This architecture allows the TLV906xS to operate as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10k Ω load to midsupply ($V_S / 2$) is required. If using the TLV906xS without a load, the resulting turnoff time is significantly increased.

6.4 Device Functional Modes

The TLV906x family are operational when the power-supply voltage is between 1.8V ($\pm 0.9V$) and 5.5V ($\pm 2.75V$). The TLV906xS devices feature a shutdown mode and are shut down when a valid logic low is applied to the shutdown pin.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV906x family features 10MHz bandwidth and 6.5V/ μ s slew rate with only 538 μ A of supply current per channel, providing good AC-performance at very low power consumption. DC applications are well served with a very low input noise voltage of 10nV/ $\sqrt{\text{Hz}}$ at 10kHz, low input bias current, and a typical input offset voltage of 0.3mV.

7.2 Typical Applications

7.2.1 Typical Low-Side Current Sense Application

Figure 7-1 shows the TLV906x configured in a low-side current-sensing application.

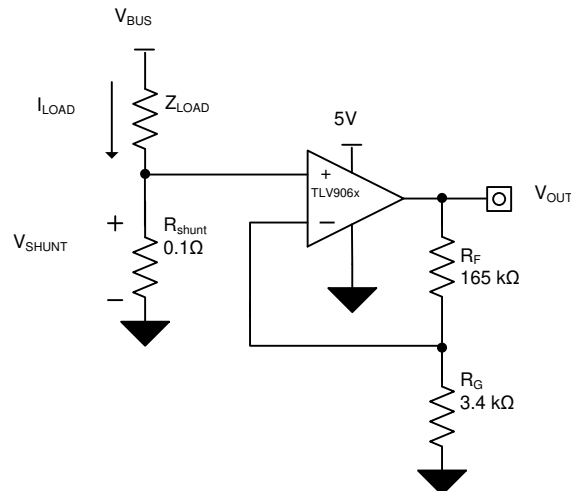


Figure 7-1. TLV906x in a Low-Side, Current-Sensing Application

7.2.2 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.95V
- Maximum shunt voltage: 100mV

7.2.3 Detailed Design Procedure

The transfer function of the circuit in [Figure 7-1](#) is given in [Equation 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times GAIN \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using [Equation 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using [Equation 2](#), R_{SHUNT} equals 100m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV906x to produce an output voltage of approximately 0V to 4.95V. [Equation 3](#) calculates the gain required for the TLV906x to produce the required output voltage.

$$Gain = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using [Equation 3](#), the required gain equals 49.5V/V, which is set with the R_F and R_G resistors. [Equation 4](#) sizes the R_F and R_G resistors to set the gain of the TLV906x to 49.5V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F to equal 165k Ω and R_G to equal 3.4k Ω provides a combination that equals approximately 49.5V/V. [Figure 7-2](#) shows the measured transfer function of the circuit shown in [Figure 7-1](#). Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistor values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

7.2.4 Application Curve

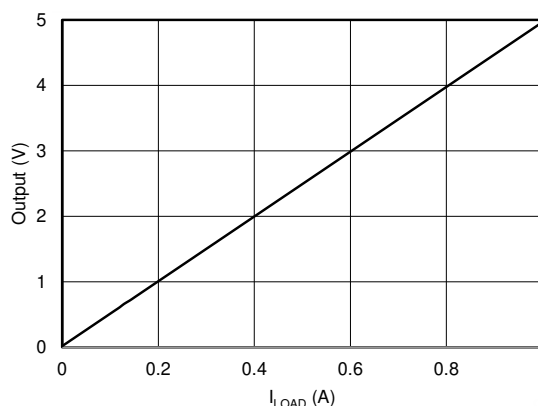


Figure 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV906x series is specified for operation from 1.8V to 5.5V ($\pm 0.9V$ to $\pm 2.75V$); many specifications apply from $-40^{\circ}C$ to $125^{\circ}C$. The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6V can permanently damage the device; see the [Absolute Maximum Ratings](#) table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout](#) section.

7.3.1 Input and ESD Protection

The TLV906x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA, as shown in the [Absolute Maximum Ratings](#) table. [Figure 7-3](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

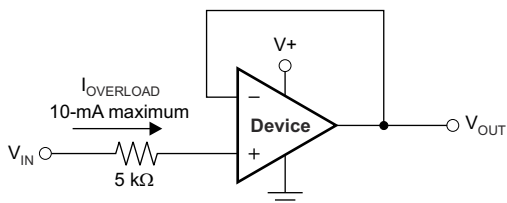


Figure 7-3. Input Current Protection

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1 μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [Figure 7-5](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

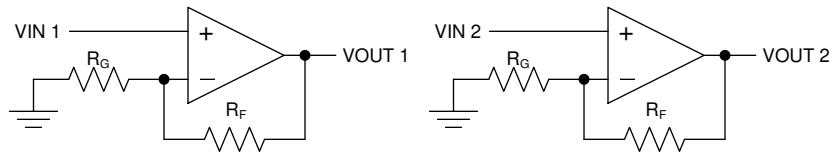


Figure 7-4. Schematic Representation for the Layout Example

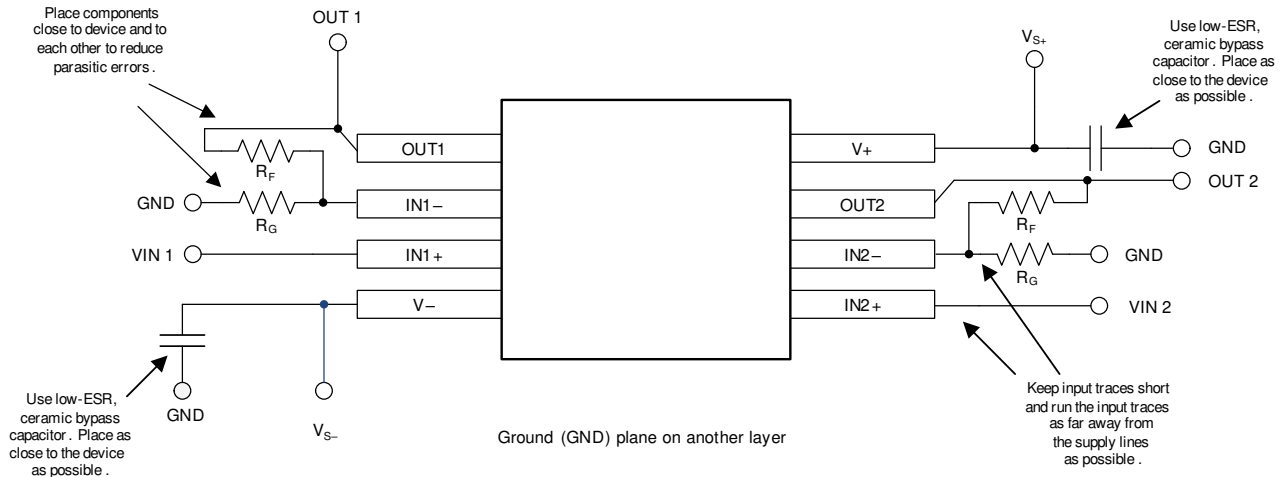


Figure 7-5. Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Circuit Board Layout Techniques](#)
- Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#) application note
- Texas Instruments, [QFN/SON PCB Attachment](#) application note
- Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#) application note
- Texas Instruments, [Single-Ended Input to Differential Output Conversion Circuit](#) design guide
- Texas Instruments, [TLVx313 Low-Power, Rail-to-Rail In/Out, 500-μV Typical Offset, 1MHz Operational Amplifier for Cost-Sensitive Systems](#) data sheet
- Texas Instruments, [TLVx314 3MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier](#) data sheet

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

Bluetooth® is a registered trademark of Bluetooth SIG, Inc.

All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision L (September 2024) to Revision M (December 2024) | Page |
|--|------|
| • Changed TLV9061S DBV (SOT-23) pinout drawing to match the <i>Pin Functions</i> table..... | 4 |
| Changes from Revision K (July 2024) to Revision L (September 2024) | Page |
| • Deleted package preview note from TLV9062S (YCK, DSBGA) package in <i>Device Information</i> table | 1 |

| Changes from Revision J (September 2019) to Revision K (July 2024) | Page |
|---|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Updated the <i>Device Information</i> table..... | 1 |
| • Added package preview note for TLV9062S (YCK, DSBGA) package in <i>Device Information</i> table | 1 |
| • Added YCK packages to the <i>Device Comparison</i> table..... | 3 |
| • Added TLV9062S YCK (DSBGA) pinout drawing to <i>Pin Configuration and Functions</i> section..... | 4 |

| Changes from Revision I (May 2019) to Revision J (September 2019) | Page |
|--|-------------|
| • Deleted TLV9062IDDFR (SOT-23, 8) package preview notations throughout data sheet..... | 1 |
| • Added industry standard package names to <i>Device Comparison Table</i> | 3 |
| • Added note to packages with thermal pads, specifying that the thermal pads need to be connected to V–..... | 4 |
| • Added link to <i>Shutdown Function</i> section in $\overline{\text{SHDN}}$ pin function rows..... | 4 |
| • Added <i>EMI Rejection</i> section to the <i>Feature Description</i> section..... | 21 |
| • Changed <i>Shutdown Function</i> section to add more clarification | 22 |

| Changes from Revision H (April 2019) to Revision I (May 2019) | Page |
|--|-------------|
| • Added DDF (SOT-23) thermal information to replace TBDs..... | 10 |

| Changes from Revision G (December 2018) to Revision H (April 2019) | Page |
|---|-------------|
| • Added (SOT-23, 8) information to <i>Device Information</i> | 1 |
| • Added DDF package column to <i>Device Comparison Table</i> | 3 |
| • Added DDF (SOT-23) package, to <i>Pin Functions</i> | 4 |
| • Added DDF (SOT-23) package to <i>Thermal Information</i> | 10 |

| Changes from Revision F (September 2018) to Revision G (December 2018) | Page |
|---|-------------|
| • Changed TLV9064 RUC package name from: (WQFN, 14) to: (X2QFN, 14) in <i>Device Information</i> table..... | 1 |
| • Added RUC (X2QFN) package, pinout information to Pin Functions: TLV9064 table..... | 4 |
| • Added TLV9064 RUC (X2QFN) pinout drawing to <i>Pin Configuration and Functions</i> section..... | 4 |
| • Added RUC (X2QFN) to Thermal Information: TLV9064 table..... | 11 |

| Changes from Revision E (July 2018) to Revision F (September 2018) | Page |
|--|-------------|
| • Deleted Shutdown part numbers from data sheet header | 1 |
| • Deleted (X2QFN, 10) package from TLV9062 <i>Device Information</i> table..... | 1 |
| • Added references to shutdown part numbers in Description section | 1 |
| • Changed TLV906xS series to TLV906xS family throughout data sheet..... | 1 |
| • Added Shutdown devices to Device Comparison Table | 3 |
| • Changed pin namings for all pinout drawings to reflect updated nomenclature | 4 |
| • Added TLV9061S Thermal Information Table..... | 10 |
| • Added TLV9064S Thermal Information Table..... | 11 |
| • Deleted Partial Shutdown Amplifier Enable Time..... | 12 |
| • Added clarification on selecting resistors for a current sensing application in the Typical Applications Section | 24 |
| • Changed wording of third bullet in Layout Guidelines..... | 26 |

| Changes from Revision D (June 2018) to Revision E (July 2018) | Page |
|---|------|
| • Added TLV9061S device to <i>Device Information</i> table..... | 1 |
| • Added TLV9064S device to <i>Device Information</i> table..... | 1 |
| • Added RUC and RUG packages to the <i>Device Comparison</i> table..... | 3 |
| • Added TLV9061S DBV (SOT-23) pinout drawing to <i>Pin Configuration and Functions</i> section..... | 4 |
| • Added TLV9061S DBV (SOT-23) package, pinout information to <i>Pin Functions: TLV9061S</i> table..... | 4 |
| • Added TLV9062S RUG (VSSOP) package, pinout drawing to <i>Pin Configuration and Functions</i> section..... | 4 |
| • Added TLV9064 RTE pinout information to <i>Pin Functions: TLV9064</i> table..... | 4 |
| • Added TLV9064S RTE (WQFN) pinout drawing to <i>Pin Configuration and Functions</i> section | 4 |
| • Added TLV9062S RUG (VSSOP) package, pinout information to <i>Pin Functions: TLV9062S</i> table..... | 4 |
| • Added TLV9064 RTE (WQFN) pinout drawing to <i>Pin Configuration and Functions</i> section | 4 |

| Changes from Revision C (March 2018) to Revision D (June 2018) | Page |
|--|------|
| • Added shutdown suffix to "TLV906x" to document title..... | 1 |
| • Added "Shutdown Version" bullet to <i>Features</i> list | 1 |
| • Added TLV9062S device to <i>Device Information</i> table..... | 1 |
| • Added shutdown text to <i>Description (continued)</i> section..... | 1 |
| • Added " $V_S = [V+] - [V-]$ " supply voltage parameter in <i>Absolute Maximum Ratings</i> table..... | 9 |
| • Added "input voltage range" and "output voltage range" parameters and values to <i>Recommended Operating Conditions</i> table..... | 9 |
| • Added shutdown pin recommended operating conditions in <i>Recommended Operating Conditions</i> table..... | 9 |
| • Added " T_A " symbol to "specified temperature" parameter to <i>Recommended Operating Conditions</i> table | 9 |
| • Added <i>Thermal Information: TLV9062S</i> thermal table data..... | 11 |
| • Added shutdown section to <i>Electrical Characteristics: V_S (Total Supply Voltage) = $(V+) - (V-) = 1.8V$ to $5.5V$</i> table..... | 12 |
| • Added <i>Shutdown Function</i> section | 22 |

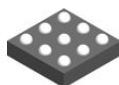
| Changes from Revision B (October 2017) to Revision C (March 2018) | Page |
|--|------|
| • Changed device status from Production Data/Mixed Status to Production Data | 1 |
| • Deleted package preview note from TLV9061 (DPW, X2SON) package in <i>Device Information</i> table | 1 |
| • Deleted package, preview note from TLV9061 DPW (X2SON) package, pinout drawing | 4 |
| • Changed formatting of <i>ESD Ratings</i> table to show different results for all packages | 9 |
| • Deleted package preview note from DPW (X2SON) package in <i>Thermal Information: TLV9061</i> table | 10 |
| • Deleted package preview note from DPW (X2SON) package in <i>Thermal Information: TLV9061</i> table | 10 |

| Changes from Revision A (June 2017) to Revision B (October 2017) | Page |
|--|------|
| • Added 8-pin PW package, to <i>Pin Configuration and Functions</i> section | 4 |
| • Added DSG (WSO) package to <i>Thermal Information</i> table..... | 10 |
| • Added PW (TSSOP) to TLV9062 <i>Thermal Information</i> table | 10 |
| • Changed maximum input offset voltage value from $\pm 1.6mV$ to $2mV$ | 12 |
| • Changed maximum input offset voltage value from ± 1.5 to $\pm 1.6mV$ | 12 |
| • Changed minimum common-mode rejection ratio input voltage range from 86dB to 80dB | 12 |
| • Changed typical input current noise density value from 10 to $23fA/\sqrt{Hz}$ | 12 |
| • Changed THD + N test conditions from $V_S = 5V$ to $V_S = 5.5V$ | 12 |
| • Added $V_{CM} = 2.5V$ test condition to THD + N parameter in <i>Electrical Characteristics</i> table | 12 |
| • Added maximum output voltage swing value from 25mV to 60mV..... | 12 |
| • Changed maximum output voltage swing value from 15mV to 20mV | 12 |

| Changes from Revision * (March 2017) to Revision A (June 2017) | Page |
|---|-------------------|
| • Changed device status from Advance Information to Production Data | 1 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

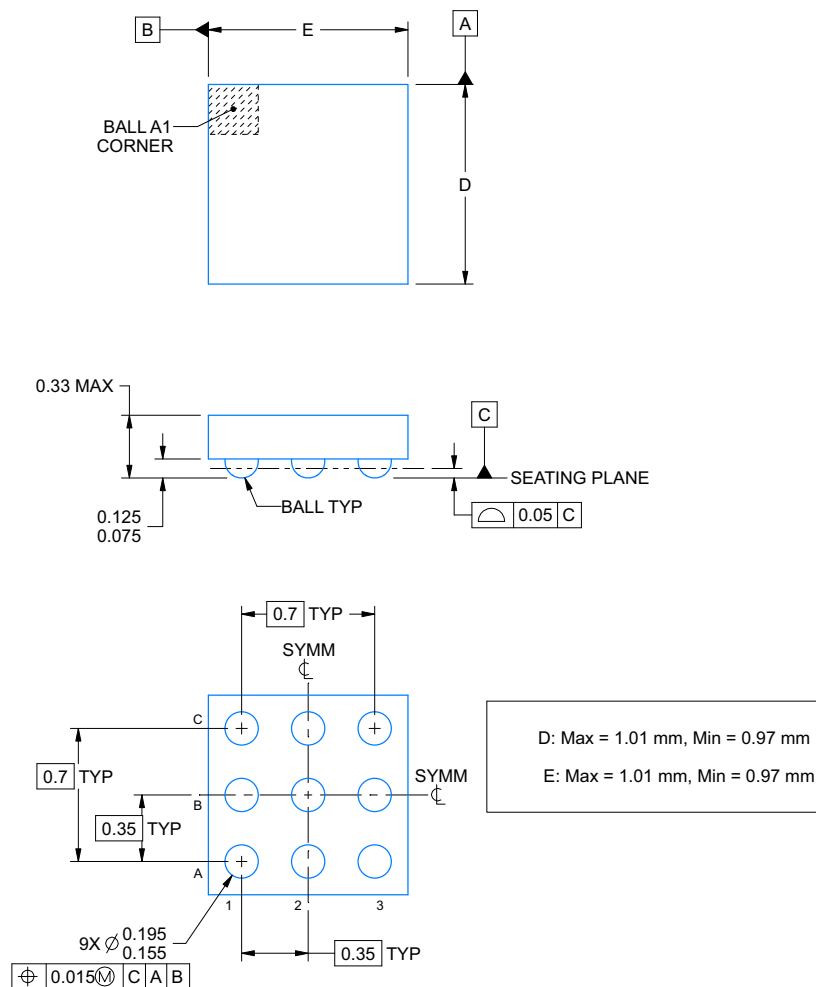


YCK0009-C01

PACKAGE OUTLINE

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



4226891/A 06/2021

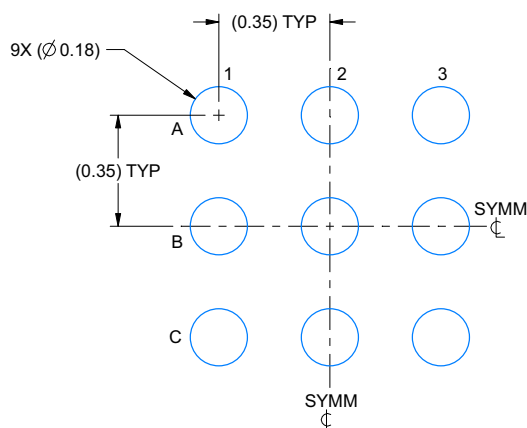
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

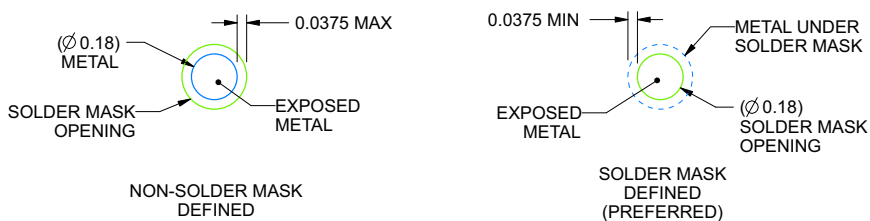
YCK0009-C01

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4226891/A 06/2021

NOTES: (continued)

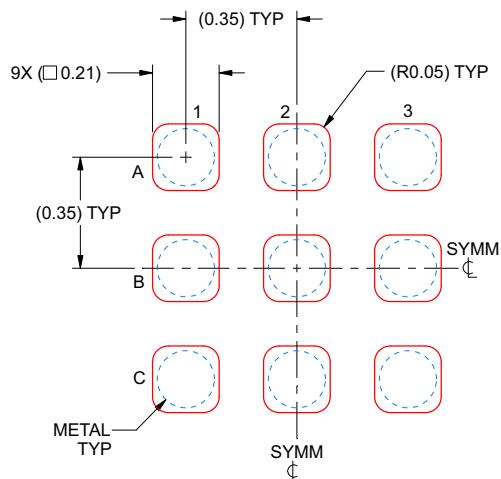
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0009-C01

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4226891/A 06/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|-----------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TLV9061IDBVR | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | 1OAF |
| TLV9061IDBVR.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OAF |
| TLV9061IDBVR.B | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | - | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OAF |
| TLV9061IDBVRG4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OAF |
| TLV9061IDBVRG4.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OAF |
| TLV9061IDCKR | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 1CA |
| TLV9061IDCKR.A | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | 1CA |
| TLV9061IDPWR | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (C, CG) |
| TLV9061IDPWR.A | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | (C, CG) |
| TLV9061SIDBVR | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OEF |
| TLV9061SIDBVR.A | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OEF |
| TLV9061SIDBVR.B | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | - | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OEF |
| TLV9061SIDBVRG4 | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OEF |
| TLV9061SIDBVRG4.A | Active | Production | SOT-23 (DBV) 6 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1OEF |
| TLV9062IDDFR | Active | Production | SOT-23-THIN (DDF) 8 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDDFR.A | Active | Production | SOT-23-THIN (DDF) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDDFR.B | Active | Production | SOT-23-THIN (DDF) 8 | 3000 LARGE T&R | - | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDGKR | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU SN NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | T062 |
| TLV9062IDGKR.A | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | T062 |
| TLV9062IDGKR.B | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | - | SN | Level-2-260C-1 YEAR | -40 to 125 | T062 |
| TLV9062IDGKRG4 | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDGKRG4.A | Active | Production | VSSOP (DGK) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDGKT | Active | Production | VSSOP (DGK) 8 | 250 SMALL T&R | Yes | NIPDAU SN NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | T062 |
| TLV9062IDGKT.A | Active | Production | VSSOP (DGK) 8 | 250 SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | T062 |
| TLV9062IDR | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9062 |
| TLV9062IDR.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9062 |
| TLV9062IDRG4 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9062 |
| TLV9062IDRG4.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL9062 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TLV9062IDSGR | Active | Production | WSON (DSG) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDSGR.A | Active | Production | WSON (DSG) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDSGRG4 | Active | Production | WSON (DSG) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDSGRG4.A | Active | Production | WSON (DSG) 8 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDSGT | Active | Production | WSON (DSG) 8 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IDSGT.A | Active | Production | WSON (DSG) 8 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T062 |
| TLV9062IPWR | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-2-260C-1 YEAR | -40 to 125 | TL9062 |
| TLV9062IPWR.A | Active | Production | TSSOP (PW) 8 | 2000 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | TL9062 |
| TLV9062SIDGSR | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 1TDX |
| TLV9062SIDGSR.A | Active | Production | VSSOP (DGS) 10 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | 1TDX |
| TLV9062SIRUGR | Active | Production | X2QFN (RUG) 10 | 3000 LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | EOF |
| TLV9062SIRUGR.A | Active | Production | X2QFN (RUG) 10 | 3000 LARGE T&R | Yes | NIPDAUAG | Level-2-260C-1 YEAR | -40 to 125 | EOF |
| TLV9062SIYCKR | Active | Production | DSBGA (YCK) 9 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | EH |
| TLV9062SIYCKR.A | Active | Production | DSBGA (YCK) 9 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | EH |
| TLV9064IDR | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV9064D |
| TLV9064IDR.A | Active | Production | SOIC (D) 14 | 2500 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TLV9064D |
| TLV9064IPWR | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | NIPDAU SN | Level-2-260C-1 YEAR | -40 to 125 | TLV9064 |
| TLV9064IPWR.A | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | TLV9064 |
| TLV9064IPWR.B | Active | Production | TSSOP (PW) 14 | 2000 LARGE T&R | - | SN | Level-2-260C-1 YEAR | -40 to 125 | TLV9064 |
| TLV9064IPWT | Active | Production | TSSOP (PW) 14 | 250 SMALL T&R | Yes | NIPDAU SN | Level-2-260C-1 YEAR | -40 to 125 | TLV9064 |
| TLV9064IPWT.A | Active | Production | TSSOP (PW) 14 | 250 SMALL T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 125 | TLV9064 |
| TLV9064IRTER | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9064 |
| TLV9064IRTER.A | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9064 |
| TLV9064IRUCR | Active | Production | QFN (RUC) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 1DD |
| TLV9064IRUCR.A | Active | Production | QFN (RUC) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 1DD |
| TLV9064IRUCRG4 | Active | Production | QFN (RUC) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 1DD |
| TLV9064IRUCRG4.A | Active | Production | QFN (RUC) 14 | 3000 LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 1DD |
| TLV9064SIRTER | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9064S |
| TLV9064SIRTER.A | Active | Production | WQFN (RTE) 16 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | T9064S |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9061, TLV9062, TLV9064 :

- Automotive : [TLV9061-Q1](#), [TLV9062-Q1](#), [TLV9064-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV9061IDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9061IDBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9061IDBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9061IDCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.3 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| TLV9061IDPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q2 |
| TLV9061SIDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9061SIDBVRG4 | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9062IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9062IDGKRG4 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9062IDGKT | VSSOP | DGK | 8 | 250 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9062IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9062IDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV9062IDSGR | WSO | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV9062IDSGRG4 | WSO | DSG | 8 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV9062IDSGT | WSO | DSG | 8 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV9062IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9062SIDGSR | VSSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV9062SIRUGR | X2QFN | RUG | 10 | 3000 | 178.0 | 8.4 | 1.75 | 2.25 | 0.56 | 4.0 | 8.0 | Q1 |
| TLV9062SIYCKR | DSBGA | YCK | 9 | 3000 | 180.0 | 8.4 | 1.1 | 1.1 | 0.4 | 2.0 | 8.0 | Q1 |
| TLV9064IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV9064IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9064IPWT | TSSOP | PW | 14 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV9064IRTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TLV9064IRUCR | QFN | RUC | 14 | 3000 | 180.0 | 9.5 | 2.16 | 2.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TLV9064IRUCRG4 | QFN | RUC | 14 | 3000 | 180.0 | 9.5 | 2.16 | 2.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TLV9064SIRTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV9061IDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TLV9061IDBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9061IDBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9061IDCKR | SC70 | DCK | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9061IDPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| TLV9061SIDBVR | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9061SIDBVRG4 | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9062IDDFR | SOT-23-THIN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 356.0 | 356.0 | 36.0 |
| TLV9062IDGKR | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9062IDGKRG4 | VSSOP | DGK | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9062IDGKT | VSSOP | DGK | 8 | 250 | 353.0 | 353.0 | 32.0 |
| TLV9062IDR | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9062IDRG4 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9062IDSGR | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9062IDSGRG4 | WSON | DSG | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV9062IDSGT | WSON | DSG | 8 | 250 | 210.0 | 185.0 | 35.0 |
| TLV9062IPWR | TSSOP | PW | 8 | 2000 | 353.0 | 353.0 | 32.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV9062SIDGSR | VSSOP | DGS | 10 | 2500 | 366.0 | 364.0 | 50.0 |
| TLV9062SIRUGR | X2QFN | RUG | 10 | 3000 | 205.0 | 200.0 | 33.0 |
| TLV9062SIYCKR | DSBGA | YCK | 9 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV9064IDR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV9064IPWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| TLV9064IPWT | TSSOP | PW | 14 | 250 | 353.0 | 353.0 | 32.0 |
| TLV9064IRTER | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TLV9064IRUCR | QFN | RUC | 14 | 3000 | 205.0 | 200.0 | 30.0 |
| TLV9064IRUCRG4 | QFN | RUC | 14 | 3000 | 205.0 | 200.0 | 30.0 |
| TLV9064SIRTER | WQFN | RTE | 16 | 3000 | 367.0 | 367.0 | 35.0 |

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

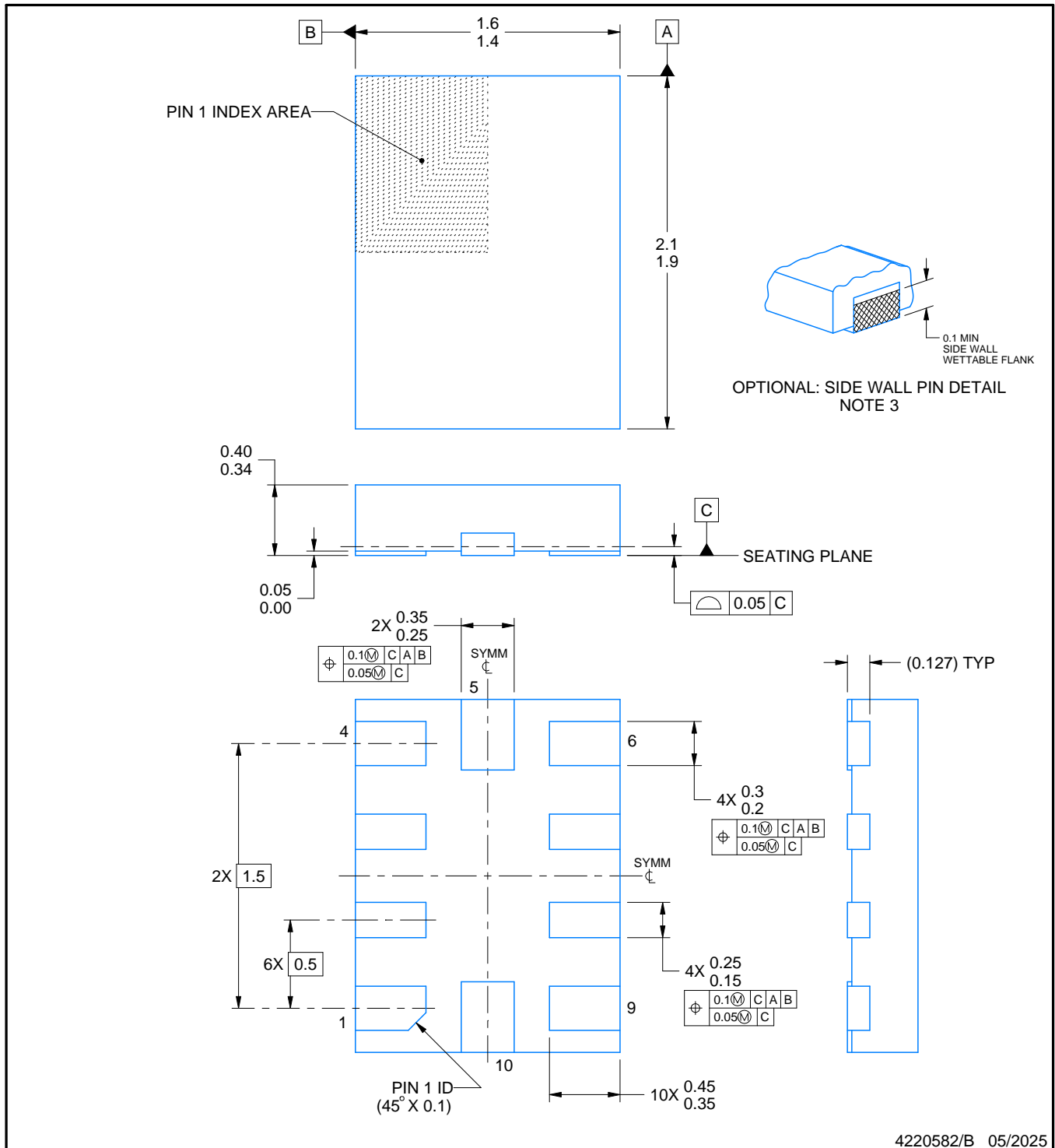
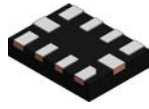


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220582/B 05/2025

NOTES:

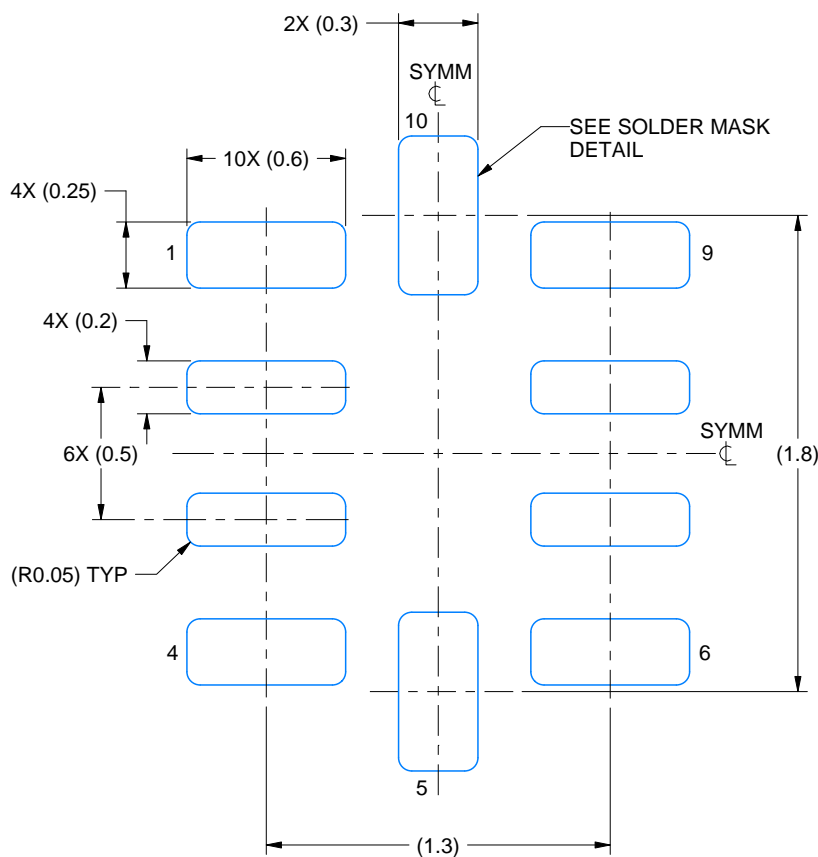
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.

EXAMPLE BOARD LAYOUT

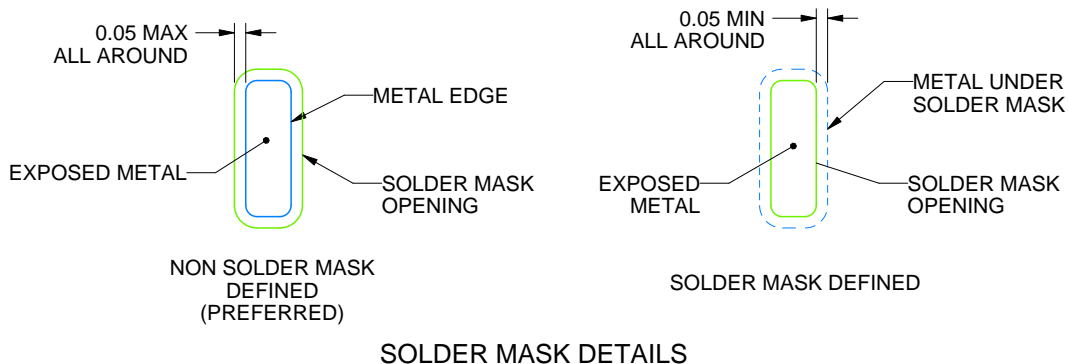
RUG0010B

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X



4220582/B 05/2025

NOTES: (continued)

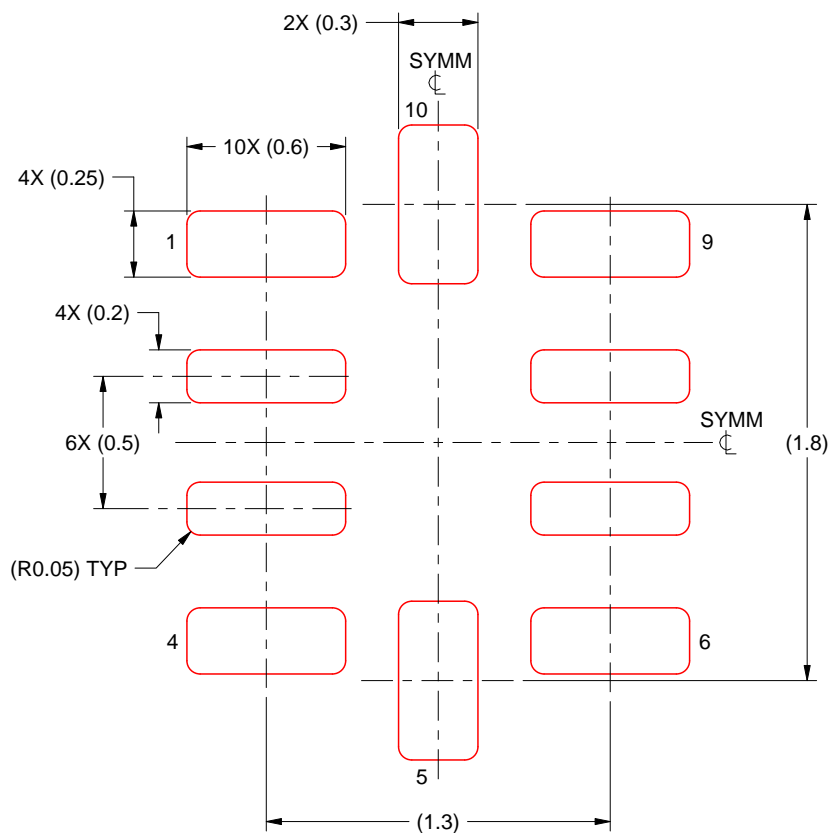
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RUG0010B

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

4220582/B 05/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4221984/A 05/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

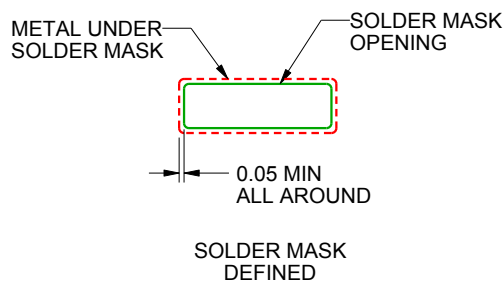
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

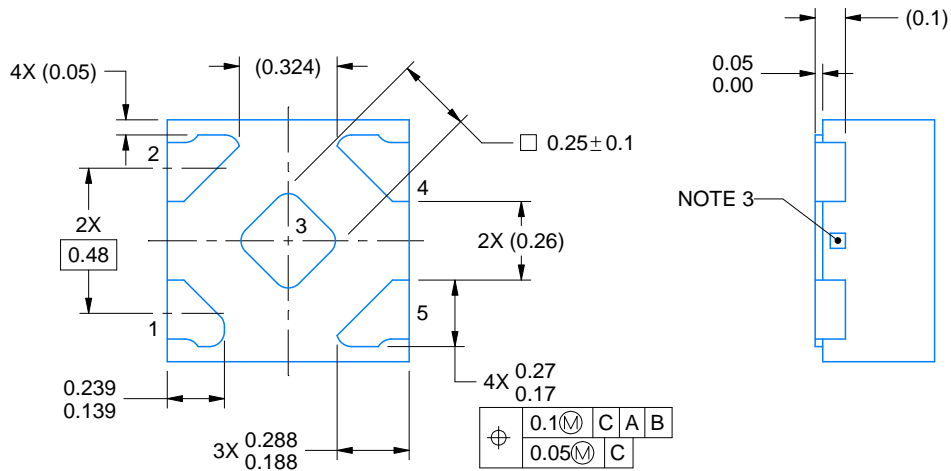
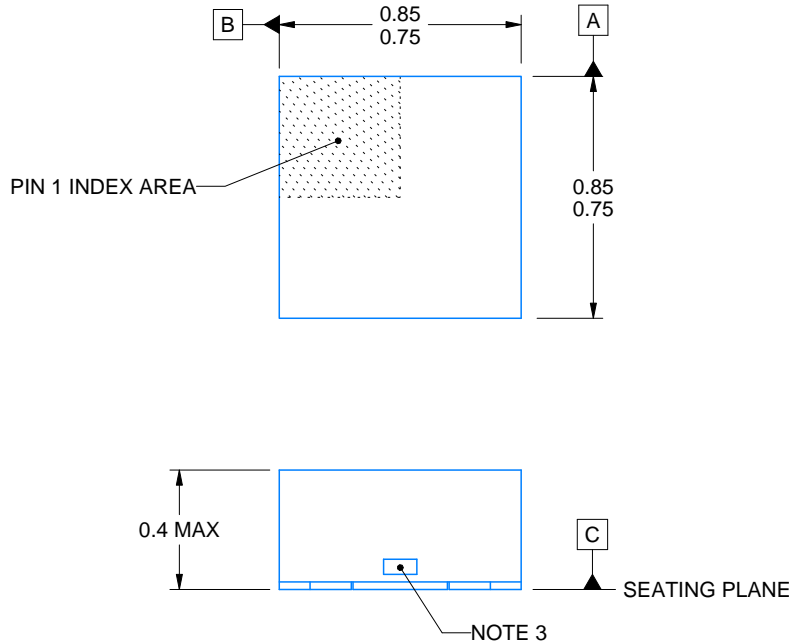
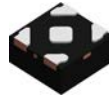
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

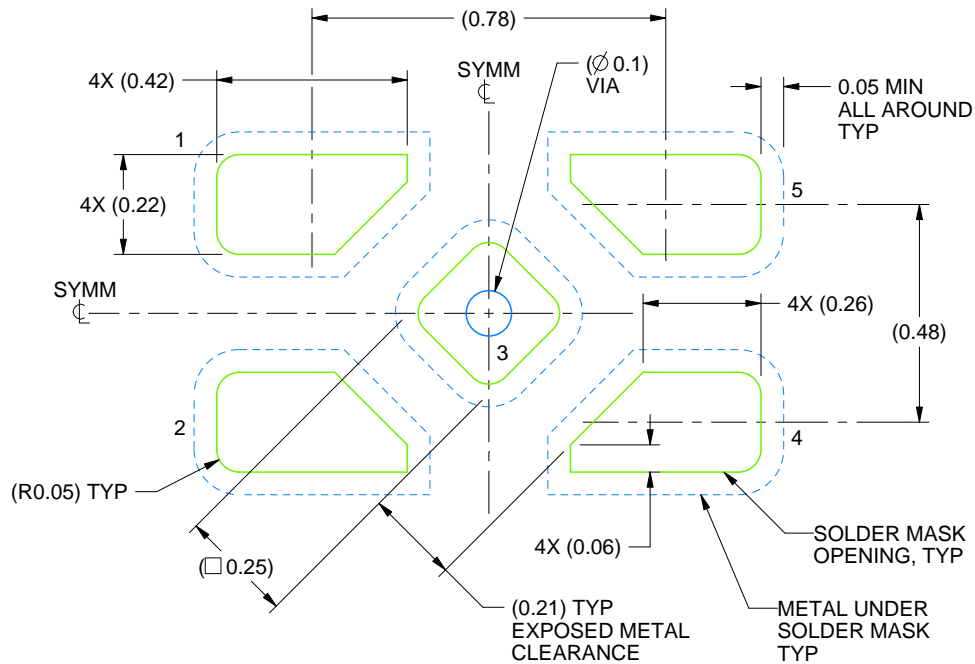
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



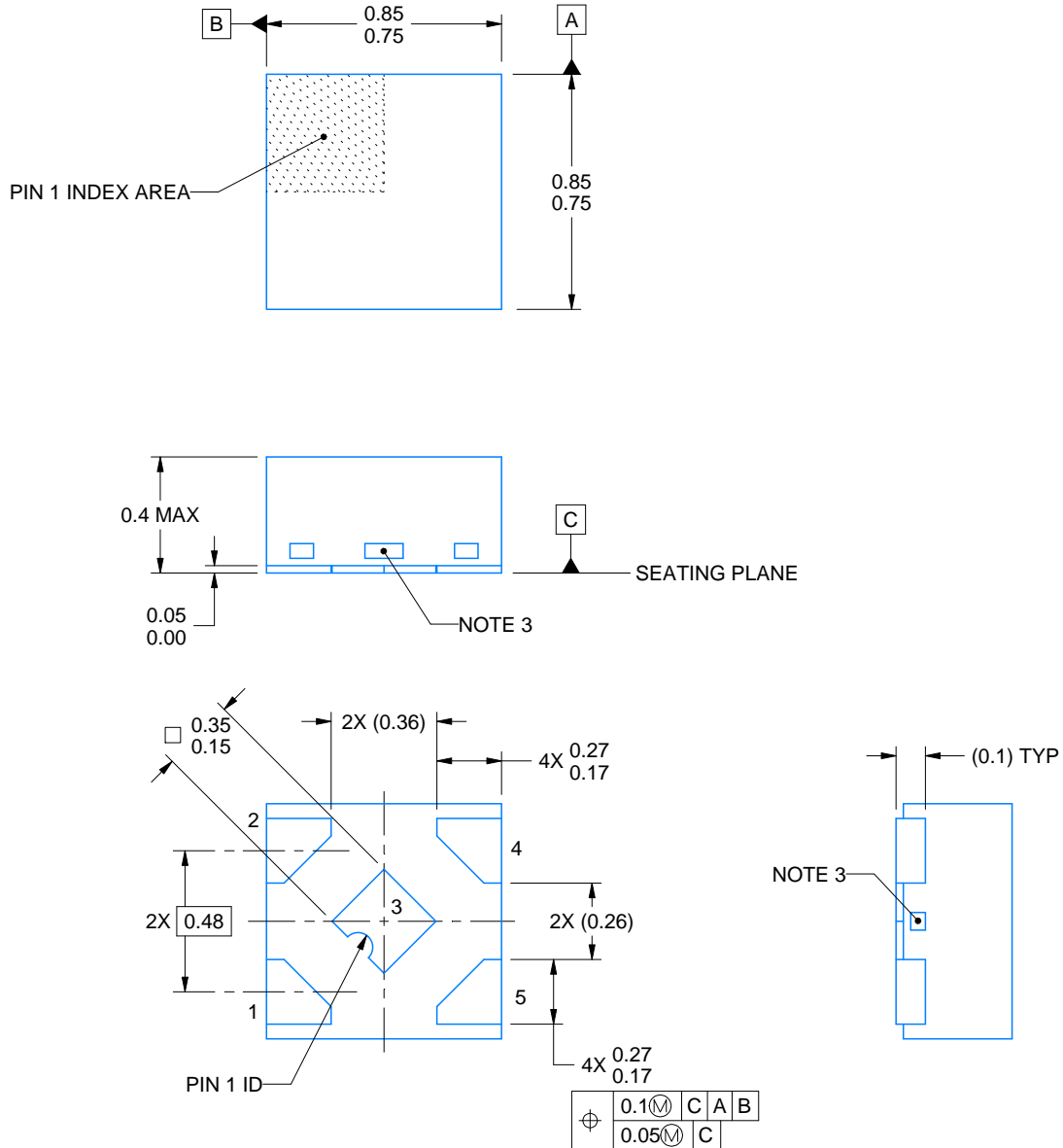
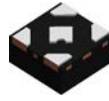
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4228233/D 09/2023

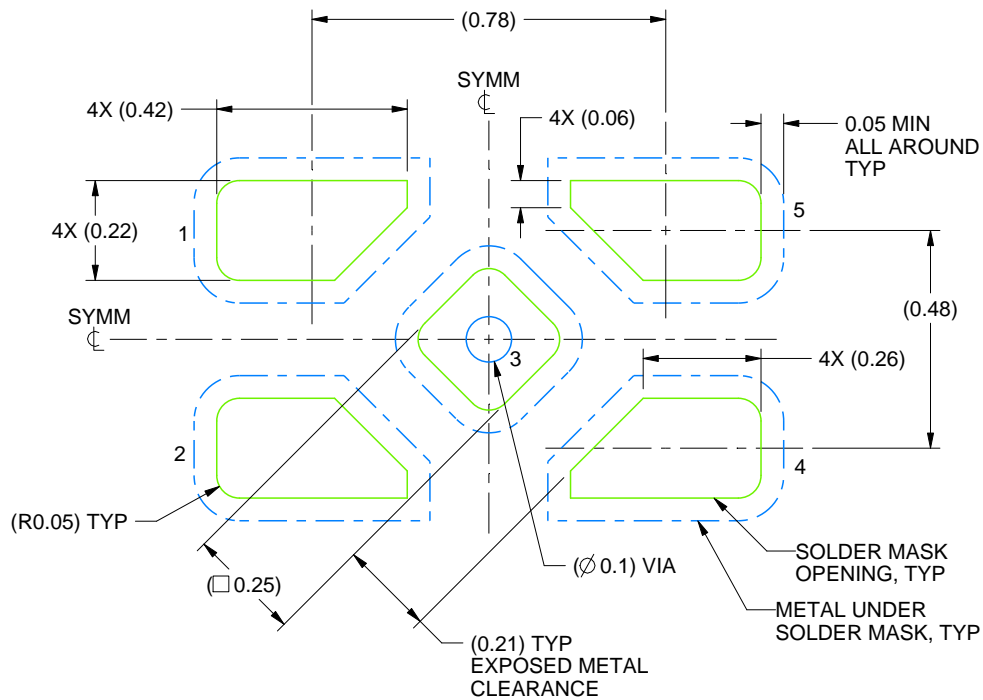
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

DPW0005B

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

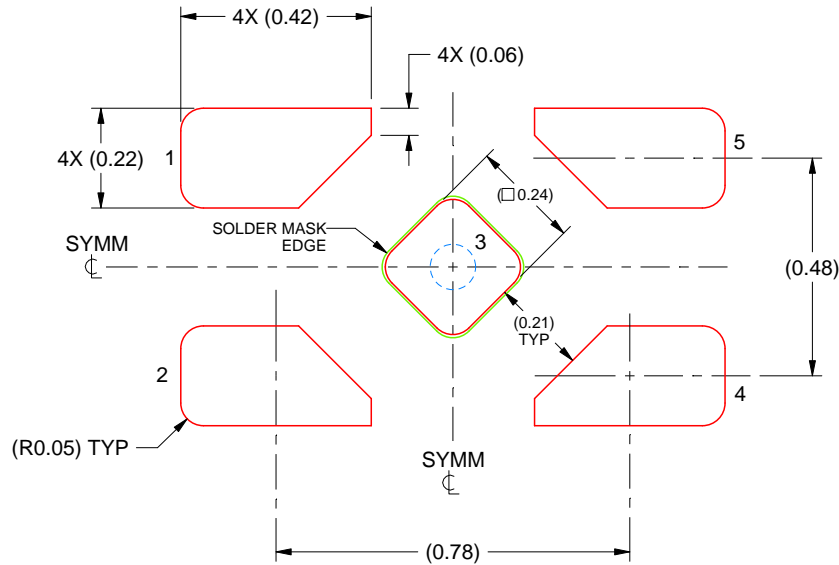
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005B

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/D 09/2023

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side.

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

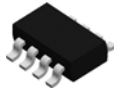


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

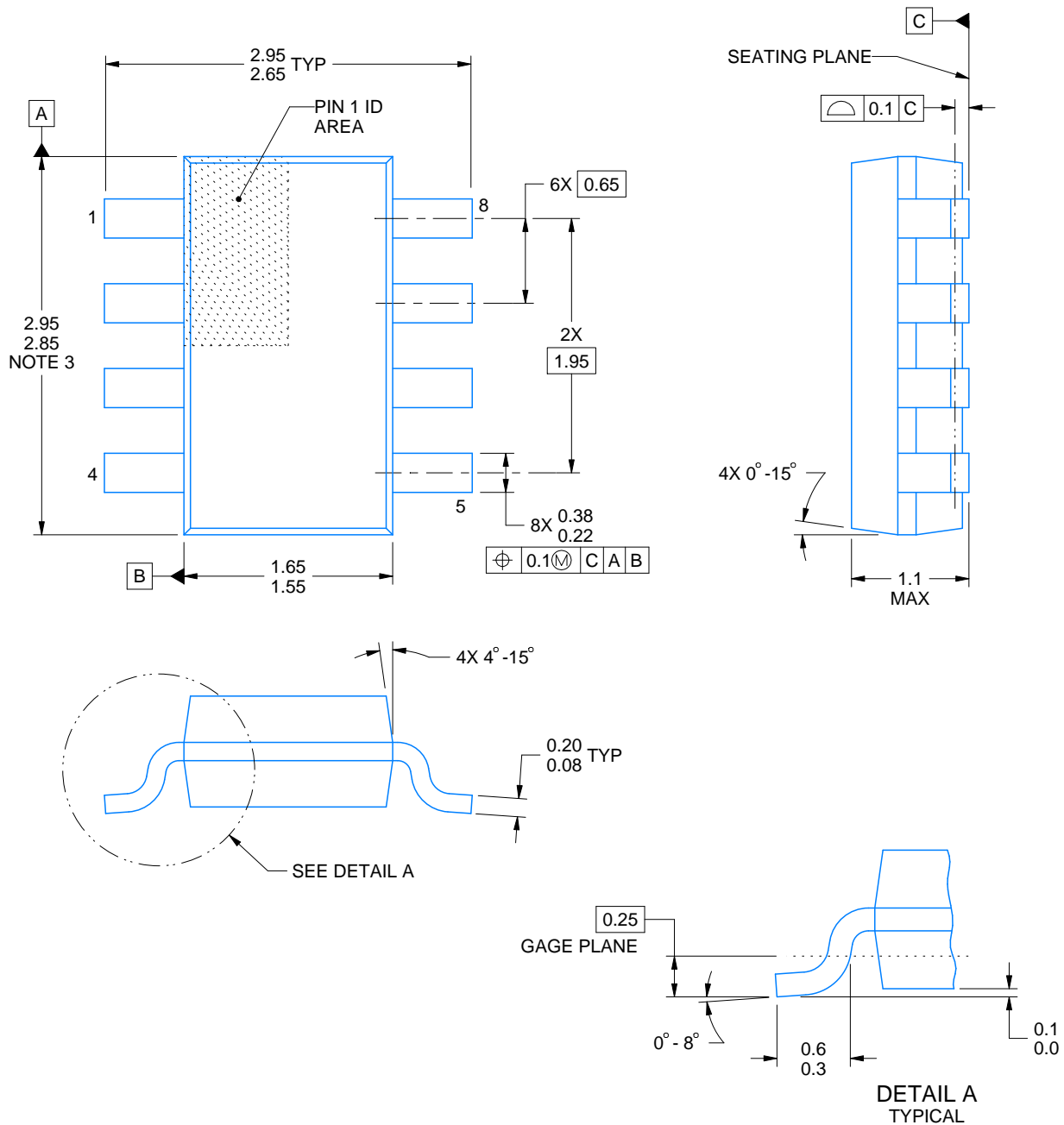
4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

DDF0008A**PACKAGE OUTLINE****SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

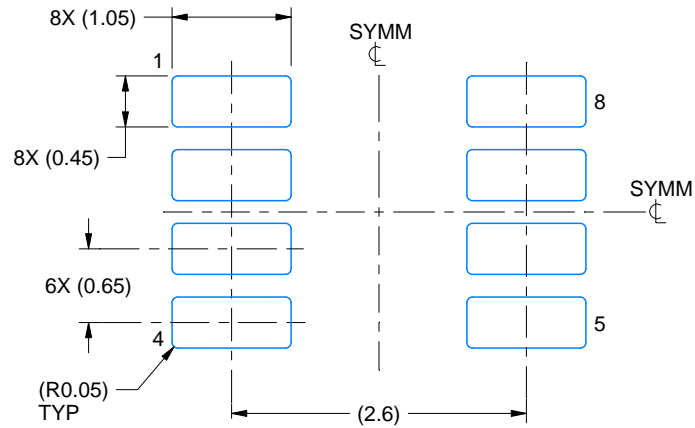
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

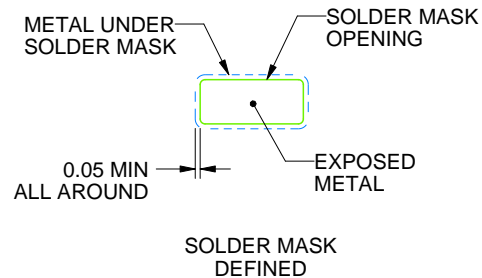
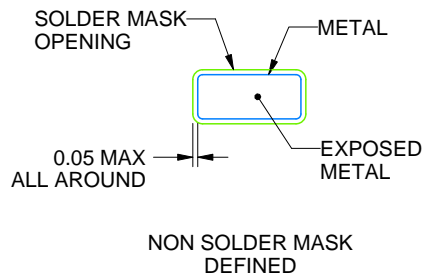
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.

4. This dimension does not include interlead flash.

5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

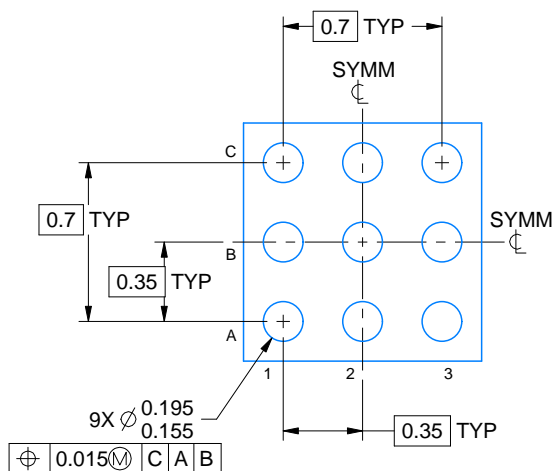
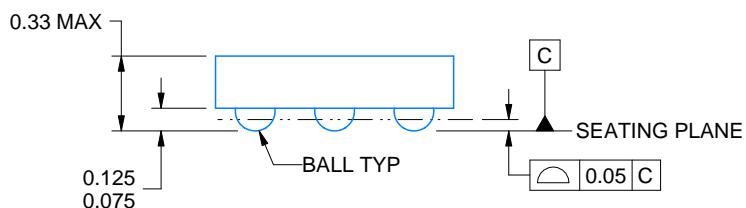


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



E: Max = 0.98 mm, Min = 0.92 mm

NOTES:

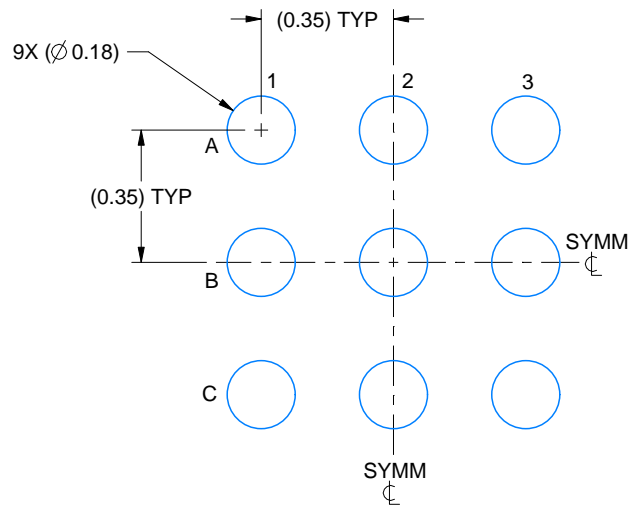
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

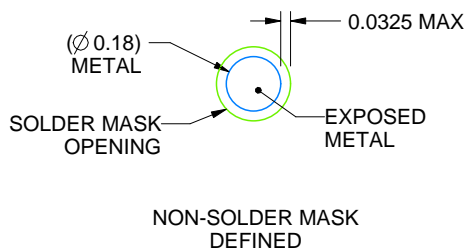
YCK0009

DSBGA - 0.33 mm max height

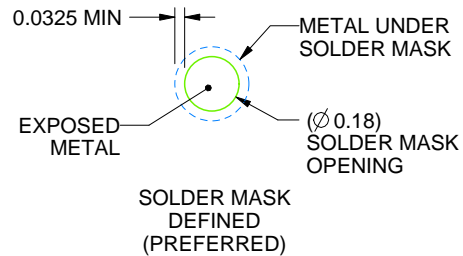
DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



NON-SOLDER MASK
DEFINED



SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS
NOT TO SCALE

4225837/A 04/2020

NOTES: (continued)

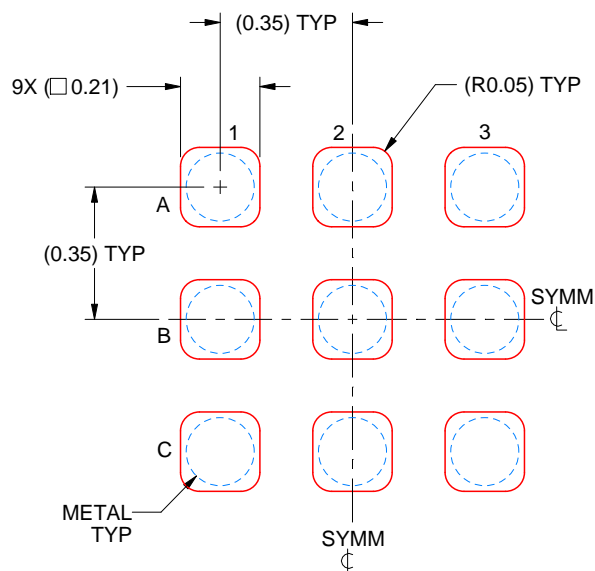
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCK0009

DSBGA - 0.33 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4225837/A 04/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

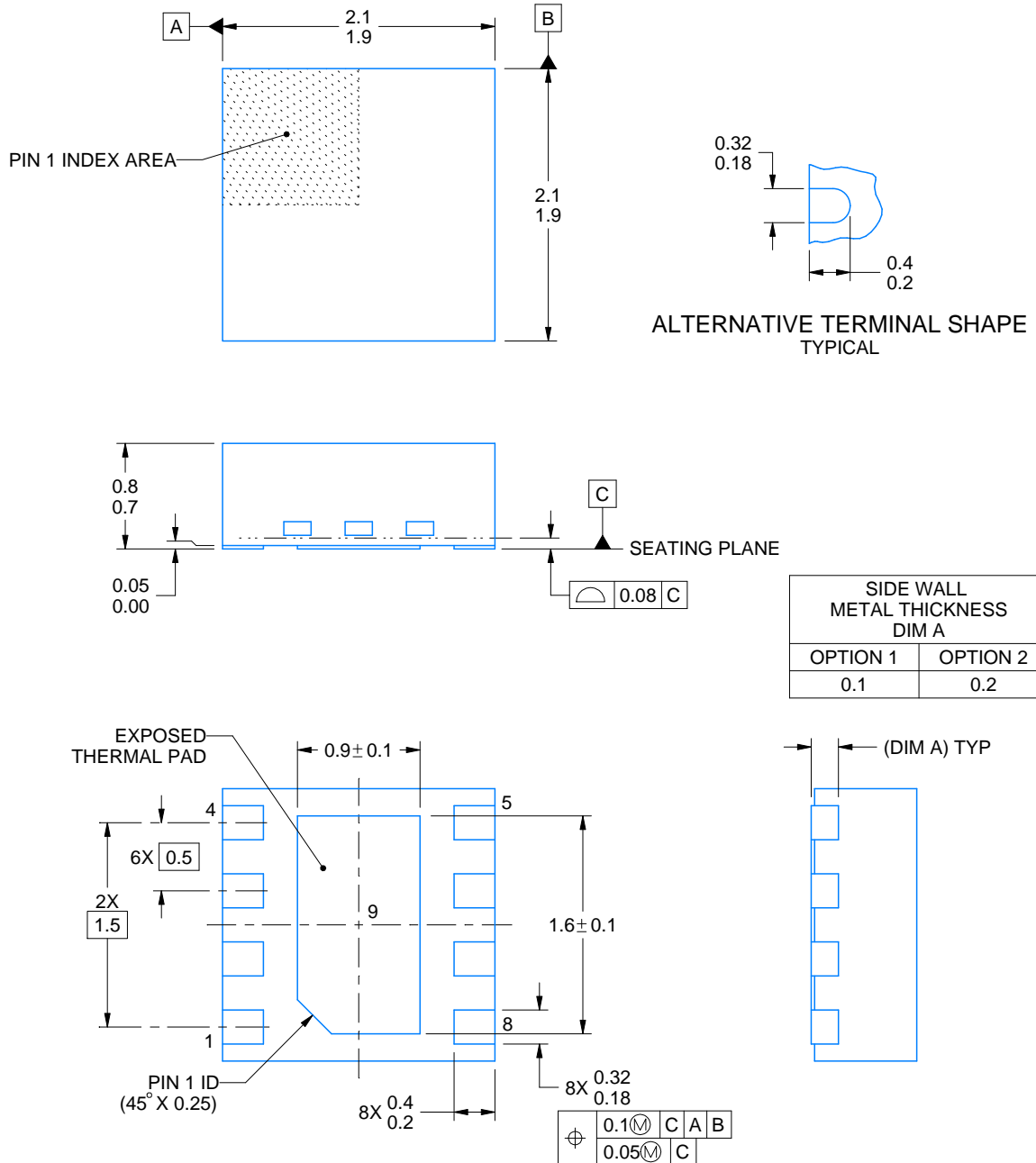
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A



4218900/E 08/2022

NOTES:

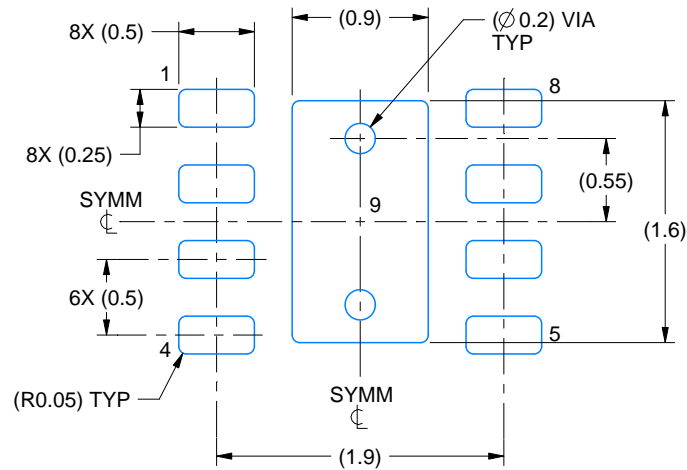
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

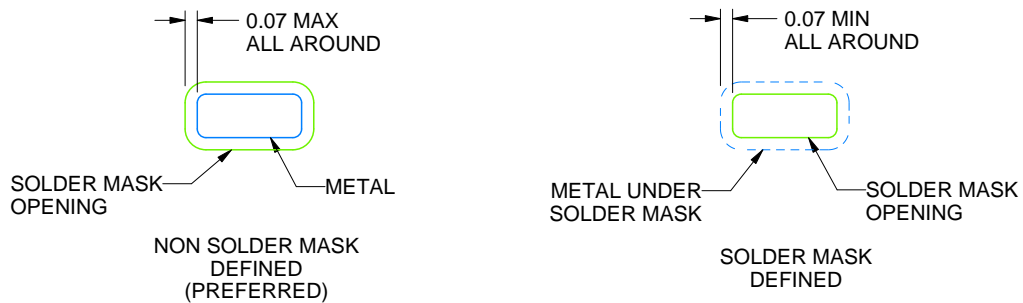
DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

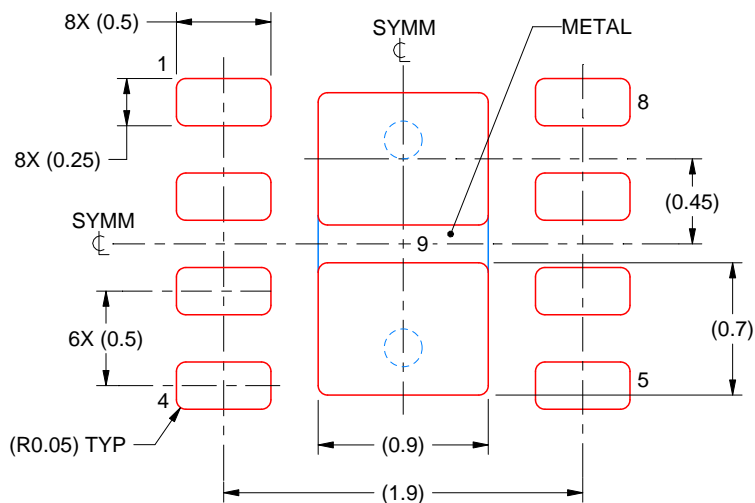
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

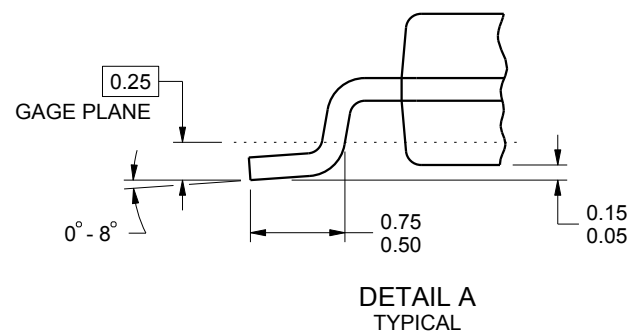
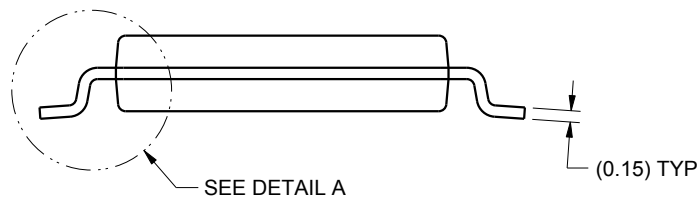
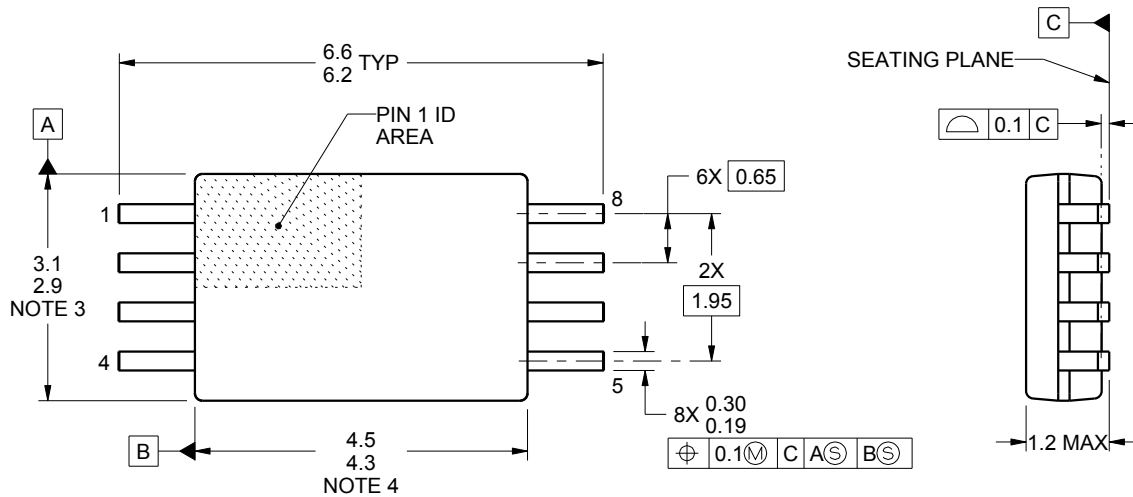
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

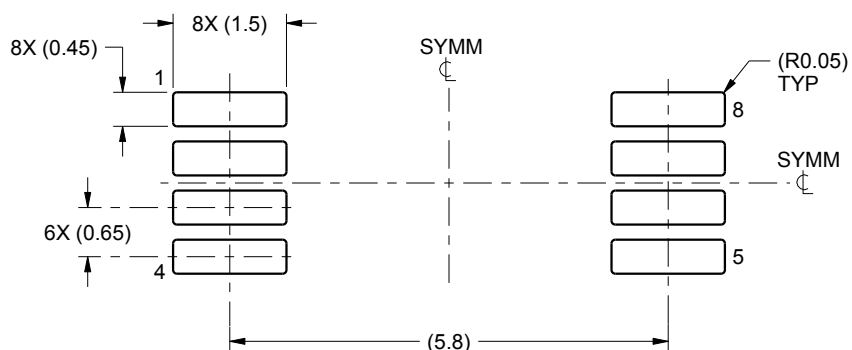
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

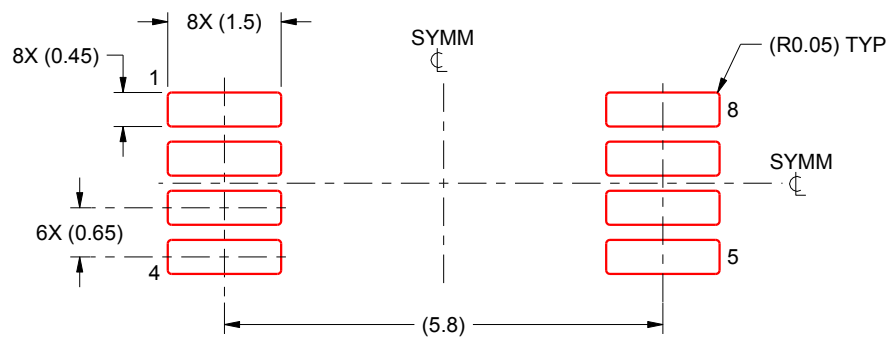
6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

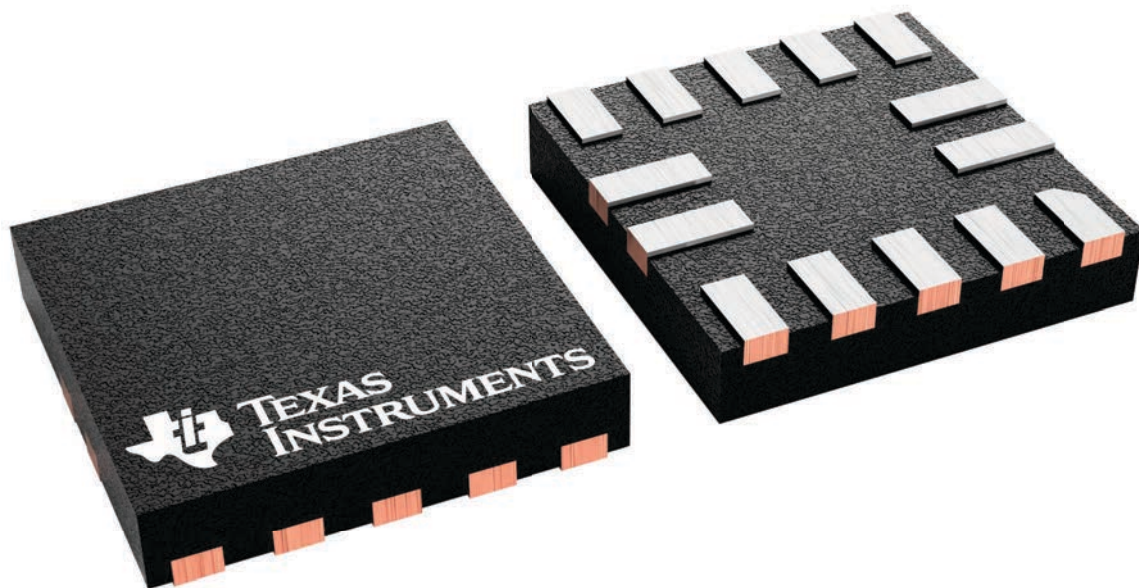
RUC 14

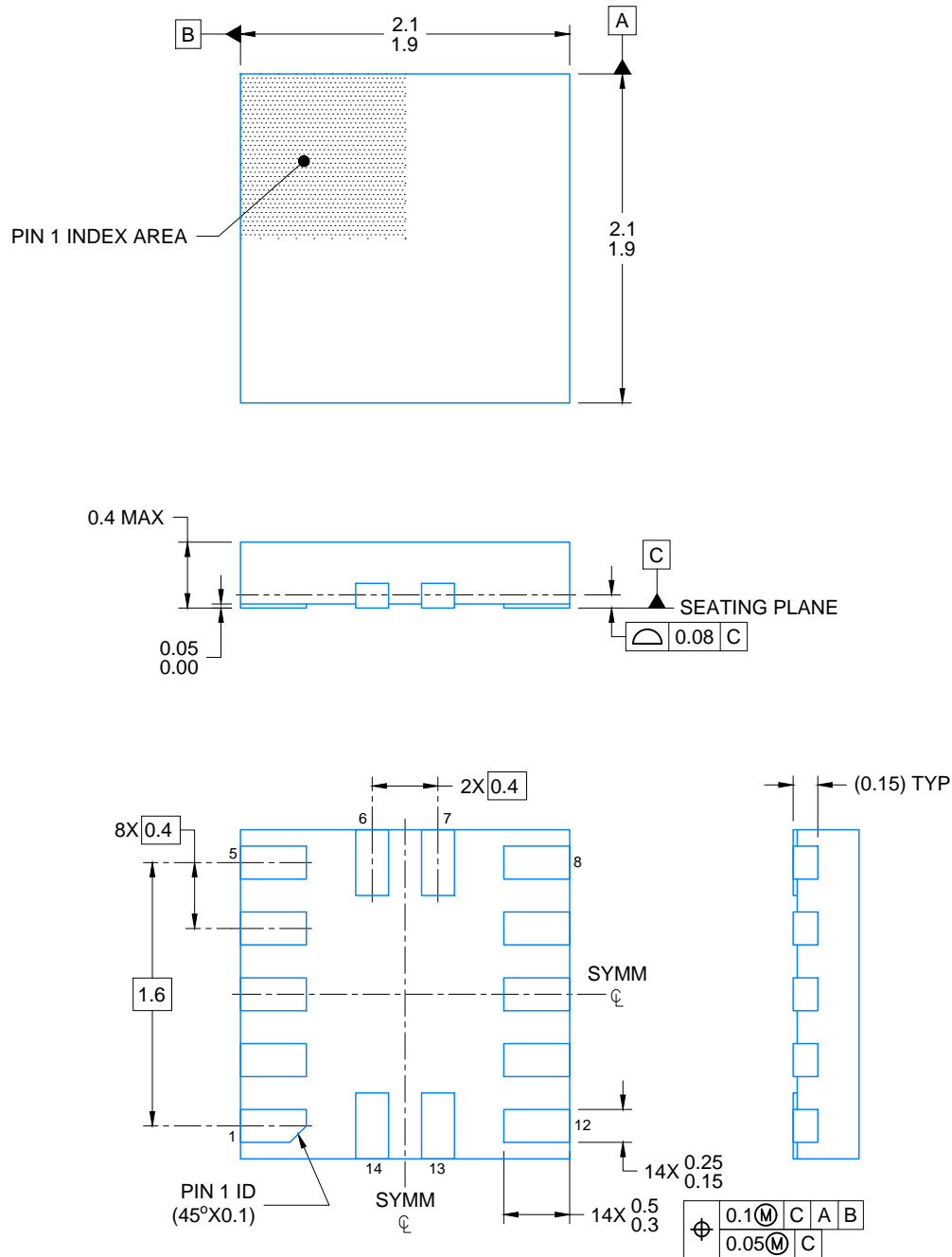
X2QFN - 0.4 mm max height

2 x 2, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

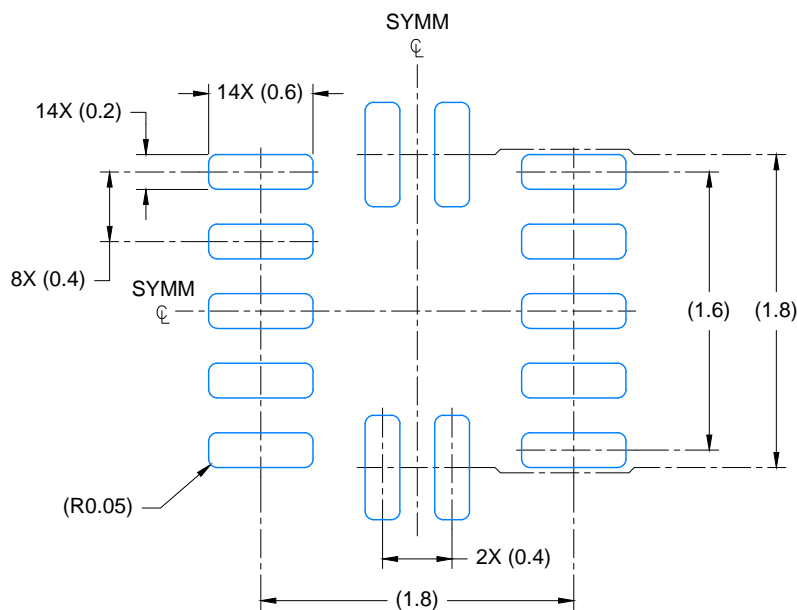




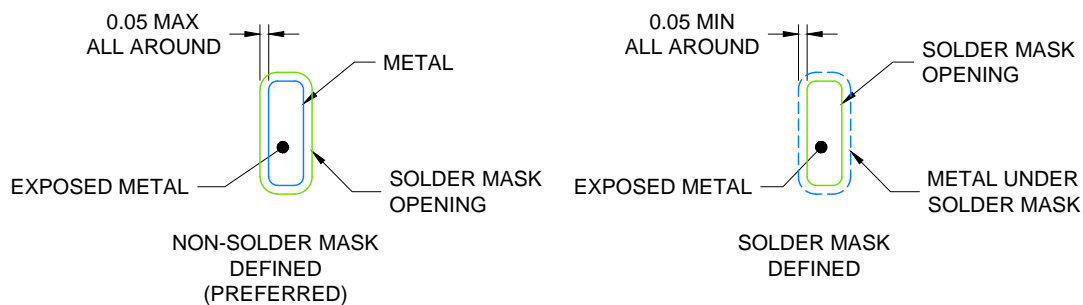
4220584/A 05/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X



SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

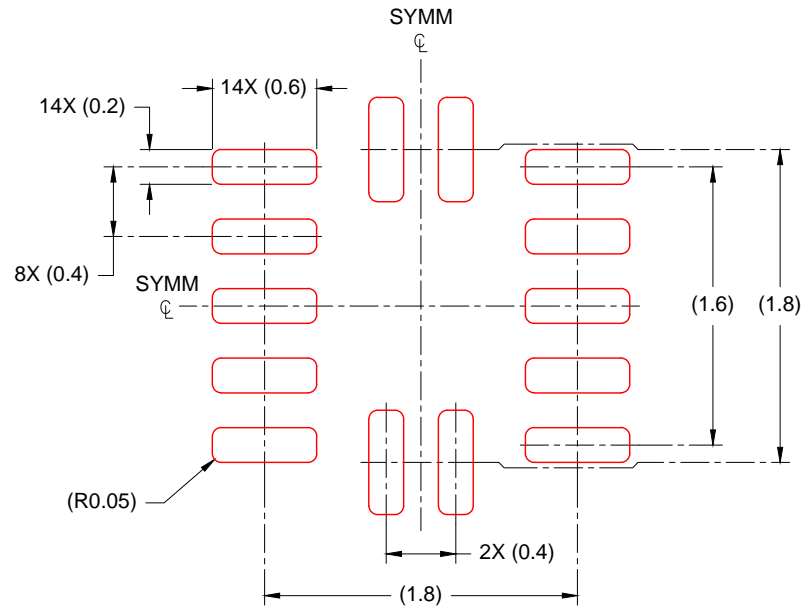
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

RUC0014A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A**PACKAGE OUTLINE****VSSOP - 1.1 mm max height**

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

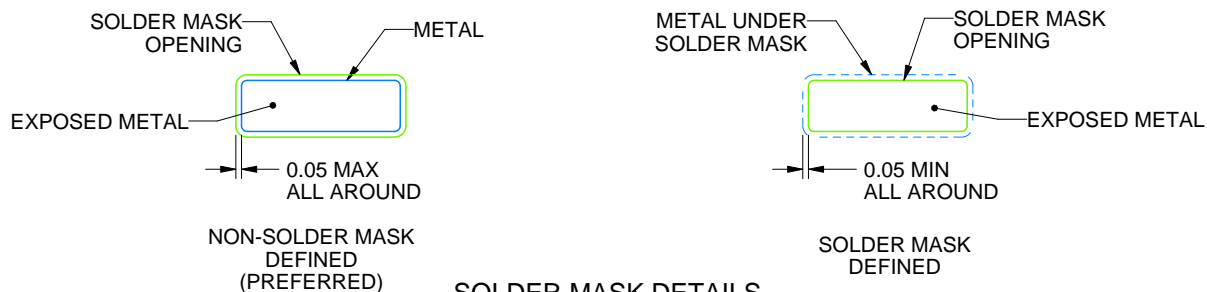
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



4219117/B 04/2022

NOTES:

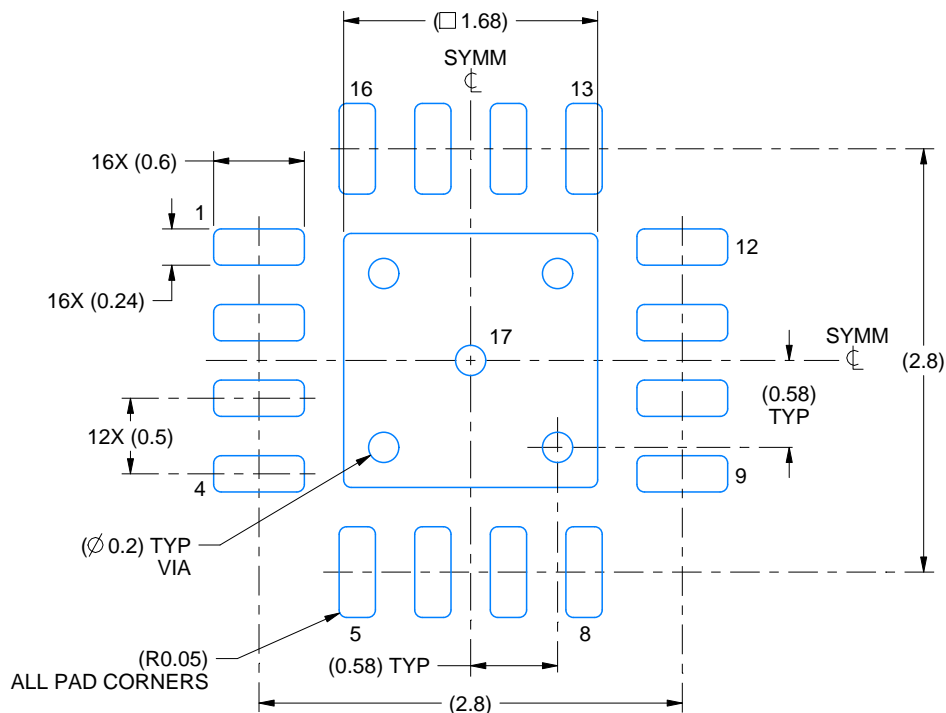
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

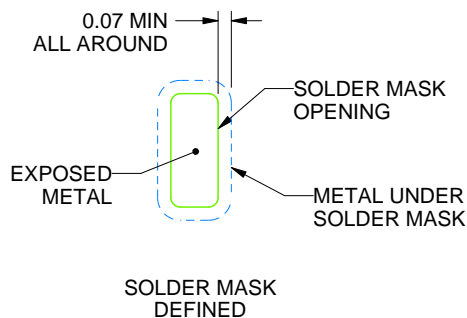
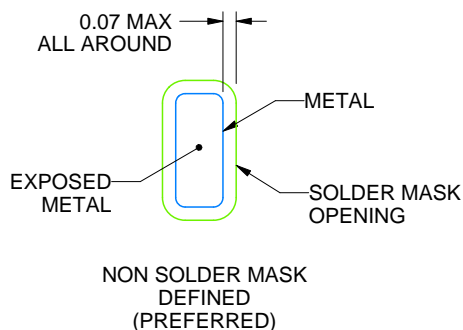
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

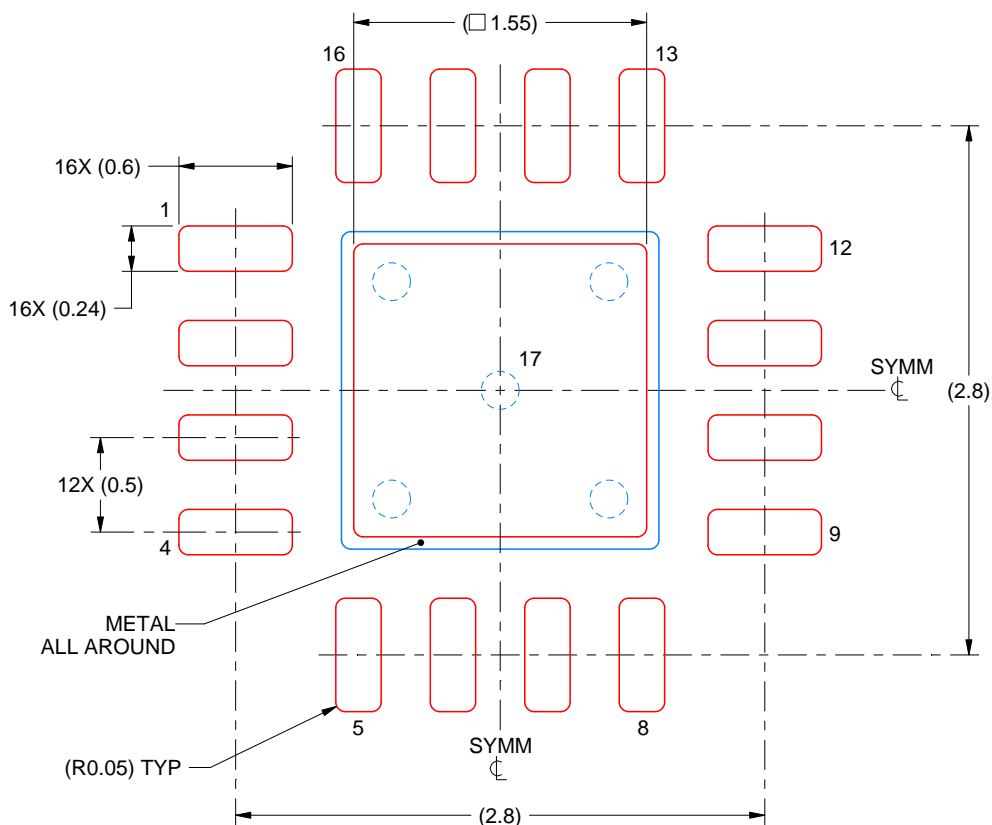
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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