TLV902xL and TLV903xL Precision, Self-Latching Comparator Family

1 Features

- Output latch with falling-edge triggered clear
- Power-on Reset (POR) for known start-up
- Selectable Start-up State:
  - Un-Latched on Power-up ("**L1**" option)
  - Latched on Power-up ("**L2**" option)
- 1.65V to 5.5V supply range
- Precision input offset voltage: 300µV
- Rail-to-Rail inputs with fault tolerance
- 110ns typical propagation delay
- Low quiescent current: 22µA per channel
- Low input bias current: 5pA
- Open-drain output option (TLV90**2**xL)
- Push-pull output option (TLV90**3**xL)
- Full -40°C to +125°C temperature range
- 2kV ESD protection

2 Applications

- Appliance Power Module
- AC Drive Control
- Power Conversion Systems
- Battery Backup Unit
- Battery Test Equipment

3 Description

The TLV902xL and TLV903xL are a family of single and dual channel latching comparators. The family also offers low input offset voltage, power on reset (POR), and fault-tolerant rail-to-rail inputs. These devices have an excellent speed-to-power combination with a propagation delay of 110ns with a quiescent supply current of only 22µA per channel.

The unique feature of the TLV90xxL is the output latching capability. The output latches upon the first threshold crossing, allowing capture of an event or error condition without the full attention of a system controller. This allows events to be captured at start up while the system controller is still initializing or busy with other tasks. The falling-edge triggered clear input allows system controller to reset the latch after performing any needed tasks and meets safety-critical requirements. The "L1" and "L2" options define power-up latching behavior.

These comparators also feature fault-tolerant inputs that can go up to 6V without damage with no output phase inversion. This makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

The TLV902xL have an open-drain output that can be pulled-up below or beyond the supply voltage, designed for OR'ing multiple outputs or level translation. Latching occurs on the high to low output transition.

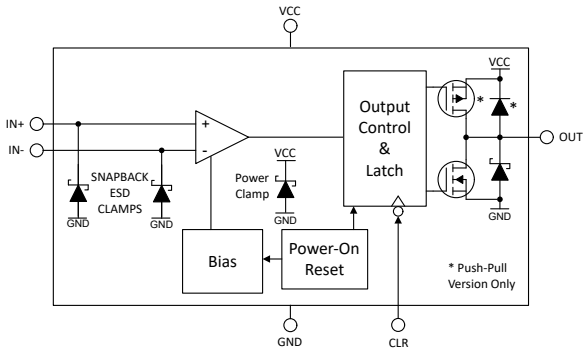
The TLV903xL have a push-pull output stage capable of sinking and sourcing up to 85mA to drive a capacitive load such as a MOSFET gate. Latching occurs on the low to high output transition.

The family is specified for the Industrial temperature range of -40°C to +125°C and are available in standard leaded and leadless packages.

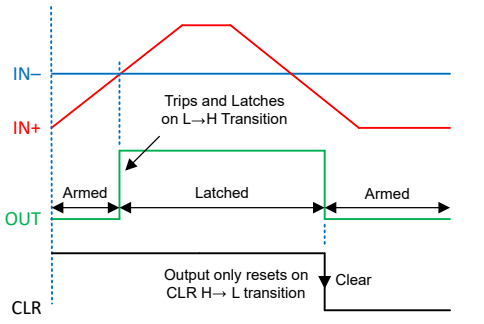
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TLV9020Lx (Pre), TLV9030Lx (Pre), (Single)	SC-70 (6) (Preview)	1.25mm × 2.00mm
	SOT-23 (6) (Preview)	1.60mm x 2.90mm
	WSON (6) (Preview)	1.50mm × 1.50mm
TLV9022Lx, TLV9032Lx (Pre) (Dual)	VSSOP (10) (Preview)	3.00mm × 3.00mm
	X2QFN (10)	2.00mm × 1.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram



TLV903xL Push-Pull Latching Response

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4 Pin Configuration and Functions

Pin Functions: TLV9020L and TLV9030L Single

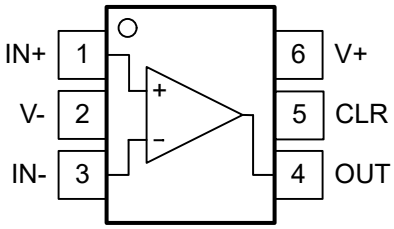


Figure 4-1. DCK and DBV Packages
Standard "South East" Pinout with Clear Pin
6-Pin SC-70 and SOT-23
Top View

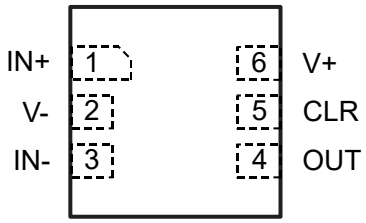
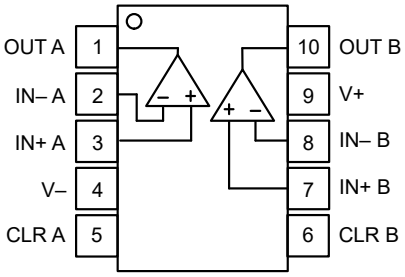


Figure 4-2. DSE Package
6-Pin WSON
Top View

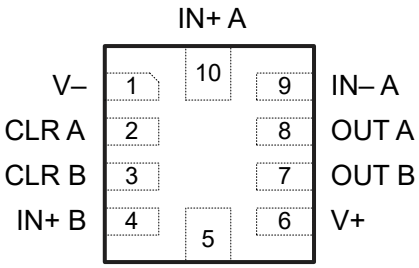
Table 4-1. Pin Functions: TLV9020L and TLV9030L

NAME	TLV9020L , TLV9030L			I/O	DESCRIPTION
	PINS	PINS	PINS		
	SC-70	SOT-23	WSON		
IN+	1	1	1	I	Non-Inverting (+) Input
V-	2	2	2	-	Negative Supply Voltage
IN-	3	3	3	I	Inverting (-) Input
OUT	4	4	4	O	Output
CLR	5	5	5	I	Clear Input - Pulse high (>1.2V) to clear output
V+	6	6	6	-	Positive Supply Voltage

Pin Configurations:TLV9022L and TLV9032L Dual



DGK Package
10-Pin VSSOP
Top View



RUG Package
10-Pin X2QFN
Top View

Table 4-2. Pin Functions: TLV9022L and TLV9032L

NAME	TLV9022L, TLV9032L		I/O	DESCRIPTION
	PINS	PINS		
	VSSOP	X2QFN		
OUT A	1	8	O	Output of comparator A
IN– A	2	9	I	Inverting (–) input of comparator A
IN+ A	3	10	I	Non-Inverting (+) input of comparator A
V–	4	1	–	Negative Supply Voltage
CLR A	5	2	I	Clear input for comparator A - clears on falling edge
CLR B	6	3	I	Clear input for comparator B - clears on falling edge
IN+ B	7	4	I	Non-Inverting (+) input of comparator B
IN– B	8	5	I	Inverting (–) input of comparator B
V+	9	6	–	Positive Supply Voltage
OUT B	10	7	O	Output of comparator B

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	6	V
Input pins (IN+, IN–, CLR) from (V–)(2)	–0.3	6	V
Current into Input pins (IN+, IN–, CLR)	–10	10	mA
Output (OUT) from (V–)(3)	–0.3	6	V
Output (OUT) (Open Drain) from (V–)	–0.3	(V+) + 0.3	V
Output short circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond (V-) must be current-limited to 10mA or less. Additionally, Inputs (IN+, IN–,CLR) can be greater than (V+) and OUT as long as the voltage is within the –0.3V to 6V range
(3) Output (OUT) for open drain can be greater than (V+)
(4) Short-circuit to (V–) or (V+).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) - (V-)	1.65	5.5	V
Input voltage range (IN+, IN–, CLR) from (V–)	–0.2	5.5	V
Input common mode voltage range (IN+, IN–) from (V–)	– 0.2	(V+) + 0.2	V
Output voltage range, open drain output, from (V-)	0	5.5	V
Output voltage range, push-pull output	(V-)	(V+)	V
Ambient Temperature, T_A	–40	125	°C

5.4 Thermal Information - Single

THERMAL METRIC (1)		TLV9020L, TLV9030L			UNIT
		DBV (SOT-23)	DCK (SC-70)	DSE (WSON)	
		6 PINS	6 PINS	6 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	-	210.5	-	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	-	143.9	-	°C/W
R_{qJB}	Junction-to-board thermal resistance	-	64.7	-	°C/W
y_{JT}	Junction-to-top characterization parameter	-	46.1	-	°C/W
y_{JB}	Junction-to-board characterization parameter	-	64.5	-	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.5 Thermal Information - Dual

THERMAL METRIC (1)		TLV9022L, TLV9032L		UNIT
		DGK (VSSOP)	RUG (X2QFN)	
		10 PINS	10 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	-	222.8	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	-	94.2	°C/W
R_{qJB}	Junction-to-board thermal resistance	-	147.1	°C/W
y_{JT}	Junction-to-top characterization parameter	-	3.4	°C/W
y_{JB}	Junction-to-board characterization parameter	-	146.4	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.6 Electrical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V-) = 5V, V_{CM} = (V-) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_T	Input threshold voltage	V_S = 1.8V and 5V	–1.75	±0.3	1.75	mV
V_T	Input threshold voltage	V_S = 1.8V and 5V, T_A = –40°C to +125°C	–2.25		2.25	
dV_T/dT	Input threshold voltage drift	V_S = 1.8V and 5V, T_A = –40°C to +125°C		±0.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8V and 5V, No Load, Output Low		22	30	µA
I_Q	Quiescent current per comparator	V_S = 1.8V and 5V, No Load, Output Low, T_A = –40°C to +125°C			42	
V_{POR} (postive)	Power-On Reset Voltage			1.25		V
PSRR	Power-supply rejection ratio	V_S = 1.8V to 5V, T_A = –40°C to +125°C (push-pull only)	75	95		dB
PSRR	Power-supply rejection ratio	V_S = 1.8V to 5V, T_A = –40°C to +125°C (open drain only)	80	95		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
V_{IH_CLR}	Voltage input high threshold of CLR		1.2			V
V_{IL_CLR}	Voltage input low of threshold CLR				0.6	V
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8V and 5V, T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 5V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V, T_A = –40°C to +125°C	60	70		dB
CMRR	Common-mode rejection ratio	V_S = 1.8V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V, T_A = –40°C to +125°C	50	60		dB
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA, T_A = 25°C		75	125	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA, T_A = –40°C to +125°C			175	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4mA, T_A = 25°C (push-pull only)		75	125	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 4mA, T_A = –40°C to +125°C (push-pull only)			175	mV
I_{LKG}	Open-drain output leakage current	V_{PULLUP} = (V+), T_A = 25°C		100		pA
I_{SC}	Short-circuit current	V_S = 5V, Sinking	75	85		mA
I_{SC}	Short-circuit current	V_S = 5V, Sourcing (push-pull only)	75	85		mA

5.7 Switching Characteristics

V_S = 5V, CLR = 5V_{PP}, V_L = 0V, V_H = 5V, 2.5V DC offset, V_{CM} = V_S/2, C_L = 15pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low, open-drain only	V_{ID} = –100mV, CLR = 0V, Delay from mid-point of input to mid-point of output, R_P = 2.5KΩ		110		ns
T_{PD-LH}	Propagation delay time, low-to-high, push-pull only	V_{ID} = +100mV, CLR = 0V, Delay from mid-point of input to mid-point of output		125		ns
$T_{PD-CLR-F}$	Clear Fall to Latch Reset propagation delay time	CLR = 1.8V to 5V, Delay from CLR falling edge signal to unlatched output condition		25	70	ns
$_{CLR\_Min}$	Minimum Clear Hold Pulse time to register latch disable and transition output state	CLR = 1.8V to 5V, Minimum CLR pulse size required to register a change of state (latch reset) upon CLR falling edge	10			ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100mV		3		ns
T_{RISE}	5V Output Rise Time, 20% to 80%	V_{ID} = +100mV, push-pull only		3		ns
POWER ON TIME						
P_{ON}	Power on-time			35		µs

5.8 Typical Characteristics

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k to 5V (push-pull only), C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

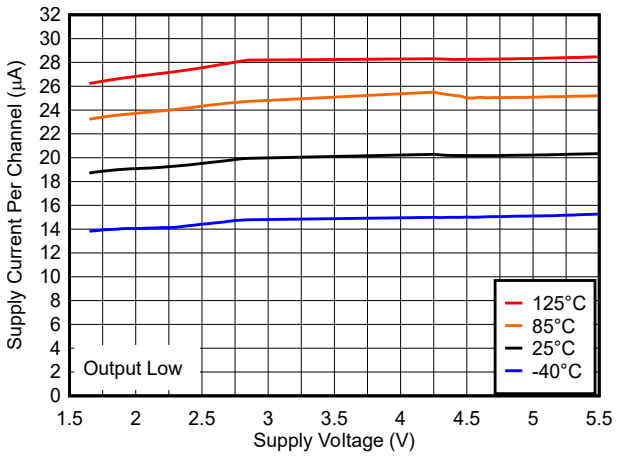


Figure 5-1. Supply Current vs. Supply Voltage

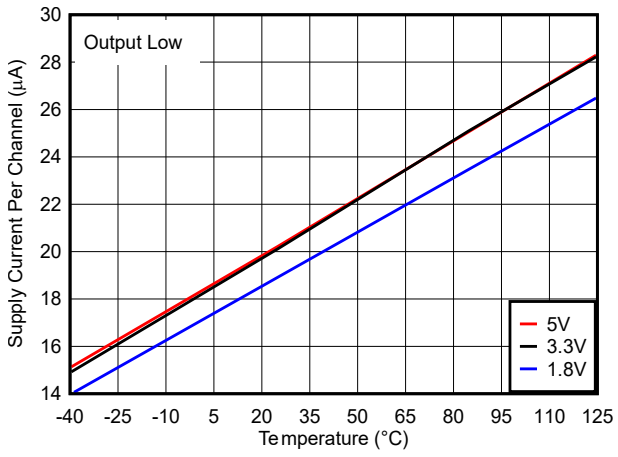


Figure 5-2. Supply Current vs. Temperature

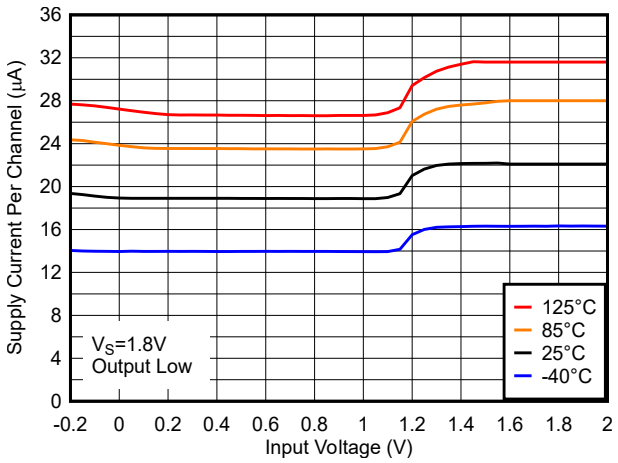


Figure 5-3. Supply Current vs. Input Voltage, 1.8V

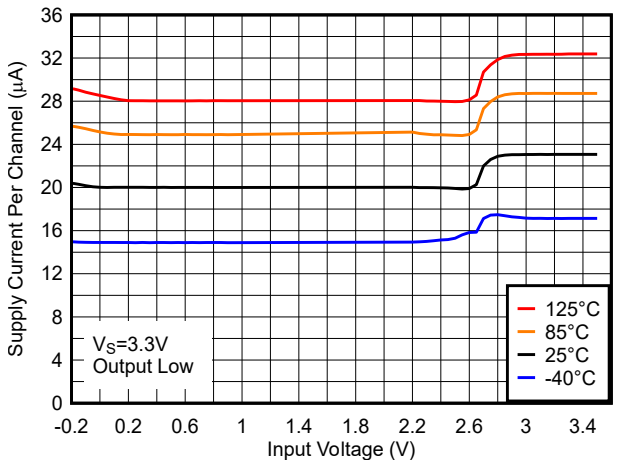


Figure 5-4. Supply Current vs. Input Voltage, 3.3V

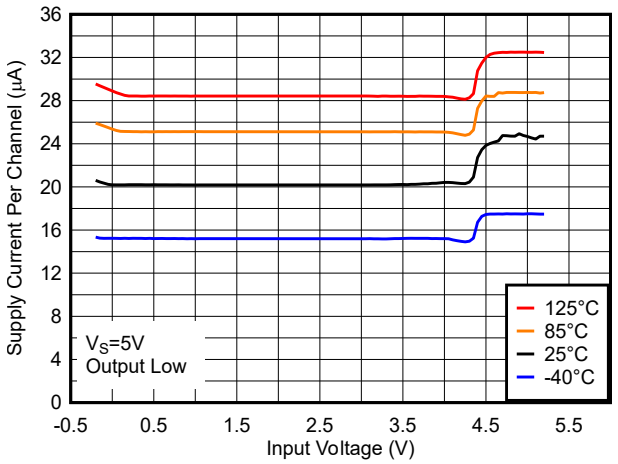


Figure 5-5. Supply Current vs. Input Voltage, 5V

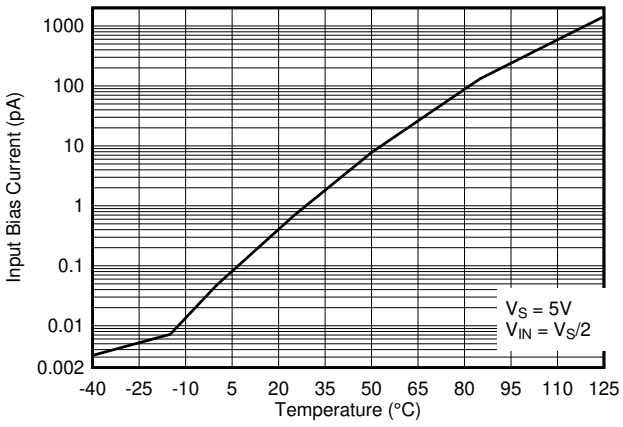


Figure 5-6. Input Bias Current vs. Temperature

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k to 5V (push-pull only), C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

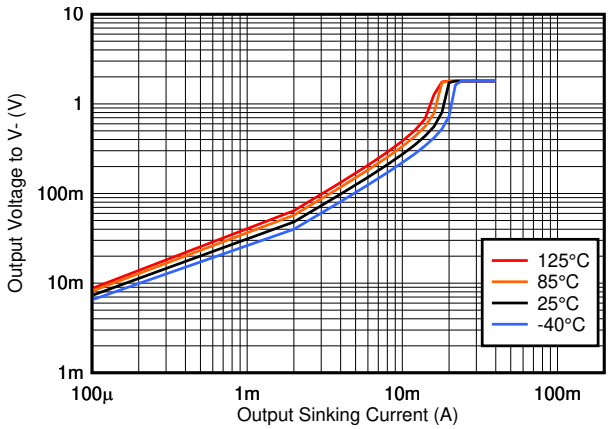


Figure 5-7. Output Sinking Current vs. Output Voltage, 1.8V

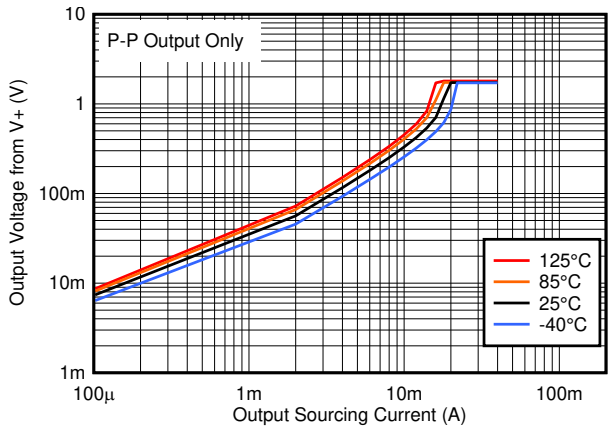


Figure 5-8. Output Sourcing Current vs. Output Voltage, 1.8V

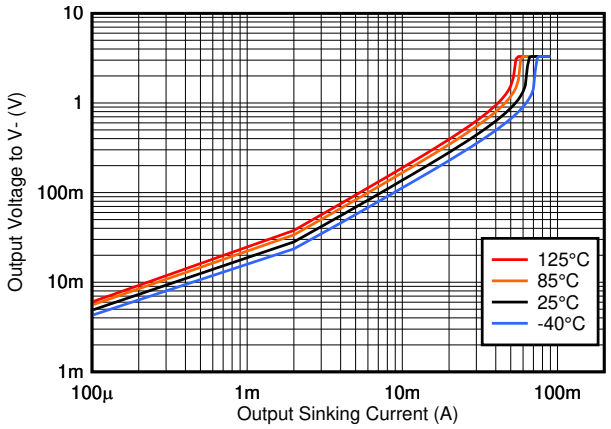


Figure 5-9. Output Sinking Current vs. Output Voltage, 3.3V

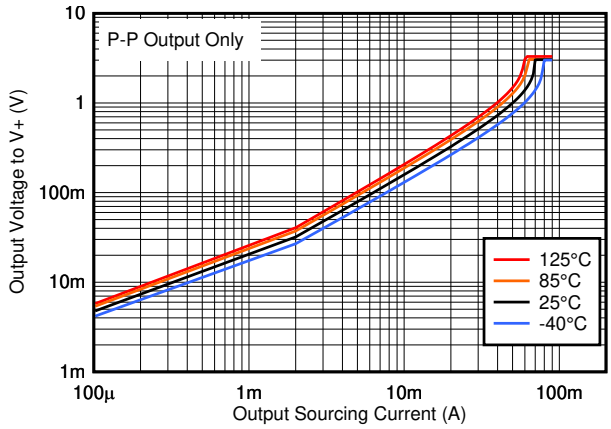


Figure 5-10. Output Sourcing Current vs. Output Voltage, 3.3V

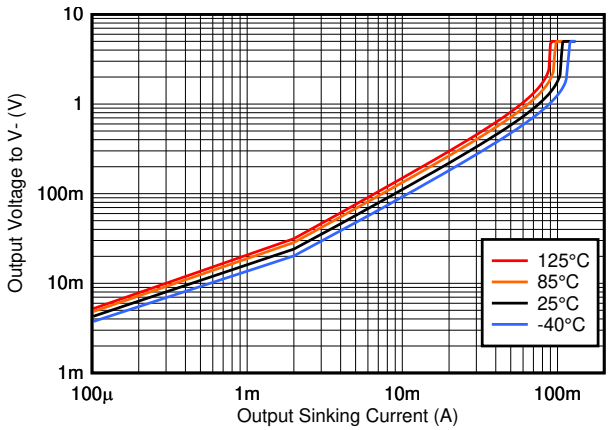


Figure 5-11. Output Sinking Current vs. Output Voltage, 5V

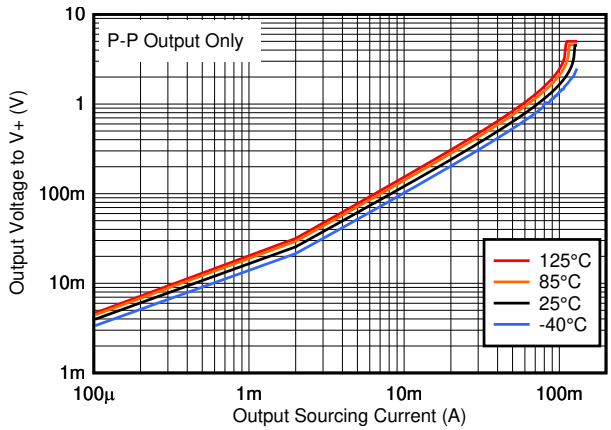


Figure 5-12. Output Sourcing Current vs. Output Voltage, 5V

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k to 5V (push-pull only), C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

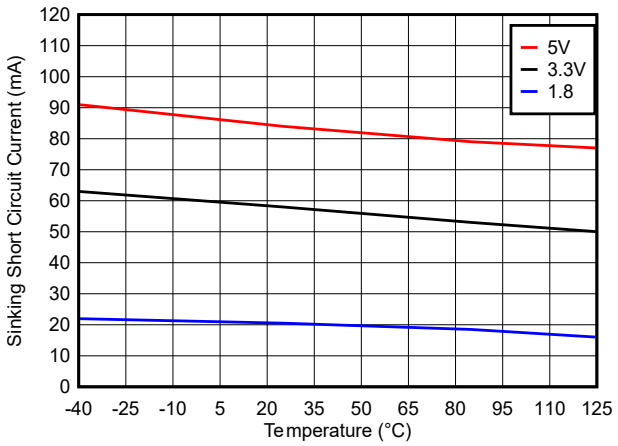


Figure 5-13. Sinking Short Circuit Current vs. Temperature

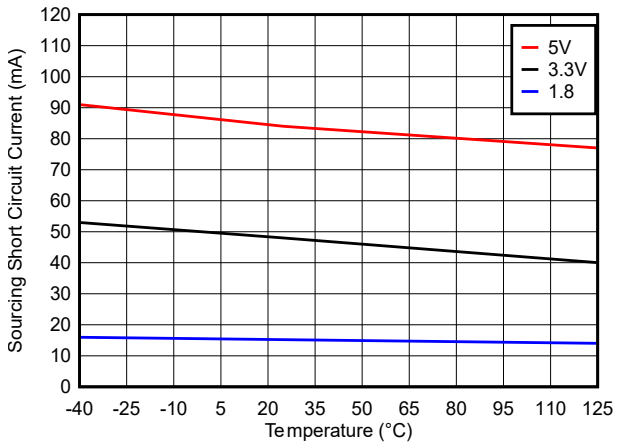


Figure 5-14. Sourcing Short Circuit Current vs. Temperature

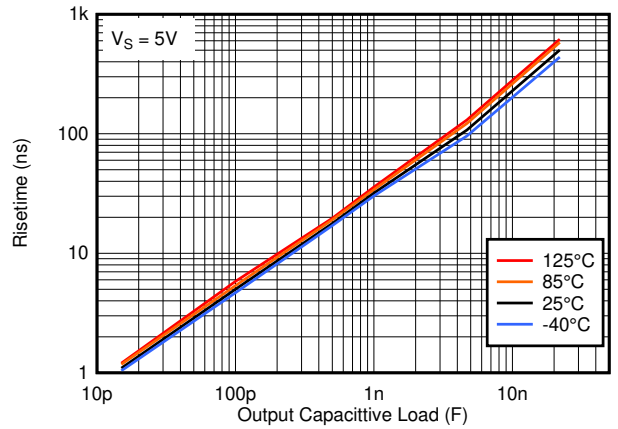


Figure 5-15. Risetime vs. Capacitive Load

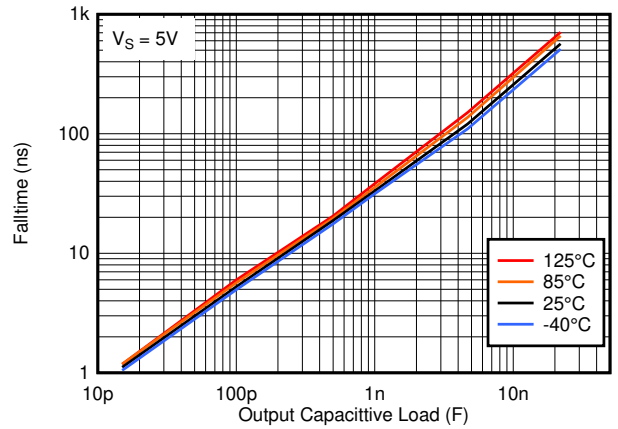


Figure 5-16. Falltime vs. Capacitive Load

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k to 5V (push-pull only), C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

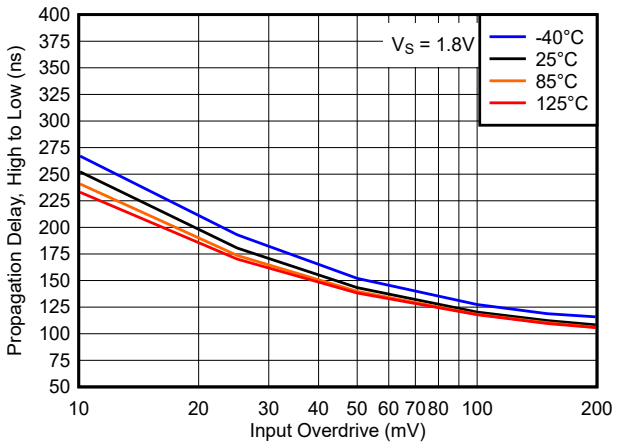


Figure 5-17. Propagation Delay, High to Low, 1.8V

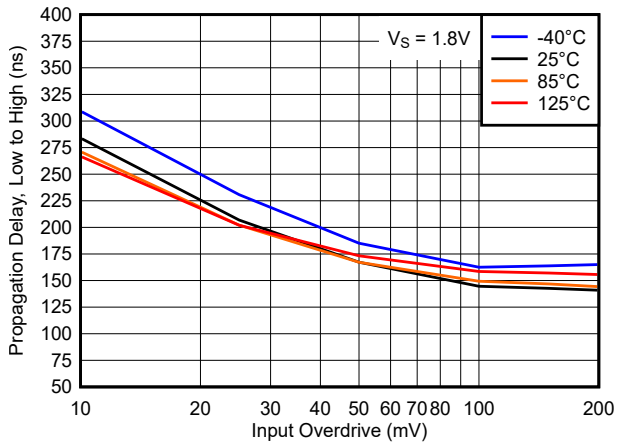


Figure 5-18. Propagation Delay, Low to High, 1.8V

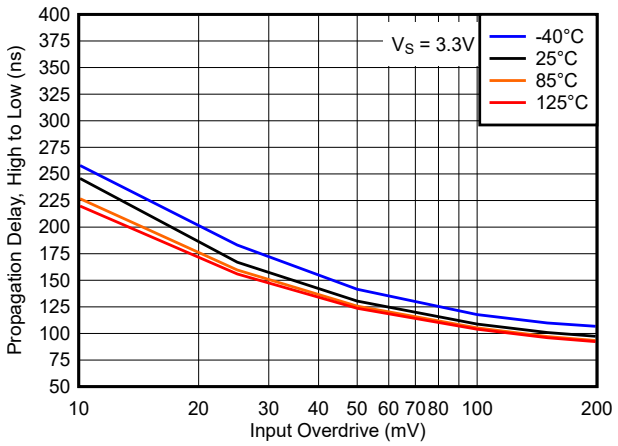


Figure 5-19. Propagation Delay, High to Low, 3.3V

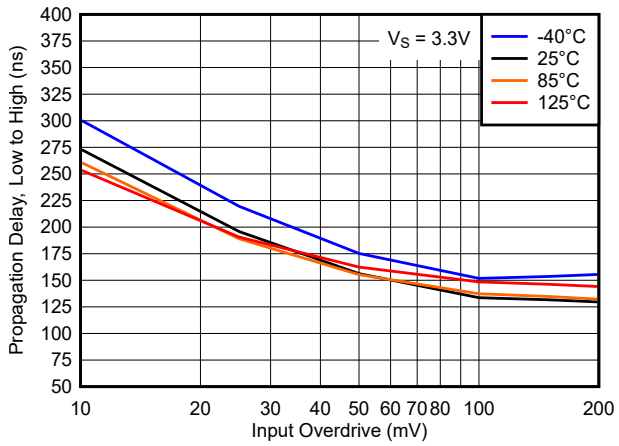


Figure 5-20. Propagation Delay, Low to High, 3.3V

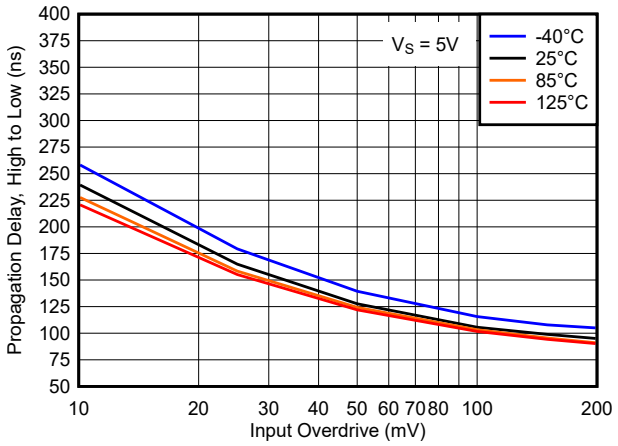


Figure 5-21. Propagation Delay, High to Low, 5V

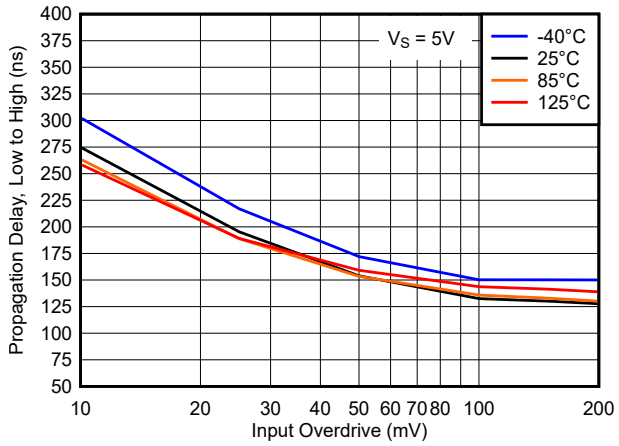


Figure 5-22. Propagation Delay, Low to High, 5V

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k to 5V (push-pull only), C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

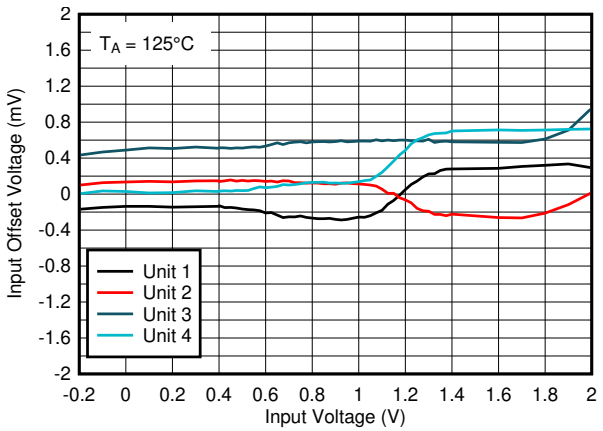


Figure 5-23. Offset Voltage vs. Input Voltage at 125°C, 1.8V

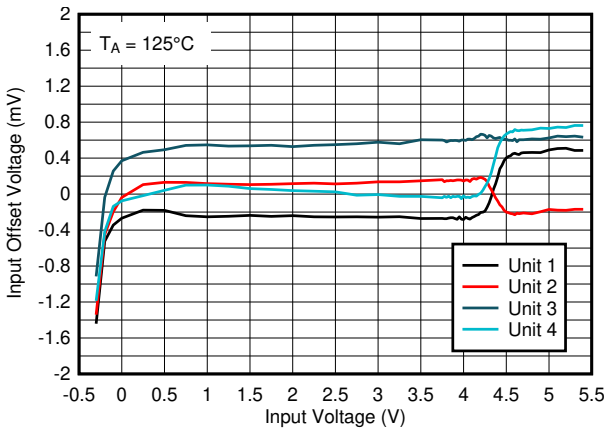


Figure 5-24. Offset Voltage vs. Input Voltage at 125°C, 5V

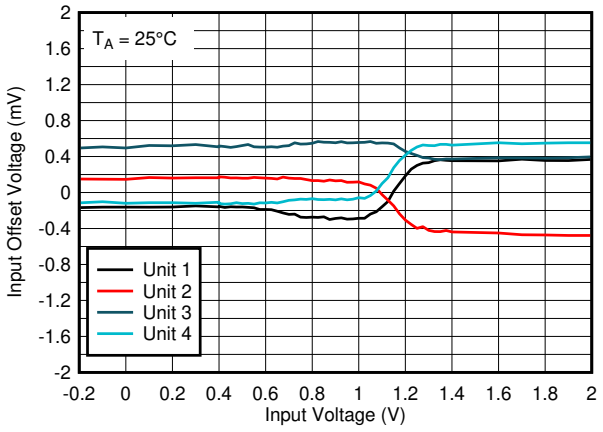


Figure 5-25. Offset Voltage vs. Input Voltage at 25°C, 1.8V

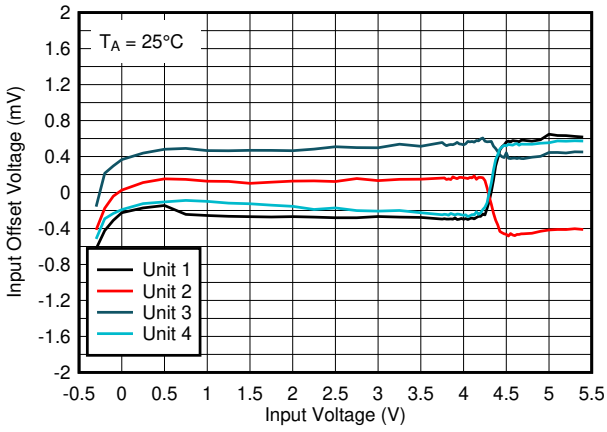


Figure 5-26. Offset Voltage vs. Input Voltage at 25°C, 5V

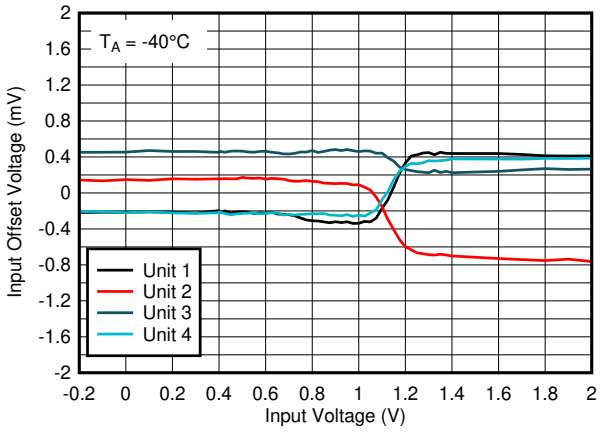


Figure 5-27. Offset Voltage vs. Input Voltage at -40°C, 1.8V

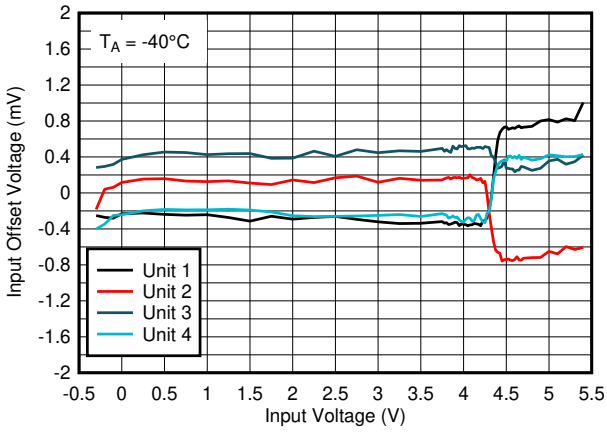


Figure 5-28. Offset Voltage vs. Input Voltage at -40°C, 5V

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 5.1k to 5V (push-pull only), C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

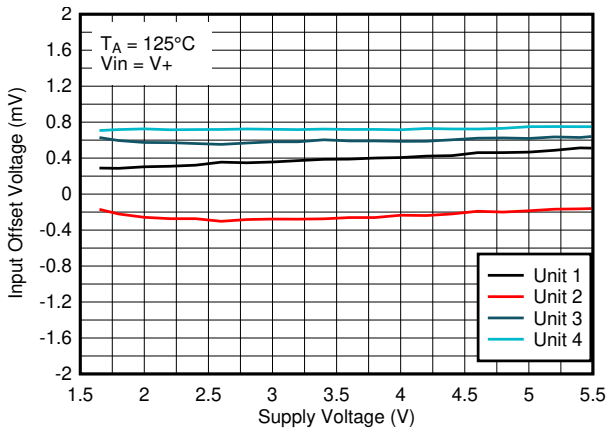


Figure 5-29. Offset Voltage vs. Supply Voltage at 125°C, V_{IN}=V+

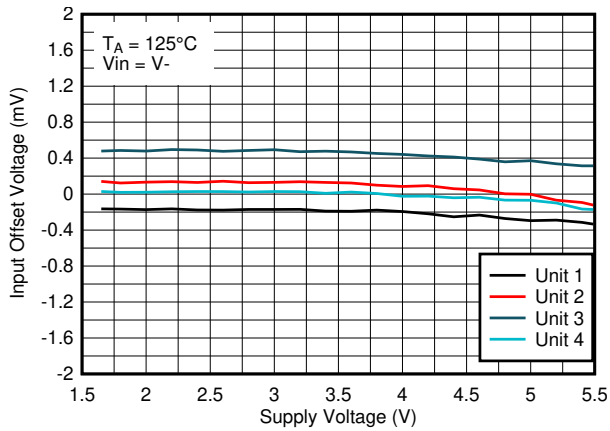


Figure 5-30. Offset Voltage vs. Supply Voltage at 125°C, V_{IN}=V-

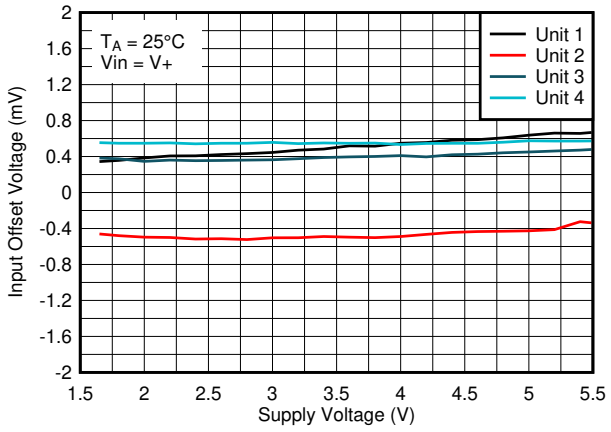


Figure 5-31. Offset Voltage vs. Supply Voltage at 25°C, V_{IN}=V+

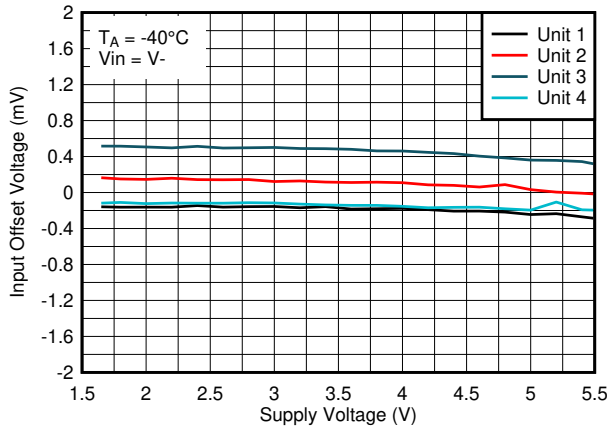


Figure 5-32. Offset Voltage vs. Supply Voltage at 25°C, V_{IN}=V-

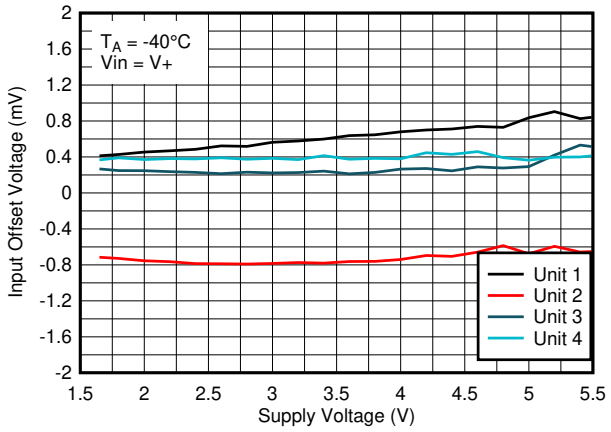


Figure 5-33. Offset Voltage vs. Supply Voltage at -40°C, V_{IN}=V+

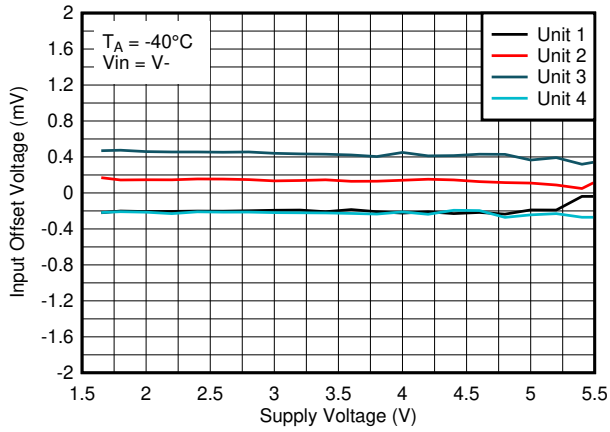


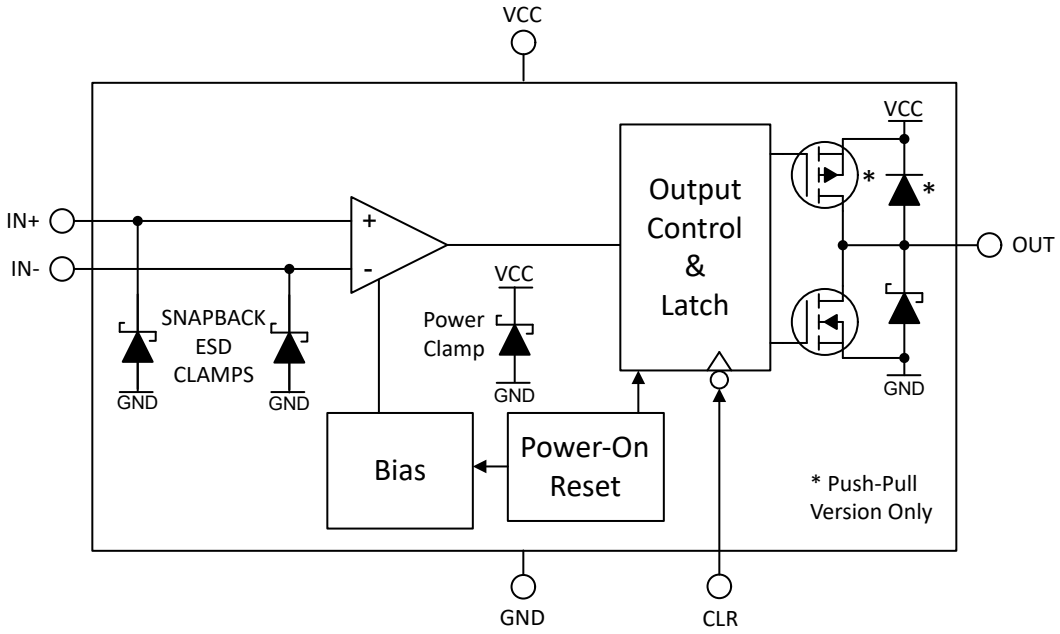
Figure 5-34. Offset Voltage vs. Supply Voltage at -40°C, V_{IN}=V-

6 Detailed Description

6.1 Overview

The TLV902xL and TLV903xL are a family of single and dual channel latching comparators. The family offers low input offset voltage, power on reset (POR), fault-tolerant inputs and an excellent speed-to-power combination with a propagation delay of 110ns with a quiescent supply current of 22µA per channel.

6.2 Functional Block Diagrams



6.3 Feature Description

The unique feature of the TLV902xL and TLV903xL is the output latching capability. The output latches upon the first threshold crossing to allow capturing of an event or error condition without the full attention of a system controller. This allows events to be captured at start up while the system controller is still initializing. The system controller can reset the latch after performing any needed tasks. The user has the option of the output being un-latched at power-on ("L1" option), or latched at power-up ("L2" option).

These comparators also feature fault-tolerant inputs that can go up to 6V without damage with no output phase inversion. This makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

6.4 Device Functional Modes

6.4.1 Outputs

6.4.1.1 TLV902xL Open-Drain Output

The TLV902xL features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to any voltage up to 5.5V, independent of the comparator supply voltage (V_S). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation.

TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower pull-up resistor values helps decrease the rising edge risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) creates an exponential rising edge due to the RC time constant and increase the risetime.

Unused open drain outputs can be left floating, or can be tied to the V- pin if floating pins are not allowed.

The open-drain output protection consists of a ESD clamp between the output and V- to allow the output to be pulled to any voltage up to a maximum of 5.5V, even if the pull-up voltage exceeds V_S.

6.4.1.2 TLV903xL Push-Pull Output

The TLV903xL features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor and provides symmetrical edge rates independent of capcitive load.

The push-pull output must never be connected to another output. Directly shorting the output to the opposite supply can result in thermal runaway and eventual device destruction. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, or ground, or any another output.

The output protection consists of a ESD clamp between the output and V-, and also between the output and V+, so the output must not exceed either supply rail.

6.4.2 Power-On Reset (POR)

The TLV90xxL has a internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V_s) is ramping up or ramping down, the POR circuitry is activated for up to 60µs (over temperature) after the minimum supply voltage threshold of V_{POR} is crossed (typically 1.25V), or immediately when the supply voltage drops below V_{POR}. During the POR period, the input conditions are ignored. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input ("L1" option), or initially in a latched condition ("L2" option).

The input levels must be settled before the end of the POR period to prevent premature latching. Attention must be payed to the time constants of any filtering or RC components on the inputs (references, dividers, bypass capacitors, et cetera).

The open drain and push-pull output types have different POR and latch behaviors. The next section explains these differences.

6.4.2.1 TLV902xL Open Drain Output POR Behavior

For the TLV902x**L1** open-drain output, the POR circuit keeps the output **high**, or high impedance ("HI-Z"), during the POR period (t_{on}).

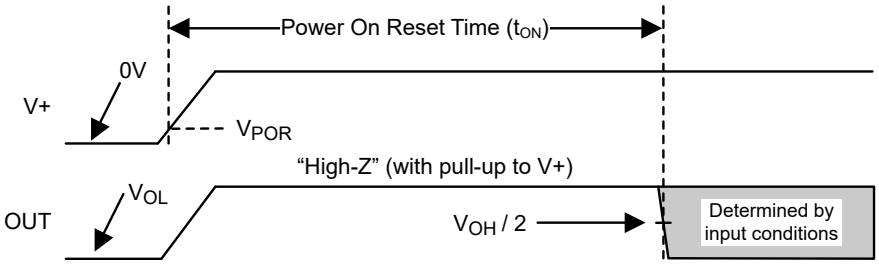


Figure 6-1. TLV902xL1 Power-On Reset Timing Diagram Example

The nature of an open collector output is that the output rises with the pull-up voltage during the POR period.

The TLV902x**L2** option starts with the output **low** through POR then remains latched **low** post-POR until cleared.

6.4.2.2 TLV903xL Push-Pull Output POR Behavior

For the TLV903x**L1** push-pull output, the POR circuit keeps the output High-Z, neither sourcing or sinking current. The output can randomly "Float" between V+ and V- during the POR period (ton). A light pull-up (to V+) or pull-down (to V-) resistor can be used to pre-bias the output condition to prevent the output from floating.

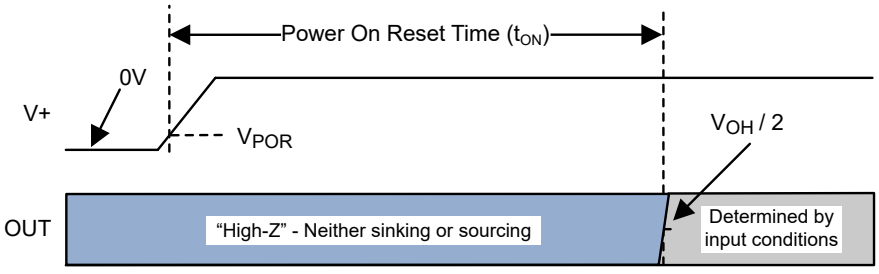


Figure 6-2. TLV903xL1 Power-On Reset Timing Diagram Example

The TLV903x**L2** option starts with the output **high** (sourcing) through POR then latched **high** post-POR until cleared.

6.4.3 Output Latching

The TLV90xxL has an output that latches upon the first input transition crossing through the input threshold after being armed. The output stays latched until the falling edge of the CLR pin.

The user has the option of the output being **un-latched at power-on** ("L1" option), or **latched at power-on** ("L2" option).

The latch behavior is different between the Open-Drain and Push-Pull output types. The behaviors are explained in the following sections.

6.4.3.1 "L1" and "L2" Power-On Options

The TLV90xxL is available with two power-on options.

The "**L1**" option comes out of POR with the output in the **un-latched** state and is armed for the next latch event.

The "**L2**" option comes out of POR with the output held in the **latched** condition, and must be cleared by a high-to-low transition on the CLR pin to arm the comparator for the next latch event.

The Function Summary table below summarizes the behaviors.

Table 6-1. Function Summary

Device	Output Type	Output state during POR	Output State after POR	Armed output latches on:	Output Latch Condition
TLV902xL1	Open-Drain	High	Armed	H → L	Low
TLV902xL2	Open-Drain	Low	Latched Low	H → L	Low
TLV903xL1	Push-Pull	Hi-Z	Armed	L → H	High
TLV903xL2	Push-Pull	High	Latched High	L → H	High

See the following sections describing the latched state behavior for the different output types in detail.

6.4.3.2 TLV902xL1 Open-Drain Latch Behavior

The TLV902xL1 open-drain output is high during the POR period. After the POR period the latch is armed and **latches low** upon the first **high-to-low** output transition.The following is a summary of the latch operation.

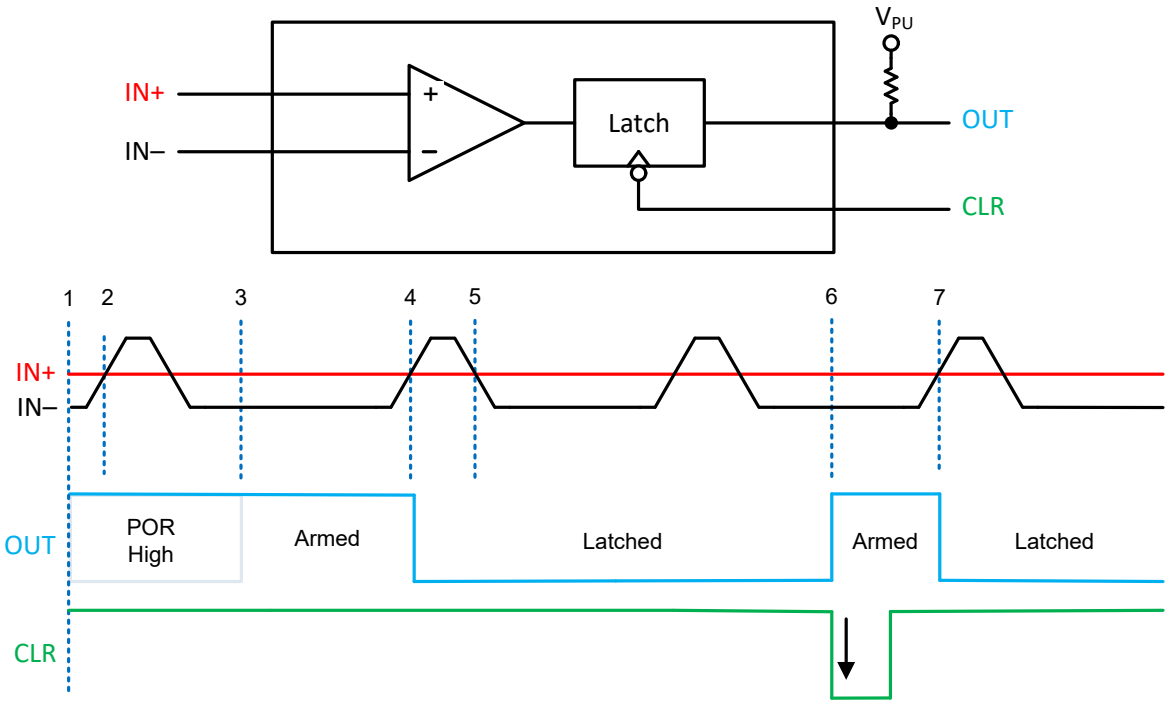


Figure 6-3. Open Drain Latch Timing Example ("L1" option)

1. Output is high during the POR period at first power-up.
2. During POR period, input transition is ignored.
3. Following the POR period, comparator is armed and monitors inputs.
4. IN- now higher than IN+, setting output low and latching low.
5. IN+ greater then IN-, but output still remains low (latched).
6. CLR falling edge resets latch for next transition. IN+ > IN-, output remains high and armed for next input transition.
7. IN- > IN+, setting output low and latching again. Output remains latched even when IN+ > IN-.

6.4.3.3 TLV902xL2 Open-Drain Latch Behavior

The TLV902xL2 open-drain output latches **low** during the POR period. Following the POR period, the output is **latched low** and must be cleared with a **high-to-low** transition on the CLR pin.The following is a summary of the latch operation.

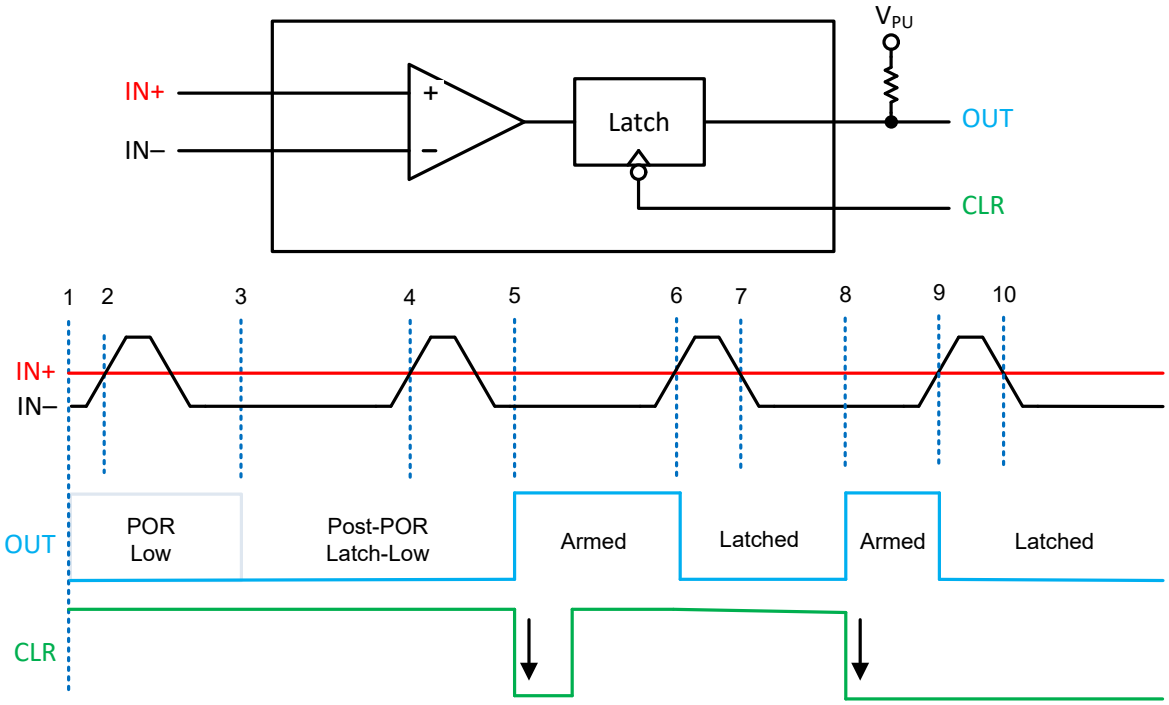


Figure 6-4. Open Drain Latch Timing Example ("L2" option)

The following is a summary of the latch operation.

1. Output is low during the POR period following first power-on.
2. Input transition is ignored during POR period.
3. Following the POR period, the OUT stays latched low.
4. IN- passes IN+, but transition is ignored during latch.
5. CLR falling edge resets and arms latch awaiting next transition.
6. IN- > IN+, so OUT goes low and latches.
7. IN+ > IN-, but OUT remains latched low.
8. CLR falling edge resets and arms latch for next transition.
9. IN- crosses IN+, output goes low and latches again.
10. Output remains latched low even when IN+ > IN-.

6.4.3.4 TLV903xL1 Push-Pull Latch Behavior

The TLV903xL1 push-pull output is **High-Z** (niether sinking or sourcing current) during the POR period. Following the POR period, the latch is armed and **latches high** upon the first **low-to-high** output transition.

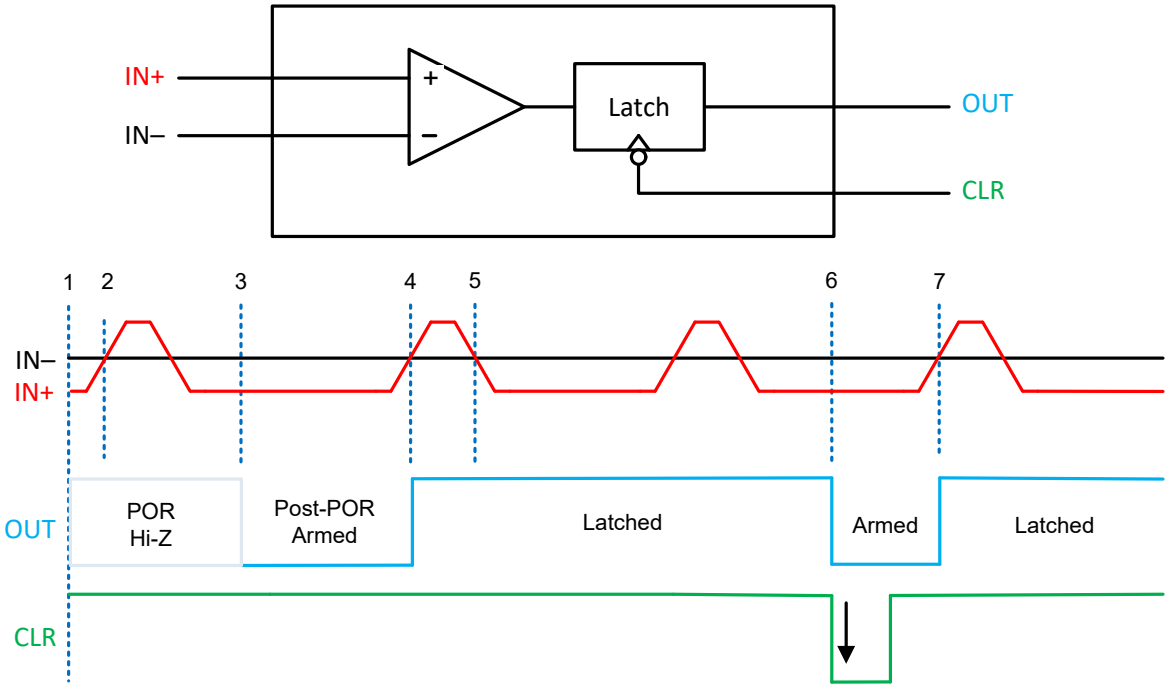


Figure 6-5. Push-Pull Latch Timing Example ("L1" option)

The following is a summary of the latch operation.

1. Output is Hi-Z during the POR period at first power-up.
2. During POR period, input transition is ignored.
3. Following the POR period, comparator is armed and monitors inputs.
4. IN+ now higher than IN-, setting output high and latching high.
5. IN- greater than IN+, but output still remains high (latched).
6. CLR falling edge resets latch for next transition. IN- > IN+, output remains low and armed for next input transition.
7. IN+ > IN-, setting output high and latching again. Output remains latched even when IN- > IN+.

6.4.3.5 TLV903xL2 Push-Pull Latch Behavior

The TLV903xL2 push-pull output latches **high (sourcing current)** during the POR period. Following the POR period, the output is **latched high** and must be cleared by a high-to-low transition on the CLR pin.

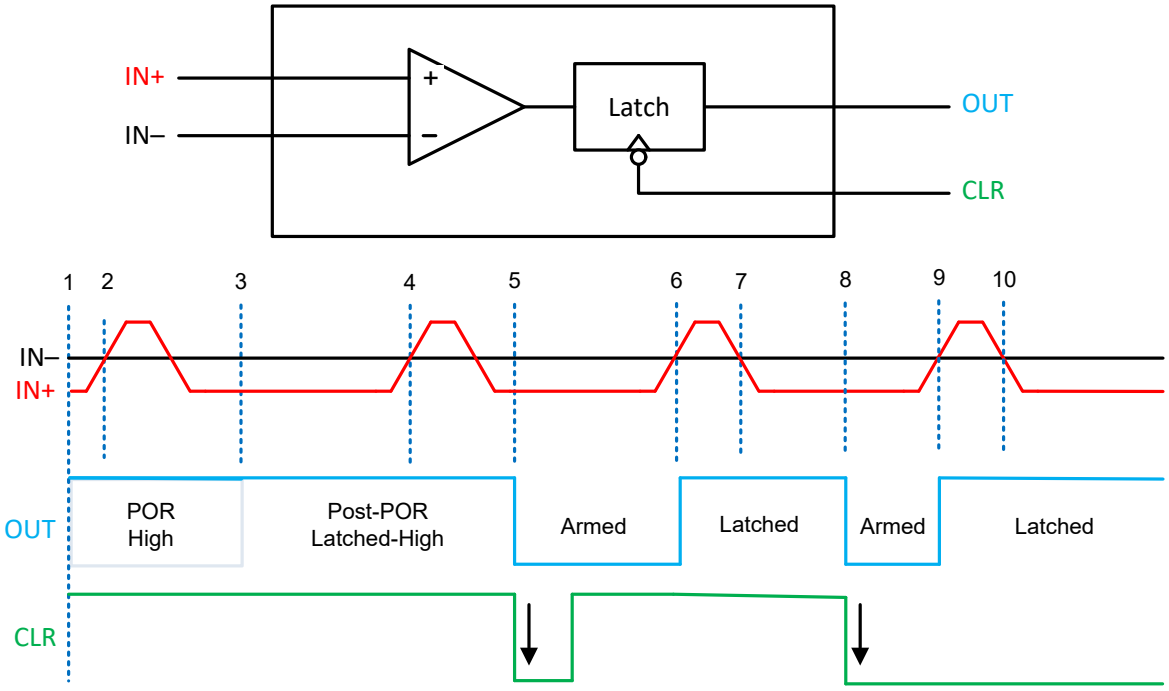


Figure 6-6. Push-Pull Latch Timing Example ("L2" option)

The following is a summary of the latch operation.

1. Output is high during the POR period following first power-on.
2. Input transition is ignored during POR period.
3. Following the POR period, the OUT latches high.
4. IN+ passes IN-, but transition is ignored during latch.
5. CLR falling edge resets and arms latch awaiting next transition.
6. IN+ > IN-, so OUT goes high and latches.
7. IN- > IN+, but OUT remains latched high.
8. CLR falling edge resets and arms latch for next transition.
9. IN+ crosses IN-, output goes high and latches again.
10. Output remains latched high even when IN- > IN+.

6.4.3.6 Clear (CLR) Input

When CLR is high or low, and the comparator is not in a latched condition, the comparator is active ("armed") and responding to the input conditions, ready for the next qualifying condition to latch.

The CLR input only clears the output latch on the high-to-low (falling) edge of the CLR input. The comparator is then active (armed) after the clear until the next latch condition event.

Using the falling-edge to trigger the reset allows the CLR pin to be either a steady high or low, which prevents a hardware or software failure from locking-up the comparator and allows meeting saftey-critical design requirements.

There can be a setup-time contention if the CLR pin is transitioning (falling) at the same time as the comparator output transitions. The output state is indeterminate during the CLR falling edge time. The recommendation is to make the CLR falling-edge as fast as possible to aviod this contention (<100ns fall time).

The CLR pin features a Failsafe, or "5V Compatible" input, accepting logic high levels up to 5V, independent of the comparator supply voltage. The logic high (VOH) threshold is 1.2V.

The CLR input also has a light 200nA active pull-down current to make sure that the CLR pin is low during start-up and the comparator is active. Even with this pull-down, floating the CLR input is not recommended.

6.4.4 Inputs

6.4.4.1 Rail to Rail Input

The TLV90xxL input voltage range extends from 200mV below V- to 200mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input pins exceed V+ or V-.

6.4.4.2 Fail-Safe Inputs

The TLV90xxL inputs are fault tolerant up to 5.5V independent of V_S. Fault tolerant is defined as maintaining the same high input impedance when V_S is un-powered or within the recommended operating ranges.

The fault tolerant inputs can be any value between 0V and 5.5V, even while V_S is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the maximum specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains high impedance even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state is correct.

The following is a summary of input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random). *Do not* operate in this region. The output can randomly flip.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain data sheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

6.4.4.3 Input Protection

The TLV90xxL family incorporates internal ESD protection circuits on all pins. The inputs use a proprietary "snapback" type ESD clamp from each pin to V-. There is no "upper" ESD clamp to V+, which allows the input pins to exceed the supply voltage (V+). During an ESD event, the snapback diodes "short" and go low impedance to V- (like an SCR).

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct due to transients. The current must be limited 10mA or less. This series resistance can be part of any resistive input dividers or networks.

The ESD diodes can not clamp on the upper voltages. The ESD clamps do not "hold" at a fixed maximum voltage like a Zener diode. If the inputs are connected to a source that can exceed 5.5V, then external clamping is required to prevent exceeding the maximum input voltage.

The input bias current is typically 5pA for input voltages between V+ and V-. Input bias current typically doubles for each 10°C temperature increase.

6.4.4.4 Internal Hysteresis

The TLV90xxL does NOT have built-in hysteresis. The latching function negates the need for hysteresis as the output latches upon the first output transition. The reference level must be set to the desired threshold level, and the input signals well filtered to remove any noise or transients that can cause early triggering.

6.4.4.5 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output.

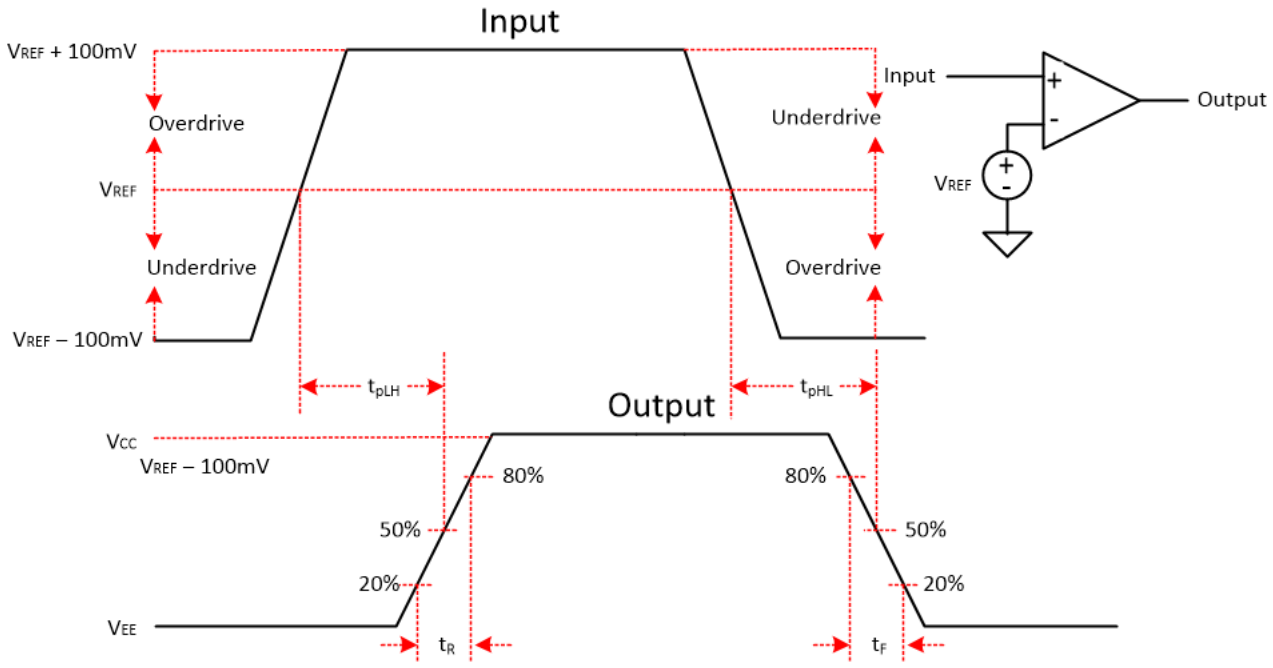


Figure 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 7-2 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV902xL1) if the outputs are directly connected together.

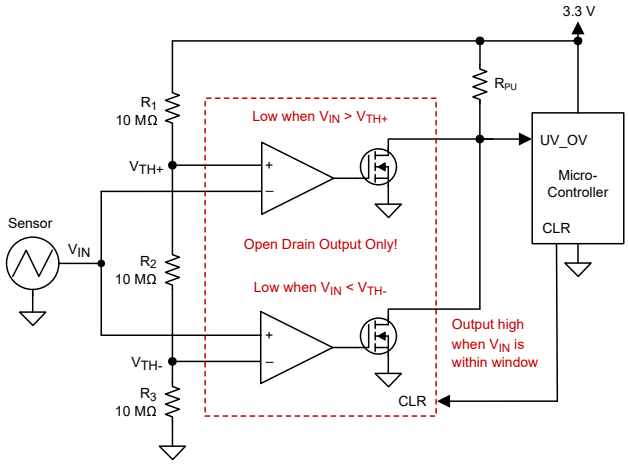


Figure 7-2. Window Comparator using TLV9022L1

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Latch (logic low output) when an input signal is less than 1.1V
- Latch (logic low output) when an input signal is greater than 2.2V
- Operate from a 3.3V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 7-2. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and non-inverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-OR'ed together.

The respective comparator outputs latches low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in Figure 7-3.

The CLR pin must be toggled high to low to reset the output and arm the comparator.

7.2.1.3 Application Curve

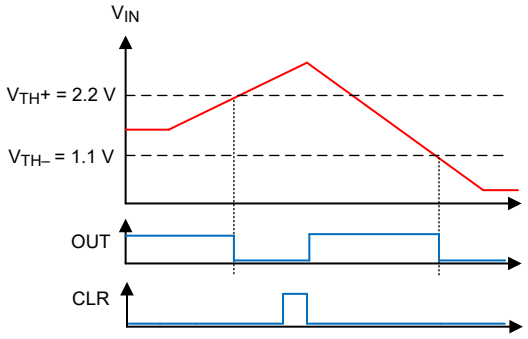


Figure 7-3. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.3 Power Supply Recommendations

Due to the fast output edges, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) and (V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications, maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

7.4.2 Layout Example

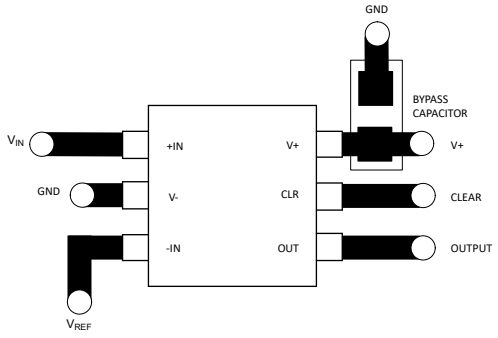


Figure 7-4. Single Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9022L1RUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WD
TLV9032L1RUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1WE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

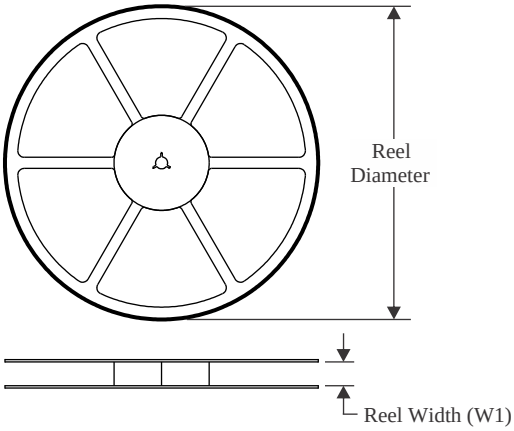
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

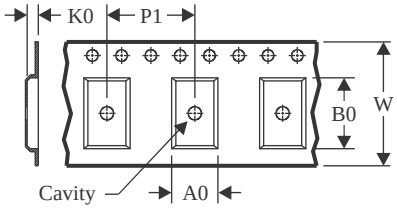
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

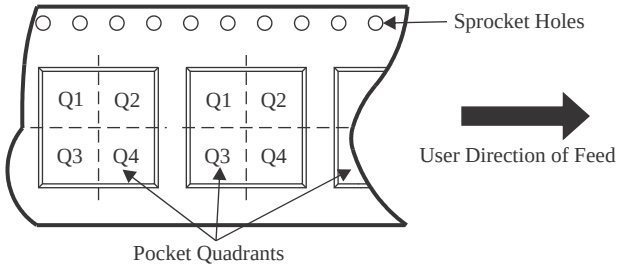


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

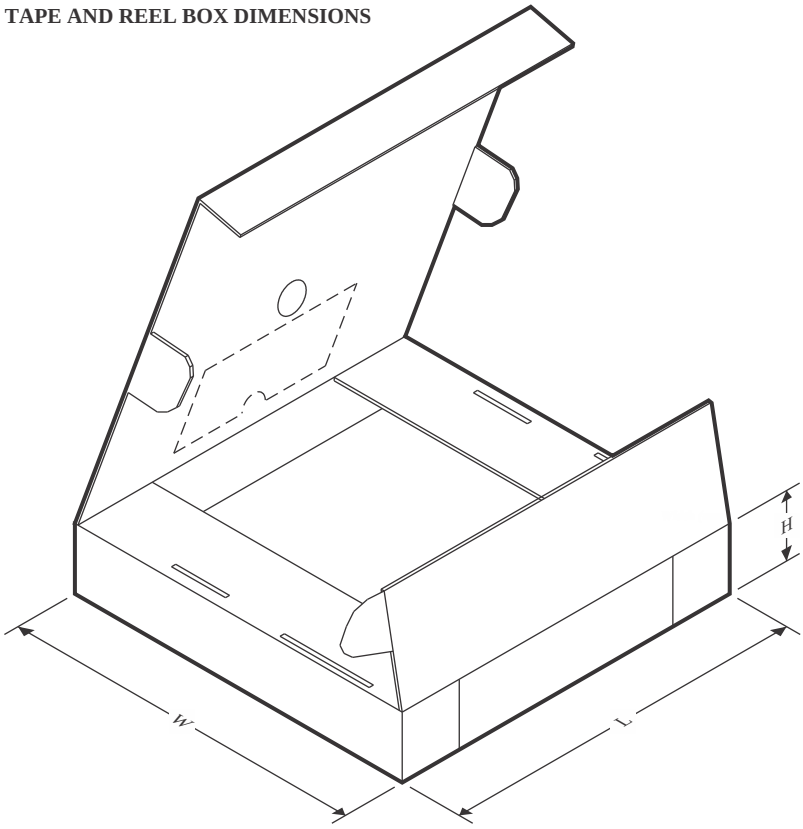
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9022L1RUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1
TLV9032L1RUGR	X2QFN	RUG	10	3000	180.0	8.4	1.75	2.25	0.55	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

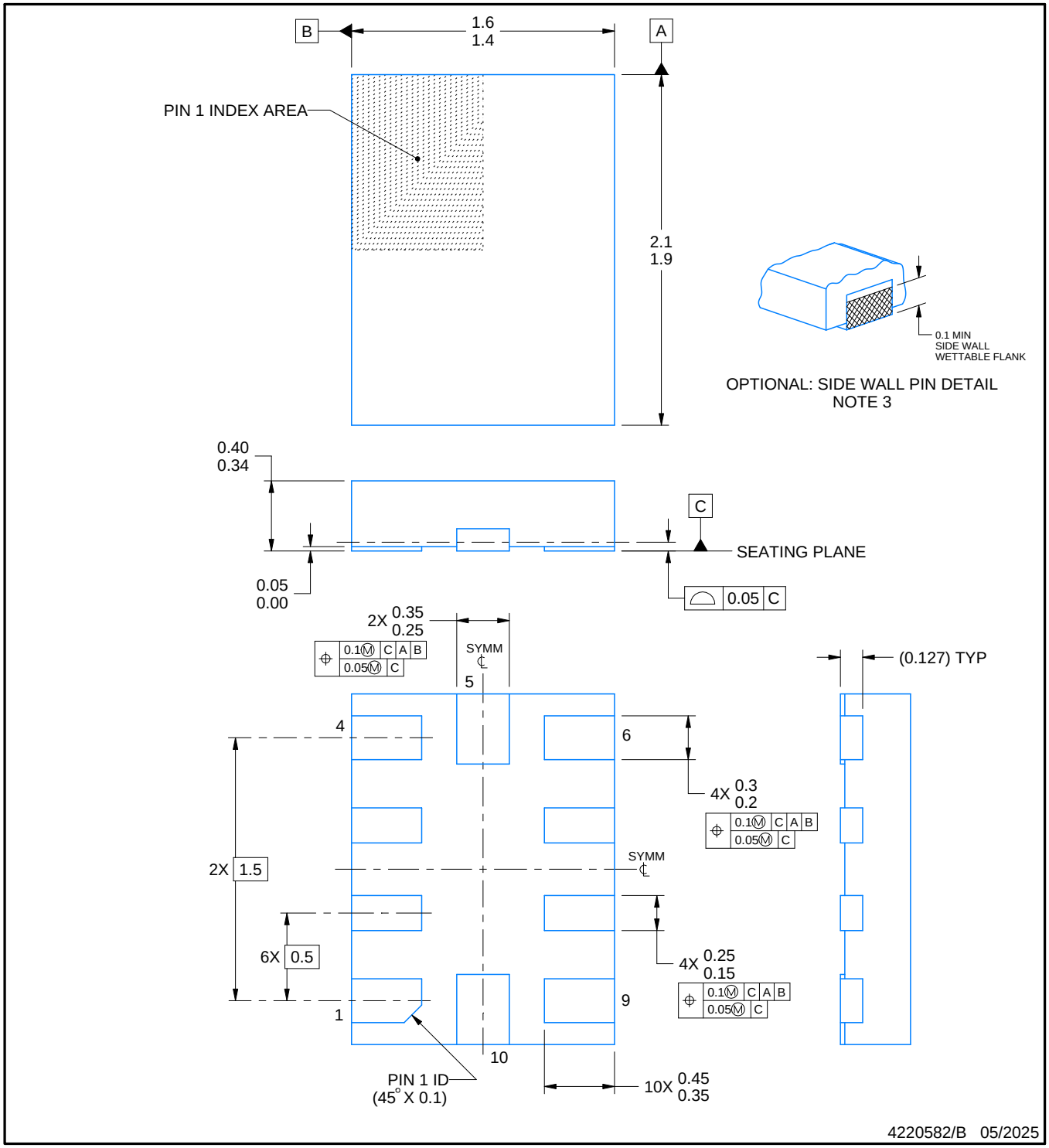
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9022L1RUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0
TLV9032L1RUGR	X2QFN	RUG	10	3000	210.0	185.0	35.0

RUG0010B

PACKAGE OUTLINE

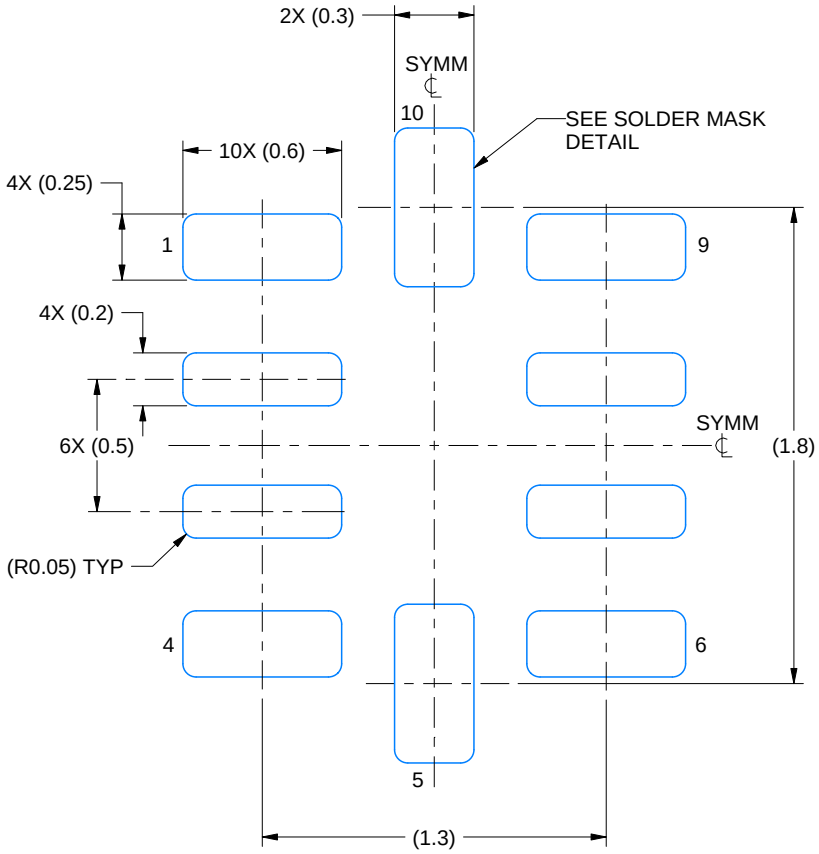
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

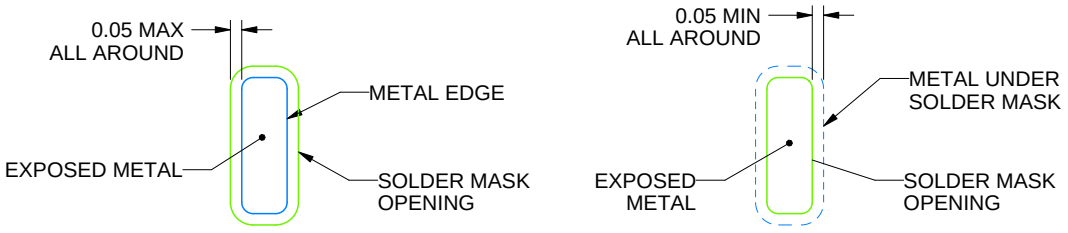


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X



SOLDER MASK DETAILS

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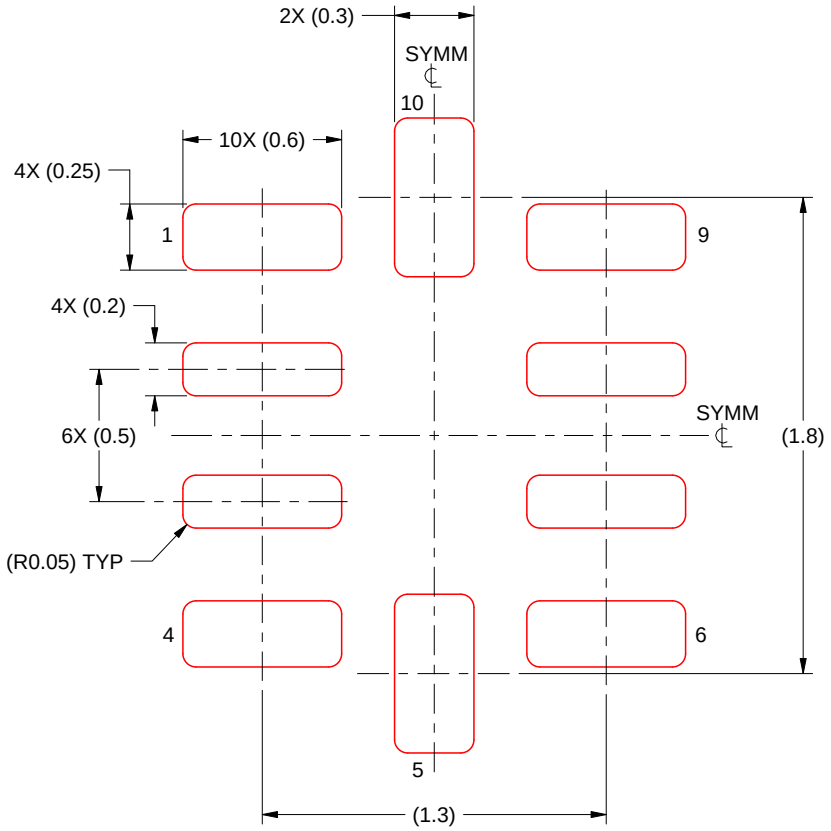
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

4220582/B 05/2025

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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