TLV900x-Q1 Low-Power RRIO 1MHz Automotive Operational Amplifier

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- Scalable CMOS amplifier for low-cost applications
- Rail-to-rail input and output
- Low input offset voltage: ±0.4mV
- Unity-gain bandwidth: 1MHz
- Low broadband noise: $27\text{nV}/\sqrt{\text{Hz}}$
- Low input bias current: 5pA
- Low quiescent current: 60µA/Ch
- Unity-gain stable
- Internal RFI and EMI filter
- Operational at supply voltages as low as 1.8V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Functional Safety-Capable
  - Functional Safety Information

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment and Cluster
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- On-board (OBC) and wireless charger
- Power-train current sensor
- Advanced driver assistance systems (ADAS)
- Single-supply, low-side, unidirectional current-sensing circuit

3 Description

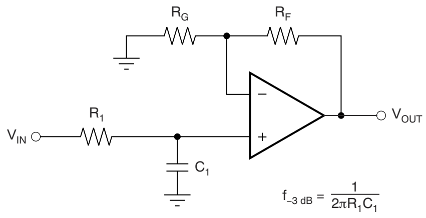
The TLV900x-Q1 family includes single (TLV9001-Q1), dual (TLV9002-Q1), and quad-channel (TLV9004-Q1) low-voltage (1.8V to 5.5V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective option for space-constrained automotive applications such as infotainment and lighting where low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the TLV900x-Q1 family is 500pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (1.8V to 5.5V) with performance specifications similar to the TLV600x-Q1 devices.

The robust design of the TLV900x-Q1 family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

Package Information (2)

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
TLV9001-Q1	DBV (SOT-23, 5)	1.60mm × 2.90mm
	DCK (SC70, 5)	1.25mm × 2.00mm
TLV9002-Q1	D (SOIC, 8)	3.91mm × 4.90mm
	PW (TSSOP, 8)	3.00mm × 4.40mm
	DGK (VSSOP, 8)	3.00mm × 3.00mm
TLV9004-Q1	DYY (SOT-23, 14)	4.20mm × 1.90mm
	D (SOIC, 14)	8.65mm × 3.91mm
	PW (TSSOP, 14)	4.40mm × 5.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) See *Device Comparison Table*



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Single-Pole, Low-Pass Filter

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4 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS					
		SOT-23 DBV	SC70 DCK	SOIC D	TSSOP PW	VSSOP DGK	SOT-23 DYY
TLV9001-Q1	1	5	5	—	—	—	
TLV9002-Q1	2	—	—	8	8	8	—
TLV9004-Q1	4	—	—	14	14	—	14

5 Pin Configuration and Functions

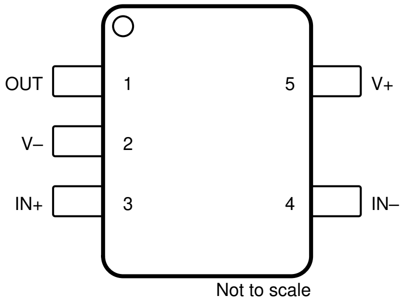


Figure 5-1. TLV9001-Q1 DBV Package, 5-Pin SOT-23 (Top View)

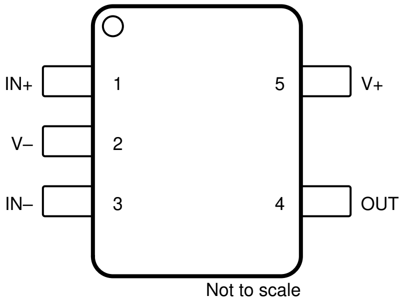


Figure 5-2. TLV9001-Q1 DCK Package, 5-Pin SC70 (Top View)

Table 5-1. Pin Functions: TLV9001-Q1

PIN			TYPE[1]	DESCRIPTION
NAME	SOT-23	SC70		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	5	I	Positive (high) supply

(1) I = input, O = output

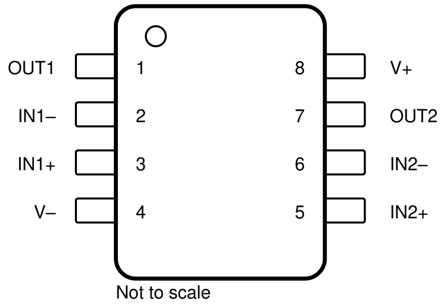


Figure 5-3. TLV9002-Q1 D, DGK, PW Packages, 8-Pin SOIC, VSSOP, TSSOP (Top View)

Table 5-2. Pin Functions: TLV9002-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I or —	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

(1) I = input, O = output

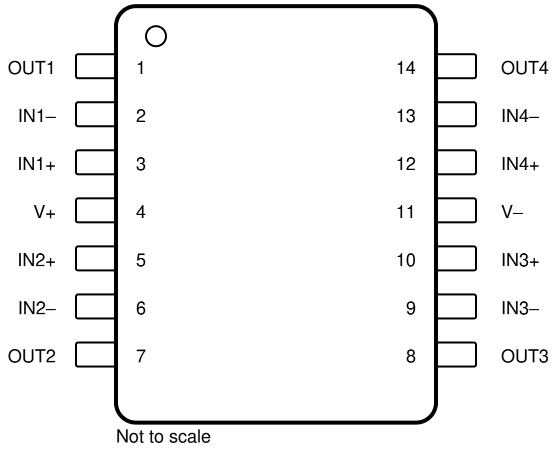


Figure 5-4. TLV9004-Q1 D, PW, DYY Packages, 14-Pin SOIC, TSSOP, SOT-23 (Top View)

Table 5-3. Pin Functions: TLV9004-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage ([V+] – [V–])			0	6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential (4)		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		mA
Operating, T_A			–55	150	°C
Junction, T_J				150	°C
Storage, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.
(4) Differential input voltages greater than 0.5V applied continuously can result in a shift to the input offset voltage and quiescent current above the maximum specifications of these parameters. The magnitude of this effect increases as the ambient operating temperature rises.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 Specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TLV9001-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	232.5	239.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	131.0	148.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.6	82.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	66.5	54.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	99.1	81.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TLV9002-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.9	196.6	180.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	92.0	86.2	84.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95.4	118.3	120.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	40.2	23.2	15.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.7	116.7	117.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		TLV9004-Q1			UNIT
		D (SOIC)	DYY (SOT-23)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.1	154.3	135.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	71.2	86.8	63.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.1	67.9	78.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.6	10.1	13.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.7	67.5	77.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

6.7 Electrical Characteristics

For V_S = (V+) – (V–) = 1.8V to 5.5V (±0.9V to ±2.75V), T_A = 25°C, R_L = 10kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	Vs = 5V		±0.4	±1.85	mV
		Vs = 5V, T_A = –40°C to 125°C			±2	mV
dV_{OS}/dT	V_{OS} vs temperature	T_A = –40°C to 125°C		±0.6		μV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8V to 5.5V, V_{CM} = (V–)	80	105		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 1.8V, (V–) – 0.1V < V_{CM} < (V+) – 1.4V, T_A = –40°C to 125°C		86		dB
		V_S = 5.5V, (V–) – 0.1V < V_{CM} < (V+) – 1.4V, T_A = –40°C to 125°C		95		dB
		V_S = 5.5V, (V–) – 0.1V < V_{CM} < (V+) + 0.1V, T_A = –40°C to 125°C	63	77		dB
		V_S = 1.8V, (V–) – 0.1V < V_{CM} < (V+) + 0.1V, T_A = –40°C to 125°C		68		dB
INPUT BIAS CURRENT						
I_B	Input bias current	Vs = 5V		±5		pA
I_{OS}	Input offset current			±2		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	f = 0.1Hz to 10Hz, Vs = 5V		4.7		μV_{PP}
e_n	Input voltage noise density	f = 1kHz, Vs = 5V		30		$nV/\sqrt{Hz}$
		f = 10kHz, Vs = 5V		27		$nV/\sqrt{Hz}$
i_n	Input current noise density	f = 1kHz, Vs = 5V		23		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			1.5		pF
C_{IC}	Common-mode			5		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5V, (V–) + 0.05V < V_O < (V+) – 0.05V, R_L = 10kΩ	104	117		dB
		V_S = 1.8V, (V–) + 0.04V < V_O < (V+) – 0.04V, R_L = 10kΩ		100		dB
		V_S = 1.8V, (V–) + 0.1V < V_O < (V+) – 0.1V, R_L = 2kΩ		115		dB
		V_S = 5.5V, (V–) + 0.15V < V_O < (V+) – 0.15V, R_L = 2kΩ		130		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	Vs = 5V		1		MHz
φ_m	Phase margin	V_S = 5.5V, G = 1		78		degrees
SR	Slew rate	Vs = 5V		2		V/μs
t_S	Settling time	To 0.1%, V_S = 5V, 2V Step , G = +1, C_L = 100pF		2.5		μs
		To 0.01%, V_S = 5V, 2V Step , G = +1, C_L = 100pF		3		μs
t_{OR}	Overload recovery time	V_S = 5V, V_{IN} × gain > V_S		0.85		μs
THD+N	Total harmonic distortion + noise	V_S = 5.5V, V_{CM} = 2.5V, V_O = 1V_{RMS}, G = +1, f = 1kHz, 80kHz measurement BW		0.004		%
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5V, R_L = 10kΩ		10	20	mV
		V_S = 5.5V, R_L = 2kΩ		35	55	mV
I_{SC}	Short-circuit current	Vs = 5.5V		±40		mA
Z_O	Open-loop output impedance	Vs = 5V, f = 1MHz		1200		Ω

6.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 1.8V to 5.5V (±0.9V to ±2.75V), T_A = 25°C, R_L = 10kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	I_O = 0mA, V_S = 5.5V		60	80	µA
		I_O = 0mA, V_S = 5.5V, TLV9002RQDGKRQ1		60	85	µA
		I_O = 0mA, V_S = 5.5V, T_A = –40°C to 125°C			85	µA
	Power-on time	V_S = 0V to 5V, to 90% I_Q level		50		µs

6.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

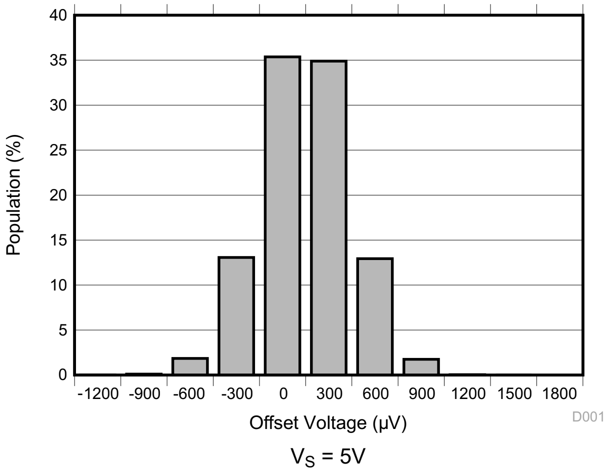


Figure 6-1. Offset Voltage Distribution Histogram

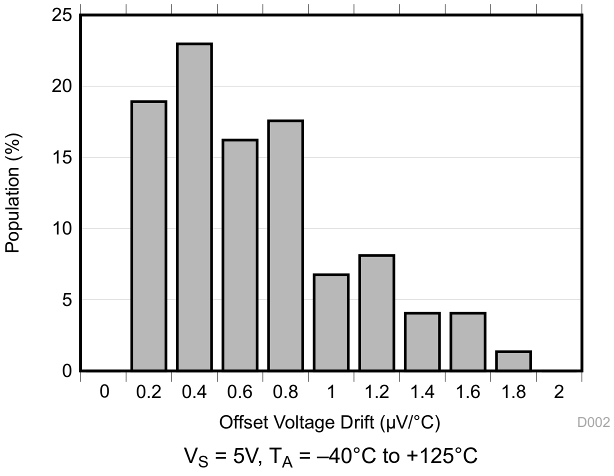


Figure 6-2. Offset Voltage Drift Distribution Histogram

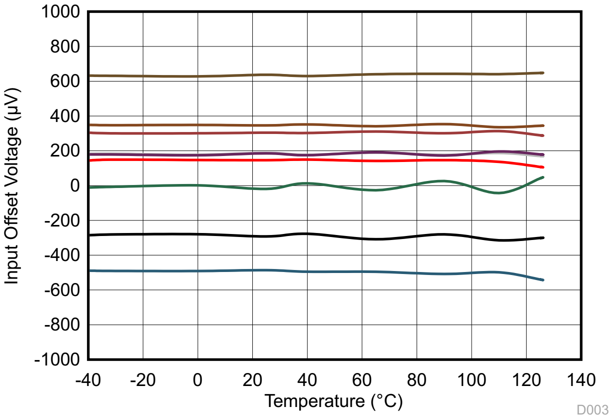


Figure 6-3. Input Offset Voltage vs Temperature

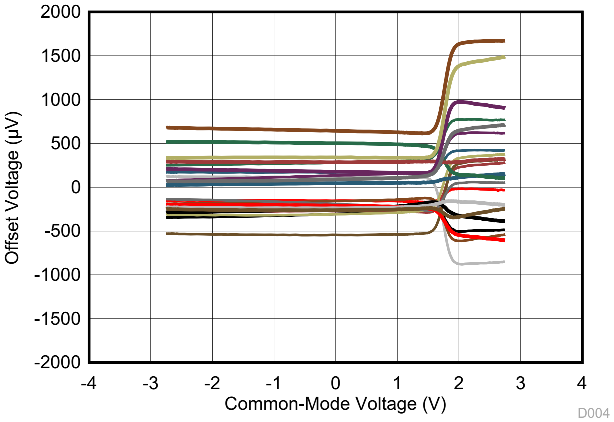


Figure 6-4. Offset Voltage vs Common-Mode

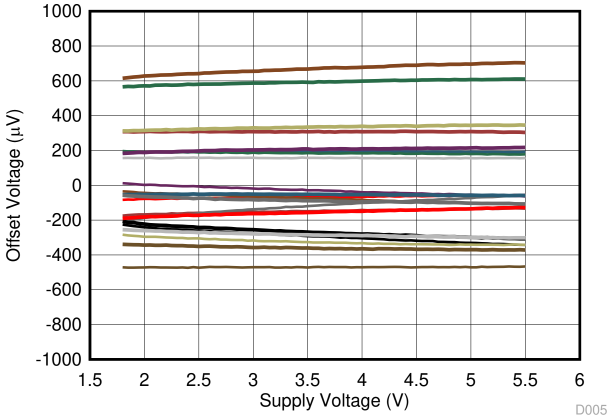


Figure 6-5. Offset Voltage vs Supply Voltage

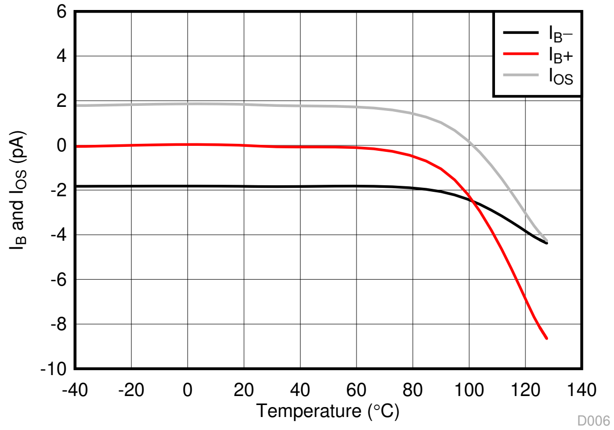


Figure 6-6. I_B and I_{OS} vs Temperature

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

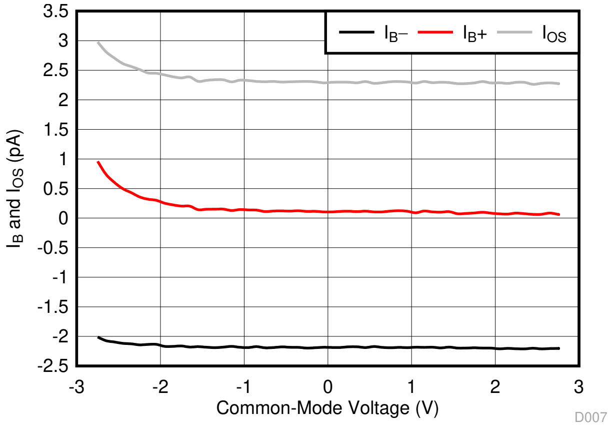


Figure 6-7. I_B and I_{OS} vs Common-Mode Voltage

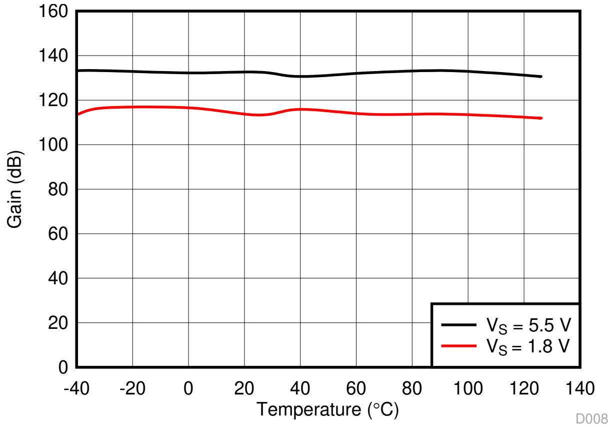
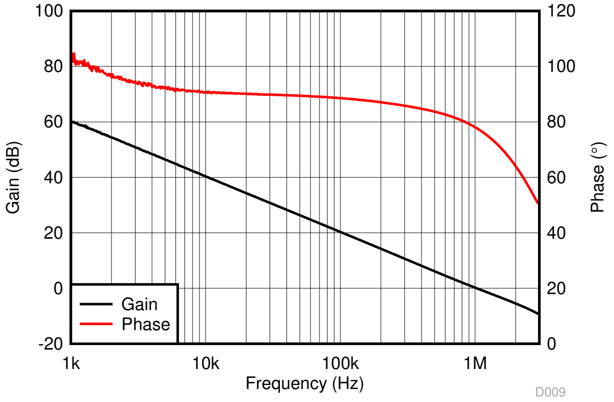


Figure 6-8. Open-Loop Gain vs Temperature



C_L = 10pF

Figure 6-9. Open-Loop Gain and Phase vs Frequency

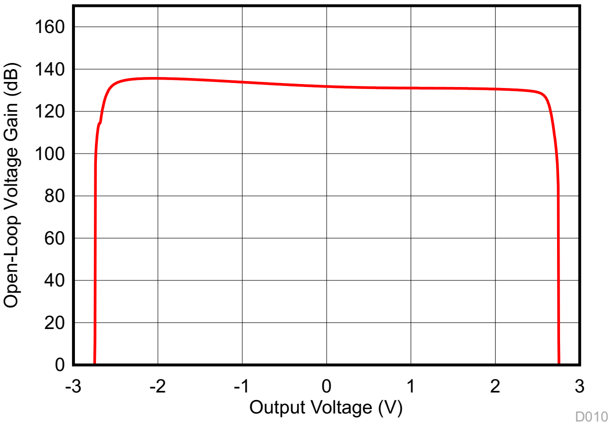
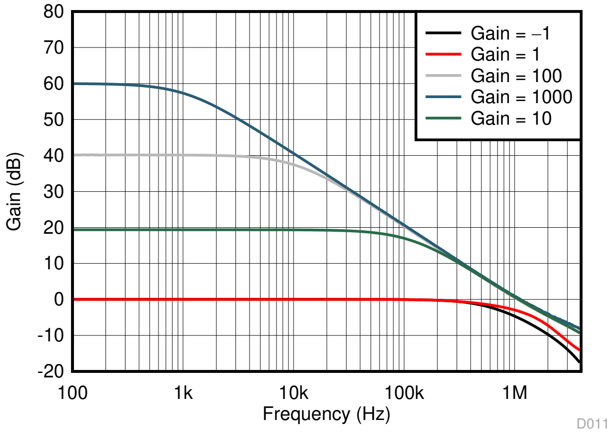


Figure 6-10. Open-Loop Gain vs Output Voltage



C_L = 10pF

Figure 6-11. Closed-Loop Gain vs Frequency

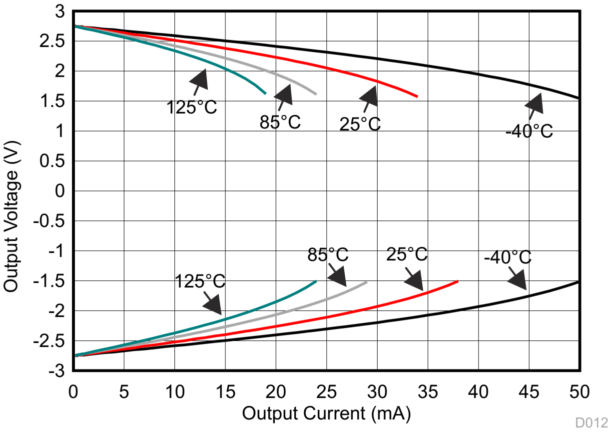


Figure 6-12. Output Voltage vs Output Current (Claw)

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

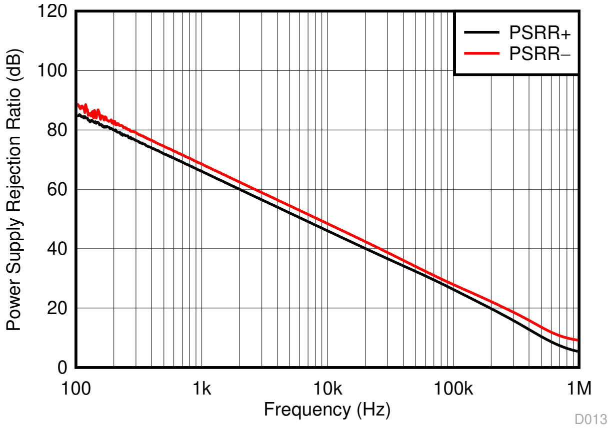
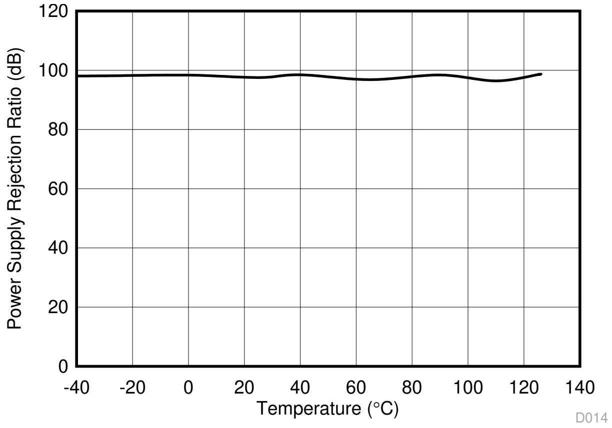


Figure 6-13. PSRR vs Frequency



V_S = 1.8V to 5.5V

Figure 6-14. DC PSRR vs Temperature

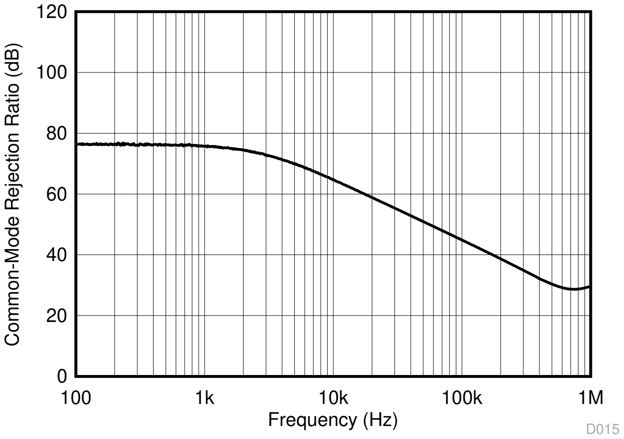
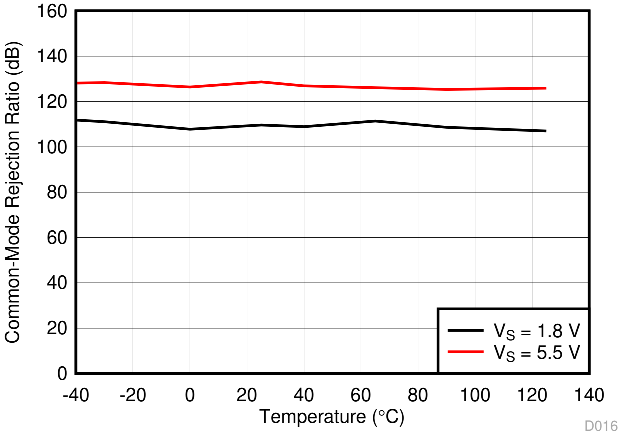


Figure 6-15. CMRR vs Frequency



V_{CM} = (V–) – 0.1V to (V+) – 1.4V

Figure 6-16. DC CMRR vs Temperature

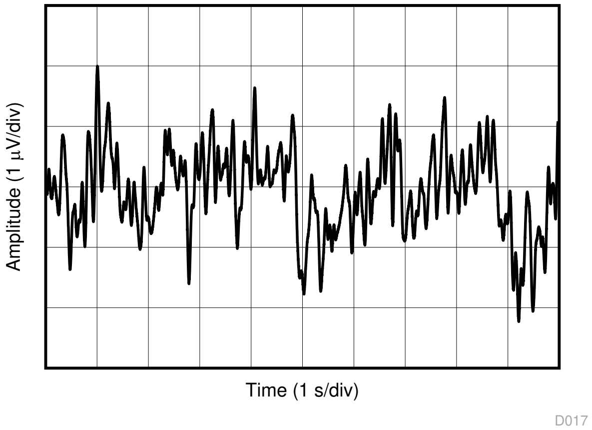


Figure 6-17. 0.1Hz to 10Hz Integrated Voltage Noise

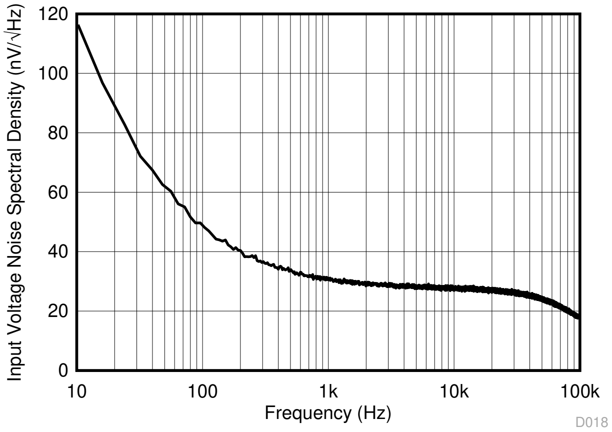
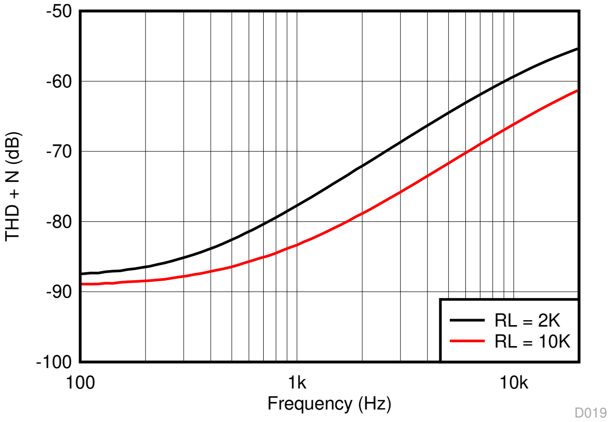


Figure 6-18. Input Voltage Noise Spectral Density

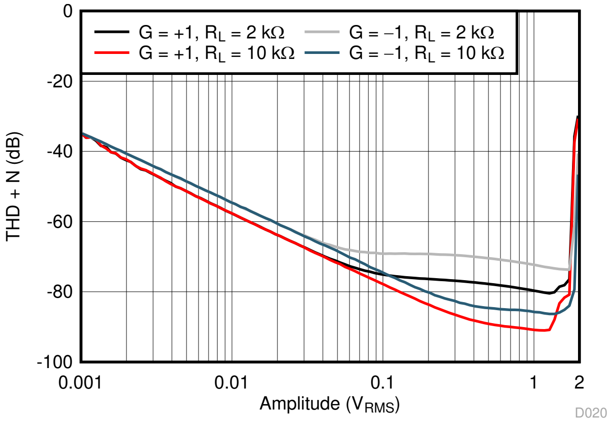
6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5V V_{CM} = 2.5V G = 1
BW = 80kHz V_{OUT} = 0.5V_{RMS}

Figure 6-19. THD + N vs Frequency



V_S = 5.5V V_{CM} = 2.5V f = 1kHz
G = 1 BW = 80kHz

Figure 6-20. THD + N vs Amplitude

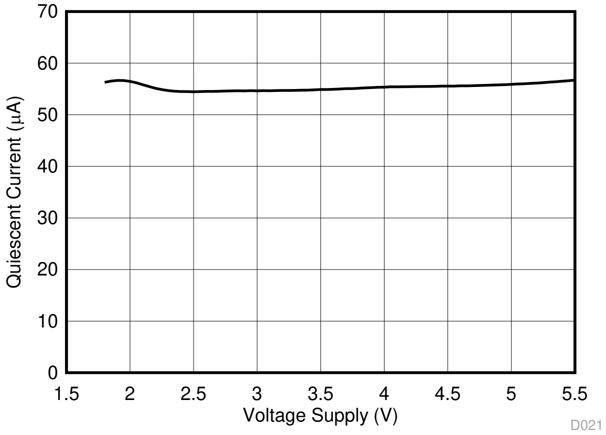


Figure 6-21. Quiescent Current vs Supply Voltage

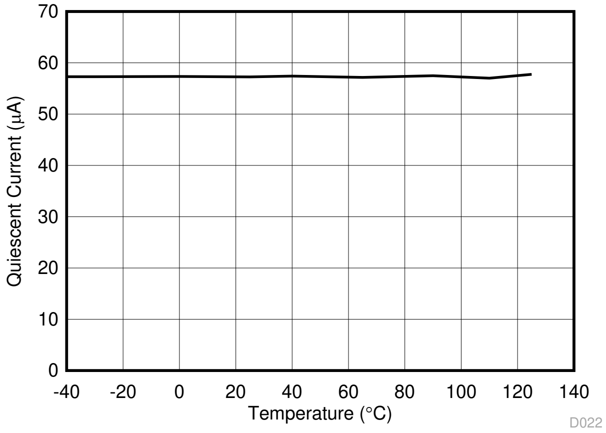


Figure 6-22. Quiescent Current vs Temperature

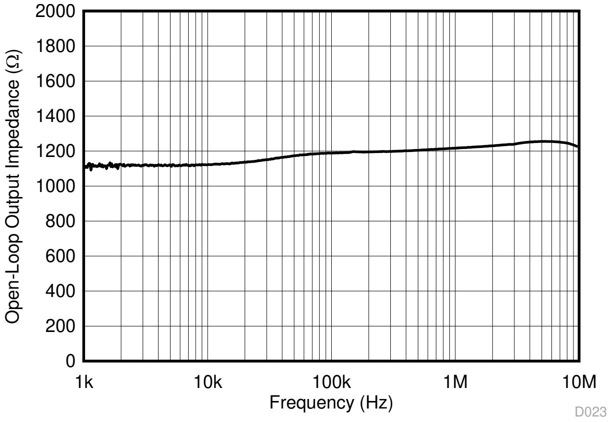
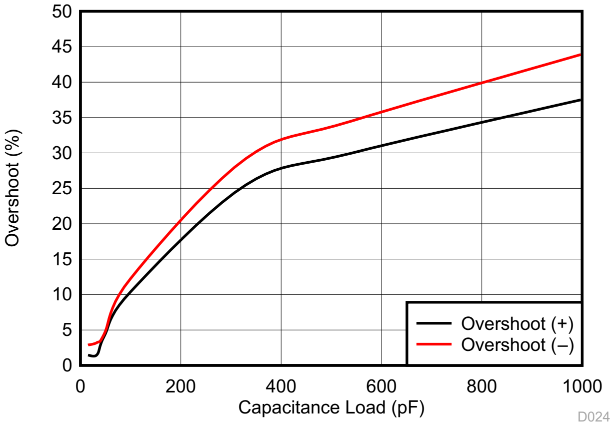


Figure 6-23. Open-Loop Output Impedance vs Frequency

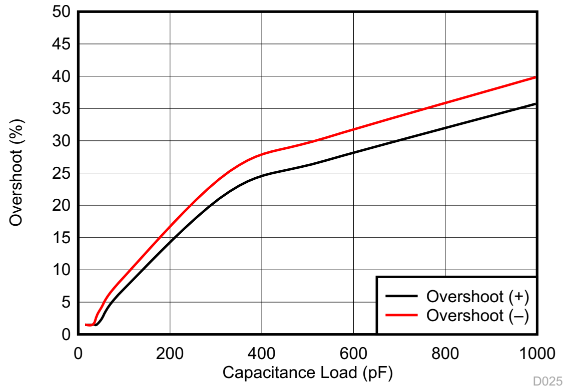


G = 1 V_{IN} = 100mVpp

Figure 6-24. Small Signal Overshoot vs Capacitive Load

6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = –1 V_{IN} = 100mVpp

Figure 6-25. Small Signal Overshoot vs Capacitive Load

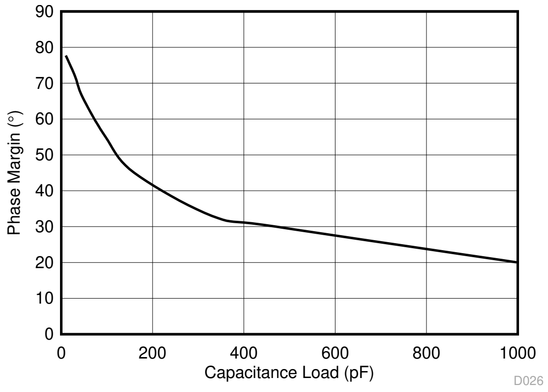
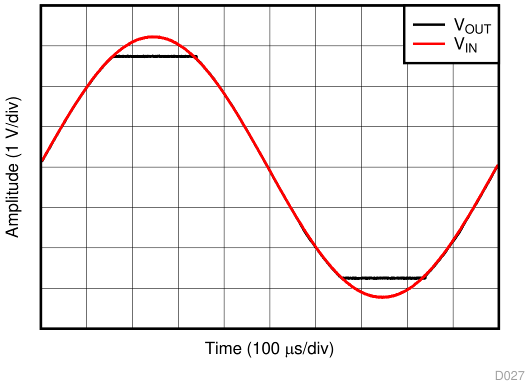
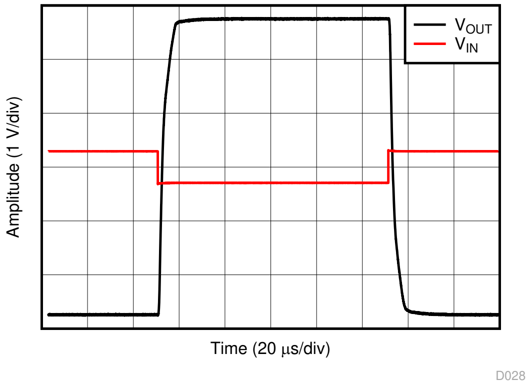


Figure 6-26. Phase Margin vs Capacitive Load



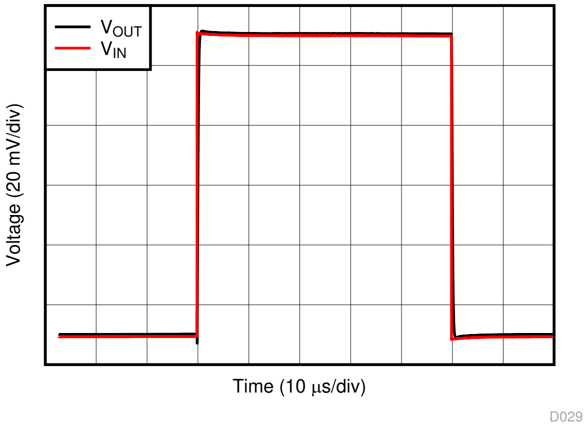
G = 1 V_{IN} = $6.5V_{PP}$

Figure 6-27. No Phase Reversal



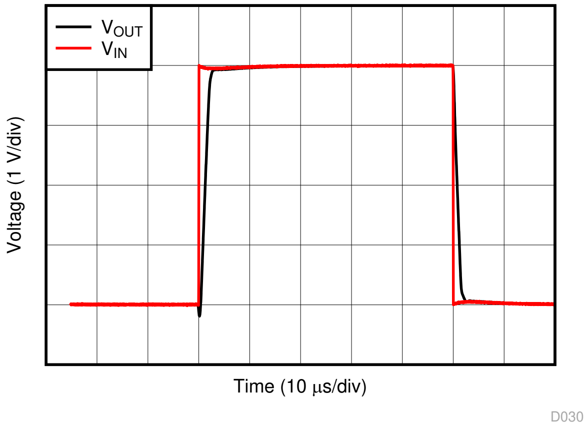
G = –10 V_{IN} = $600mV_{PP}$

Figure 6-28. Overload Recovery



G = 1 V_{IN} = $100mV_{PP}$ C_L = 10pF

Figure 6-29. Small-Signal Step Response

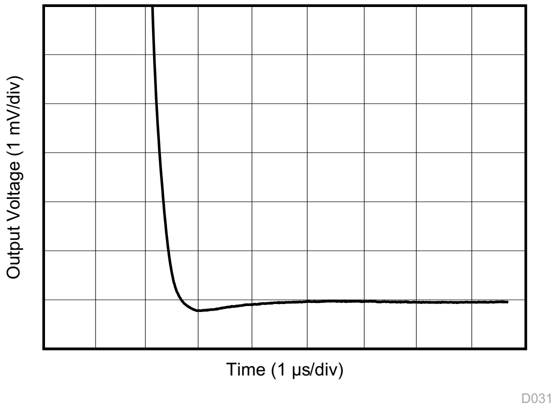


G = 1 V_{IN} = $4V_{PP}$ C_L = 10pF

Figure 6-30. Large-Signal Step Response

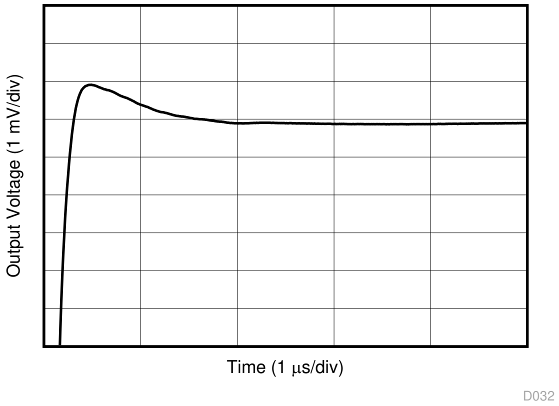
6.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75V, V– = –2.75V, R_L = 10kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 1 C_L = 100pF 2V step

Figure 6-31. Large-Signal Settling Time (Negative)



G = 1 C_L = 100pF 2V step

Figure 6-32. Large-Signal Settling Time (Positive)

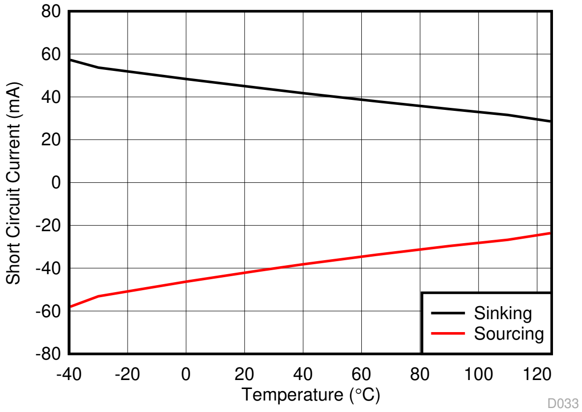


Figure 6-33. Short-Circuit Current vs Temperature

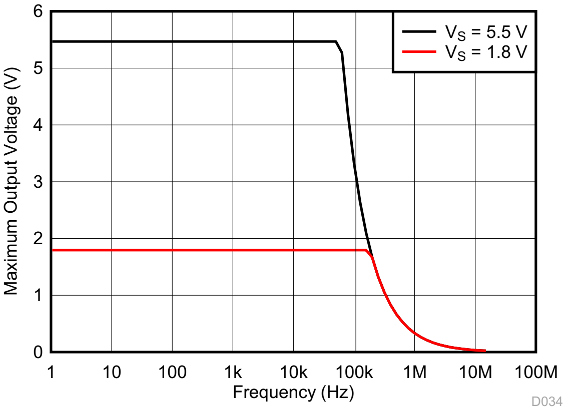


Figure 6-34. Maximum Output Voltage vs Frequency

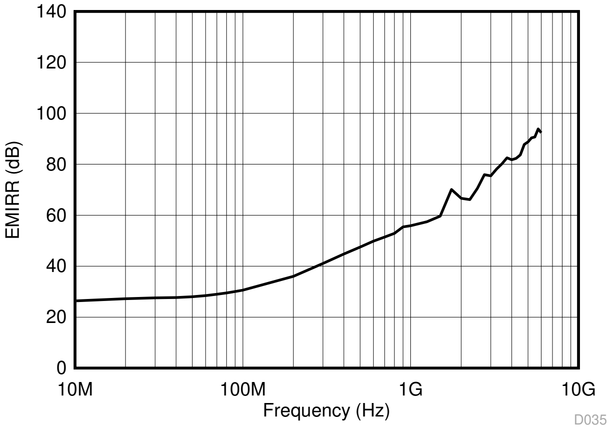


Figure 6-35. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

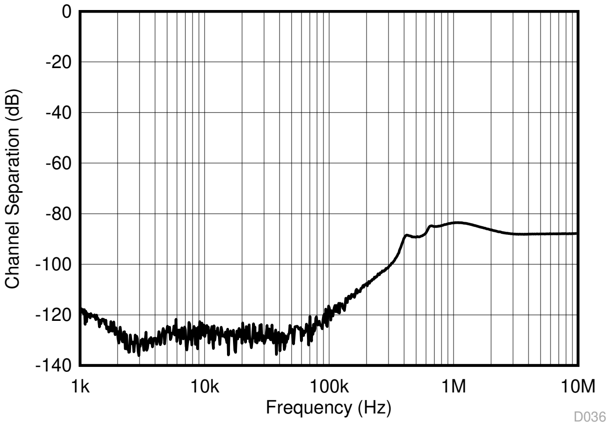


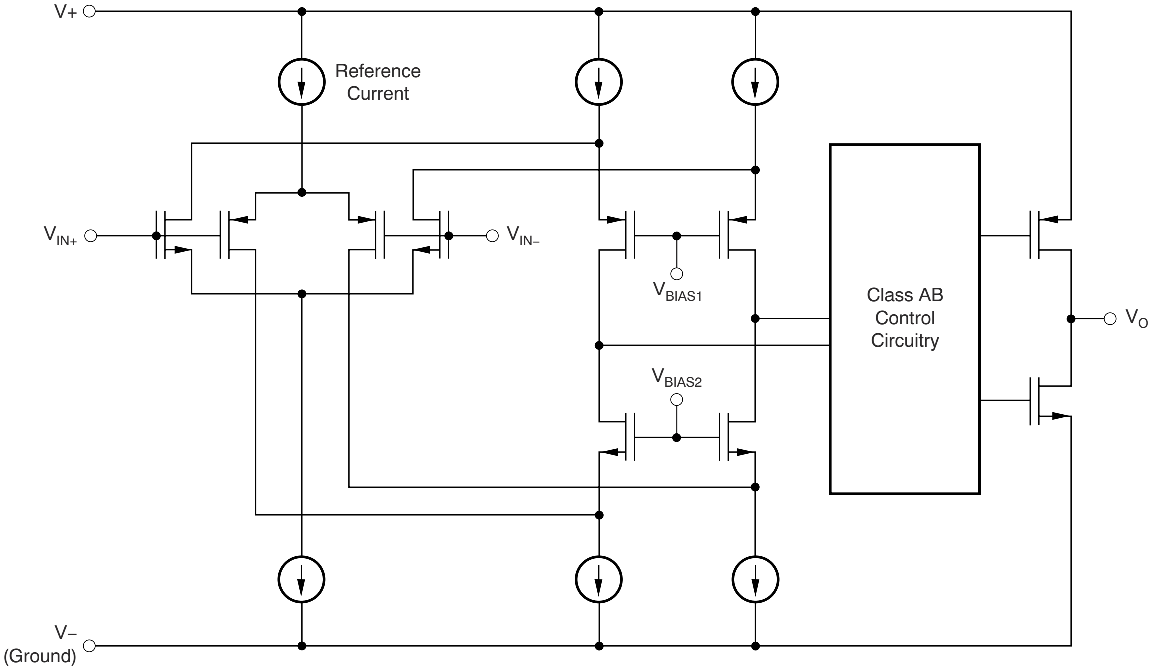
Figure 6-36. Channel Separation

7 Detailed Description

7.1 Overview

The TLV900x-Q1 is a family of automotive qualified, low-power, rail-to-rail input and output op amps. These devices operate from 1.8V to 5.5V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV900x-Q1 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them an excellent choice for driving sampling analog-to-digital converters (ADCs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The TLV900x-Q1 family of op amps are for operation from 1.8V to 5.5V. In addition, many specifications such as input offset voltage, quiescent current, offset current, and short circuit current apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the typical characteristics section.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV900x-Q1 family extends 100mV beyond the supply rails for the full supply voltage range of 1.8V to 5.5V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4V to 100mV above the positive supply, whereas the P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+) – 1.4V. There is a small transition region, typically (V+) – 1.2V to (V+) – 1V, in which both pairs are on. This 100mV transition region can vary up to 100mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4V to (V+) – 1.2V on the low end, and up to (V+) – 1V to (V+) – 0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

7.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV900x-Q1 family delivers a robust output drive capability. A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10kΩ, the output swings to within 20mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

7.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV900x-Q1 family is approximately 850ns.

7.4 Device Functional Modes

The TLV900x-Q1 family has a single functional mode. The devices are powered on as long as the power-supply voltage is between 1.8V (±0.9V) and 5.5V (±2.75V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLV900x-Q1 family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable applications. The devices operate from 1.8V to 5.5V, are unity-gain stable, and are an excellent choice for a wide range of general-purpose applications. The class AB output stage is capable of driving less than or equal to 10-kΩ loads connected to any point between V+ and V–. The input common-mode voltage range includes both rails, and allows the TLV900x-Q1 devices to be used in any single-supply application.

8.2 Typical Application

8.2.1 TLV900x-Q1 Low-Side, Current Sensing Application

Figure 8-1 shows the TLV900x-Q1 configured in a low-side current sensing application.

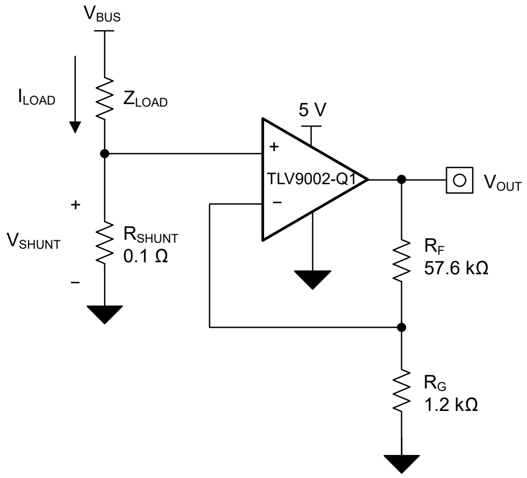


Figure 8-1. TLV900x-Q1 in a Low-Side, Current-Sensing Application

8.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.9V
- Maximum shunt voltage: 100mV

8.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 8-1 is given in Equation 1:

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is shown using Equation 2:

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV900x-Q1 to produce an output voltage of approximately 0Vto 4.9V. The gain needed by the TLV900x-Q1 to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using Equation 3, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 4 sizes the resistors R_F and R_G, to set the gain of the TLV900x-Q1 to 49V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Selecting R_F as 57.6kΩ and R_G as 1.2kΩ provides a combination that equals 49V/V. Figure 8-2 shows the measured transfer function of the circuit shown in Figure 8-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no specific impedance selection that works for every system, choose an impedance based on the system parameters.

8.2.1.3 Application Curve

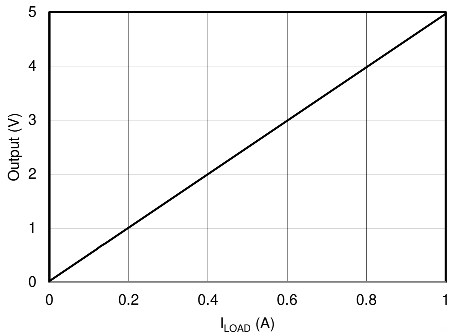


Figure 8-2. Low-Side, Current-Sense Transfer Function

8.2.2 Single-Supply Photodiode Amplifier

Photodiodes are used in many applications to convert light signals to electrical signals. The current through the photodiode is proportional to the photon energy absorbed, and is commonly in the range of a few hundred picoamps to a few tens of microamps. An amplifier in a transimpedance configuration is typically used to convert the low-level photodiode current to a voltage signal for processing in an MCU. The circuit shown in Figure 8-3 is an example of a single-supply photodiode amplifier circuit using the TLV9002-Q1.

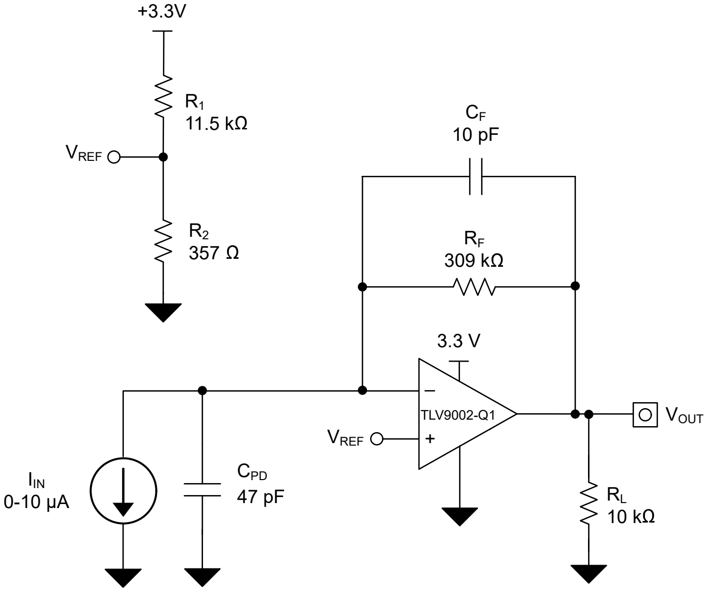


Figure 8-3. Single-Supply Photodiode Amplifier Circuit

8.2.2.1 Design Requirements

The design requirements for this design are:

- Supply voltage: 3.3V
- Input: 0μA to 10μA
- Output: 0.1V to 3.2V
- Bandwidth: 50kHz

8.2.2.2 Detailed Design Procedure

The transfer function between the output voltage (V_{OUT}), the input current, (I_{IN}) and the reference voltage (V_{REF}) is defined in Equation 5.

$$V_{OUT} = I_{IN} \times R_F + V_{REF} \tag{5}$$

Where:

$$V_{REF} = V_+ \times \left(\frac{R_1 \times R_2}{R_1 + R_2}\right) \tag{6}$$

Set V_{REF} to 100mV to meet the minimum output voltage level by setting R1 and R2 to meet the required ratio calculated in Equation 7.

$$\frac{V_{REF}}{V_+} = \frac{0.1\,V}{3.3\,V} = 0.0303 \tag{7}$$

The closest resistor ratio to meet this ratio sets R1 to 11.5kΩ and R2 to 357Ω.

The required feedback resistance can be calculated based on the input current and desired output voltage.

$$R_F = \frac{V_{OUT} - V_{REF}}{I_{IN}} = \frac{3.2\,V - 0.1\,V}{10\,\mu A} = 310\,\frac{kV}{A} \approx 309\,k\Omega \tag{8}$$

Calculate the value for the feedback capacitor based on R_F and the desired –3dB bandwidth, (f_{-3dB}) using Equation 9.

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_{-3\,dB}} = \frac{1}{2 \times \pi \times 309\,k\Omega \times 50\,kHz} = 10.3\,pF \approx 10\,pF \tag{9}$$

The minimum op amp bandwidth required for this application is based on the value of R_F, C_F, and the capacitance on the INx– pin of the TLV9002-Q1 which is equal to the sum of the photodiode shunt capacitance, (CPD) the common-mode input capacitance, (CCM) and the differential input capacitance (CD) as Equation 10 shows.

$$C_{IN} = C_{PD} + C_{CM} + C_D = 47\,pF + 5\,pF + 1\,pF = 53\,pF \tag{10}$$

The minimum op amp bandwidth is calculated in Equation 11.

$$f = BGW \geq \frac{C_{IN} + C_F}{2 \times \pi \times R_F \times C_F{}^2} \geq 324\,kHz \tag{11}$$

The 1MHz bandwidth of the TLV900x-Q1 meets the minimum bandwidth requirement and remains stable in this application configuration.

8.2.2.3 Application Curves

The measured current-to-voltage transfer function for the photodiode amplifier circuit is shown in Figure 8-4. The measured performance of the photodiode amplifier circuit is shown in Figure 8-5.

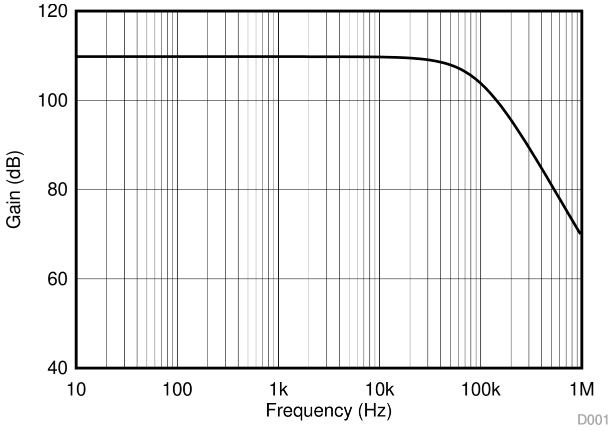


Figure 8-4. Photodiode Amplifier Circuit AC Gain Results

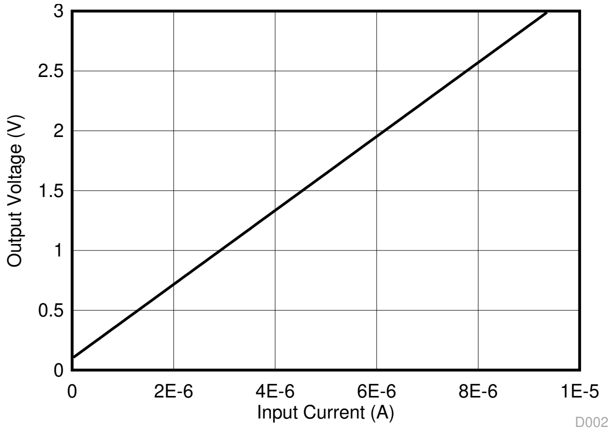


Figure 8-5. Photodiode Amplifier Circuit DC Results

8.3 Power Supply Recommendations

The TLV900x-Q1 family is specified for operation from 1.8V to 5.5V (±0.9V to ±2.75V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

8.3.1 Input and ESD Protection

The TLV900x-Q1 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10mA. Figure 8-6 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

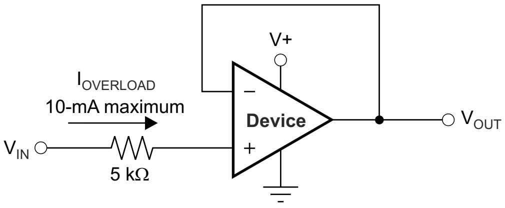


Figure 8-6. Input Current Protection

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in Figure 8-8. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example

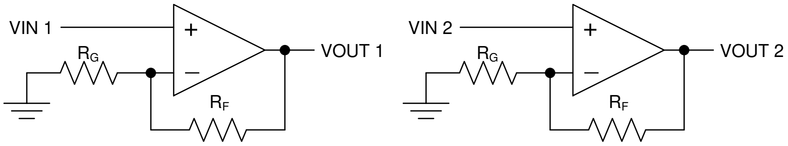
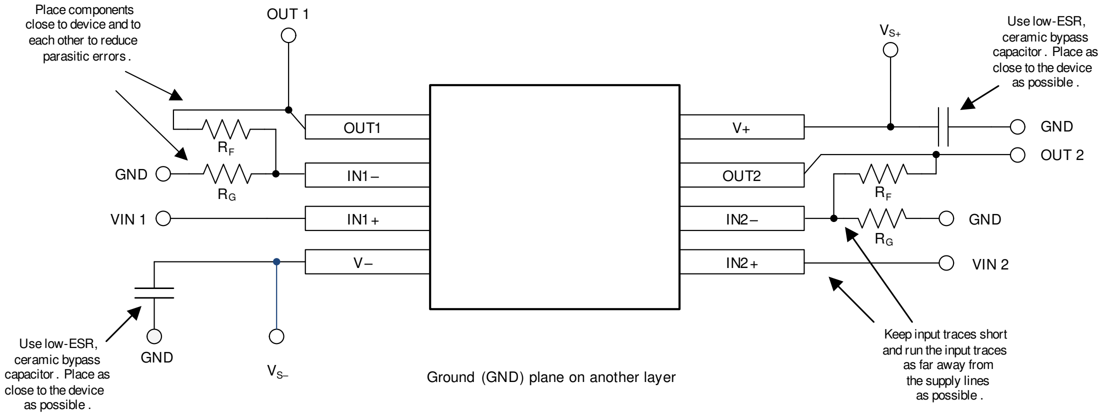


Figure 8-7. Schematic Representation for Figure 11-2



Place components close to device and to each other to reduce parasitic errors.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Keep input traces short and run the input traces as far away from the supply lines as possible.

Ground (GND) plane on another layer

Figure 8-8. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2023) to Revision F (April 2025)	**Page**
• Changed the status of the PW (TSSOP, 8) package from: *preview* to: *active*	1
• Added TLV9002RQDGKRQ1 to the data sheet with 85µA Iq maximum	9

Changes from Revision D (November 2022) to Revision E (April 2023)	**Page**
• Changed the status of the DBV package from: *preview* to: *active*	1

Changes from Revision C (October 2021) to Revision D (December 2022)	**Page**
• Deleted preview tag for SC70 (5) from *Device information* section	1
• Changed formatting of *Pin Configuration and Functions* section	4
• Added Thermal Information for Single Channel DCK package	7

Changes from Revision B (March 2021) to Revision C (October 2021) **Page**

- Deleted preview tag for SOT-23 (14) and TSSOP (14) from *Device information* section....................................1
- Added preview tags for TLV9001-Q1 SOT-23 (5) and SC70 (5) packages to *Device information* section.........1
- Added TLV9001-Q1 GPN to the data sheet.. 1
- Added TLV9001-Q1 to *Device Comparison Table* section 3
- Added TLV9001-Q1 DBV (SOT-23) and DCK (SC70) in *Pin Configuration and Functions* section 4

Changes from Revision A (June 2020) to Revision B (March 2021) **Page**

- Changed the numbering format for tables, figures and cross-references throughout the document................. 1
- Added Functional Safety-Capable document link in the *Features* section... 1
- Deleted preview tag for VSSOP (8) from *Device information* section.. 1
- Added note 4 to differential input voltage in *Absolute Maximum Ratings* table 7
- Added Thermal Information for DGK package.. 8
- Added Thermal Information for DYY package...8

Changes from Revision * (May 2019) to Revision A (June 2020) **Page**

- Changed the device status from *Advance Information* to *Production Data* 1
- Added end equipment links in *Application* section 1
- Deleted preview tag for SOIC (8) from *Device information* section..1
- Added SOT-23 (14) in *Device Information* section 1
- Deleted preview tag for SOIC (14) from *Device information* section..1
- Added SOT-23 (DYY) package in *Device Comparison Table* section 3
- Added DYY (SOT-23) in *Pin Functions: TLV9004-Q1* section 4

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9001QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2T5H
TLV9001QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2T5H
TLV9001QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MZ
TLV9001QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MZ
TLV9002QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27DT
TLV9002QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27DT
TLV9002QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9002Q
TLV9002QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9002Q
TLV9002QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9002Q
TLV9002QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9002Q
TLV9002RQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3N8S
TLV9002RQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3N8S
TLV9004QDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV9004Q
TLV9004QDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV9004Q
TLV9004QDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9004Q
TLV9004QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9004Q
TLV9004QDYYRQ1.B	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9004Q
TLV9004QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9004Q
TLV9004QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9004Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9001-Q1, TLV9002-Q1, TLV9004-Q1 :

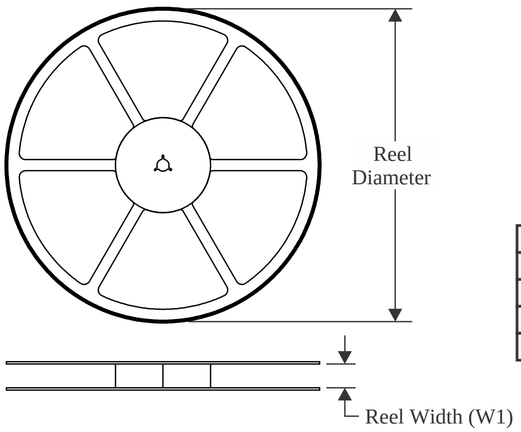
- Catalog : TLV9001, TLV9002, TLV9004

NOTE: Qualified Version Definitions:

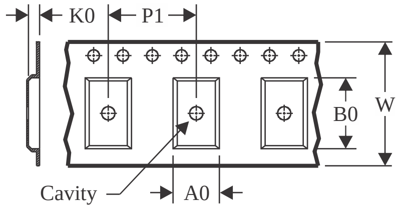
  - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

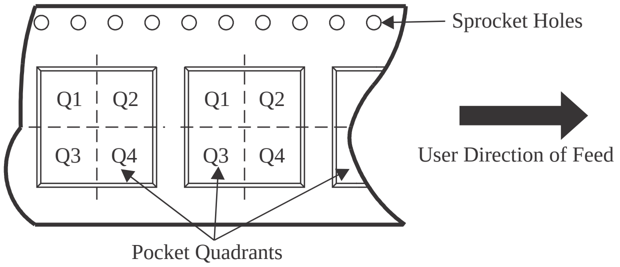


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

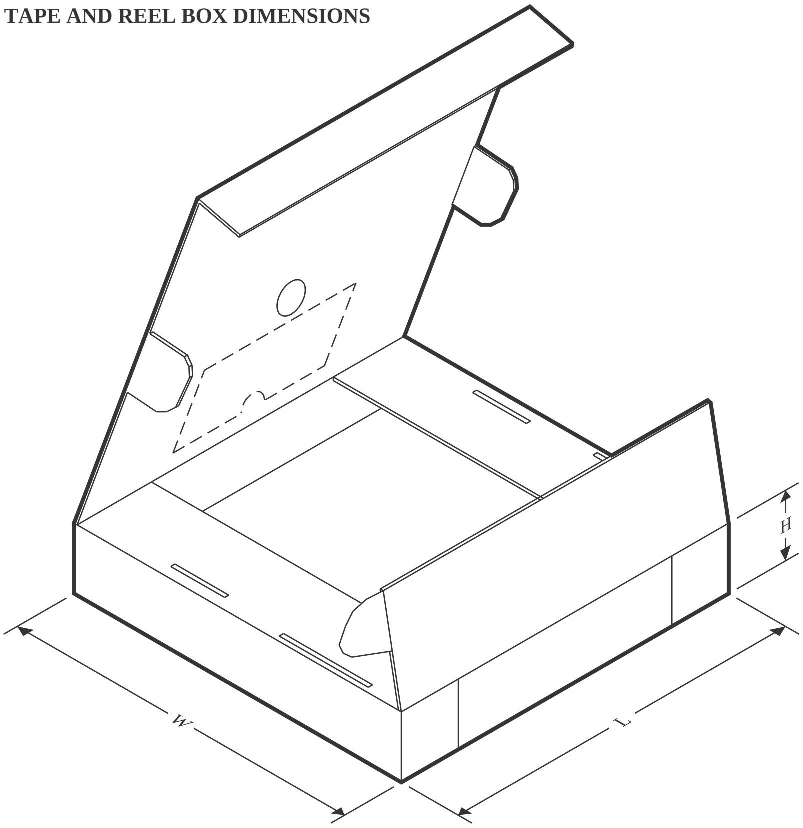
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

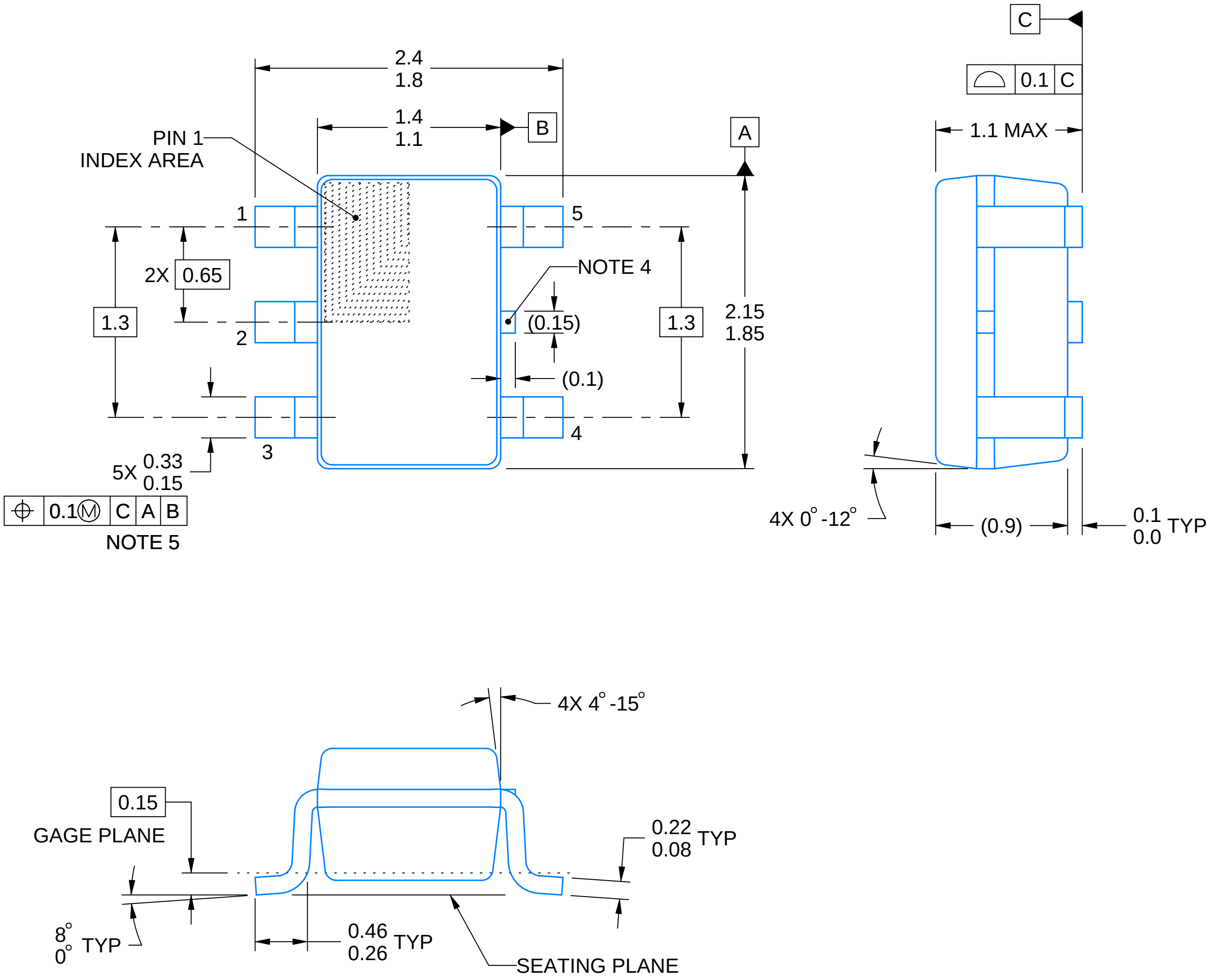
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9001QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9001QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9002QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV9002QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9002QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9002RQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV9004QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9004QDYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV9004QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

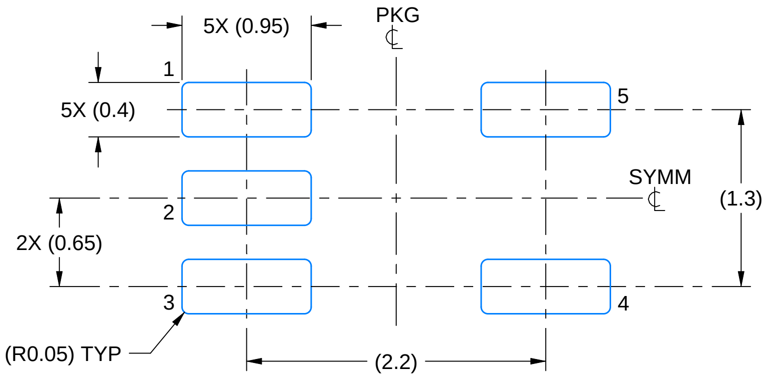
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9001QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9001QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9002QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9002QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TLV9002QPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV9002RQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9004QDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
TLV9004QDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV9004QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0



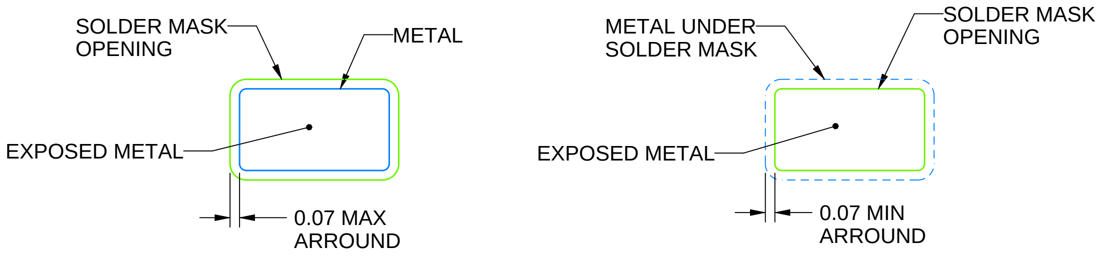
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



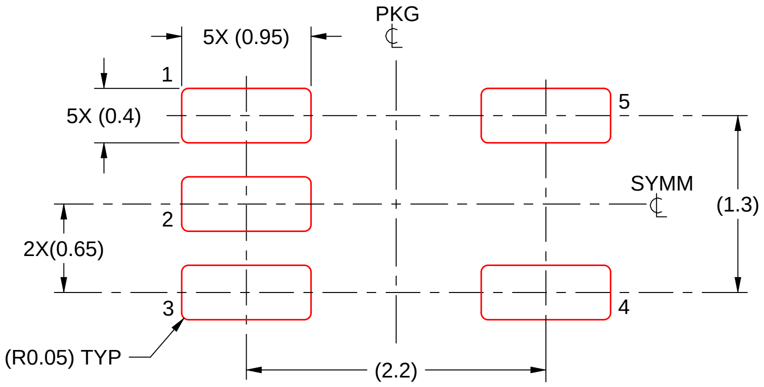
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

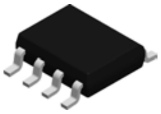


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

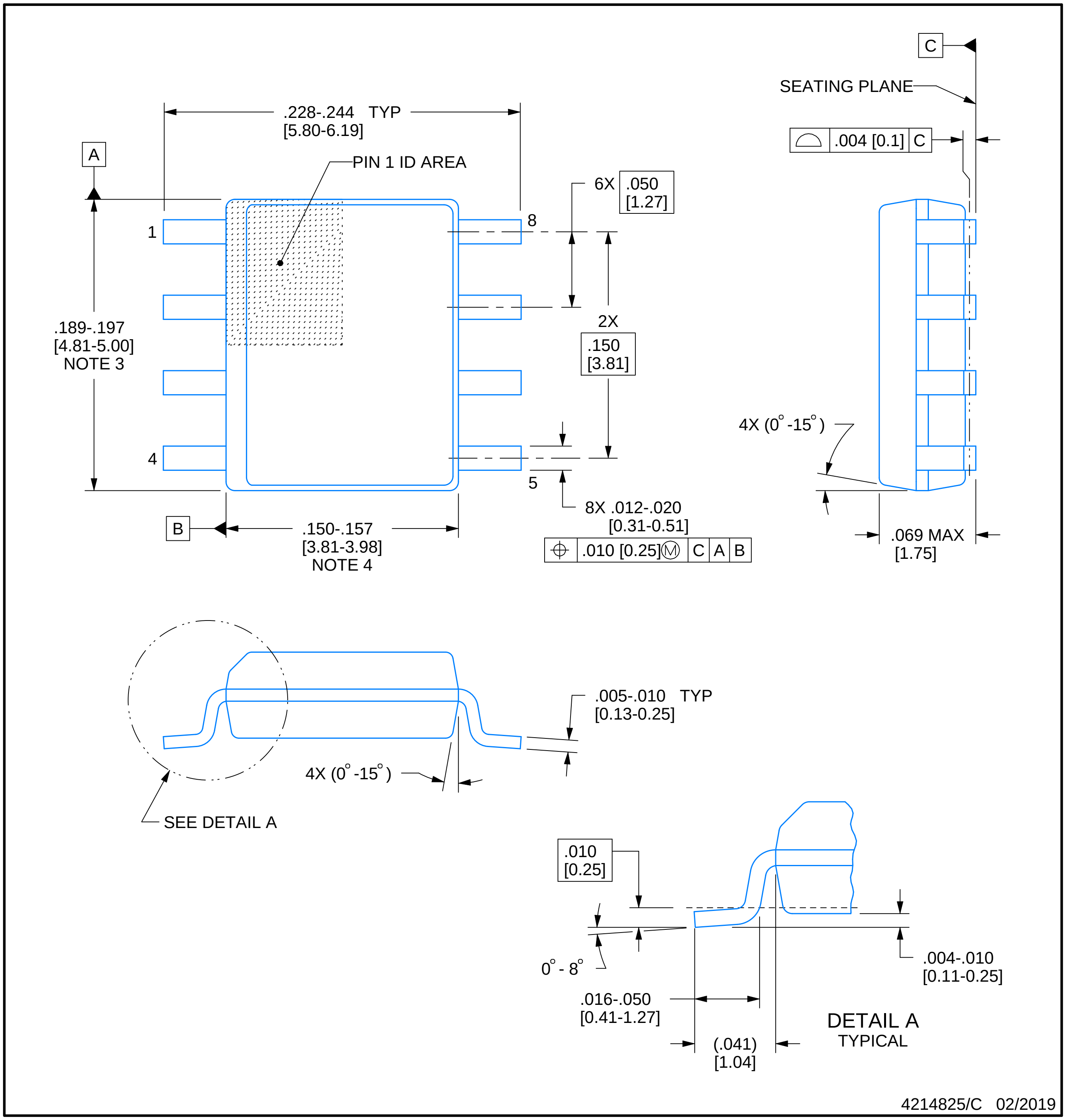
PACKAGE OUTLINE



D0008A

SOIC - 1.75 mm max height

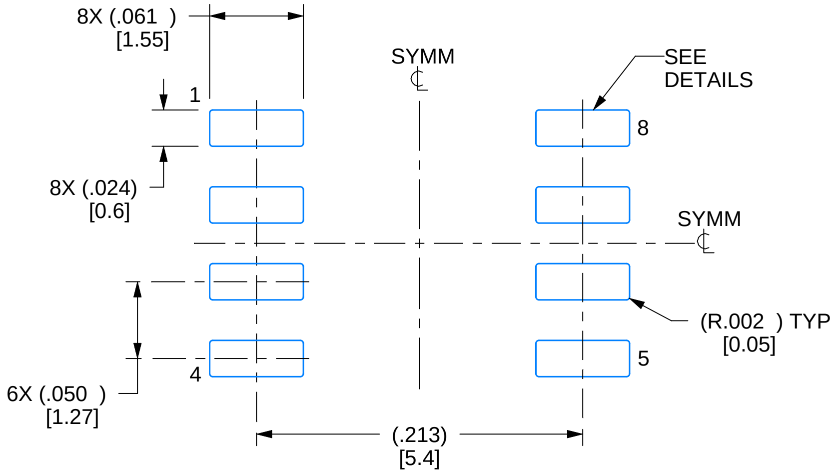
SMALL OUTLINE INTEGRATED CIRCUIT



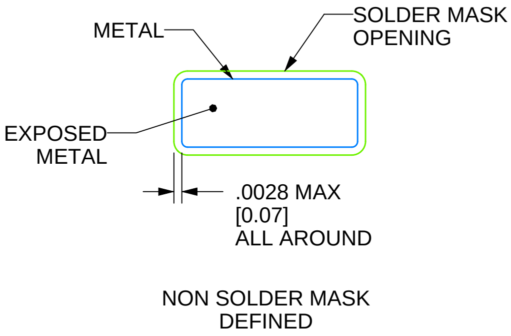
4214825/C 02/2019

NOTES:

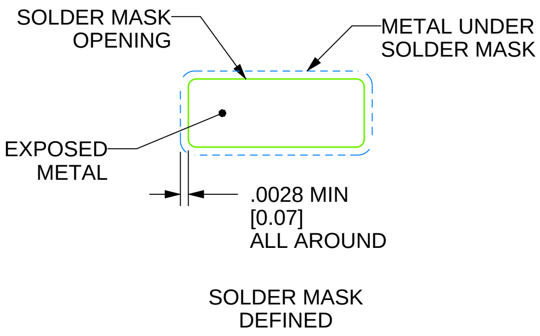
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

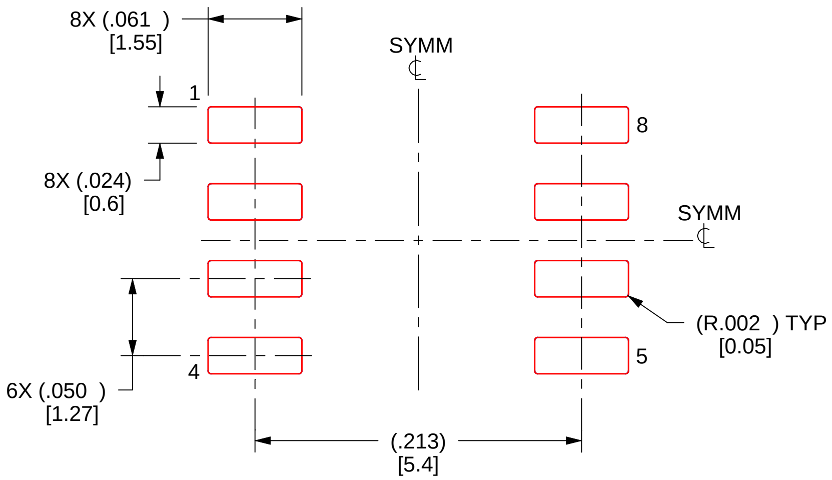


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

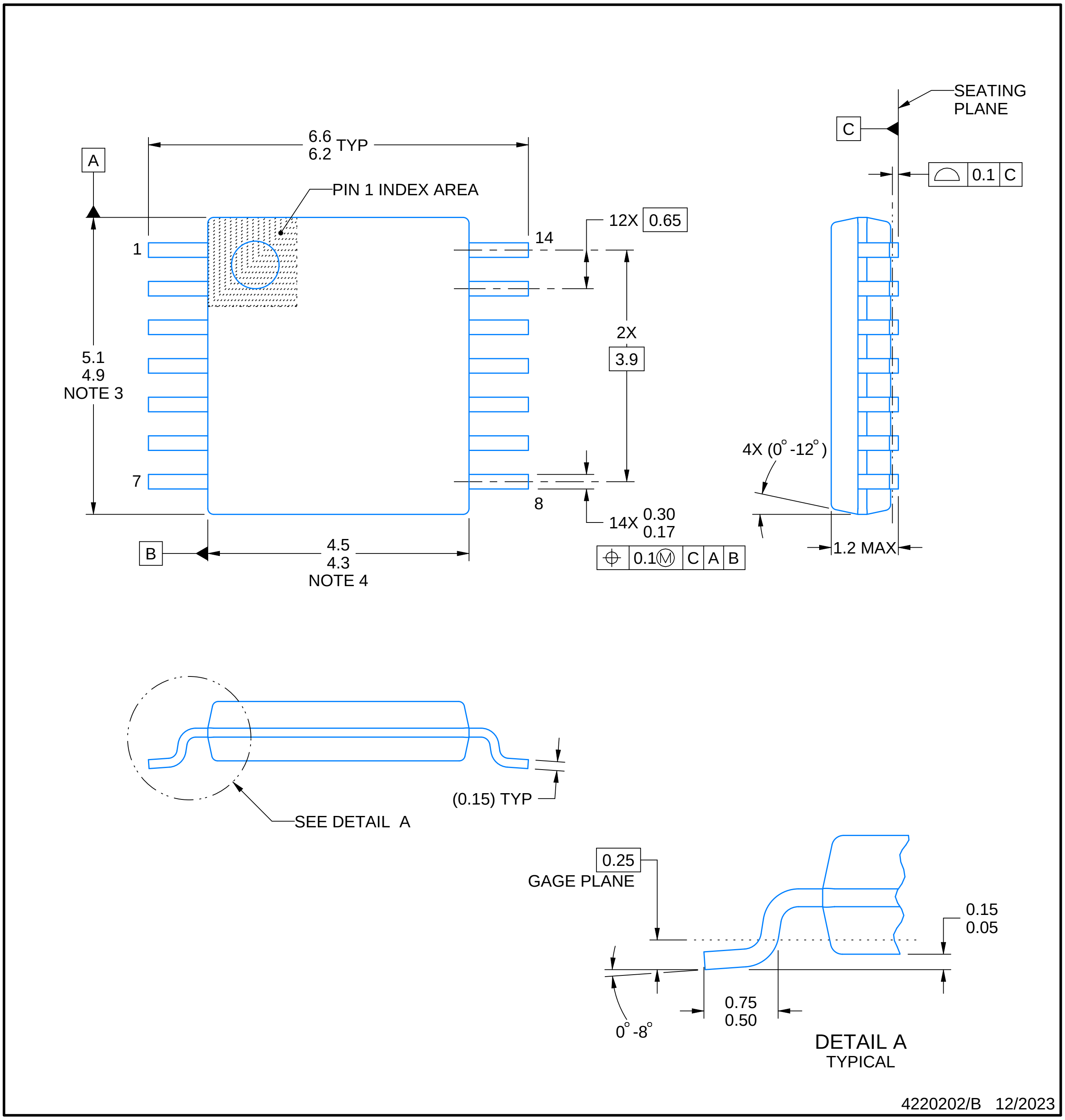
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

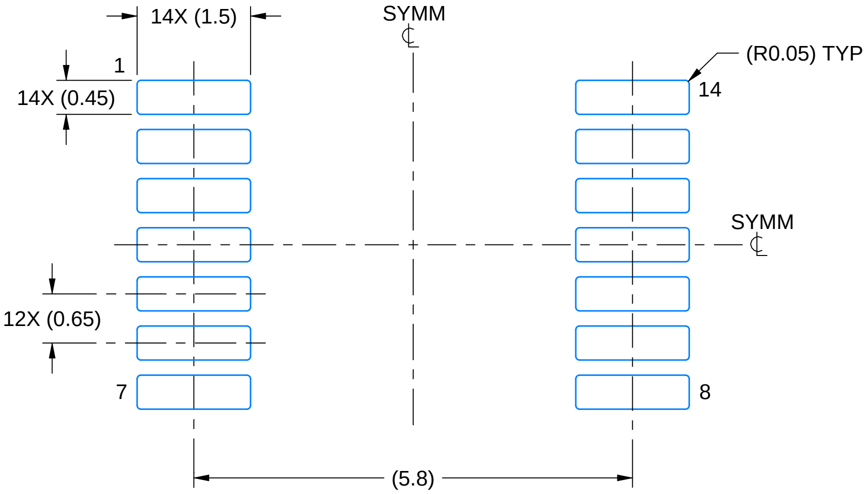
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

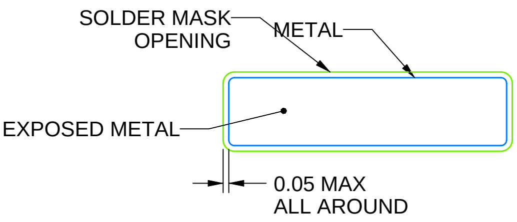


NOTES:

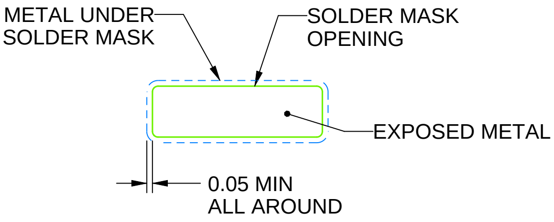
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)



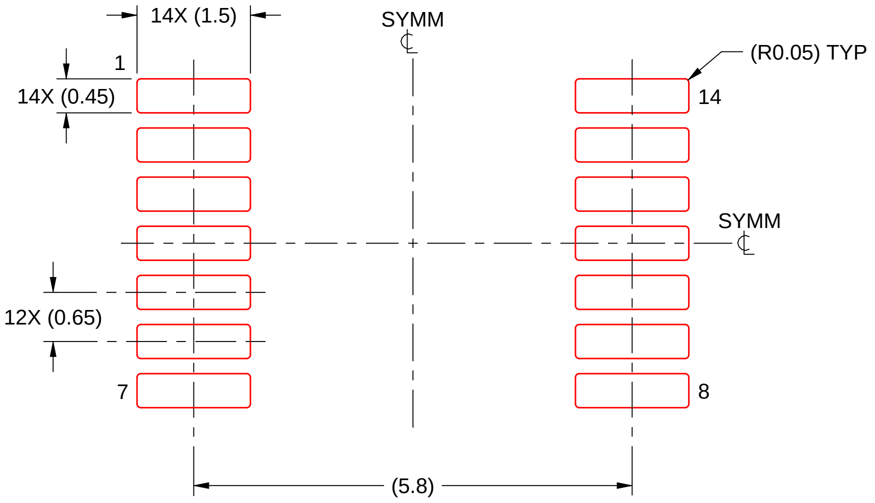
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

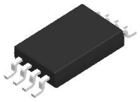


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

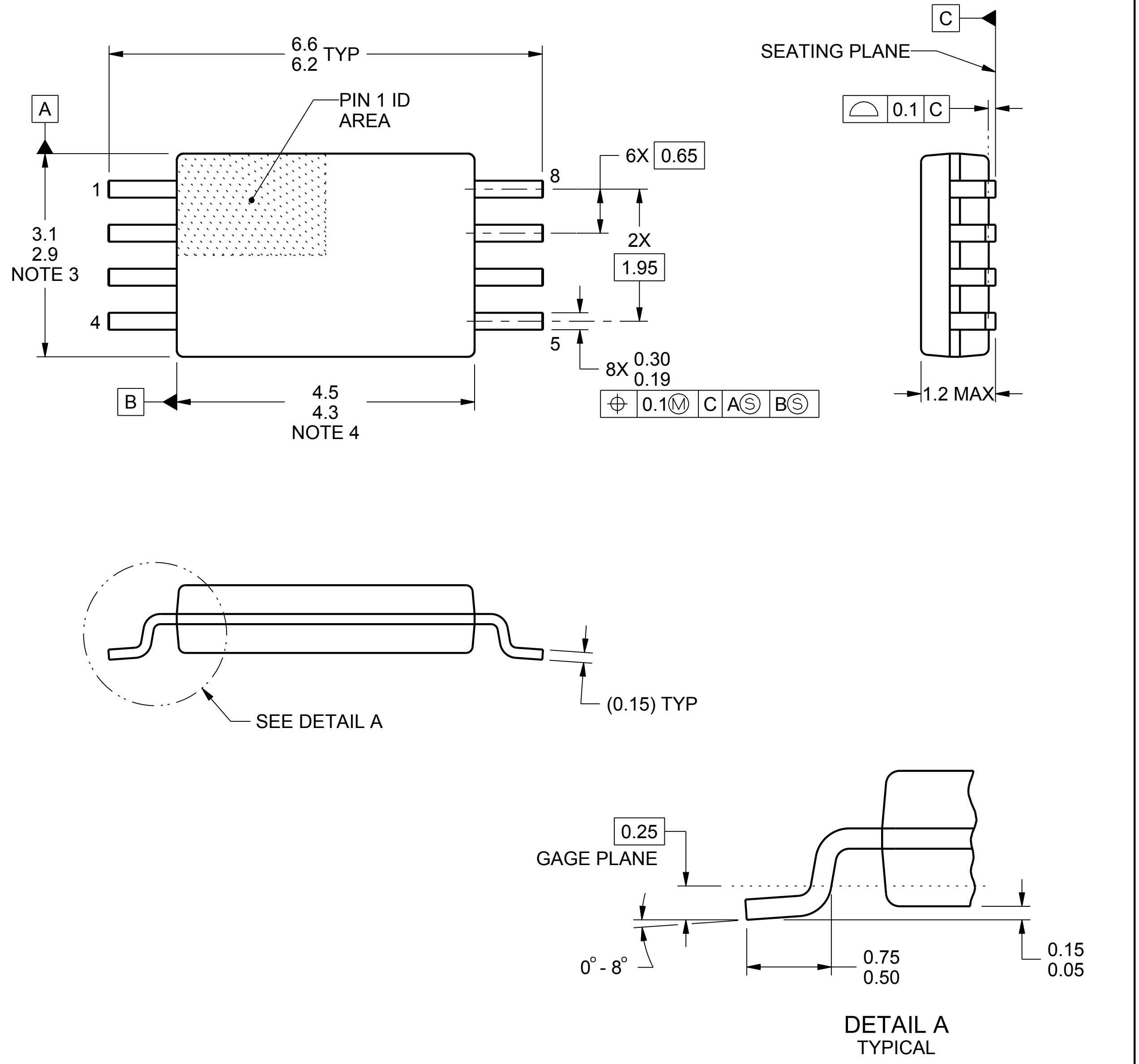
PACKAGE OUTLINE



PW0008A

TSSOP - 1.2 mm max height

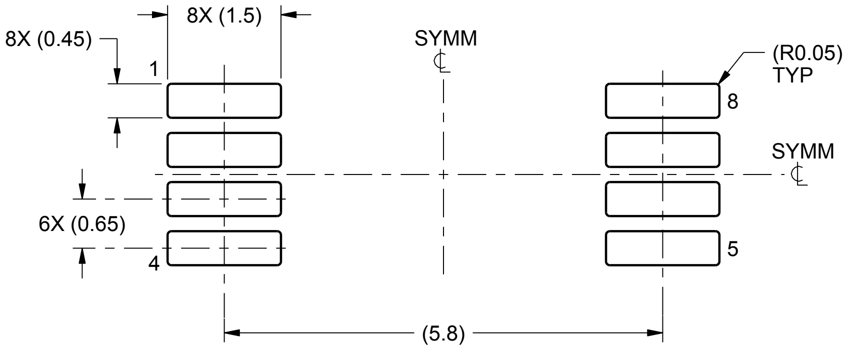
SMALL OUTLINE PACKAGE



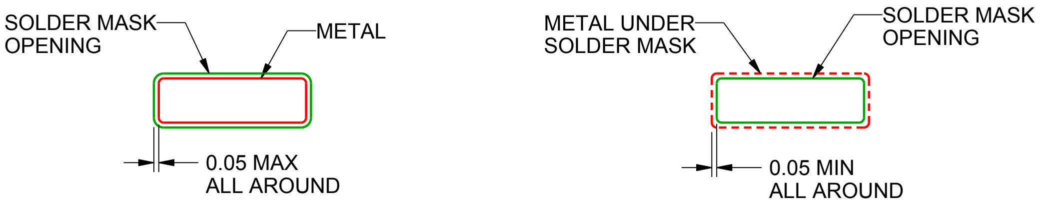
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



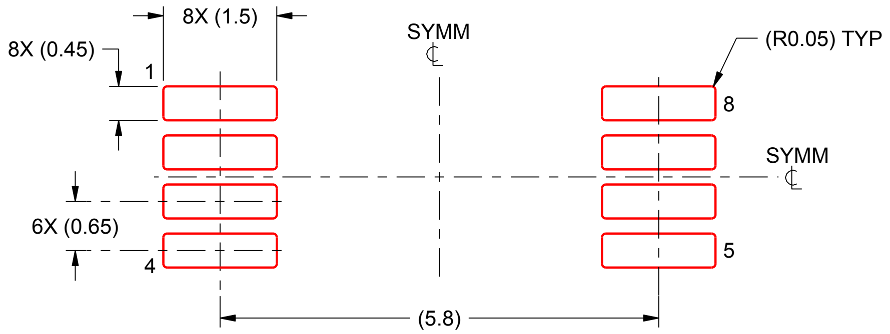
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

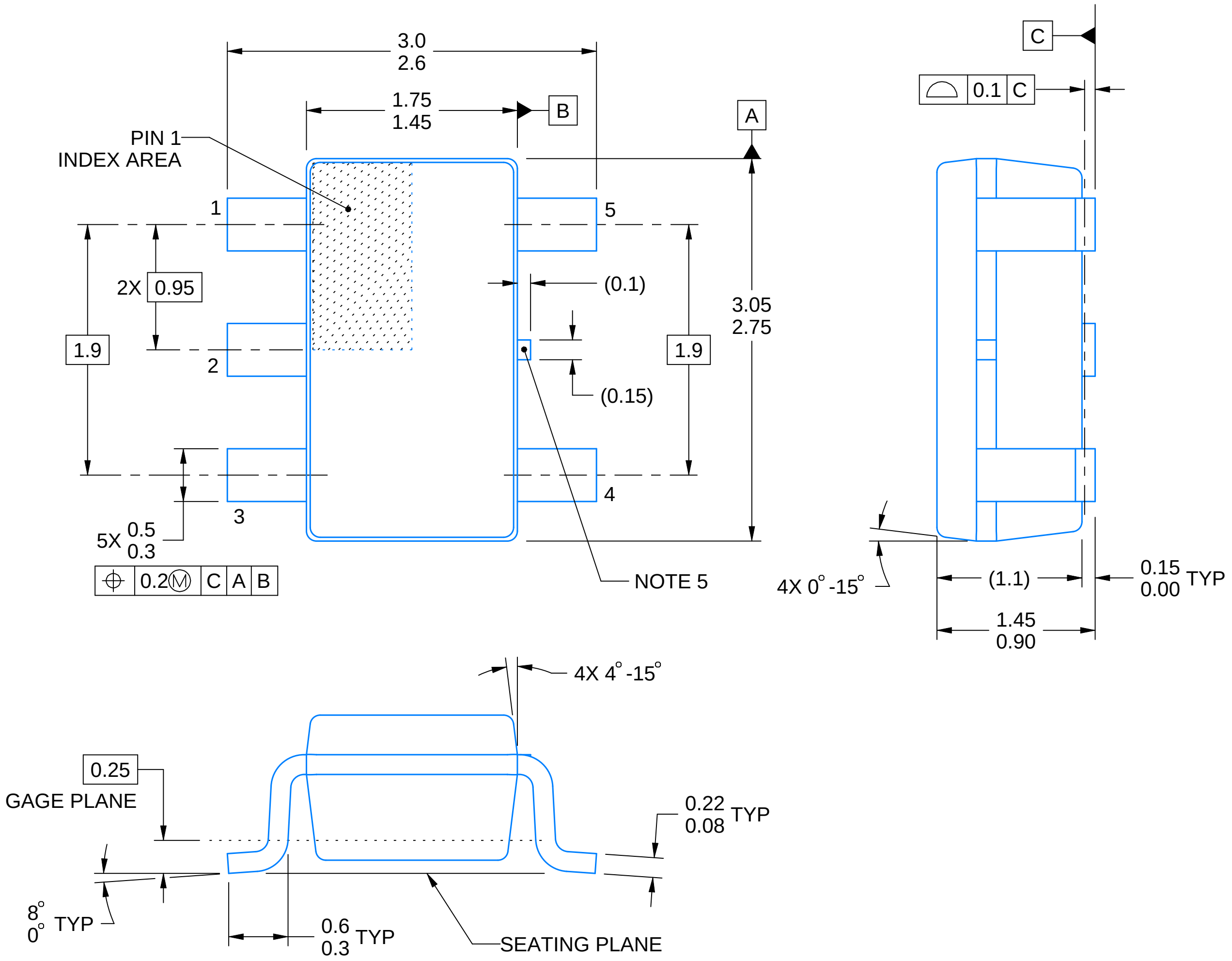
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

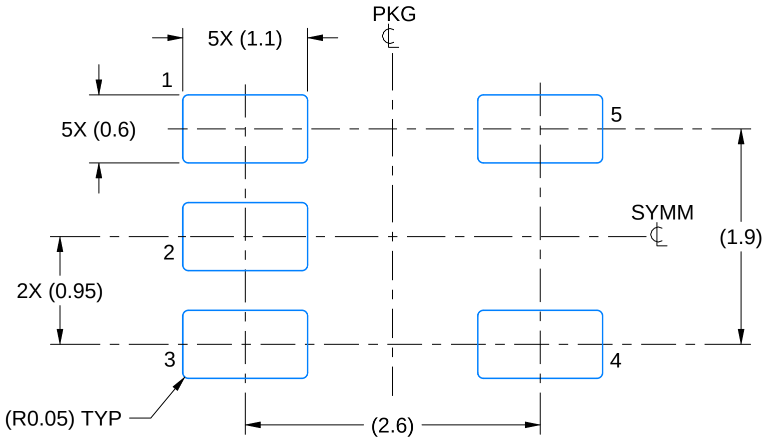


4214839/K 08/2024

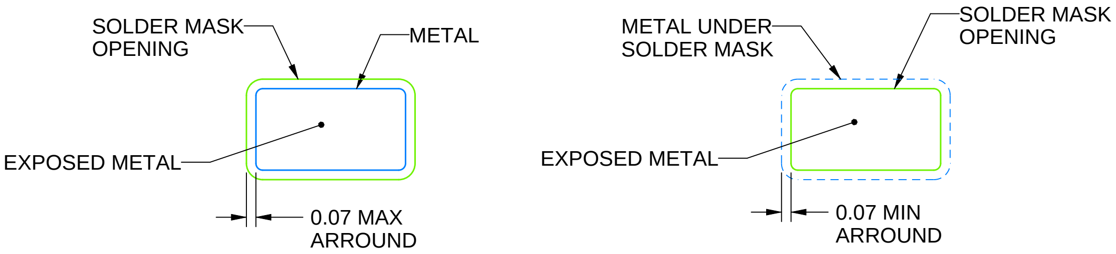
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



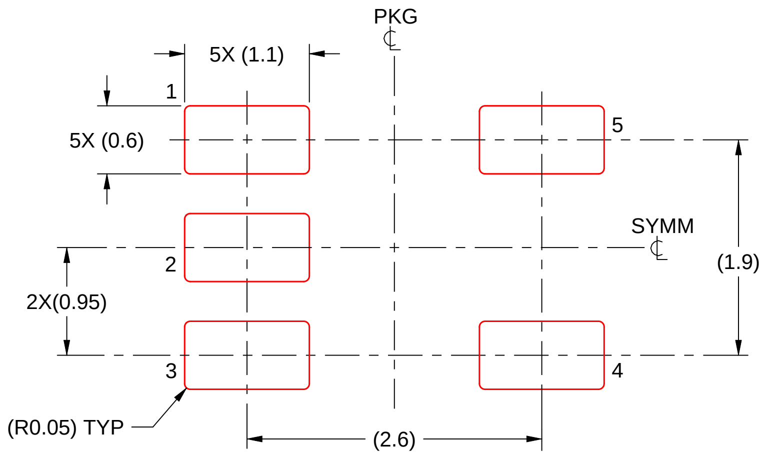
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

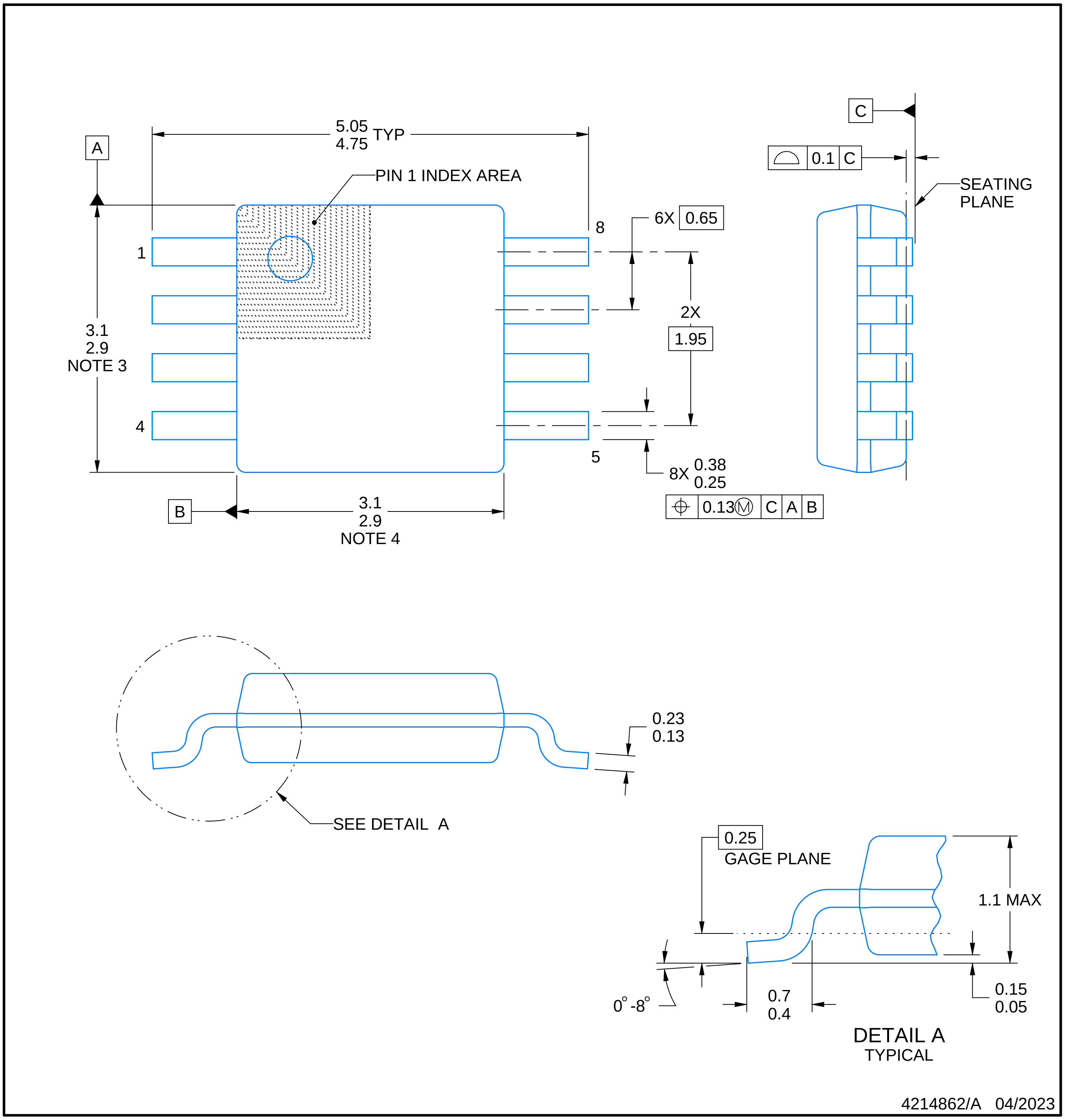
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

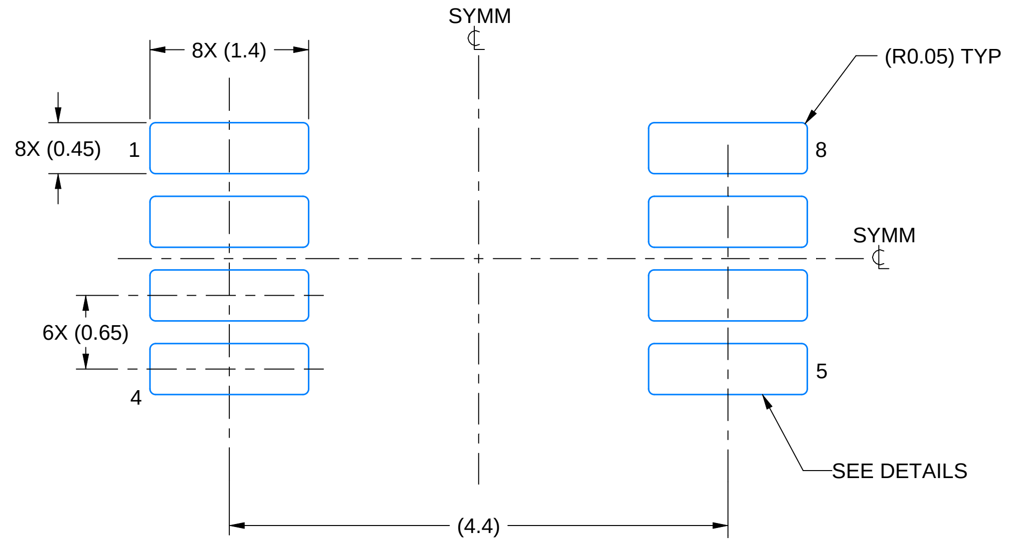


4214862/A 04/2023

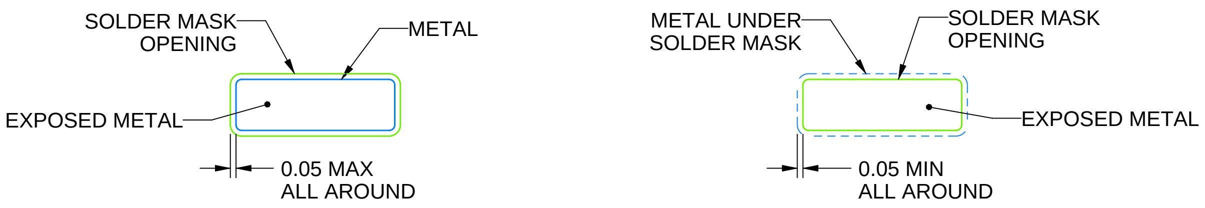
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



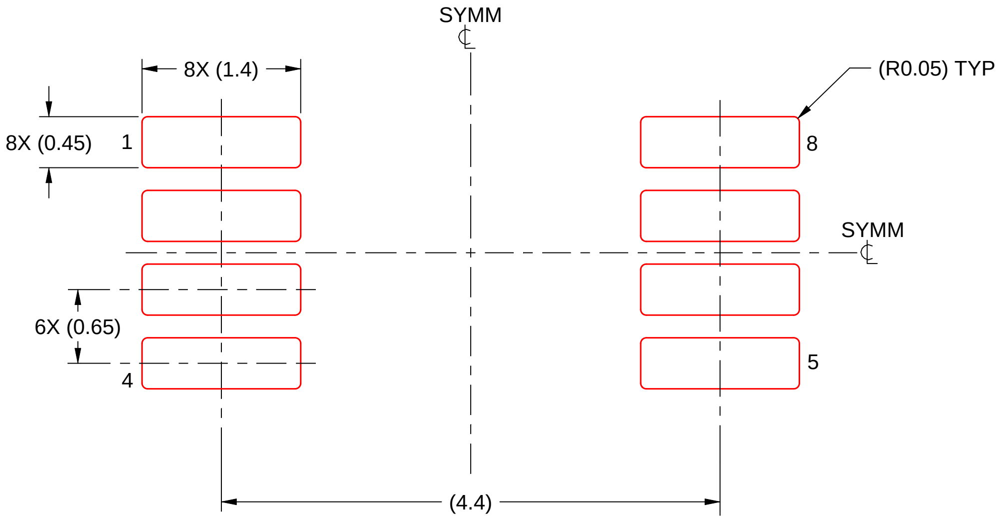
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

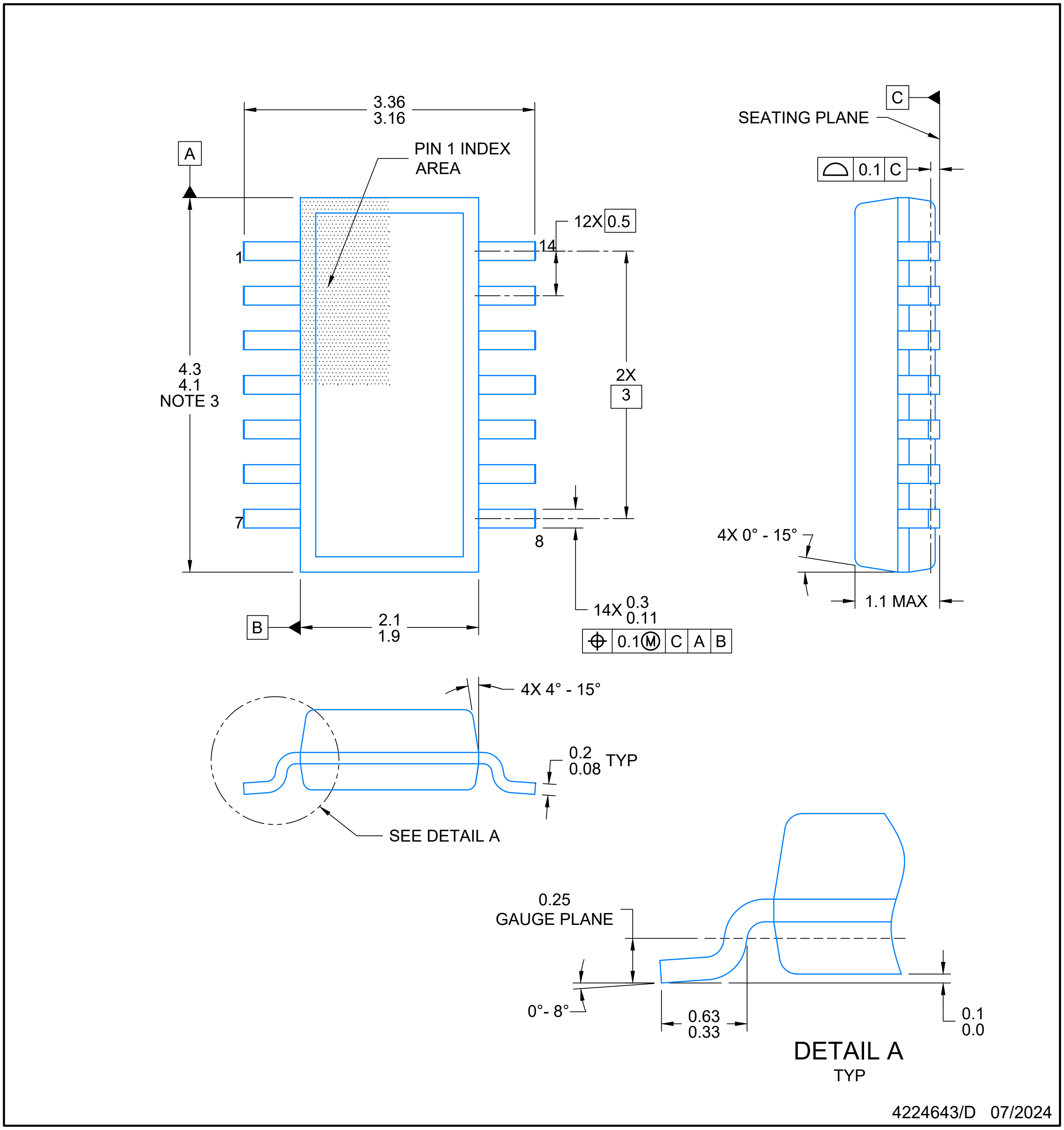
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

SOT-23-THIN - 1.1 mm max height

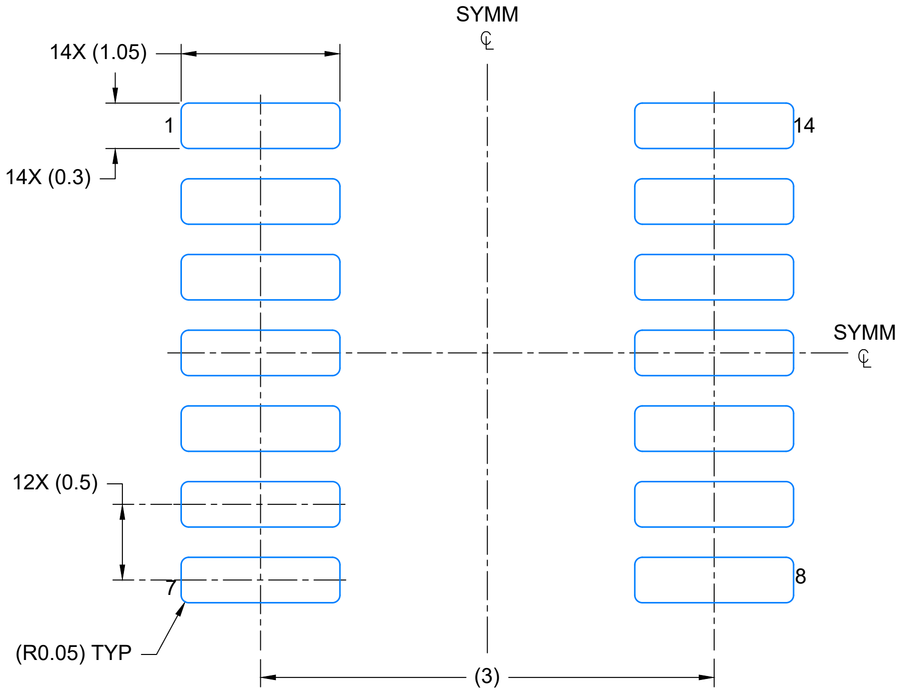
PLASTIC SMALL OUTLINE



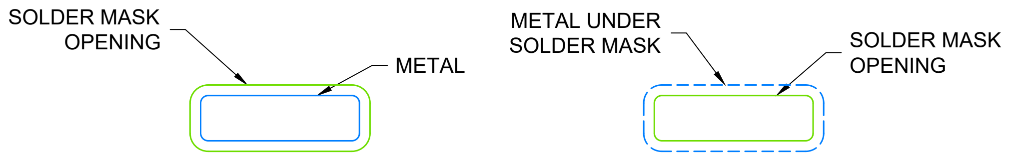
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



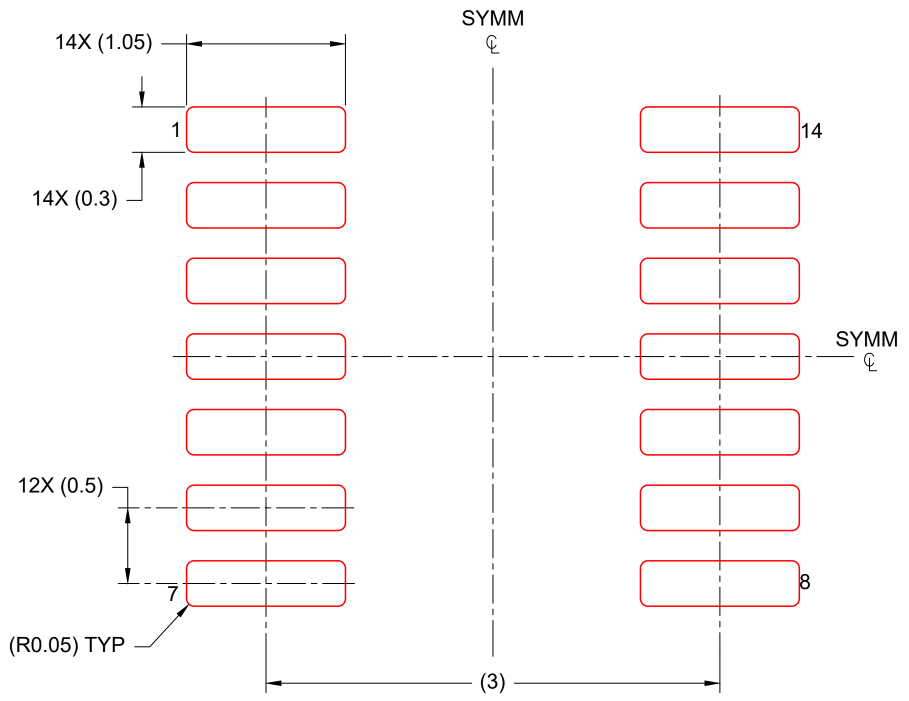
NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

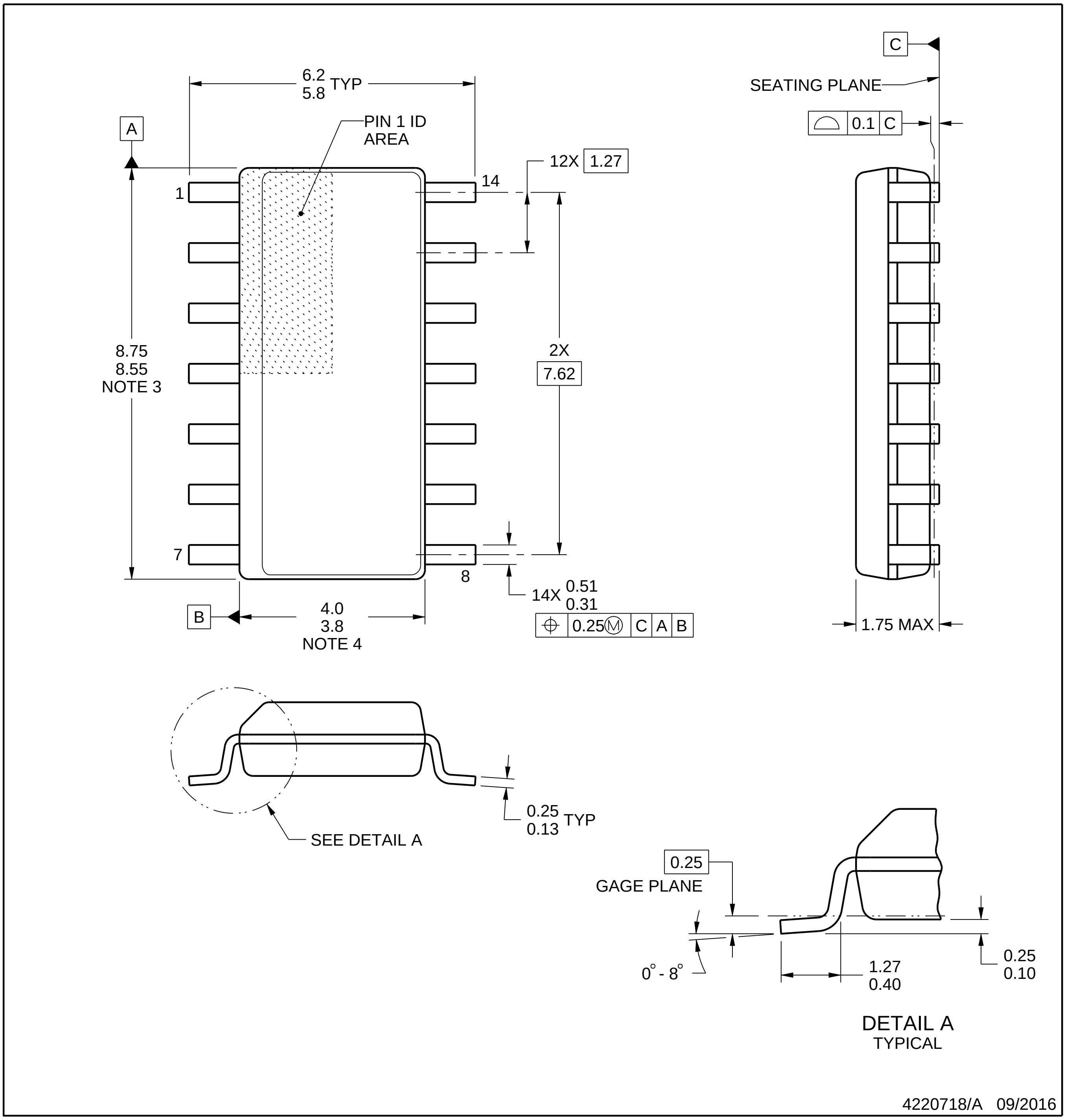


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

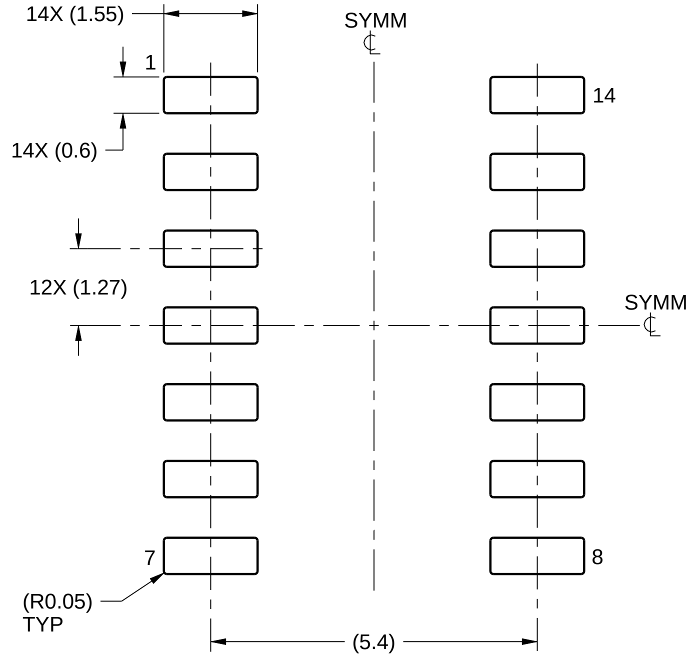
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

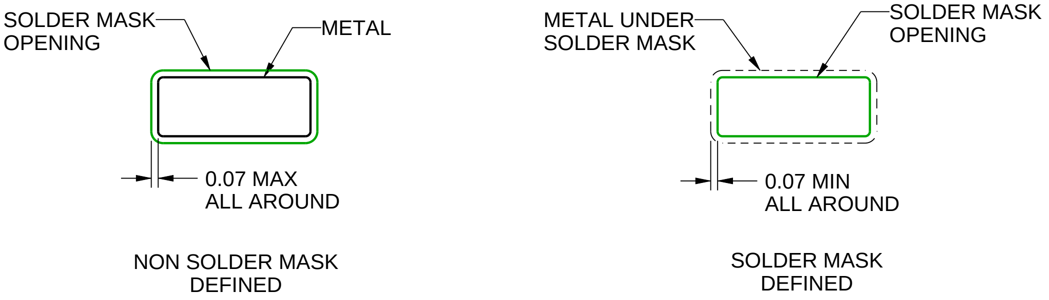


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

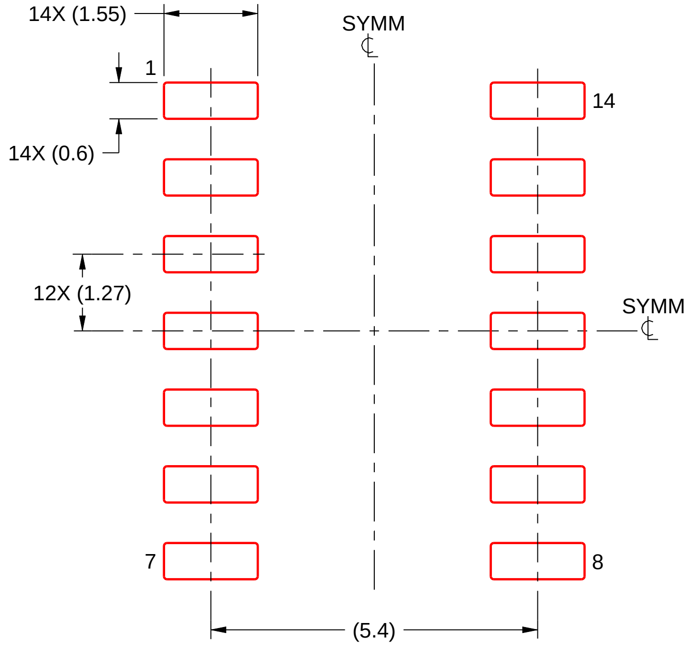


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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