TLV767-Q1 1-A, 16-V Linear Voltage Regulator

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Input voltage range: 2.5 V to 16 V (18 V max)
- Output voltage range:
  - 0.8 V to 14.6 V (adjustable)
  - 1.2 V to 12 V (fixed)
- 1% output accuracy over load and temperature
- Low quiescent current (I_Q):
  - 50 µA (typ) with no load
  - 4 µA (max) when disabled
- High PSRR: 70 dB at 1 kHz, 46 dB at 1 MHz
- Internal soft-start time: 500 µs (typical)
- Fold-back current limiting and thermal protection
- Stable with a 1-µF or larger capacitor
- Package: 8-pin, 3-mm × 3-mm WSON with wettable flanks
  - Low thermal resistance ($R_{\theta JA}$): 51.9°C/W

2 Applications

- DC/DC converters
- Inverter and motor controls
- On-board (OBC) and wireless chargers
- Automotive head units

3 Description

The TLV767-Q1 is a wide input linear voltage regulator supporting an input voltage range from 2.5 V to 16 V and up to 1 A of load current. The output range is from 0.8 V to 12 V or up to 14.6 V with the adjustable version.

The wide input voltage range makes the device a good choice for operating from transformer secondary windings and regulated rails such as 10 V or 12 V. Additionally, the wide output voltage range allows the device to generate the bias voltage for silicon carbide (SiC) gate drivers and microphones as well as power microcontrollers (MCUs) and processors.

The TLV767-Q1 has a 1% output accuracy that is required for powering digital loads with tight supply requirements.

The internal soft-start circuit reduces inrush current during startup, thus allowing for smaller input capacitance.

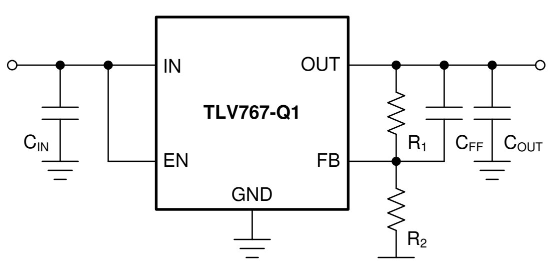
Wide bandwidth PSRR performance is greater than 70 dB at 1 kHz and 46 dB at 1 MHz, which helps attenuate the switching frequency of an upstream DC/DC converter and minimizes post regulator filtering. The high ripple rejection from 20 Hz to 20 kHz make the device a good choice for powering audio components.

The TLV767-Q1 is available in a 8-pin, 3-mm × 3-mm VSON (DRB) package with wettable flanks and low thermal resistance.

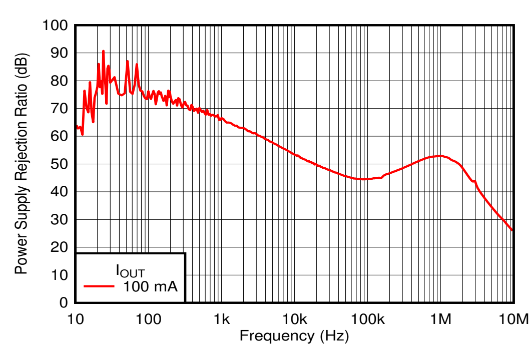
Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV767-Q1	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit



PSRR Performance

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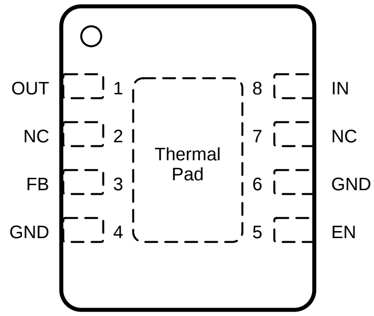
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2020) to Revision A (December 2020)	Page
• Changed document status from advance information to production data	1

5 Pin Configuration and Functions



Not to scale

Figure 5-1. DRB Package (Adjustable Version), 8-Pin WSON, Top View

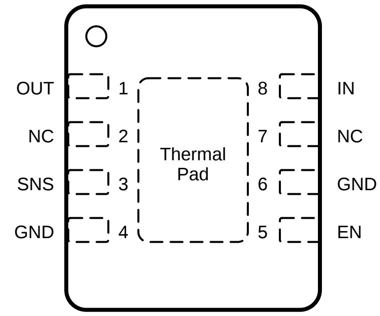


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Figure 5-2. DRB Package (Fixed Version), 8-Pin WSON, Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DRB (Adjustable)	DRB (Fixed)		
EN	5	5	Input	Enable pin. Driving the enable pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. This pin has an internal pullup resistor and can be left floating to enable the device or the pin can be connected to the input pin.
FB	3	—	Input	Feedback pin. Input to the control-loop error amplifier. This pin is used to set the output voltage of the device with the use of external resistors. Do not float this pin. For adjustable-voltage version devices only.
GND	4, 6	4, 6	—	Ground pin. All ground pins must be grounded.
NC	2, 7	2, 7	—	NC pin. Not internally connected. This pin can be either floated or connected to GND for best thermal performance.
IN	8	8	Input	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUT	1	1	Output	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
SNS	—	3	Input	Output sense pin. Connect the SNS pin to the OUT pin, or to remotely sense the output voltage at the load, connect the SNS pin to the load. Do not float this pin. For fixed-voltage version devices only.
Thermal pad			—	Exposed pad of the package. Connect this pad to ground or leave floating. Connect the thermal pad to a large-area ground plane for best thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage[(2)]	Input pin, IN	–0.3	18	V
	Output pin, OUT[(3)]	–0.3	V_{IN} + 0.3	
	Sense pin, SNS[(3)]	–0.3	V_{IN} + 0.3	
	Feedback pin, FB	–0.3	3	
	Enable pin, EN	–0.3	18	
Current	Maximum output current	Internally limited		A
Temperature	Ambient (T_A)	–40	125	°C
	Operating junction (T_J)	–50	150	
	Storage (T_{STG})	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages with respect to GND.

(3) V_{IN} + 0.3 V or 18 V (whichever is smaller).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		16	V
V_{EN}	Enable voltage	0		16	V
V_{OUT}	Output voltage	0.8		14.6	V
I_{OUT}	Output current	0		1	A
C_{OUT}	Output capacitor(1)	1	2.2	220	µF
C_{OUT} ESR	Output capacitor ESR	2		500	mΩ
C_{IN}	Input capacitor		1		µF
C_{FF}	Feed-forward capacitor (optional(2), for adjustable device only)		10		pF
$I_{FB\_DIVIDER}$	Feedback divider current(2) (adjustable device only)	5			µA
T_A	Ambient temperature range	–40		125	°C
T_J	Junction temperature range	–40		150	°C

(1) Effective output capacitance of 0.5 µF minimum required for stability.
(2) C_{FF} required for stability if the feedback divider current < 5 µA. Feedback divider current = V_{OUT} / (R_1 + R_2). See the *Feed-Forward Capacitor (C_{FF})* section for details.

6.4 Thermal Information

THERMAL METRIC(1)		TLV767-Q1 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

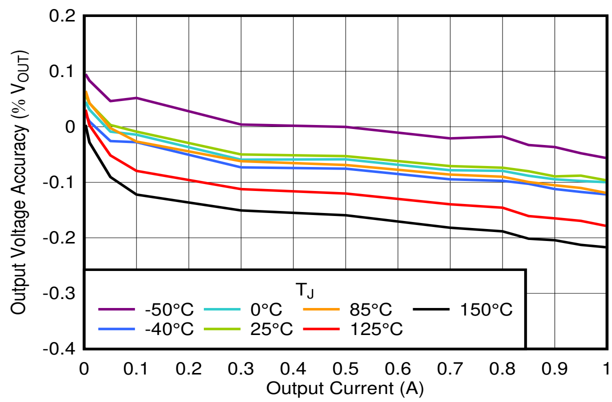
specified at T_J = –40°C to 150°C, V_{IN} = $V_{OUT(nom)}$ + 1.5 V or V_{IN} = 2.5 V (whichever is greater), FB/SNS tied to OUT, I_{OUT} = 10 mA, V_{EN} = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted); typical values are at T_J= 25ºC

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output accuracy	T_J = 25°C		–0.5		0.5	%
		T_J = –40°C to 150°C	V_{IN} ≥ 3.0 V, 1 mA ≤ I_{OUT} ≤ 1 A	–1		1	%
			2.5 V ≤ V_{IN} < 3.0 V, 1 mA ≤ I_{OUT} ≤ 800 mA	–1		1	%
V_{FB}	Feedback voltage				0.8		V
V_{REF}	Internal reference (adjustable device)	T_J = 25°C		–0.5		0.5	%
		T_J = –40°C to 150°C		–1		1	
I_{FB}	Feedback pin current	V_{FB} = 1 V		–20	1	50	nA
$\Delta V_{OUT(\Delta VIN)}$	Line regulation(1)	$V_{OUT(NOM)}$ +1.5 V ≤ V_{IN} ≤ 16 V, I_{OUT} = 10 mA				0.02	%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1 mA ≤ I_{OUT} ≤ 1 A, V_{IN} ≥ 3.0 V			0.1	0.5	%/A
		1 mA ≤ I_{OUT} ≤ 800 mA, 2.5 V ≤ V_{IN} < 3.0 V			0.1	0.5	
V_{DO}	Dropout voltage(2)	$V_{IN(NOM)}$ ≥ 3.0V, I_{OUT} = 1 A		0.63	0.94	1.5	V
		2.5 V ≤ $V_{IN(NOM)}$ < 3.0 V, I_{OUT} = 800 mA		0.48	0.8	1.4	
I_{CL}	Output current limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$, V_{IN} ≥ 3.0V		1.1	1.37	1.6	A
		V_{OUT} = 0.9 x $V_{OUT(NOM)}$, 2.5 V ≤ V_{IN} < 3.0 V		0.81	1.28	1.6	
I_{SC}	Short-circuit current limit	V_{OUT} = 0 V		150	250	350	mA
I_Q	Quiescent current	Adjustable output device, I_{OUT} = 0 mA		25	50	80	µA
		Fixed output devices, I_{OUT} = 0 mA		25	60	95	
I_{GND}	Ground current	I_{OUT} = 1 A, V_{IN} ≥ 3.0 V			1.5		mA
$I_{SHUTDOWN}$	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 16 V		0.1	1.6	4	µA
$V_{EN(HIGH)}$	Enable pin logic high	2.5 V ≤ V_{IN} ≤ 16 V		1.2			V
$V_{EN(LOW)}$	Enable pin logic low	2.5 V ≤ V_{IN} ≤ 16 V				0.4	V
I_{EN}	Enable pullup current	V_{EN} = 0 V		200	400	800	nA
$I_{PULLDOWN}$	Output pulldown current	V_{IN} = 16 V, V_{OUT} = 2.5 V, V_{EN} = 0 V		0.9	1.4	1.6	mA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 1.8 V, I_{OUT} = 300 mA, f = 120 Hz			70		dB
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{IN} = 3.3 V, V_{OUT} = 0.8 V, I_{OUT} = 100 mA			60		μV_{RMS}
V_{UVLO+}	UVLO threshold rising	V_{IN} rising		2	2.22	2.4	V
V_{UVLO-}	UVLO threshold falling	V_{IN} falling		1.9	2.09	2.3	V
$V_{UVLO(HYS)}$	UVLO hysteresis			100	130	200	mV
$T_{SD(shutdown)}$	Thermal shutdown temperature	Temperature increasing			180		ºC
$T_{SD(reset)}$	Thermal shutdown reset temperature	Temperature falling			160		ºC

(1) Line regulation is measured with V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater).
(2) V_{DO} is measured with V_{IN} = 95% x $V_{OUT(nom)}$ for fixed output devices. V_{DO} is not measured for fixed output devices when V_{OUT} < 2.5 V. For the adjustable output device, V_{DO} is measured with V_{FB} = 95% x $V_{FB(nom)}$.

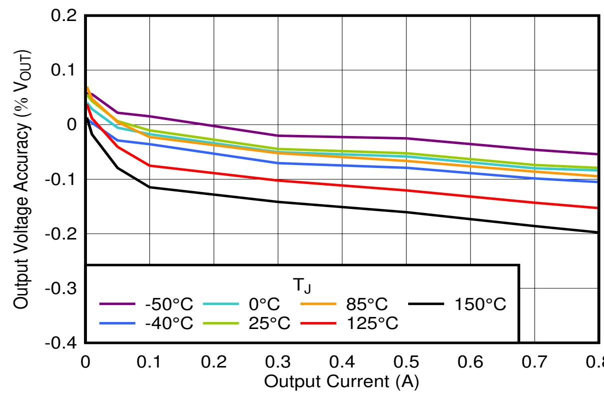
6.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



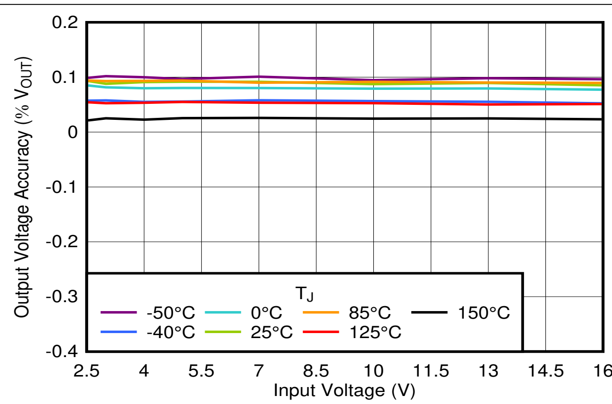
V_{IN} = 3.0 V

Figure 6-1. V_{OUT} Accuracy vs I_{OUT}



V_{IN} = 2.5 V

Figure 6-2. V_{OUT} Accuracy vs I_{OUT}



I_{OUT} = 10 mA

Figure 6-3. V_{OUT} Accuracy vs V_{IN}

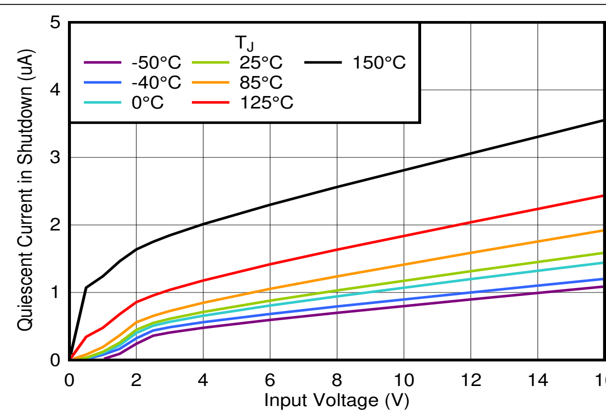
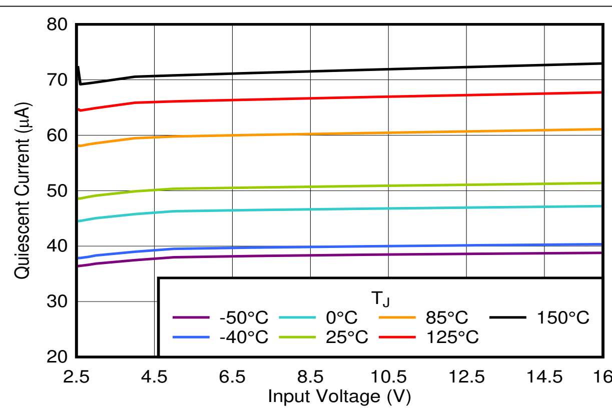
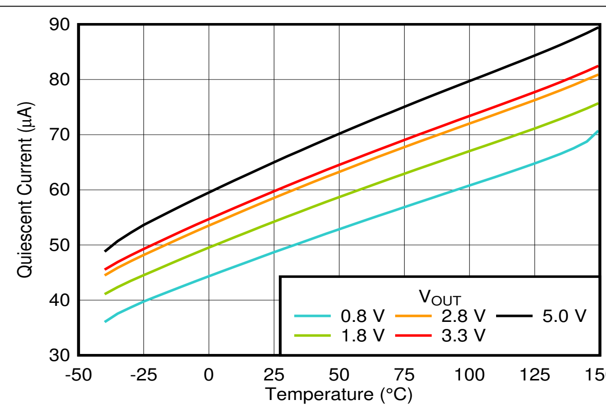


Figure 6-4. $I_{SHUTDOWN}$ vs V_{IN}



I_{OUT} = 0 mA, adjustable-voltage version devices

Figure 6-5. I_Q vs V_{IN}

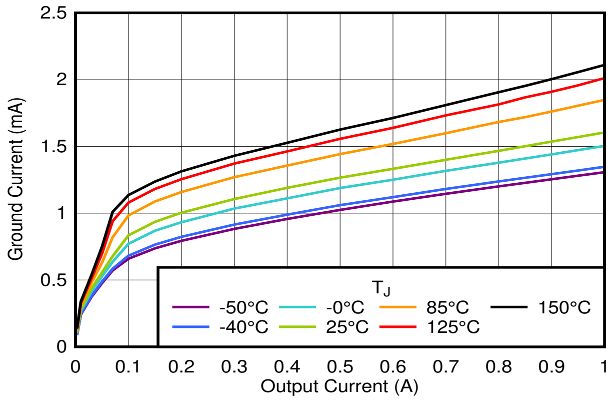


I_{OUT} = 0 mA, fixed-voltage version devices

Figure 6-6. I_Q vs Temperature

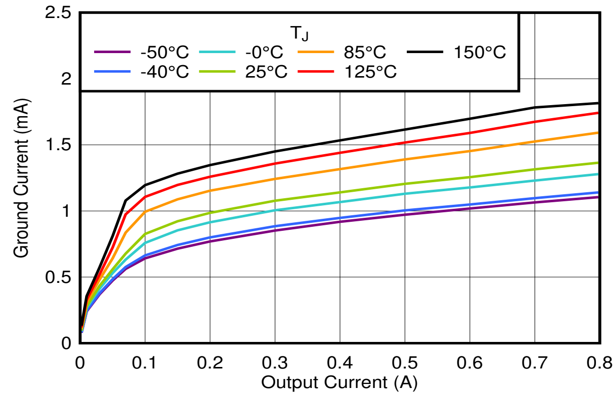
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



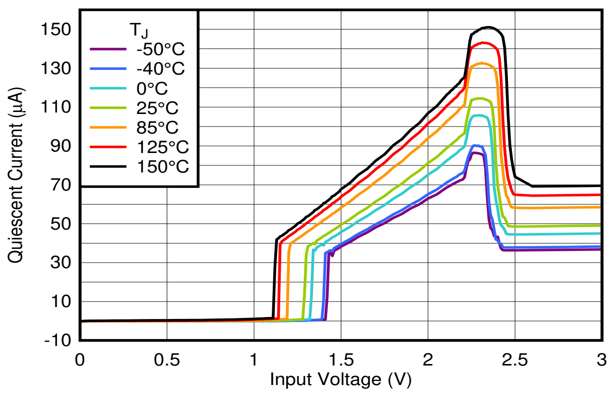
V_{IN} = 3.0 V

Figure 6-7. I_{GND} vs I_{OUT}



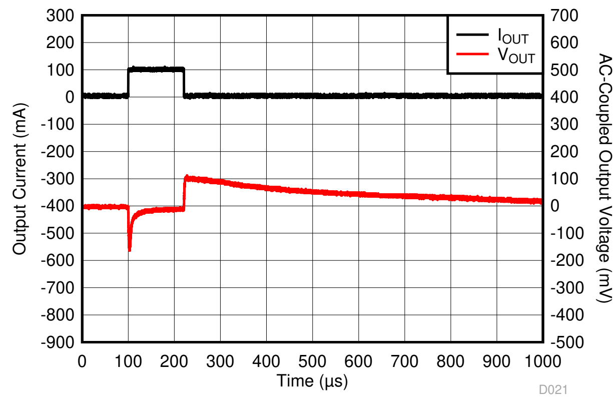
V_{IN} = 2.5 V

Figure 6-8. I_{GND} vs I_{OUT}



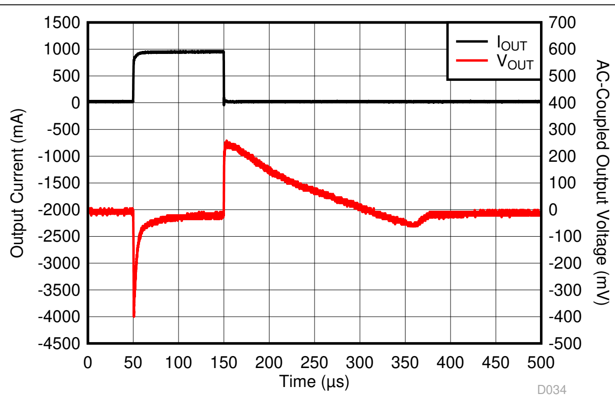
I_{OUT} = 0 mA

Figure 6-9. I_Q Increase Below Minimum V_{IN}



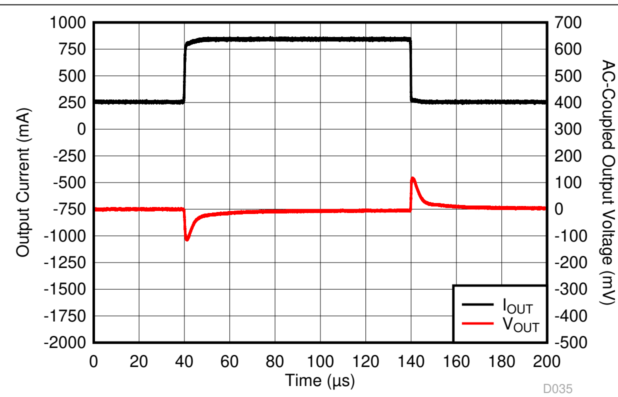
V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{FF} = 10 pF, ramp rate = 0.4 A/µs

Figure 6-10. I_{OUT} Transient From 0 mA to 100 mA



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{FF} = 10 pF, ramp rate = 0.5 A/µs

Figure 6-11. I_{OUT} Transient From 1 mA to 1 A

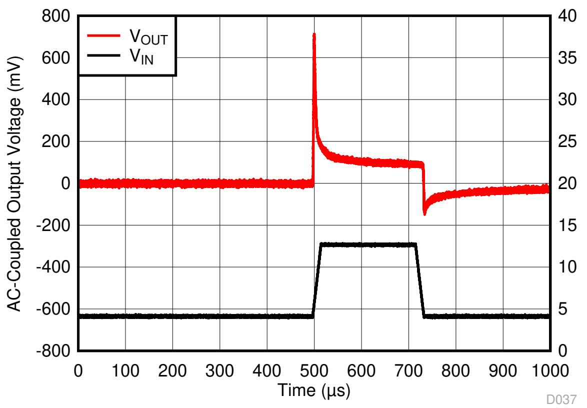


V_{IN} = 5 V, V_{OUT} = 3.3 V, ramp rate = 0.8 A/µs

Figure 6-12. I_{OUT} Transient From 250 mA to 850 mA

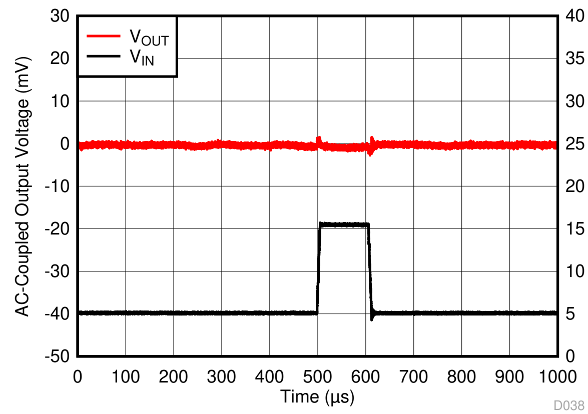
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



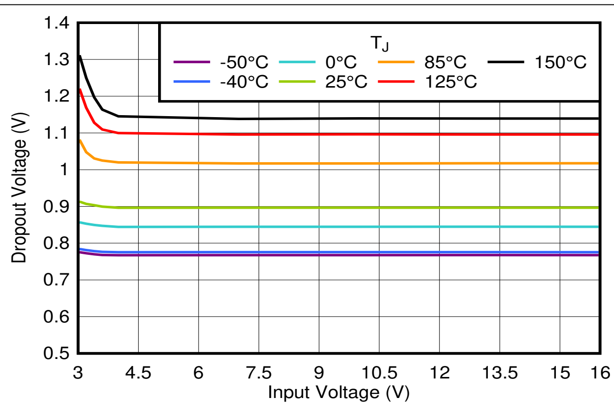
V_{OUT} = 3.3 V, I_{OUT} = 1 A, V_{IN} ramp rate = 0.6 V/µs

Figure 6-13. V_{IN} Transient in Dropout From 4 V to 13 V



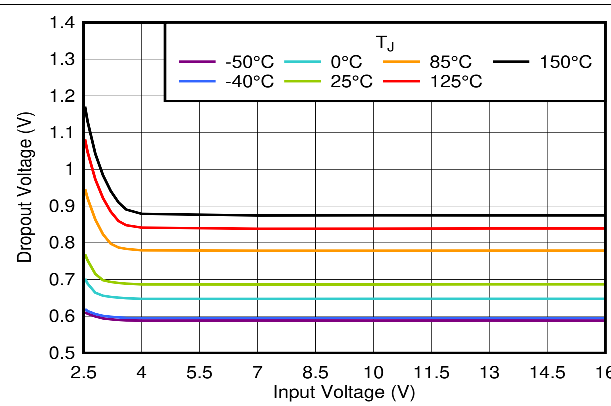
V_{OUT} = 3.3 V, I_{OUT} = 33 µA, V_{IN} ramp rate = 1.6 V/µs

Figure 6-14. V_{IN} Transient From 5 V to 16 V



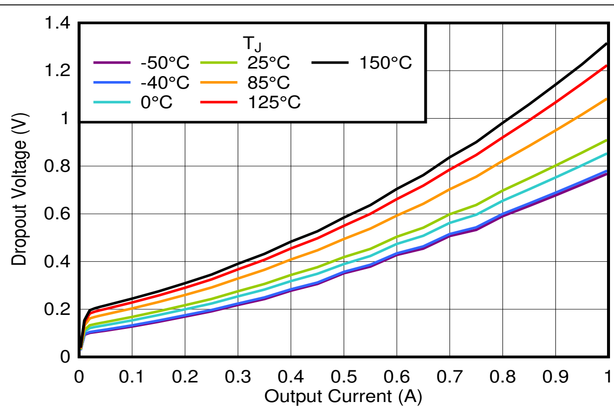
I_{OUT} = 1.0 A

Figure 6-15. V_{DO} vs V_{IN}



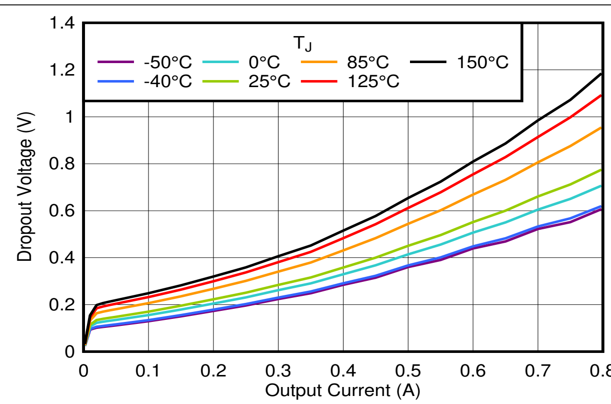
I_{OUT} = 0.8 A

Figure 6-16. V_{DO} vs V_{IN}



V_{IN} = 3.0 V

Figure 6-17. V_{DO} vs I_{OUT}

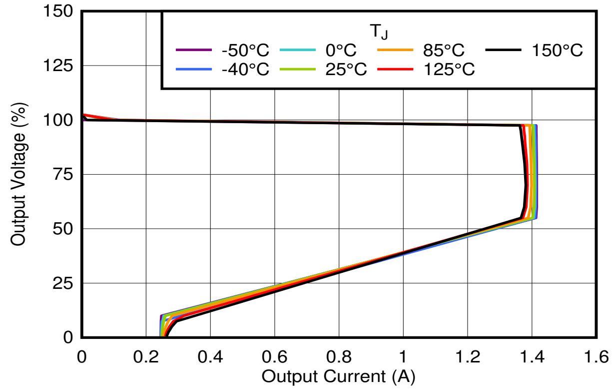


V_{IN} = 2.5 V

Figure 6-18. V_{DO} vs I_{OUT}

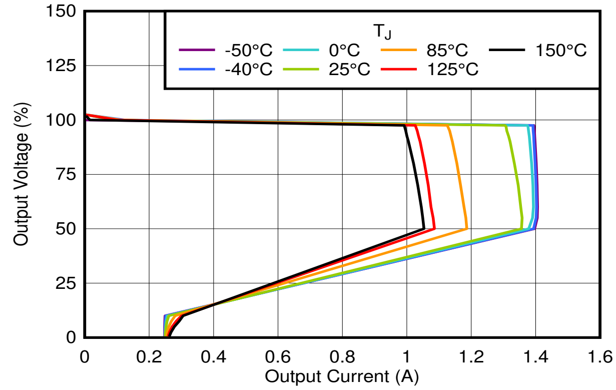
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



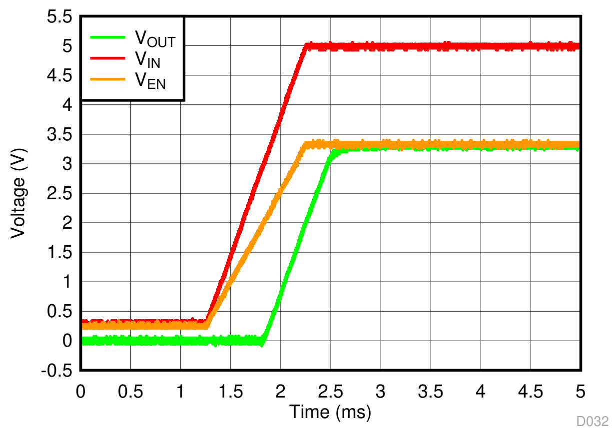
V_{IN} = 3.0 V

Figure 6-19. Foldback Current Limit vs I_{OUT} and Temperature



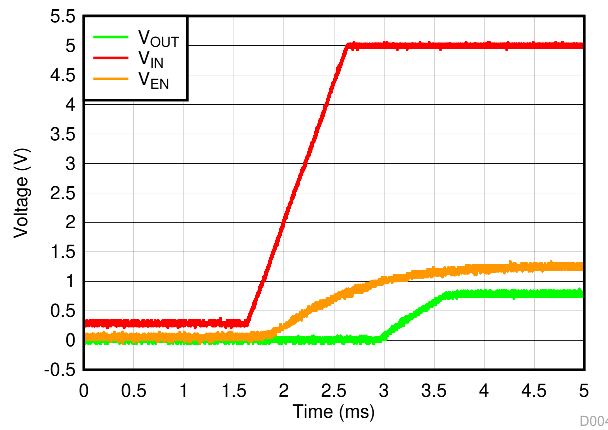
V_{IN} = 2.5 V

Figure 6-20. Foldback Current Limit vs I_{OUT} and Temperature



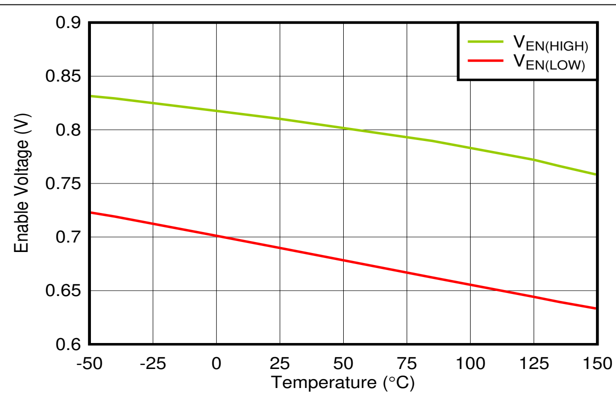
V_{OUT} = 3.3 V

Figure 6-21. Startup With Separate V_{EN} and V_{IN}



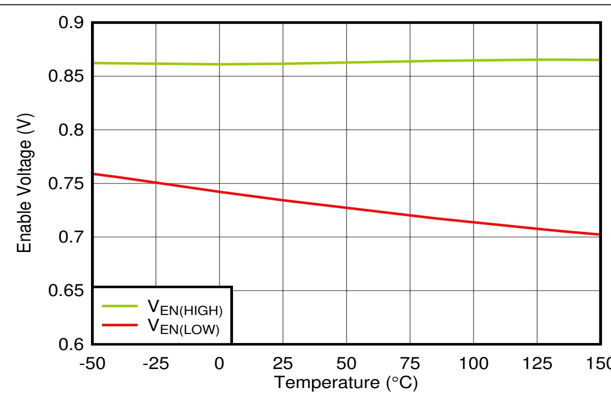
EN pulled up internally, V_{OUT} = 0.8 V

Figure 6-22. Startup With V_{EN} Floating



V_{IN} = 2.5 V

Figure 6-23. V_{EN} Thresholds vs Temperature



V_{IN} = 16 V

Figure 6-24. V_{EN} Thresholds vs Temperature

6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)

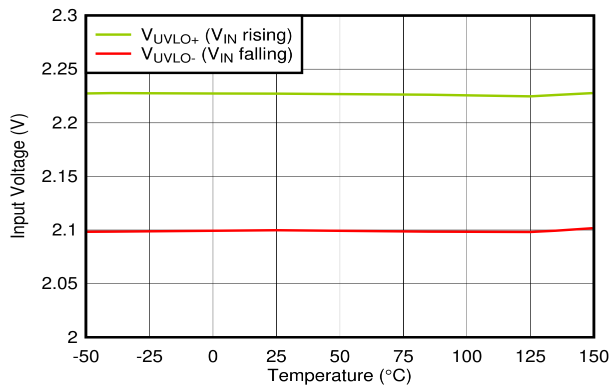
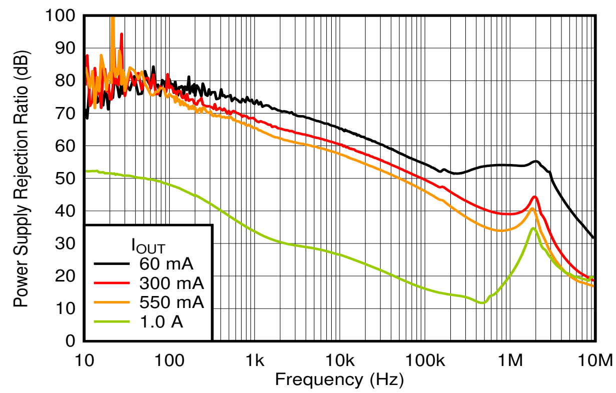
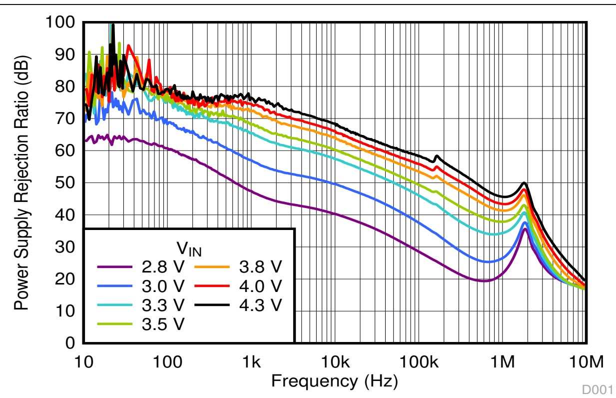


Figure 6-25. UVLO Thresholds vs Temperature



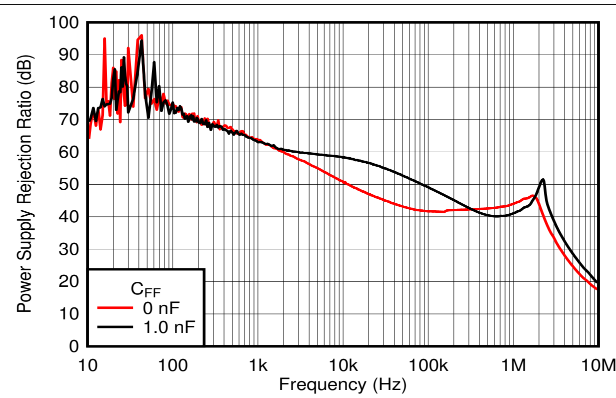
V_{OUT} = 1.8 V, V_{IN} = 3.3 V, C_{FF} = 1 nF

Figure 6-26. PSRR vs Frequency and I_{OUT}



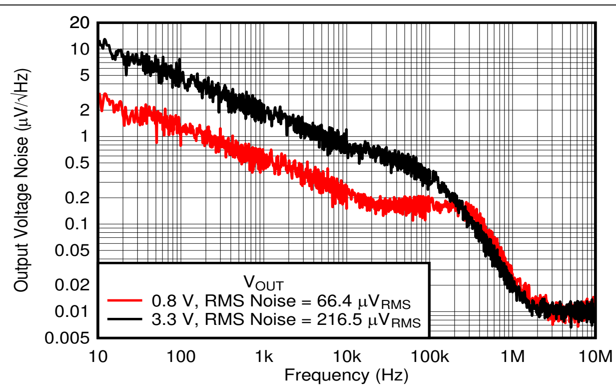
V_{OUT} = 1.8 V, I_{OUT} = 0.55 A, C_{FF} = 1 nF

Figure 6-27. PSRR vs Frequency and V_{IN}



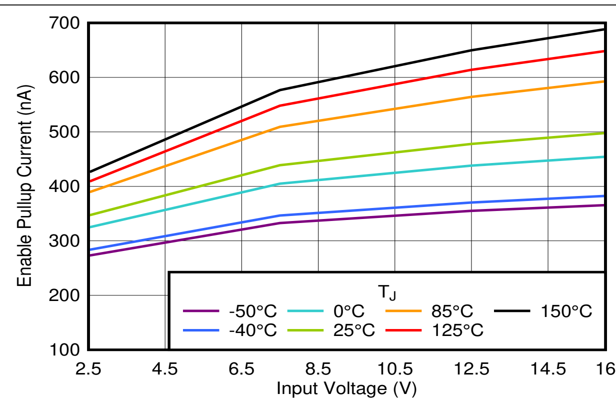
V_{OUT} = 3.3 V, V_{IN} = 4.8 V, I_{OUT} = 0.33 A

Figure 6-28. PSRR vs Frequency and C_{FF}



C_{FF} = 0 nF, I_{OUT} = 0.1 A, RMS noise BW = 10 Hz to 100 kHz

Figure 6-29. Output Noise (V_n) vs Frequency and V_{OUT}

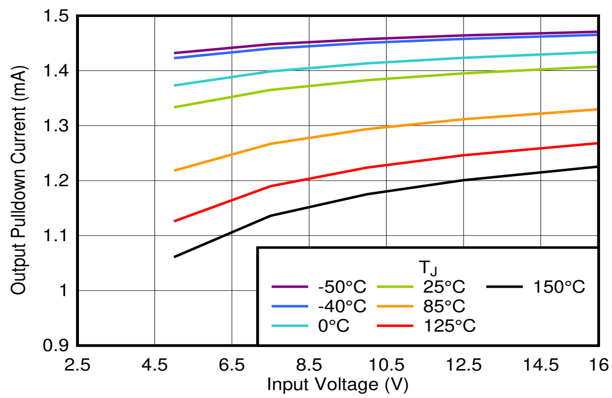


V_{EN} = 0 V

Figure 6-30. I_{EN} vs V_{IN}

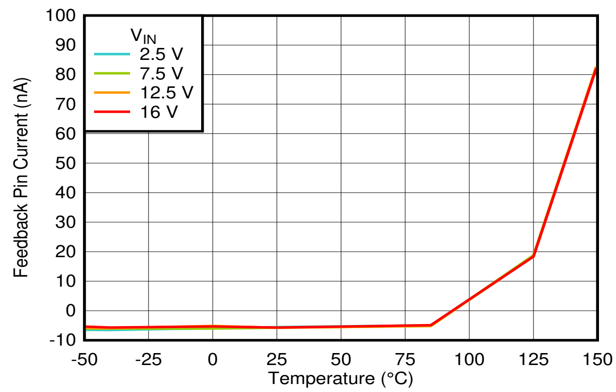
6.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.5 V or 2.5 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = 2.0 V, C_{IN} = 1.0 µF, and C_{OUT} = 1.0 µF (unless otherwise noted)



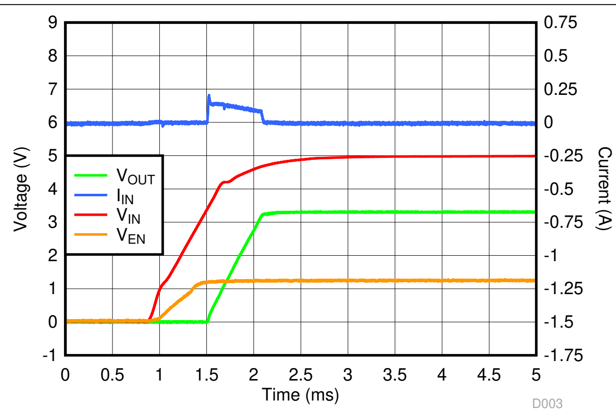
V_{OUT} = 2.5 V

Figure 6-31. $I_{PULLDOWN}$ vs V_{IN}



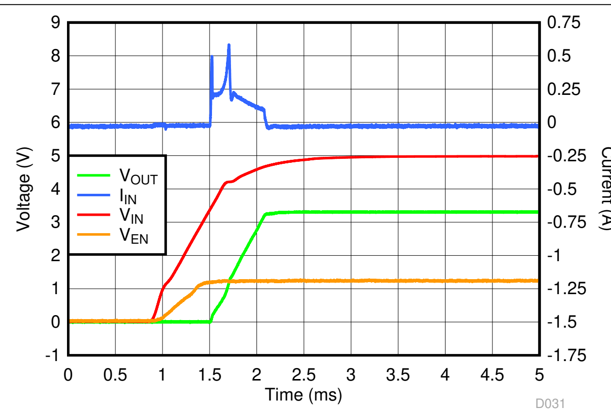
V_{FB} = 1.0 V

Figure 6-32. I_{FB} vs Temperature



V_{OUT} = 3.3 V, I_{OUT} = 33 µA

Figure 6-33. Startup Inrush Current With C_{OUT} = 22 µF



V_{OUT} = 3.3 V, I_{OUT} = 33 µA

Figure 6-34. Startup Inrush Current With C_{OUT} = 47 µF

7 Detailed Description

7.1 Overview

The TLV767-Q1 is a low quiescent current, high PSRR linear regulator capable of handling up to 1 A of load current. Unlike typical high current linear regulators, the TLV767-Q1 consumes significantly less quiescent current. This device is ideal for high current applications that require very sensitive power-supply rails.

This device features an integrated foldback current limit, thermal shutdown, output enable, internal output pulldown, and undervoltage lockout (UVLO). This device delivers excellent line and load transient performance. This device is low noise and exhibits very good PSRR. The operating ambient temperature range of the device is –40°C to +125°C.

7.2 Functional Block Diagrams

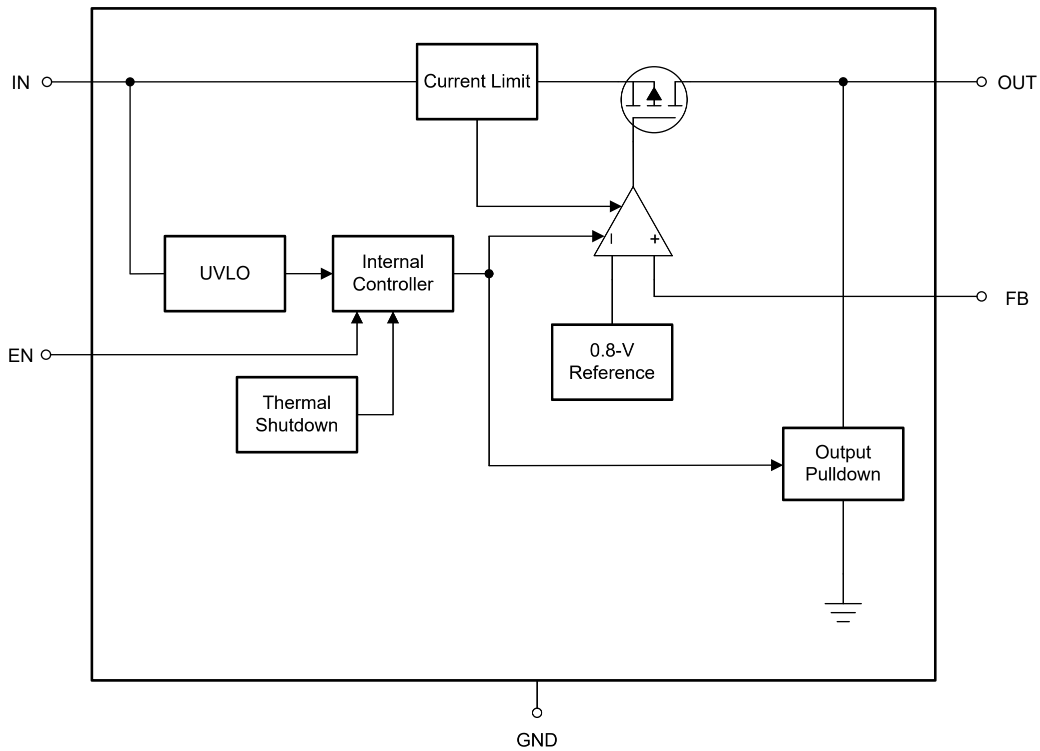


Figure 7-1. Adjustable-Version Block Diagram

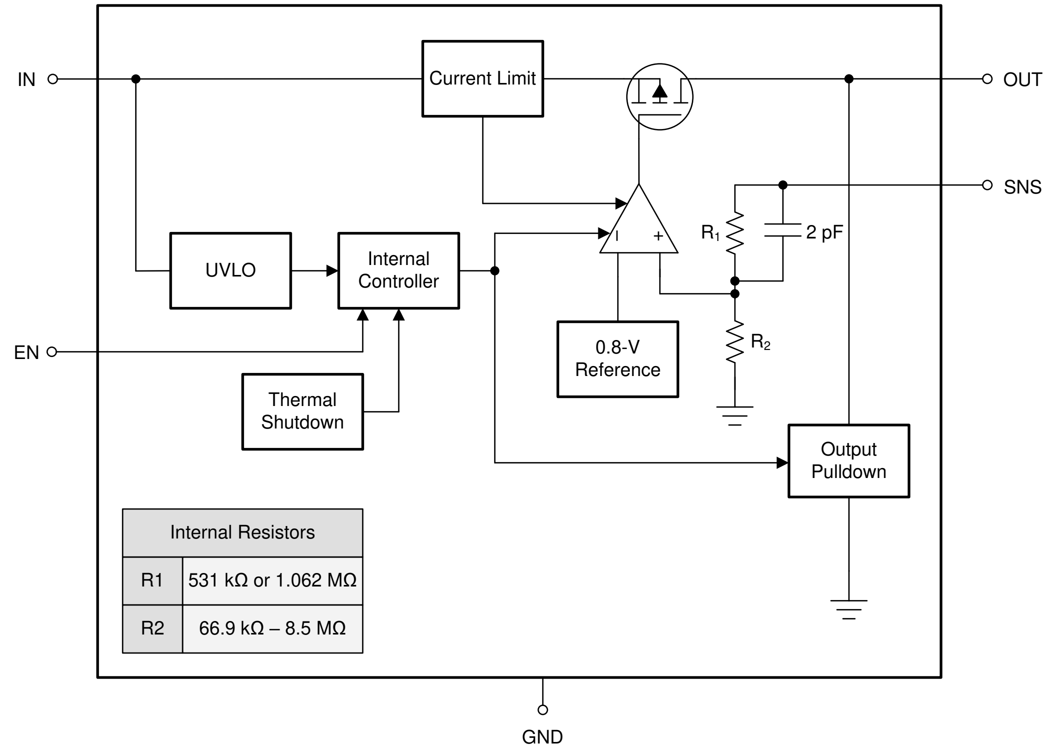


Figure 7-2. Fixed-Version Block Diagram

7.3 Feature Description

7.3.1 Output Enable

The enable pin for the device is an active-high pin. The output voltage is enabled when the voltage of the enable pin is greater than the high-level input voltage of the EN pin and disabled with the enable pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the enable pin to the input of the device.

This device has an internal pullup current on the EN pin. The EN pin can be left floating to enable the device.

The device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

7.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 50% × $V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{SC}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application report.

Figure 7-3 shows a diagram of the foldback current limit.

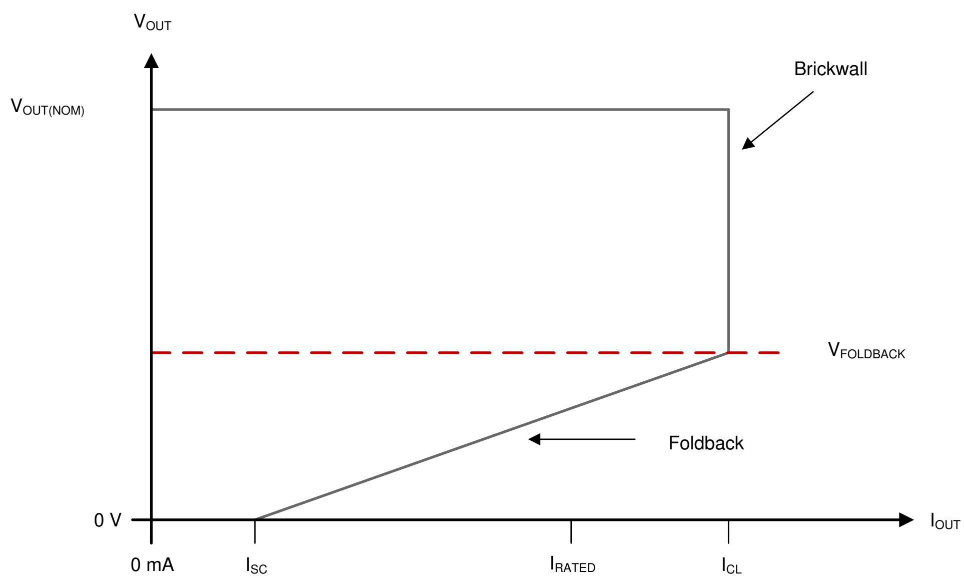


Figure 7-3. Foldback Current Limit

7.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.5 Output Pulldown

The device has an output pulldown circuit. V_{OUT} pulldown sink to ground capability is listed in the *Electrical Characteristics* table. The output pulldown activates under the following conditions:

- Device disabled
- 1.0 V < V_{IN} < V_{UVLO}

The output pulldown current for this device is 1.2 mA typical, as listed in the *Electrical Characteristics* table of the *Specifications* section.

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the set MID_OUT output voltage plus the V_{MID_OUT} dropout voltage ($V_{MID\_OUT(nom)} + V_{DO(MID\_OUT)}$)
- The current sourced from OUT or MID_OUT is less than the current limits ($I_{OUT} < I_{CL(OUT)}$ or $I_{MID\_OUT} < I_{CL(MID\_OUT)}$) respectively
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold or the EN pin is left floating

7.4.3 Dropout Operation

If the input voltage is lower than the set MID_OUT voltage plus the specified $V_{DO(MID\_OUT)}$ dropout voltage, but all other conditions are met for normal operation, the device operates in V_{MID_OUT} dropout mode. When the devcie operates in this mode while V_{MID_OUT} voltage is still higher than $V_{OUT(nom)} + V_{DO(OUT)}$, then V_{OUT} is still in regulation however V_{MID_OUT} voltage is in its dropout mode. In V_{MID_OUT} dropout mode, V_{MID_OUT} voltage tracks the input voltage and during this mode, the transient performance of V_{MID_OUT} voltage becomes significantly degraded because the MID_OUT pass transistor is in the ohmic or triode region, and acts as a switch. Also V_{MID_OUT} line or load transients can result in large V_{MID_OUT} voltage deviations.

The devcie enters $V_{DO(OUT)}$ dropout mode when the input voltage is lower than the set MID_OUT voltage and V_{MID_OUT} is lower than $V_{OUT(nom) + VDO(OUT)}$. In V_{OUT} dropout mode, V_{OUT} voltage tracks V_{MID_OUT} voltage which in return tracks the input voltage. During this mode, the transient performance of both V_{MID_OUT} and V_{OUT} voltages becomes significantly degraded because the pass transistors are in the ohmic or triode region and acting as switches. Also line or load transients can result in large V_{MID_OUT} and V_{OUT} voltages deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100x the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

8.1.2 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 8-1 shows one approach for protecting the device.

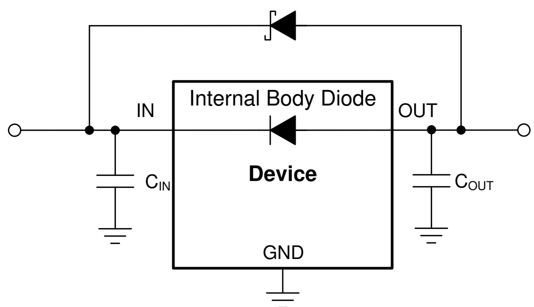


Figure 8-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the startup time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 5 µA. Equation 6 calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid startup time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$ µs.

For an output voltage of 0.8 V with the FB pin tied to the OUT pin, no C_{FF} is used.

8.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (7)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application report

8.2 Typical Application

This section discusses implementing this device for a typical application. Figure 8-2 shows the application circuit.

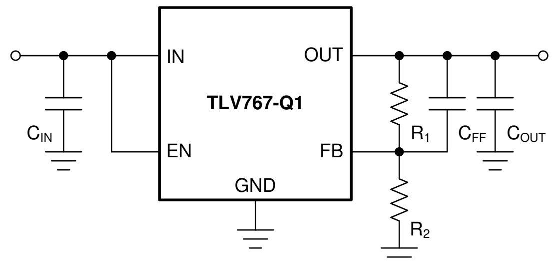


Figure 8-2. Typical Application Circuit

8.2.1 Design Requirements

Table 8-1 summarizes the design requirements for this application.

Table 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V
Output voltage	3.3 V
Output current	100 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude. If load transients are expected with ramp rates greater than 0.5 A/µs, use a 2.2-µF or larger output capacitor.

8.2.2.2 Choose Feedback Resistors

For this design example, V_{OUT} is set to 3.3 V. The following equations set the feedback divider resistors for the desired output voltage:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (11)$$

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (12)$$

For improved output accuracy, use Equation 12 and I_{FB} = 50 nA as listed in the *Electrical Characteristics* table in the *Specifications* section to calculate the upper limit for series feedback resistance ($R_1 + R_2 \leq$ 660 kΩ).

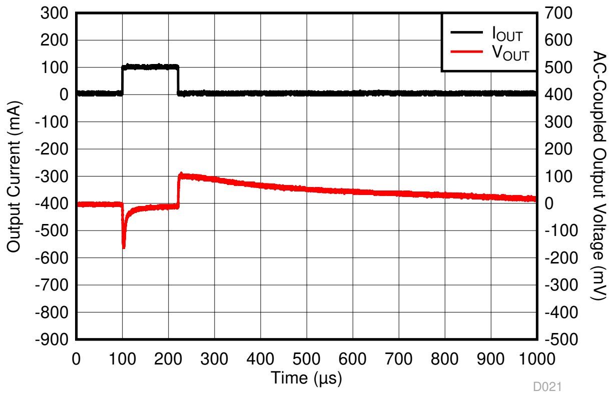
The control-loop error amplifier drives the FB pin to the same voltage as the internal reference (V_{FB} = 0.8 V, as listed in the *Electrical Characteristics* table). Use Equation 11 to determine the ratio of R_1 / R_2 = 3.125. Use this ratio and solve Equation 12 for R_2. Now calculate the upper limit for $R_2 \leq$ 160 kΩ. Select a standard value resistor for R_2 = 160 kΩ.

Reference Equation 11 and solve for R_1:

$$R_1 = (V_{OUT} / V_{FB} - 1) \times R_2 \quad (13)$$

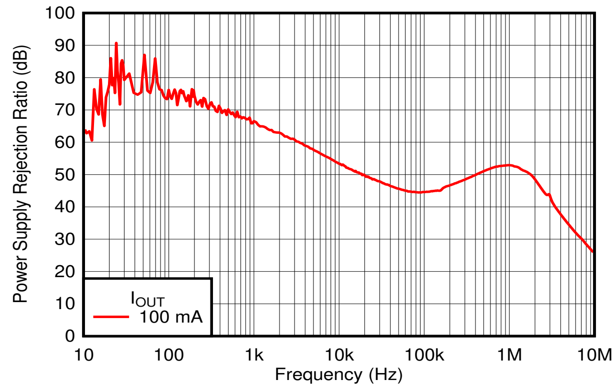
From Equation 13, R_1 = 500 kΩ can be determined. Select a standard value resistor for R_1 = 499 kΩ. V_{OUT} = 3.3 V (as determined by Equation 11).

8.2.3 Application Curves



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, C_{FF} = 10 pF

Figure 8-3. Load Transient Response, I_{OUT} 0 mA to 100 mA



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, C_{FF} = 0 pF

Figure 8-4. PSRR Performance

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2.5 V to 16 V. To ensure that the output voltage is well regulated and dynamic performance is optimum, the input supply must be at least $V_{OUT(nom)}$ + 1.5 V or 2.5 V, whichever is greater. For a 1-A output current operation, the input supply must be 3 V or greater. Connect a low output impedance power supply directly to the input pin of the TLV767-Q1.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible
- Use copper planes for device connections to IN, OUT, and GND pins to optimize thermal performance
- Place thermal vias around the device to distribute heat

10.2 Layout Examples

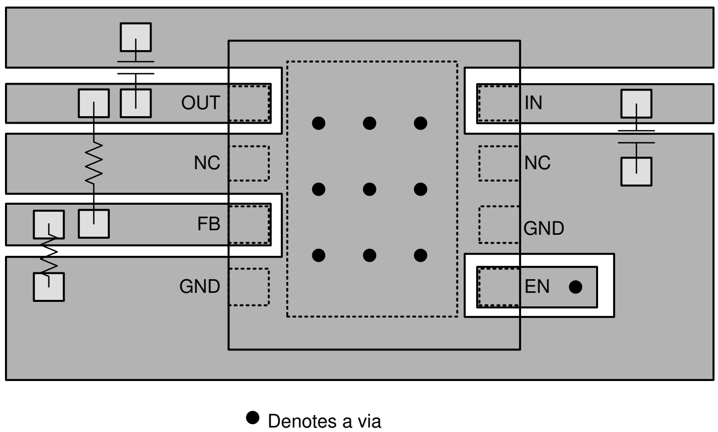


Figure 10-1. Layout Example for the Adjustable Version

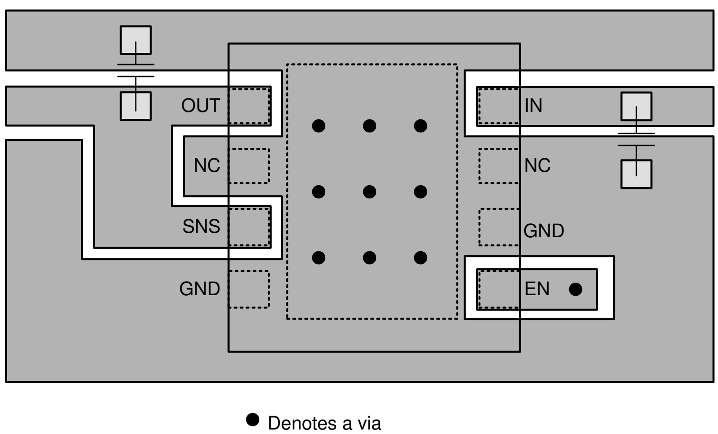


Figure 10-2. Layout Example for the Fixed Version

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Table 11-1. Available Options (1)

PRODUCT	V_{OUT}
TLV767**xx(x)QWyyyRQ1**	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 33 = 3.3 V; 125 = 1.25 V). 01 indicates the adjustable output version. **W** indicates a wettable flanks package. **yyy** is the package designator. **R** is the package quantity. R is for the large quantity reel.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TLV767EVM-014 Evaluation Module* user's guide
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application report
- Texas Instruments, *Know Your Limits* application report
- Texas Instruments, *Universal Low-Dropout (LDO) Linear Voltage Regulator MultiPkgLDOEVM-823 Evaluation Module* user's guide

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV76701QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76701
TLV76701QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76701
TLV76733QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76733
TLV76733QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76733
TLV76750QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76750
TLV76750QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76750
TLV76760QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76760
TLV76760QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76760
TLV76780QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76780
TLV76780QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76780
TLV76790QWDRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76790
TLV76790QWDRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	V76790

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV767-Q1 :

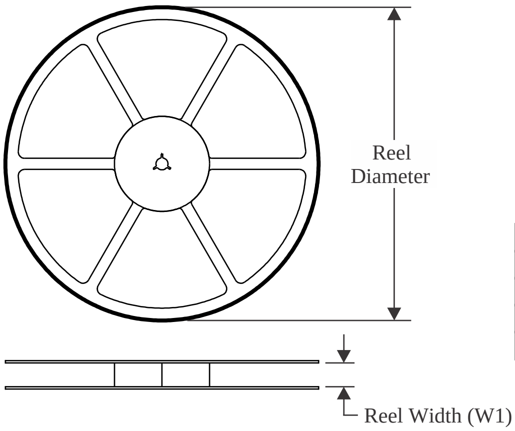
- Catalog : TLV767

NOTE: Qualified Version Definitions:

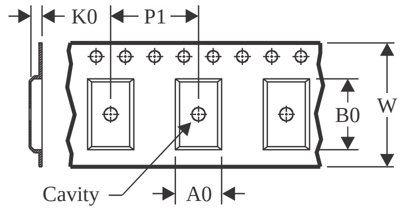
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

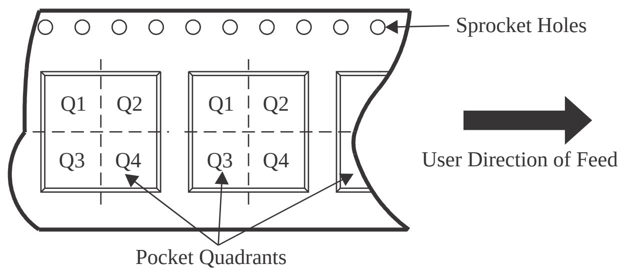


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

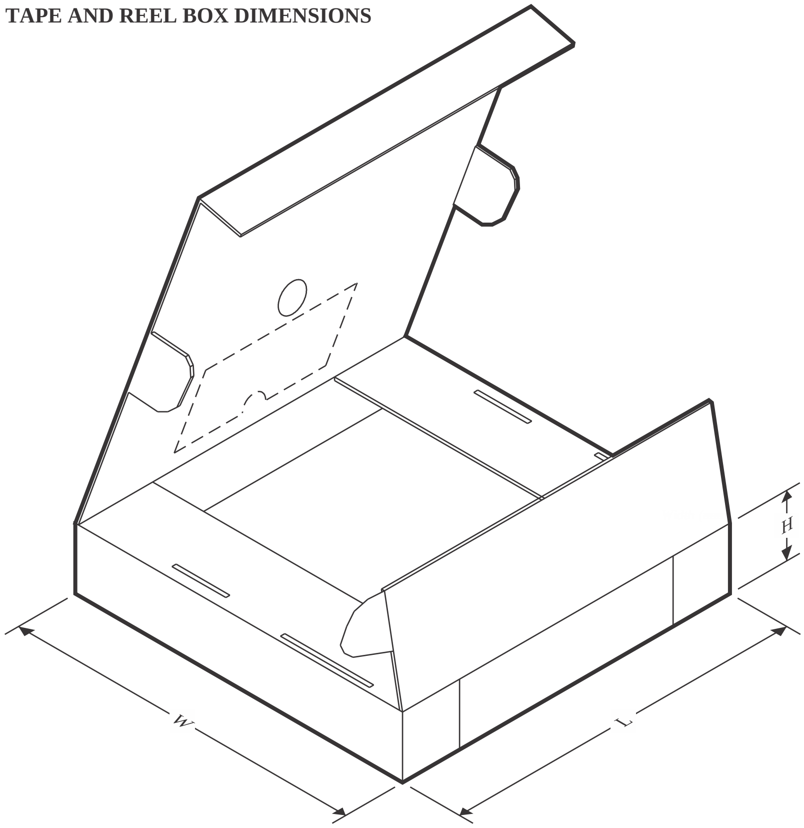
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV76701QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV76733QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV76750QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV76760QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV76780QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV76790QWDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

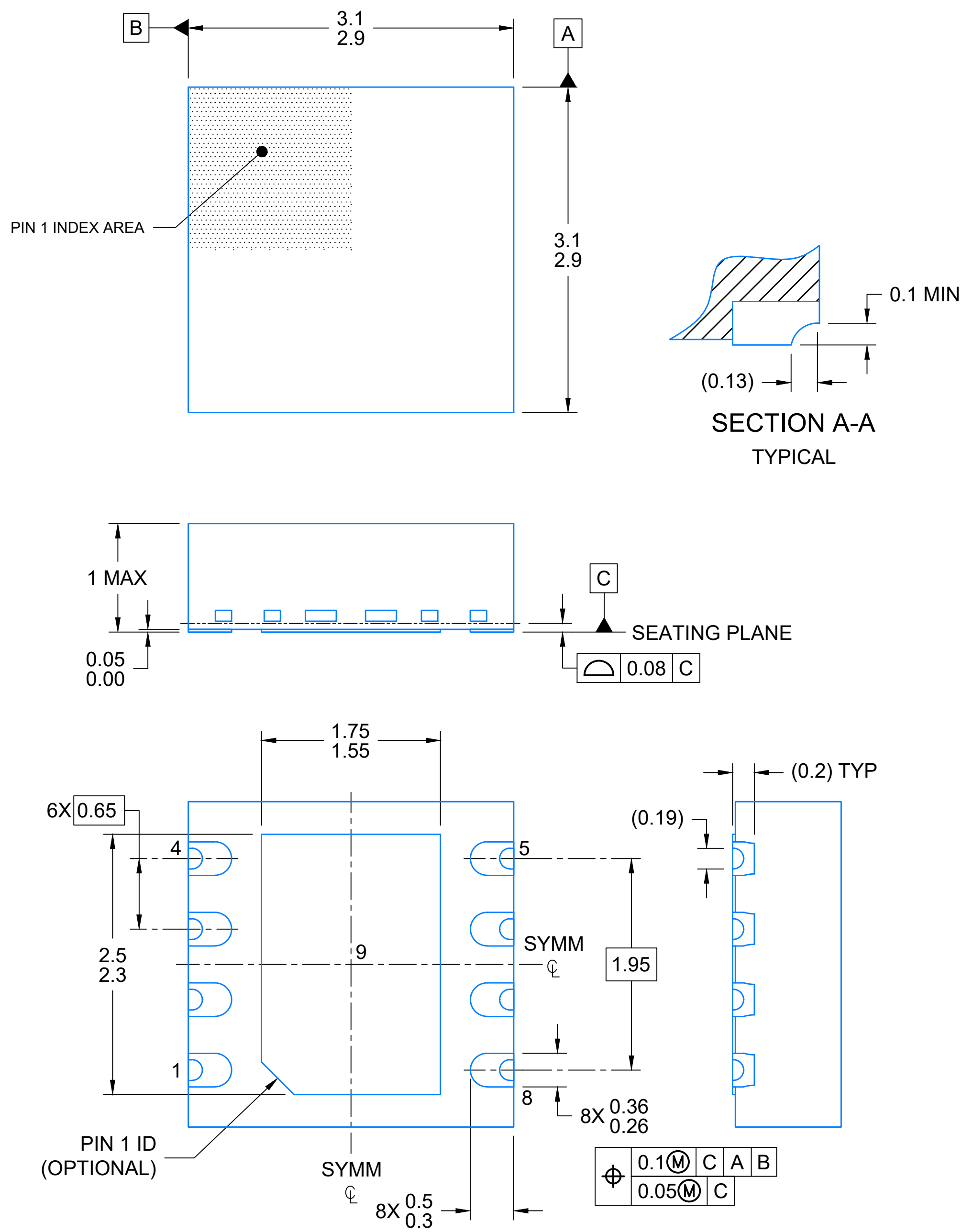
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV76701QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLV76733QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLV76750QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLV76760QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLV76780QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLV76790QWDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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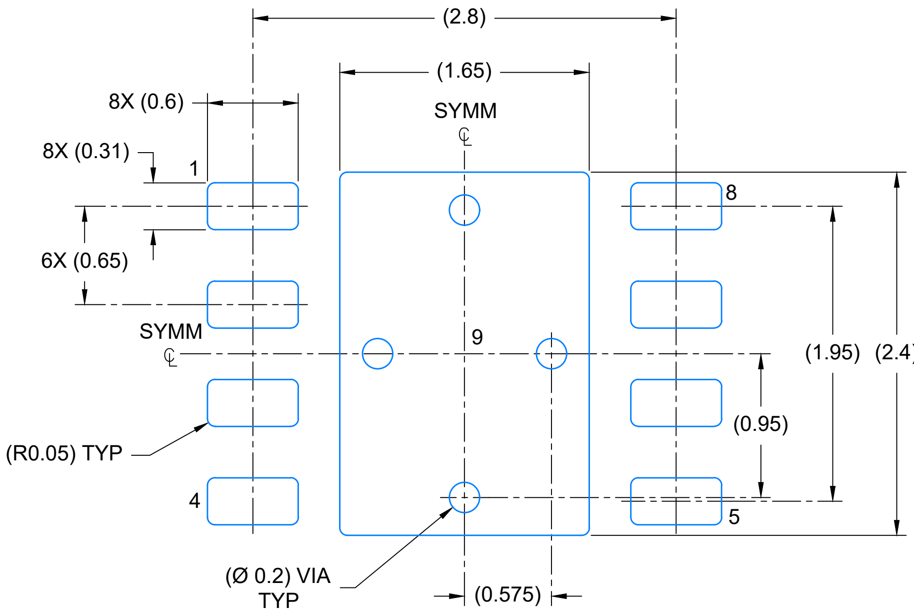
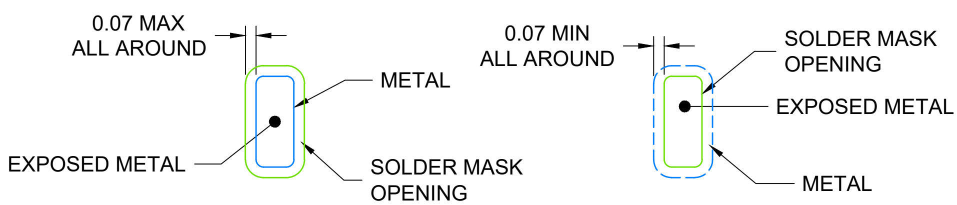
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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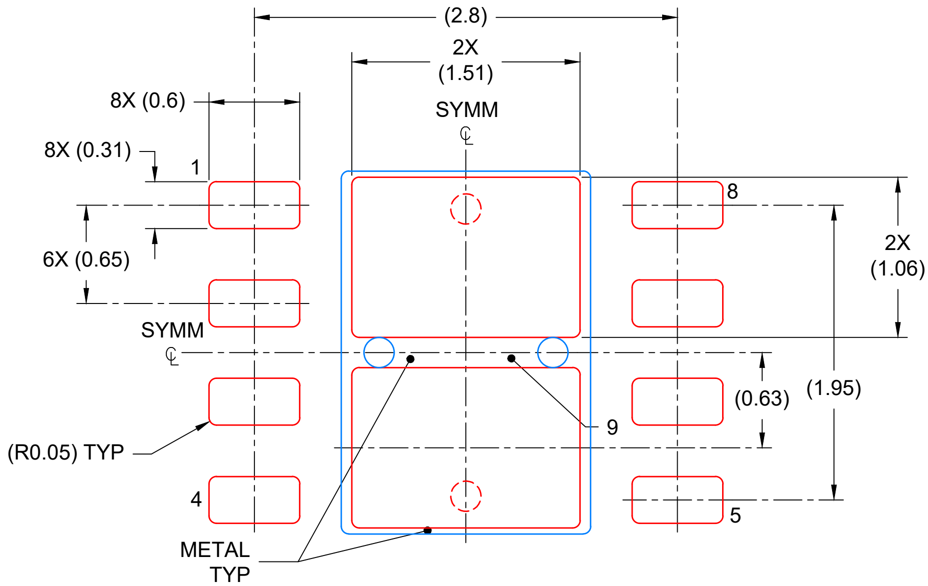
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.