





TLV758P SBVS351D - APRIL 2018 - REVISED OCTOBER 2023

# TLV758P 500-mA, High-Accuracy, Adjustable LDO in a Small Size Package

#### 1 Features

- Input voltage range: 1.5 V to 6.0 V
- Adjustable output voltage:
  - 0.55 V to 5.5 V
- Low dropout:
  - 130 mV (max) at 500 mA (3.3 V<sub>OUT</sub>)
- High output accuracy: 0.7% (typical) and 1% (maximum over temperature)
- I<sub>O</sub>: 25 μA (typical)
- Built-in soft-start with monotonic V<sub>OUT</sub> rise
- Packages:
  - 2-mm × 2-mm WSON-6 (DRV)
  - SOT23-5 (DBV)
- Active output discharge

# 2 Applications

- Gaming consoles
- Home theaters and entertainment
- PC and notebooks
- Connected peripherals and printers
- Rack and server power
- **Thermostats**
- Retail automation and payment

# 3 Description

The TLV758P is an adjustable 500-mA low-dropout (LDO) regulator. This device is available in a small, 6-pin, 2-mm × 2-mm WSON package and a 5-pin SOT23 package and consumes very low quiescent current and provides fast line and load transient performance. The TLV758P features an ultra-low dropout of 130 mV at 500 mA that can help improve the power efficiency of the system.

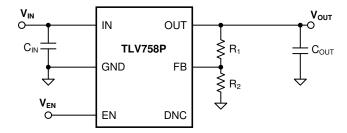
The TLV758P is optimized for a wide variety of applications by supporting an input voltage range from 1.5 V to 6.0 V and an externally adjustable output range of 0.55 V to 5.5 V. The low output voltage enables this LDO to power the modern microcontrollers with lower core voltages.

The TLV758P is stable with small ceramic output capacitors, allowing for a small overall solution size. A precision band-gap and error amplifier provides high accuracy of 0.7% (max) at 25°C and 1% (max) over temperature (85°C). This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TLV758P has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

#### **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TLV758P	DRV (WSON, 6)	2 mm × 2 mm
TLV758P	DBV (SOT-23, 5)	2.9 mm × 2.8 mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



**Typical Application** 

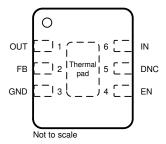


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# **4 Pin Configuration and Functions**



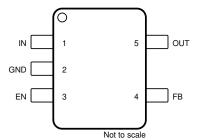


Figure 4-1. DRV Package, 6-Pin Adjustable WSON Figure 4-2. DBV Package, 5-Pin Adjustable SOT-23 (Top View) (Top View)

**Table 4-1. Pin Functions** 

PI	N	1/0	DESCRIPTION
NAME	ME NO.		DESCRIPTION
DNC	5	_	Do not connect
EN	4	Input	Enable pin. Drive EN greater than $V_{\text{EN(HI)}}$ to turn on the regulator. Drive EN less than $V_{\text{EN(LO)}}$ to put the LDO into shutdown mode.
FB	2	_	This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO.
GND	3	_	Ground pin
IN	6	Input	Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the Recommended Operating Conditions table and the Input and Output Capacitor Selection section. Place the input capacitor as close to the output of the device as possible.
OUT	1	Output	Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the <i>Recommended Operating Conditions</i> table and the <i>Input and Output Capacitor Selection</i> section. Place the output capacitor as close to output of the device as possible.
Thermal pad	Pad	_	Connect the thermal pad to a large area GND plane for improved thermal performance.



# **5 Specifications**

# 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply, V <sub>IN</sub>	-0.3	6.5	
Voltage Temperature	Enable, V <sub>EN</sub>	-0.3	6.5	V
	Feedback, V <sub>FB</sub>	-0.3	2	v
	Output, V <sub>OUT</sub>	-0.3	V <sub>IN</sub> + 0.3 <sup>(2)</sup>	
	Operating junction, T <sub>J</sub>	-40	150	°C
	Storage, T <sub>stg</sub>	-65	150	C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The absolute maximum rating is  $V_{IN}$  + 0.3V or 6.5 V, whichever is smaller.

# 5.2 ESD Ratings

			VALUE	UNIT
\ <u>\</u>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		V
V <sub>(ESD)</sub>	Liectiostatic discriarge	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	, v

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

# **5.3 Recommended Operating Conditions**

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM MAX	UNIT
V <sub>IN</sub>	Input voltage	1.5	6.0	V
V <sub>OUT</sub>	Output voltage	0.55	5.5	V
I <sub>OUT</sub>	Output current	0	500	mA
C <sub>IN</sub>	Input capacitor	1		μF
C <sub>OUT</sub>	Output capacitor <sup>(1)</sup>	1	220	μF
V <sub>EN</sub>	Enable voltage <sup>(2)</sup>	0	6.0	V
f <sub>EN</sub>	Enable toggle frequency		10	kHz
T <sub>J</sub>	Junction temperature	-40	125	°C

<sup>(1)</sup> Minimum derated capacitance of 0.47 µF is required for stability.

# **5.4 Thermal Information**

		TLV758P			
	THERMAL METRIC(1)	DBV (SOT-23)	DRV (WSON)	UNIT	
		5 PINS	6 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.9	80.3	°C/W	
R <sub>0JC(top)</sub>	Junction-to-case (top) thermal resistance	95.3	98.7	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	45.0	44.8	°C/W	
ΨЈТ	Junction-to-top characterization parameter	21.0	6.1	°C/W	
ΨЈВ	Junction-to-board characterization parameter	44.8	45.0	°C/W	
R <sub>0JC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	20.8	°C/W	

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

<sup>(2)</sup> If V<sub>EN</sub> > V<sub>IN</sub>, when V<sub>EN</sub> > V<sub>UVLO</sub> rising (min), the input pin (IN) must sink 1 mA of current to avoid the device being turn on with floating input pin.



#### 5.5 Electrical Characteristics

at operating temperature range ( $T_J$  =  $-40^{\circ}$ C to +125°C),  $V_{IN}$  =  $V_{OUT(NOM)}$  + 0.5 V or 1.5 V (whichever is greater),  $I_{OUT}$  = 1 mA,  $V_{EN}$  =  $V_{IN}$ , and  $C_{IN}$  =  $C_{OUT}$  = 1  $\mu$ F (unless otherwise noted); all typical values are at  $T_J$  = 25°C

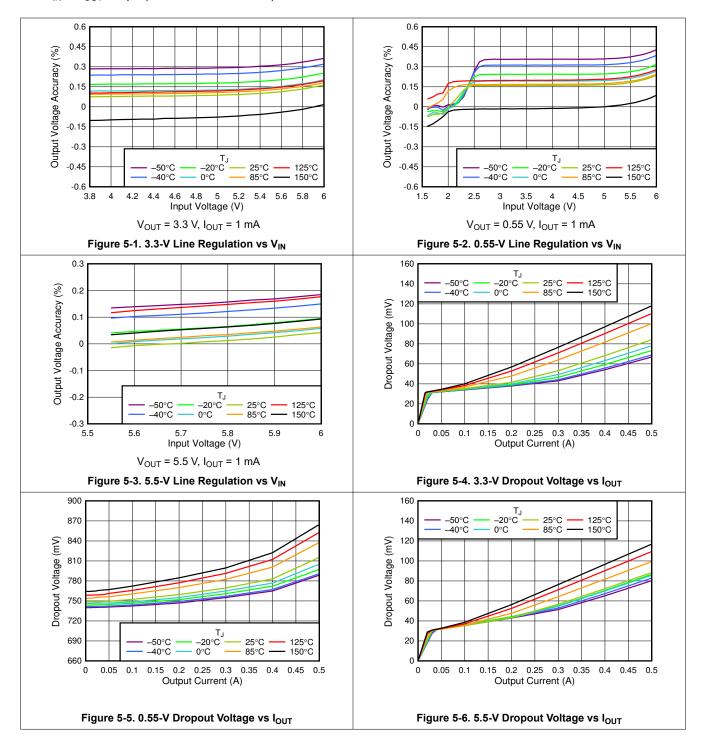
	PARAMETER	TEST	MIN	TYP	MAX	UNIT		
V <sub>FB</sub>	Feedback voltage	T <sub>J</sub> = 25°C			0.55		V	
		T <sub>J</sub> = 25°C		-0.7%		0.7%		
	Output accuracy <sup>(1)</sup>	-40°C ≤ T <sub>J</sub> ≤ +85°C		-1%		1%		
		-40°C ≤ T <sub>J</sub> ≤ +125°C	-1.5%		1.5%			
	Line regulation	$V_{OUT(NOM)} + 0.5 V^{(2)} \le V_{I N} \le$	6.0 V		2	7.5	mV	
	Load regulation	0.1 mA ≤ I <sub>OUT</sub> ≤ 500 mA, V <sub>IN</sub>	≥ 2.0 V		0.030		V/A	
I <sub>GND</sub>	Ground current		T <sub>J</sub> = 25°C	10	25	31	μA	
I <sub>GND</sub>	Ground current	I <sub>OUT</sub> = 0 mA	-40°C ≤ T <sub>J</sub> ≤ +125°C			35	μA	
I <sub>SHDN</sub>	Shutdown current	$V_{EN} \le 0.3 \text{ V}, 1.5 \text{ V} \le V_{IN} \le 6.0$	V		0.1	1	μΑ	
I <sub>FB</sub>	Feedback pin current				0.01	0.1	μA	
I	Output current limit	V <sub>IN</sub> = V <sub>OUT(NOM)</sub> + 1.0 V	$V_{OUT} = V_{OUT(NOM)} - 0.2 \text{ V},$ $V_{OUT} < 1.5 \text{ V}$	530	720	865		
I <sub>CL</sub>	Output current minit	VIN - VOUT(NOM) + 1.0 V	$V_{OUT} = 0.9 \text{ V} \times V_{OUT(NOM)},$ $V_{OUT} \ge 1.5 \text{ V}$	530	720	865	mA	
I <sub>SC</sub>	Short-circuit current limit	$V_{IN} = V_{OUT(NOM)} + 1.0 V$	V <sub>OUT</sub> = 0 V		350		mA	
		$I_{OUT} = 500 \text{ mA},$ $-40^{\circ}\text{C} \le \text{T}_{J} \le +125^{\circ}\text{C},$ $V_{OUT} = 0.95 \times V_{OUT(NOM)}$	$0.65 \text{ V} \leq \text{V}_{\text{OUT}} < 0.8 \text{ V}$		720	880		
	Dropout voltage		$0.8 \text{ V} \le \text{V}_{\text{OUT}} < 1.0 \text{ V}$		585	750		
			1.0 V ≤ V <sub>OUT</sub> < 1.2 V		420	570	mV	
$V_{DO}$			1.2 V ≤ V <sub>OUT</sub> < 1.5 V		285	400		
			1.5 V ≤ V <sub>OUT</sub> < 1.8 V		180	235		
		, ,	1.8 V ≤ V <sub>OUT</sub> < 2.5 V		140	185		
			2.5 V ≤ V <sub>OUT</sub> < 3.3 V		102	140		
			3.3 V ≤ V <sub>OUT</sub> ≤ 5.5 V		95	130		
			f = 1 kHz		50		dB	
PSRR	Power-supply rejection ratio	jection ratio $ V_{IN} = V_{OUT(NOM)} + 1.0 \text{ V}, $ $I_{OUT} = 50 \text{ mA} $	f = 100 kHz		45			
			f = 1 MHz		30			
V <sub>n</sub>	Output noise voltage	BW = 10 Hz to 100 kHz, V <sub>OU</sub>	<sub>T</sub> = 0.9 V		53		$\mu V_{RMS}$	
.,	11	V <sub>IN</sub> rising		1.21	1.33	1.47	V	
V <sub>UVLO</sub>	Undervoltage lockout	V <sub>IN</sub> falling		1.17	1.29	1.42	V	
V <sub>UVLO,</sub> HYST	Undervoltage lockout hysteresis	V <sub>IN</sub> Hysteresis			40		mV	
t <sub>STR</sub>	Start-up time	From EN low-to-high transition	n to V <sub>OUT</sub> = V <sub>OUT(NOM)</sub> × 95%		500		μs	
V <sub>EN(HI)</sub>	EN pin high voltage			1.0			V	
V <sub>EN(LO)</sub>	EN pin low voltage					0.3	V	
I <sub>EN</sub>	Enable pin current	V <sub>IN</sub> = EN = 6.0 V			10		nA	
R <sub>PULL</sub>	Pulldown resistance	V <sub>IN</sub> = 6.0 V			95		Ω	
<b>-</b>	Thormal shutda	Shutdown, temperature incre	asing		170		•••	
$T_{SD}$	Thermal shutdown	Reset, temperature decreasing	ng		155		°C	

<sup>(1)</sup> When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included

<sup>(2)</sup>  $V_{IN} = 1.5 \text{ V for } V_{OUT} < 1.0 \text{ V}.$ 

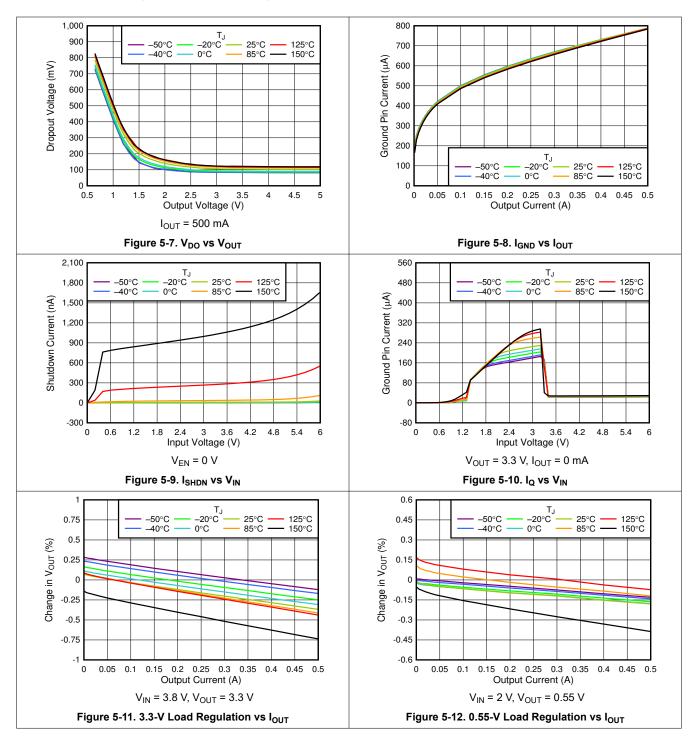
## **5.6 Typical Characteristics**

at operating temperature range  $T_J = 25^{\circ}C$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5 \text{ V}$  or 1.5 V (whichever is greater),  $I_{OUT} = 1 \text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1 \mu F$  (unless otherwise noted)





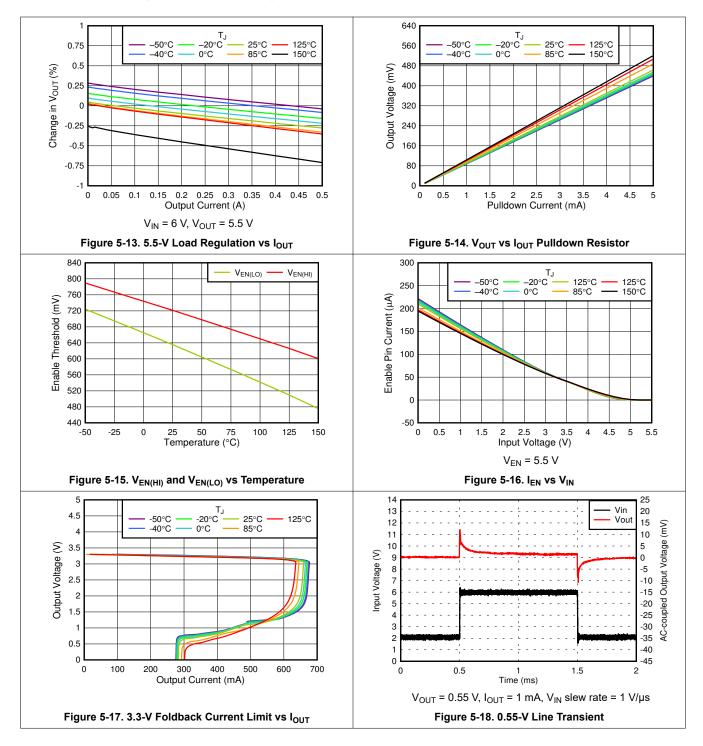
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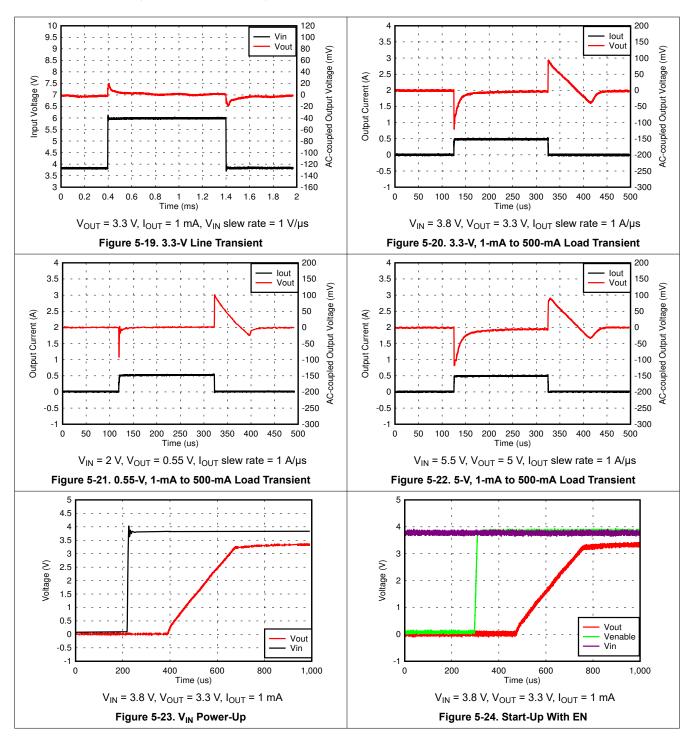
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at operating temperature range  $T_J = 25^{\circ}C$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5 \text{ V}$  or 1.5 V (whichever is greater),  $I_{OUT} = 1 \text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1 \mu F$  (unless otherwise noted)





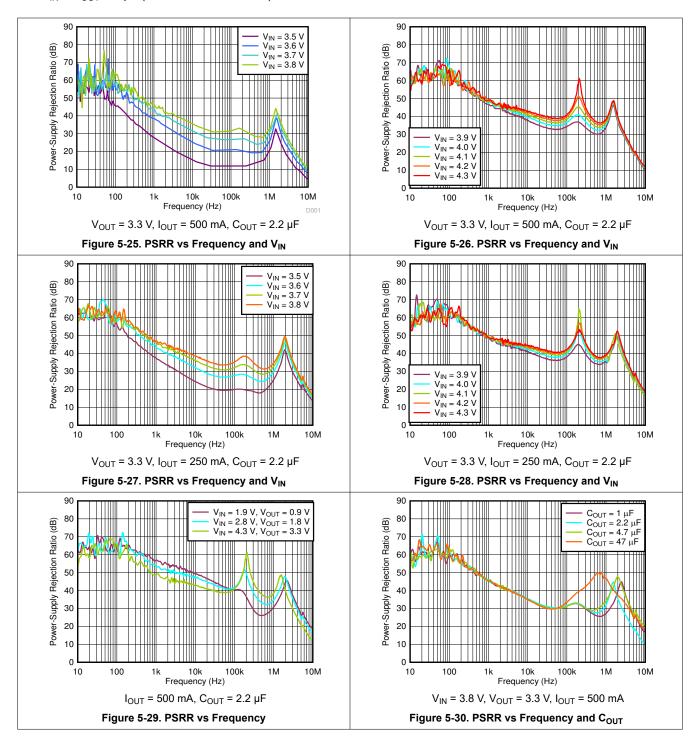
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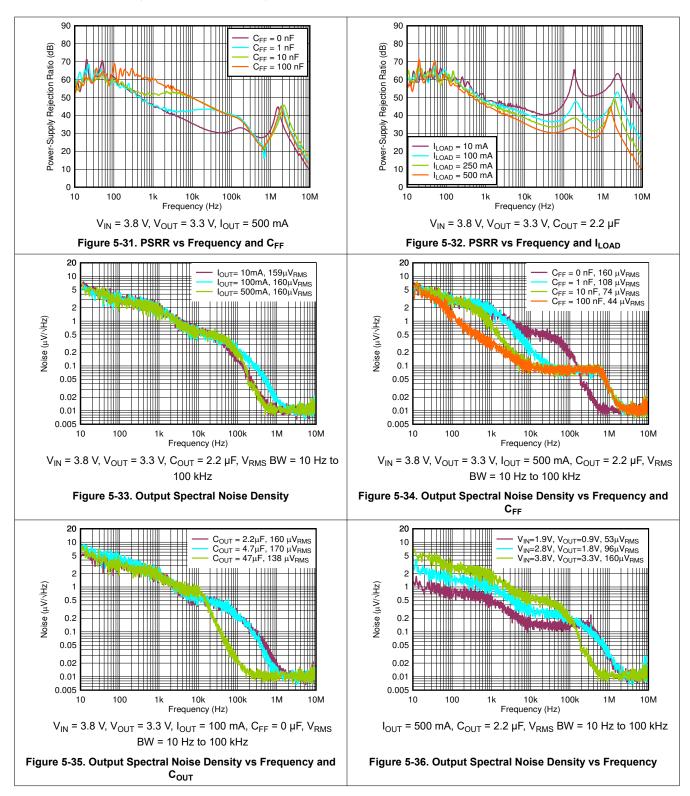


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at operating temperature range  $T_J = 25^{\circ}C$ ,  $V_{IN} = V_{OUT(NOM)} + 0.5 \text{ V}$  or 1.5 V (whichever is greater),  $I_{OUT} = 1 \text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 1 \mu F$  (unless otherwise noted)



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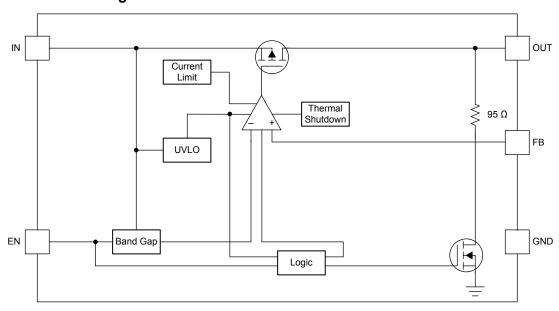
# **6 Detailed Description**

#### 6.1 Overview

The TLV758P low-dropout regulators (LDO) consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device designed for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is -40°C to +125°C.

#### 6.2 Functional Block Diagram



#### **6.3 Feature Description**

#### 6.3.1 Undervoltage Lockout (UVLO)

The TLV758P uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage ( $V_{UVLO}$ ). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When  $V_{IN}$  is less than  $V_{UVLO}$ , the output is connected to ground with a pulldown resistor ( $R_{PULLDOWN}$ ).

#### 6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed  $V_{EN(HI)}$ . Turn off the device by forcing the EN pin to drop below  $V_{EN(I,O)}$ . If shutdown capability is not required, connect EN to IN.

The TLV758P has an internal pulldown MOSFET that connects an  $R_{PULLDOWN}$  resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance ( $C_{OUT}$ ) and the load resistance ( $R_L$ ) in parallel with the pulldown resistor ( $R_{PULLDOWN}$ ). Equation 1 calculates the time constant:

$$T = (R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L)$$
(1)

#### 6.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ( $V_{FOLDBACK}$ ). In a high-load current fault with the output voltage above  $V_{FOLDBACK}$ , the brick-wall scheme limits the output current to the current limit ( $I_{CL}$ ). When the voltage drops below  $V_{FOLDBACK}$ , a foldback current limit activates that scales back the current as the

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output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ( $I_{SC}$ ).  $I_{CL}$  and  $I_{SC}$  are listed in the *Electrical Characteristics* table.

For this device,  $V_{FOLDBACK} = 0.4 \text{ V} \times V_{OUT(NOM)}$ .

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{CL}]$ . When the device output is shorted and the output is below  $V_{FOLDBACK}$ , the pass transistor dissipates power  $[(V_{IN} - V_{OUT}) \times I_{SC}]$ . If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

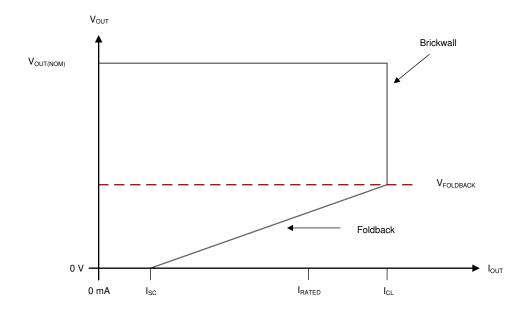


Figure 6-1. Foldback Current Limit

#### 6.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the  $(V_{IN} - V_{OUT})$  voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV758P internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TLV758P into thermal shutdown degrades device reliability.

#### 6.4 Device Functional Modes

#### 6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 6-1. Device Functional Mode Comparison** 

OPERATING MODE	PARAMETER						
OPERATING MODE	V <sub>IN</sub>	V <sub>EN</sub>	I <sub>OUT</sub>	T <sub>J</sub>			
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	V <sub>EN</sub> > V <sub>EN(HI)</sub>	$I_{OUT} < I_{OUT(max)}$	T <sub>J</sub> < T <sub>SD(shutdown)</sub>			
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	V <sub>EN</sub> > V <sub>EN(HI)</sub>	I <sub>OUT</sub> < I <sub>OUT(max)</sub>	$T_J < T_{SD(shutdown)}$			
Disabled (any true condition disables the device)	V <sub>IN</sub> < V <sub>UVLO</sub>	V <sub>EN</sub> < V <sub>EN(LOW)</sub>	Not applicable	$T_{J} > T_{SD(shutdown)}$			

#### 6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage (V<sub>OUT(nom)</sub> + V<sub>DO</sub>)
- The output current is less than the current limit (I<sub>OUT</sub> < I<sub>CL</sub>)
- The device junction temperature is less than the thermal shutdown temperature (T<sub>J</sub> < T<sub>SD</sub>)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

#### 6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout,  $V_{IN} < V_{OUT(NOM)} + V_{DO}$ , directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ( $V_{OUT(NOM)} + V_{DO}$ ), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

#### 6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

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Product Folder Links: TLV758P

# 7 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Application Information

#### 7.1.1 Adjustable Device Feedback Resistors

Figure 7-1 shows that the output voltage of the TLV758P can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

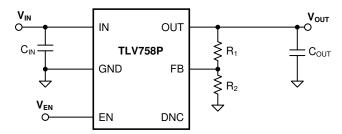


Figure 7-1. Adjustable Operation

The adjustable-version device requires external feedback divider resistors to set the output voltage. V<sub>OUT</sub> is set using the feedback divider resistors, R<sub>1</sub> and R<sub>2</sub>, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2)$$
 (2)

For this device,  $V_{FB} = 0.55 \text{ V}$ .

To ignore the FB pin current error term in the V<sub>OUT</sub> equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \le V_{OLIT} / (I_{FB} \times 100)$$
 (3)

For this device,  $I_{FR} = 10 \text{ nA}$ .

#### 7.1.2 Input and Output Capacitor Selection

The TLV758P requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

#### 7.1.3 Dropout Voltage

The TLV758P uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage  $(V_{DO})$ , the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass transistor.  $V_{DO}$  scales approximately with output current because the PMOS pass transistor behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as  $(V_{IN} - V_{OUT})$  approaches dropout operation.

# 7.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on  $V_{IN}$  during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 7-2, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

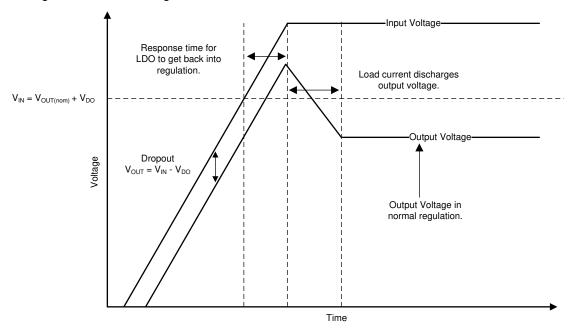


Figure 7-2. Start-Up Into Dropout

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass transistor and bring the gate back to the correct voltage for proper regulation. Figure 7-3 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass transistor the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.



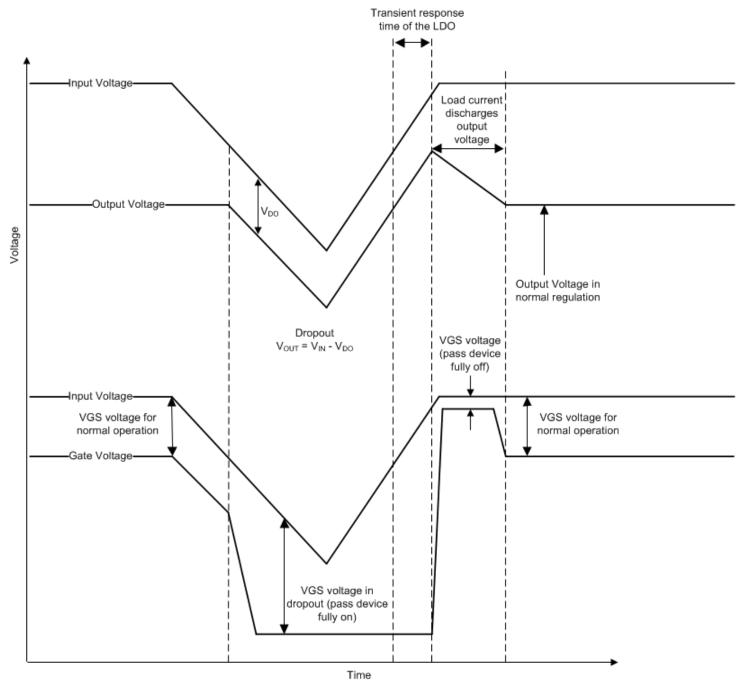


Figure 7-3. Line Transients From Dropout

#### 7.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- · Degradation caused by electromigration
- · Excessive heat dissipation
- · Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of  $V_{OUT} > V_{IN} + 0.3 \text{ V}$ :

- If the device has a large C<sub>OLIT</sub> and the input supply collapses with little or no load current
- · The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 7-4 shows one approach of protecting the device.

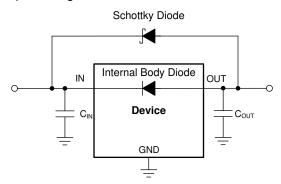


Figure 7-4. Example Circuit for Reverse Current Protection Using a Schottky Diode

#### 7.1.6 Power Dissipation (P<sub>D</sub>)

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Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation (P<sub>D</sub>).

$$P_{D} = (V_{IN} - V_{OUT}) \times I_{OUT}$$
(4)

#### Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ( $T_A$ ) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) of the combined PCB and device package and the temperature of the ambient air ( $T_A$ ).



$$T_{J} = T_{A} + (R_{\theta JA} \times P_{D}) \tag{5}$$

Thermal resistance ( $R_{\theta JA}$ ) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

#### 7.1.7 Feed-Forward Capacitor (CFF)

For the adjustable-voltage version device, a feed-forward capacitor ( $C_{FF}$ ) can be connected from the OUT pin to the FB pin.  $C_{FF}$  improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended  $C_{FF}$  values are listed in the *Recommended Operating Conditions* table. A higher capacitance  $C_{FF}$  can be used; however, the start-up time increases. For a detailed description of  $C_{FF}$  tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

## 7.1.8 Start-Up Sequencing

If  $V_{EN}$  is greater than  $V_{UVLO}$  rising (min), then the input pin (IN) must sink 1 mA of current to avoid the device being turn on with a floating input pin.

Product Folder Links: TLV758P

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## 7.2 Typical Application

Figure 7-5 shows the typical application circuit for the TLV758P. Input and output capacitances must be at least 1  $\mu$ F.

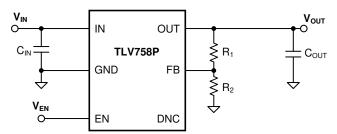


Figure 7-5. TLV758P Typical Application

#### 7.2.1 Design Requirements

Use the parameters listed in Table 7-1 for typical linear regulator applications.

 PARAMETER
 DESIGN REQUIREMENT

 Input voltage
 3.8 V

 Output voltage
 3.3 V, ±1%

 Input current
 500 mA (maximum)

 Output load
 500-mA DC

 Maximum ambient temperature
 70°C

Table 7-1. Design Parameters

# 7.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2  $\mu$ F are selected to give the maximum output capacitance in a small, low-cost package; see the *Input and Output Capacitor Selection* section for details.

Figure 7-1 illustrates the output voltage of the TLV758P; set the output voltage using the resistor divider.

#### 7.2.2.1 Input Current

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During start-up, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 6 to calculate the current through the input.

$$I_{OUT(t)} = \left(\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right) + \left(\frac{V_{OUT}(t)}{R_{LOAD}}\right)$$
(6)

#### where:

- V<sub>OLIT</sub>(t) is the instantaneous output voltage of the turn-on ramp
- dV<sub>OUT</sub>(t) / dt is the slope of the V<sub>OUT</sub> ramp
- R<sub>LOAD</sub> is the resistive load impedance

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#### 7.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ( $R_{\theta JA}$ ) and the total power dissipation ( $P_D$ ). Use Equation 7 to calculate the power dissipation. Multiply  $P_D$  by  $R_{\theta JA}$  as Equation 8 shows and add the ambient temperature ( $T_A$ ) to calculate the junction temperature ( $T_J$ ).

$$P_{D} = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \tag{7}$$

$$T_{J} = R_{\theta,JA} \times P_{D} + T_{A} \tag{8}$$

Calculate the maximum ambient temperature as Equation 9 shows if the  $(T_{J(MAX)})$  value does not exceed 125°C. Equation 10 calculates the maximum ambient temperature with a value of 104.93°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_{D} \tag{9}$$

$$T_{A(MAX)} = 125^{\circ}C - 80.3^{\circ}C/W \times (3.8 \text{ V} - 3.3 \text{ V}) \times (0.5 \text{ A}) = 104.93^{\circ}C$$
 (10)

# 7.2.3 Application Curve

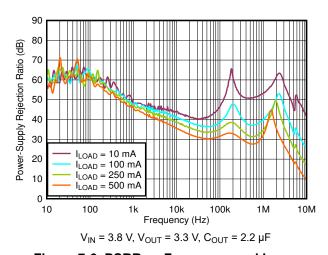


Figure 7-6. PSRR vs Frequency and I<sub>LOAD</sub>

#### 7.3 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV758P.

#### 7.4 Layout

## 7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

# 7.4.2 Layout Examples

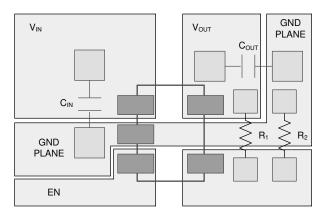


Figure 7-7. DBV Package Layout Example

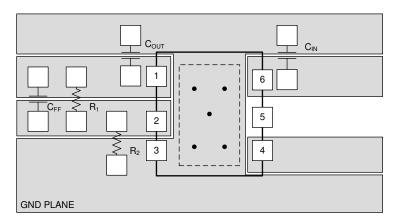


Figure 7-8. DRV Package Layout Example



# 8 Device and Documentation Support

# 8.1 Documentation Support

#### 8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature(1)

PRODUCT	V <sub>OUT</sub>
TLV758 xx(x)Pyyyz	<ul> <li>xx(x) is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). 01 is for adjustable version.</li> <li>P indicates an active output discharge feature. All members of the TLV758P family actively discharge the output when the device is disabled.</li> <li>yyy is the package designator.</li> <li>z is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).</li> </ul>

<sup>(1)</sup> For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

#### 8.1.2 Related Documentation

For related documentation see the following:

Texas Instruments, Pros and cons of using a feedforward capacitor with a low-dropout regulator application note

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 8.4 Trademarks

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#### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 8.6 Glossary

TI Glossary

24

This glossary lists and explains terms, acronyms, and definitions.



# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

, , , , , , , , , , , , , , , , , , , ,	Page
Changed 5-V to 5.5-V in title of 5.5-V Load Regulation vs I <sub>OUT</sub> figure	7
Changes from Revision B (March 2019) to Revision C (March 2019)	Page
Deleted thermal pad from DBV pin out drawing	3

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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Product Folder Links: *TLV758P* 

www.ti.com 9-Nov-2025

#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
TLV75801PDBVJ	Active	Production	SOT-23 (DBV)   5	8000   JUMBO T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1UDF
TLV75801PDBVJ.A	Active	Production	SOT-23 (DBV)   5	8000   JUMBO T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1UDF
TLV75801PDBVR	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	Call TI   Sn   Nipdau	Level-1-260C-UNLIM	-40 to 125	1UDF
TLV75801PDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1UDF
TLV75801PDBVT	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	Call TI   Sn   Nipdau	Level-1-260C-UNLIM	-40 to 125	1UDF
TLV75801PDBVT.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1UDF
TLV75801PDRVR	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MHH
TLV75801PDRVR.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MHH
TLV75801PDRVRG4	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MHH
TLV75801PDRVRG4.A	Active	Production	WSON (DRV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MHH
TLV75801PDRVT	Active	Production	WSON (DRV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MHH
TLV75801PDRVT.A	Active	Production	WSON (DRV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MHH

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# PACKAGE OPTION ADDENDUM

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# **PACKAGE MATERIALS INFORMATION**

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# TAPE AND REEL INFORMATION



# TAPE DIMENSIONS + K0 - P1 - B0 W Cavity - A0 -

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV75801PDBVJ	SOT-23	DBV	5	8000	330.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75801PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75801PDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV75801PDRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75801PDRVRG4	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV75801PDRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2



www.ti.com 5-Sep-2025



# \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV75801PDBVJ	SOT-23	DBV	5	8000	360.0	360.0	36.0
TLV75801PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV75801PDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV75801PDRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75801PDRVRG4	WSON	DRV	6	3000	210.0	185.0	35.0
TLV75801PDRVT	WSON	DRV	6	250	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4206925/F





PLASTIC SMALL OUTLINE - NO LEAD



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature
- number SLUA271 (www.ti.com/lit/slua271).

  5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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