













TLV741P SBVS309A - JULY 2017-REVISED SEPTEMBER 2018

TLV741P 150-mA, Low-Dropout Regulator With Foldback Current Limit

Features

Input Voltage Range: 1.4 V to 5.5 V

Stable Operation With 1-µF Ceramic Capacitors

Foldback Overcurrent Protection

Packages:

5-Pin SOT-23

4-Pin X2SON

Very Low Dropout: 230 mV at 150 mA

Accuracy: 1% Low Io: 50 µA

Available in Fixed-Output Voltages:

1 V to 3.3 V

High PSRR: 65 dB at 1 kHz

Active Output Discharge (P Version Only)

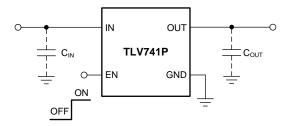
Applications

PDAs and Battery-Powered Portable Devices

MP3 Players and Other Hand-Held Products

WLAN and Other PC Add-On Cards

Typical Application Circuit



3 Description

The TLV741P low-dropout linear regulator (LDO) is a low guiescent current device with excellent line and load transient performance for power-sensitive applications. This device provides a typical accuracy of 1%.

The TLV741P is designed to be stable with a small, 1-µF output capacitor.

The TLV741P provides inrush current control during device power up and enabling. The TLV741P limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

The TLV741P is available in standard DBV (SOT-23) and DQN (X2SON) packages. The TLV741P provides an active pulldown circuit to quickly discharge output loads.

Device Information⁽¹⁾

DEVICE NAME	PACKAGE	BODY SIZE
TLV741P	SOT-23 (5)	2.90 mm × 1.60 mm
	X2SON (4)	1.00 mm × 1.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Dropout Voltage vs Output Current

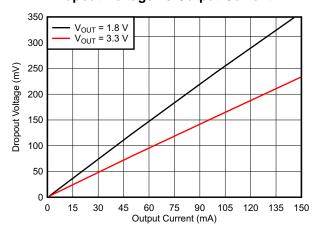




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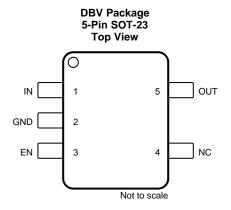
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4 Revision History

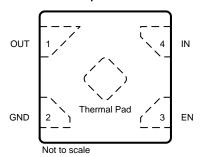
Changes from Original (July 2017) to Revision A			
• A	Added DQN (X2SON) package to data sheet		_ 1



5 Pin Configuration and Functions



DQN Package 4-Pin X2SON With Exposed Thermal Pad Top View



Pin Functions

	PIN			
NAME	NO.		1/0	DESCRIPTION
NAME	SOT-23	X2SON		
EN	3	3	1	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	2	_	Ground pin
IN	1	4	1	Input pin. Use a small capacitor from this pin to ground. See the <i>Input and Output Capacitor Considerations</i> section for more details.
NC	4	_	_	No internal connection
OUT	5	1	0	Regulated output voltage pin. For best transient response, use a small 1-µF ceramic capacitor from this pin to ground. See the <i>Input and Output Capacitor Considerations</i> section for more details.
Thermal pad	_	_	_	The thermal pad is electrically connected to the GND node. Connect the thermal pad to the ground plane for improved thermal performance.



6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted). All voltages are with respect to GND.⁽¹⁾

		MIN	MAX	UNIT
	Input, V _{IN}	-0.3	6	
Voltage	Enable, V _{EN}	-0.3	$V_{IN} + 0.3$	V
	Output, V _{OUT}	-0.3	3.6	
Current	Maximum output, I _{OUT(max)}	Internally limited		
Output short-circuit duration		Indefini	te	
Total power dissipation	Continuous, P _{D(tot)}	See Thermal In	nformation	
Tomporoturo	Junction, T _J	– 55	125	°C
Temperature	Storage, T _{stg}	– 55	150	• •

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	
V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.4		5.5	V
V _{EN}	Enable range	0		V _{IN}	V
I _{OUT}	Output current	0		150	mA
C _{IN}	Input capacitor	0	1		μF
C _{OUT}	Output capacitor	1		100	μF
T _J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

		TLV	TLV741P		
	THERMAL METRIC ⁽¹⁾	DQN (X2SON)	DBV (SOT-23)	UNIT	
		4 PINS	5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	249	°C/W	
R ₀ JC(top)	Junction-to-case (top) thermal resistance	210.4	172.7	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	174.7	76.7	°C/W	
ΨЈТ	Junction-to-top characterization parameter	21.2	49.7	°C/W	
ΨЈВ	Junction-to-board characterization parameter	174.5	75.8	°C/W	
R ₀ JC(bot)	Junction-to-case (bottom) thermal resistance	140.6	N/A	°C/W	

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.5 Electrical Characteristics

over operating temperature range $T_J = -40^{\circ}C$ to $+125^{\circ}C$, $V_{IN(nom)} = V_{OUT(nom)} + 0.5$ V or $V_{IN(nom)} = 2$ V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, and $C_{OUT} = 1$ μ F (unless otherwise noted). Typical values are at $T_J = 25^{\circ}C$.

PARAMETER		TE	TEST CONDITIONS		TYP	MAX	UNIT	
/ _{OUT}	Output voltage range			1		3.3	V	
		V _{OUT} ≥ 1.8 V T _J = 25°C		-1%		1%		
	DO suitsut session	V _{OUT} < 1.8 V T _J = 25°C		-20		20	mV	
	DC output accuracy	V _{OUT} ≥ 1.2 V -40°C ≤ T _J ≤ 125°C		-1.5%		1.5%		
		V _{OUT} < 1.2 V -40°C ≤ T _J ≤ 125°C		-50		50	mV	
V _{OUT(ΔVIN)}	Line regulation	Maximum $\{V_{OUT(nom)} + 0.5$ $V_{IN} = 2 \text{ V}\} \leq V_{IN} \leq 5.5 \text{ V}$	5 V		1	5	mV	
V _{OUT(ΔIOUT)}	Load regulation	0 mA ≤ I _{OUT} ≤ 150 mA			10	30	mV	
			$1 \text{ V} \le \text{V}_{\text{OUT}} < 1.8 \text{ V}$ $\text{I}_{\text{OUT}} = 150 \text{ mA}$		600	900		
			V _{OUT} = 1.1 V I _{OUT} = 100 mA		470	600		
			$1.8 \text{ V} \le \text{V}_{\text{OUT}} < 2.1 \text{ V}$ $\text{I}_{\text{OUT}} = 30 \text{ mA}$		70			
			$1.8 \text{ V} \le \text{V}_{\text{OUT}} < 2.1 \text{ V}$ $\text{I}_{\text{OUT}} = 150 \text{ mA}$		350	575		
V_{DO}	$V_{OUT} = 0.98 \times V_{OUT(nom)}$ $T_{J} = -40^{\circ}C \text{ to } 85^{\circ}C$ Dropout voltage $V_{OUT} = 0.98 \times V_{OUT(nom)}$ $T_{J} = -40^{\circ}C \text{ to } 125^{\circ}C$	Vo = 0.98 × Vo.	VOUT = 0.98 × VOUT(2000).	2.1 V ≤ V _{OUT} < 2.5 V I _{OUT} = 30 mA		90		
		$T_{\rm J} = -40^{\circ} {\rm C} \text{ to } 85^{\circ} {\rm C}$	2.1 V ≤ V _{OUT} < 2.5 V I _{OUT} = 150 mA		290	481	mV	
			2.5 V ≤ V _{OUT} < 3 V I _{OUT} = 30 mA		50			
			2.5 V ≤ V _{OUT} < 3 V I _{OUT} = 150 mA		246	445		
			3 V ≤ V _{OUT} < 3.6 V I _{OUT} = 30 mA		46			
			3 V ≤ V _{OUT} < 3.6 V I _{OUT} = 150 mA		230	420		
			1 V ≤ V _{OUT} < 1.8 V I _{OUT} = 150 mA		600	1020		
			V _{OUT} = 1.1 V I _{OUT} = 100 mA		470	720		
			Voux = 0.98 × Voux	1.8 V ≤ V _{OUT} < 2.1 V I _{OUT} = 150 mA		350	695	
		$T_J = -40^{\circ}\text{C} \text{ to } 125^{\circ}\text{C}$	2.1 V ≤ V _{OUT} < 2.5 V I _{OUT} = 150 mA		290	601		
			2.5 V ≤ V _{OUT} < 3 V I _{OUT} = 150 mA		246	565		
			3 V ≤ V _{OUT} < 3.6 V I _{OUT} = 150 mA		230	540		
GND	Ground pin current	I _{OUT} = 0 mA			50	75	μΑ	
SHUTDOWN	Shutdown current	$V_{EN} \le 0.4 \text{ V}, 2 \text{ V} \le V_{IN} \le 5$ $T_{J} = 25^{\circ}\text{C}$	i.5 V		0.1	1	μΑ	
		V _{IN} = 3.3 V	f = 100 Hz		70			
PSRR	R Power-supply V _{OUT} = 2.8 V	V _{OUT} = 2.8 V	f = 10 kHz		55		dB	
	3,2 2	I _{OUT} = 30 mA	f = 1 MHz		55			
n	Output noise voltage	BW = 100 Hz to 100 kHz V _{IN} = 2.3 V V _{OUT} = 1.8 V I _{OUT} = 10 mA			73		μV _{RM}	

⁽¹⁾ Start-up time is the time from EN assertion to (0.98 \times V_{OUT(nom)}).



Electrical Characteristics (continued)

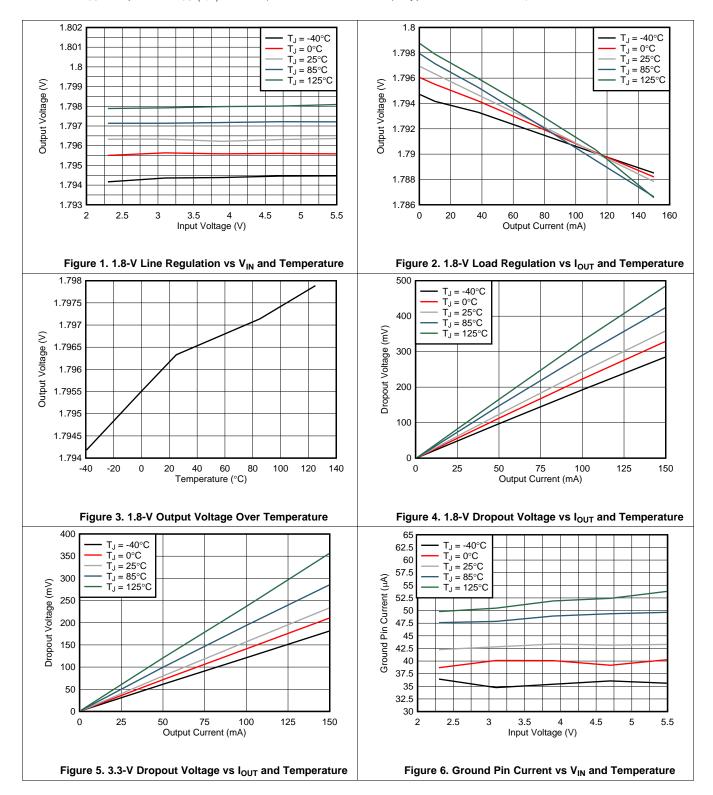
over operating temperature range $T_J = -40^{\circ}C$ to $+125^{\circ}C$, $V_{IN(nom)} = V_{OUT(nom)} + 0.5$ V or $V_{IN(nom)} = 2$ V (whichever is greater), $I_{OUT} = 1$ mA, $V_{EN} = V_{IN}$, and $C_{OUT} = 1$ μ F (unless otherwise noted). Typical values are at $T_J = 25^{\circ}C$.

P/	PARAMETER TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{HI}	Enable high (enabled)		0.9		V _{IN}	V	
V _{LO}	Enable low (disabled)		0		0.4	V	
I _{EN}	EN pin current	EN = 5.5 V		0.01		μA	
R _{PULLDOWN}	Pulldown resistor	V _{IN} = 4 V		120		Ω	
		$V_{IN} = 3.8 \text{ V}$ $V_{OUT} = 3.3 \text{ V}$ $T_{J} = -40 \text{ to } 85^{\circ}\text{C}$	180				
I _{LIM} Output	Output current limit	$V_{IN} = 2.25 \text{ V}$ $V_{OUT} = 1.8 \text{ V}$ $T_{J} = -40 \text{ to } 85^{\circ}\text{C}$	180			mA	
		$V_{IN} = 2 \text{ V}$ $V_{OUT} = 1.2 \text{ V}$ $T_{J} = -40 \text{ to } 85^{\circ}\text{C}$	180				
I _{SC}	Short-circuit current	V _{OUT} = 0 V		40		mA	
	T	Shutdown, temperature increasing	158				
T _{SD} Thermal shutdown		Reset, temperature decreasing		140		°C	



6.6 Typical Characteristics

over operating temperature range $T_J = -40^{\circ}\text{C}$ to +125°C, $V_{IN} = V_{OUT(nom)} + 0.5 \text{ V}$ or 2 V (whichever is greater), $I_{OUT} = 10 \text{ mA}$, $V_{EN} = V_{IN}$, $C_{OUT} = 1 \mu\text{F}$, and $V_{OUT(nom)} = 1.8 \text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

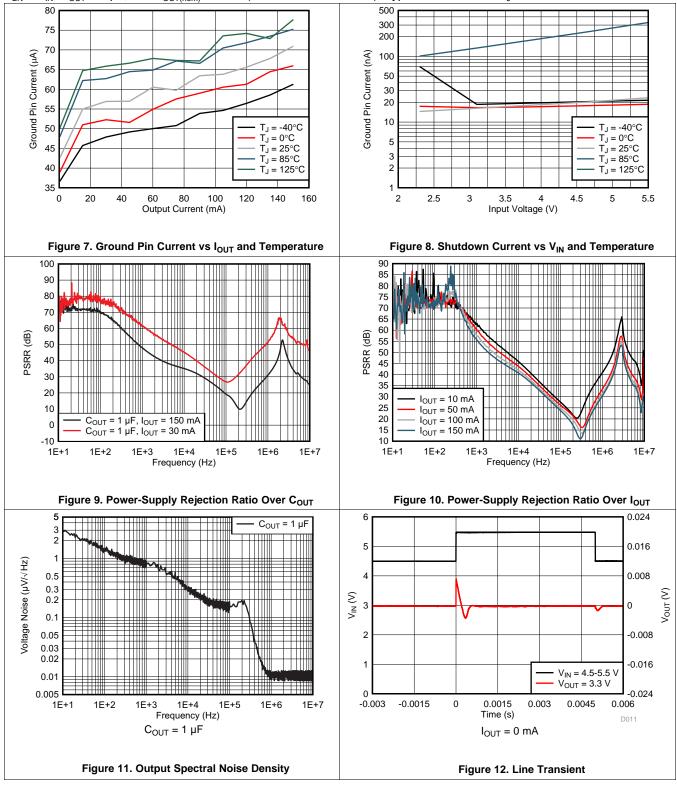


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Typical Characteristics (continued)

over operating temperature range $T_J = -40^{\circ}C$ to +125°C, $V_{IN} = V_{OUT(nom)} + 0.5$ V or 2 V (whichever is greater), $I_{OUT} = 10$ mA, $V_{EN} = V_{IN}$, $C_{OUT} = 1$ µF, and $V_{OUT(nom)} = 1.8$ V (unless otherwise noted). Typical values are at $T_J = 25^{\circ}C$.



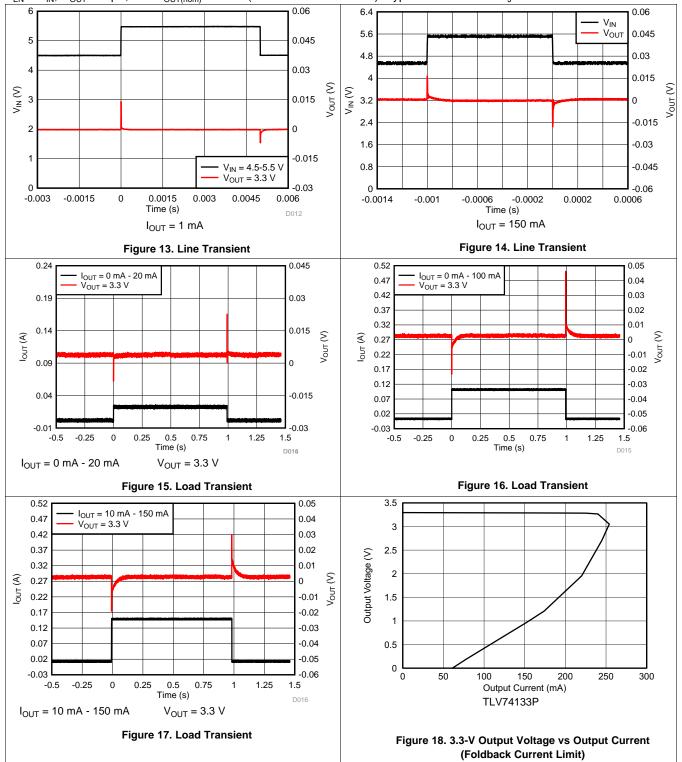
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Typical Characteristics (continued)

over operating temperature range $T_J = -40^{\circ}C$ to $+125^{\circ}C$, $V_{IN} = V_{OUT(nom)} + 0.5$ V or 2 V (whichever is greater), $I_{OUT} = 10$ mA, $V_{EN} = V_{IN}$, $C_{OUT} = 1$ µF, and $V_{OUT(nom)} = 1.8$ V (unless otherwise noted). Typical values are at $T_J = 25^{\circ}C$.

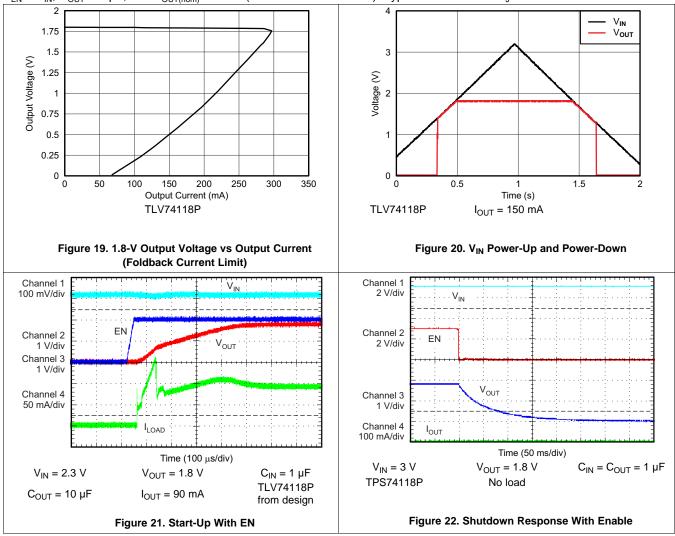


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Typical Characteristics (continued)

over operating temperature range $T_J = -40^{\circ}C$ to +125°C, $V_{IN} = V_{OUT(nom)} + 0.5$ V or 2 V (whichever is greater), $I_{OUT} = 10$ mA, $V_{EN} = V_{IN}$, $C_{OUT} = 1$ µF, and $V_{OUT(nom)} = 1.8$ V (unless otherwise noted). Typical values are at $T_J = 25^{\circ}C$.





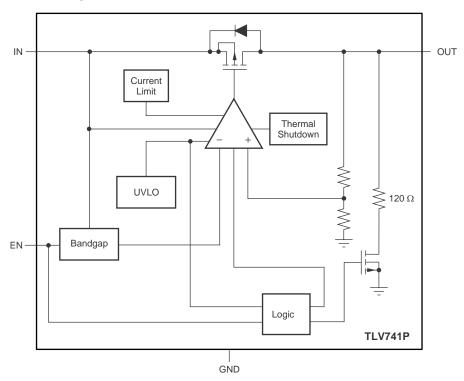
7 Detailed Description

7.1 Overview

The TLV741P belongs to a new family of next-generation value low-dropout (LDO) regulators. The TLV741P consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little $(V_{IN} - V_{OUT})$ headroom makes the device suitable for RF portable applications.

This regulator offers current limit and thermal protection. Device operating junction temperature is -40°C to +125°C.

7.2 Functional Block Diagram





7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV741P uses a UVLO circuit that disables the output until the input voltage is greater than the rising UVLO voltage. The circuit makes sure that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$. During UVLO disable, the output of the TLV741P version is connected to ground with a $120-\Omega$ pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.4 V. If shutdown capability is not required, connect EN to IN.

The TLV741P has an internal pulldown MOSFET that connects a $120-\Omega$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_{I}) in parallel with the $120-\Omega$ pulldown resistor. The time constant is calculated in Equation 1.

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \tag{1}$$

7.3.3 Foldback Current Limit

The TLV741P has an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device is gradually reduced while the output voltage decreases. When the output shorts, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is calculated by Equation 2:

$$V_{OUT} = I_{LIMIT} \times R_{LOAD}$$
 (2)

The PMOS pass transistor dissipates $[(V_{IN} - V_{OUT}) \times I_{LIMIT}]$ until thermal shutdown is triggered and the device turns off. The internal thermal shutdown circuit turns on the device during cool down. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Protection* for more details.

The TLV741P PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, TI recommends externally limiting the rated output current to 5%.

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 158°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, which protects the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV741P internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TLV741P into thermal shutdown degrades device reliability.



7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as V_{IN(min)}.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists conditions that result in different operating modes.

Table 1. Device Functional Mode Comparison

ODERATING MODE	PARAMETER					
OPERATING MODE	V _{IN}	V _{EN}	I _{OUT}	T _J		
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	I _{OUT} < I _{LIM}	T _J < 125°C		
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	_	T _J < 125°C		
Disabled mode (any true condition disables the device)	_	V _{EN} < V _{EN(low)}	_	T _J > 158°C		



8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Considerations

The TLV741P uses an advanced internal control loop to obtain stable operation by using an input or output capacitor. An output capacitance of 1 μ F or larger generally provides good dynamic response. TI recommends using X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1- μ F to 1- μ F capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. TI recommends using an input capacitor if the source impedance is more than $0.5~\Omega$. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

The TLV741P uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}) , the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} - V_{OLIT})$ approaches dropout.

8.1.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.



8.2 Typical Application

Several versions of the TLV741P are suitable for powering the MSP430 microcontroller.

Figure 23 shows a diagram of the TLV741P powering an MSP430 microcontroller. Table 2 lists potential applications of some voltage versions.

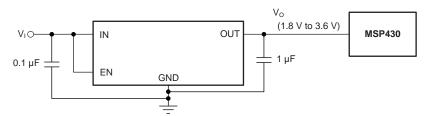


Figure 23. TLV741P Powering a Microcontroller

Table 2. Typical MSP430 Applications

DEVICE	V _{OUT} (TYPICAL)	APPLICATION
TLV741P18P	1.8 V	Allows for lowest power consumption with many MSP430s
TLV741P25P	2.5 V	2.2-V supply required by many MSP430s for flash programming and erasing

8.2.1 Design Requirements

Table 3 lists the design requirements.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT				
Input voltage	4.2 V to 3 V (Lithium Ion battery)				
Output voltage	1.8 V, ±1%				
DC output current	10 mA				
Peak output current	75 mA				
Maximum ambient temperature	65°C				

8.2.2 Detailed Design Procedure

An input capacitor is not required for this design because of the low impedance connection directly to the battery.

A small output capacitor allows for the minimal possible inrush current during start-up, and makes sure that the 180-mA maximum input current limit is not exceeded.

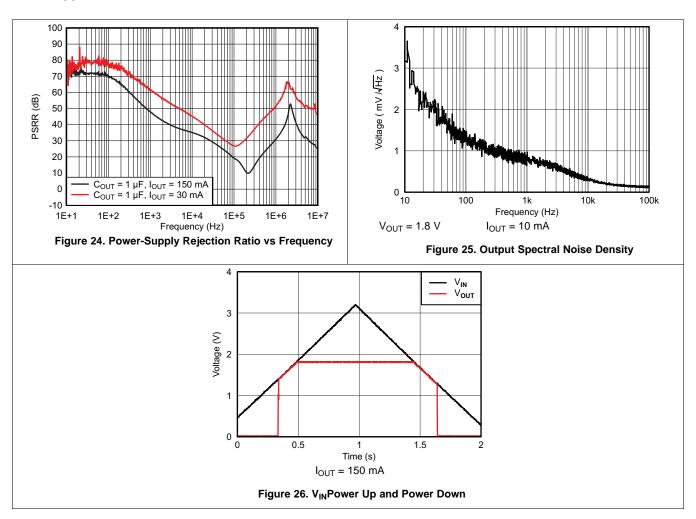
See Figure 29 to verify that the maximum junction temperature is not exceeded.

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Product Folder Links: TLV741P

TEXAS INSTRUMENTS

8.2.3 Application Curves



8.3 What to Do and What Not to Do

Place at least one $1-\mu F$ ceramic capacitor as close as possible to the OUT pin of the regulator for best transient performance.

Place at least one 1-µF capacitor as close as possible to the IN pin for best transient performance.

Do not place the output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not continuously operate the device in current limit or near thermal shutdown.



9 Power Supply Recommendations

This device is designed to operate from an input voltage supply range from 1.4 V to 5.5 V. The input voltage range must provide adequate headroom for the device to have a regulated output. This input supply must be well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

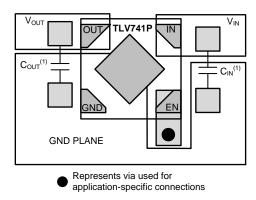
10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

Input and output capacitors must be placed as close to the device pins as possible. To improve AC performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection must be connected directly to the device GND pin. High-ESR capacitors may degrade PSRR performance.

10.2 Layout Examples



(1) Not required.

Figure 27. X2SON Layout Example

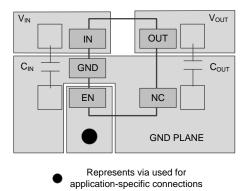


Figure 28. SOT-23 Layout Example



10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit-board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in **Thermal Information**. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 3:

$$P_{D} = (V_{IN} - V_{OUT}) \times I_{OUT}$$
(3)

Figure 29 shows the maximum ambient temperature versus the power dissipation of the TLV741P. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to make sure the TLV741P does not operate above a junction temperature of 125°C.

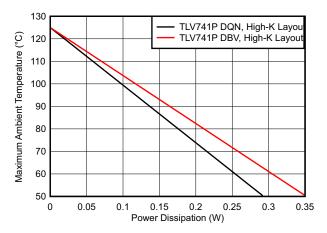


Figure 29. Maximum Ambient Temperature vs Device Power Dissipation

Estimate junction temperature by using the Ψ_{JT} and Ψ_{JB} thermal metrics, shown in *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta,JA}$. The junction temperature can be estimated with Equation 4:

$$\Psi_{JT}$$
: $T_J = T_T + \Psi_{JT} \cdot P_D$
 Ψ_{JB} : $T_J = T_B + \Psi_{JB} \cdot P_D$

where

- P_D is the power dissipation shown by Equation 3,
- T_T is the temperature at the center-top of the device package,
- T_B is the PCB temperature measured 1 mm away from the device package on the PCB surface.

NOTE

Both T_{T} and T_{B} can be measured on actual application boards using a thermogun (an infrared thermometer).

For more information about measuring T_T and T_B , see *Using New Thermal Metrics*, available for download at www.ti.com.

Product Folder Links: TLV741P

(4)



11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Universal Low-Dropout (LDO) Linear Voltage Regulator EVM User's Guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TLV741105PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1NFT
TLV741105PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1NFT
TLV74110PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1C9T
TLV74110PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1C9T
TLV74110PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8T
TLV74110PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8T
TLV74111PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1DHT
TLV74111PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1DHT
TLV74111PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8R
TLV74111PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8R
TLV74112PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	1DIT
TLV74112PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1DIT
TLV74112PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8Q
TLV74112PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8Q
TLV74115PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn Nipdau	Level-1-260C-UNLIM	-40 to 125	1DJT
TLV74115PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DJT
TLV74115PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8P
TLV74115PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8P
TLV74118PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn Nipdau	Level-1-260C-UNLIM	-40 to 125	1DKT
TLV74118PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DKT
TLV74118PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	80
TLV74118PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	80
TLV74125PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn Nipdau	Level-1-260C-UNLIM	-40 to 125	1DLT
TLV74125PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1DLT
TLV74125PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8N
TLV74125PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8N
TLV741285PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn Nipdau	Level-1-260C-UNLIM	-40 to 125	1DMT
TLV741285PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DMT
TLV741285PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8M



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Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	()	()			(-)	(4)	(5)		(-,
TLV741285PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8M
TLV74128PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn Nipdau	Level-1-260C-UNLIM	-40 to 125	1DNT
TLV74128PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DNT
TLV74128PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8L
TLV74128PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8L
TLV74130PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn Nipdau	Level-1-260C-UNLIM	-40 to 125	1DOT
TLV74130PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1DOT
TLV74130PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8K
TLV74130PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8K
TLV74133PDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI Sn Nipdau	Level-1-260C-UNLIM	-40 to 125	1CAT
TLV74133PDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-40 to 125	1CAT
TLV74133PDQNR	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8J
TLV74133PDQNR.B	Active	Production	X2SON (DQN) 4	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8J

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2025

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www.ti.com 5-Sep-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV741105PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74110PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74110PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74111PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74111PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74112PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74112PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74115PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74115PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74118PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74118PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74125PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74125PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV741285PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV741285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74128PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74128PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74130PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74130PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74133PDBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74133PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2



www.ti.com 5-Sep-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV741105PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74110PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74110PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74111PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74111PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74112PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74112PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74115PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74115PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74118PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV74118PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74125PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TLV74125PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV741285PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV741285PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74128PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74128PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74130PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0



PACKAGE MATERIALS INFORMATION

www.ti.com 5-Sep-2025

	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	TLV74130PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
	TLV74133PDBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
ĺ	TLV74133PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0



SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



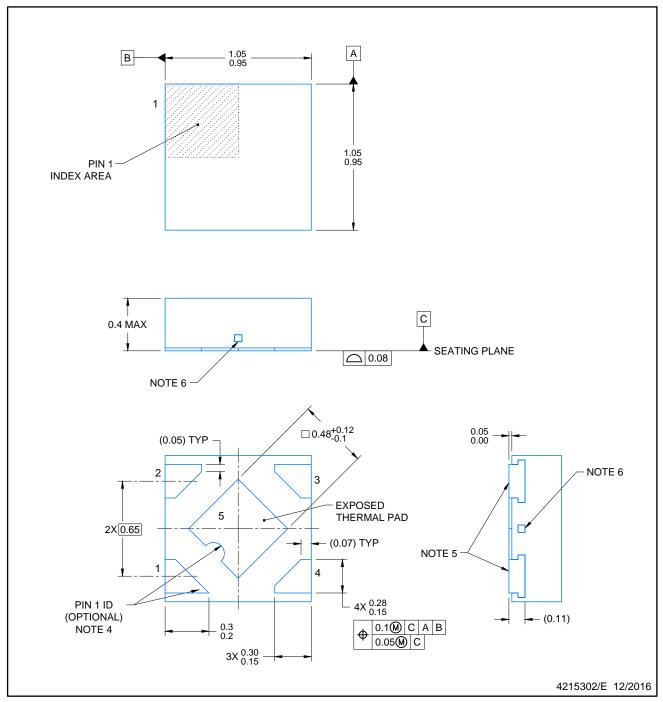


Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4210367/F



PLASTIC SMALL OUTLINE - NO LEAD

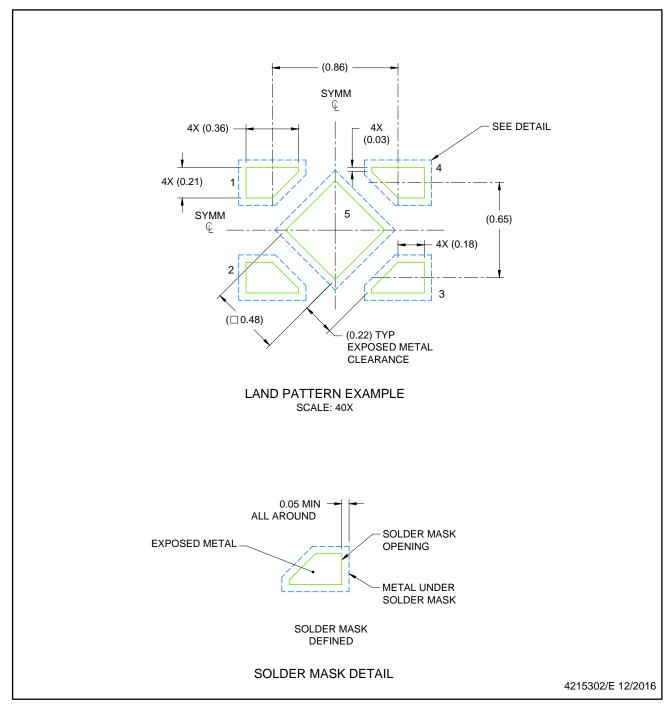


NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
- 4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
- 5. Shape of exposed side leads may differ.
- 6. Number and location of exposed tie bars may vary.



PLASTIC SMALL OUTLINE - NO LEAD

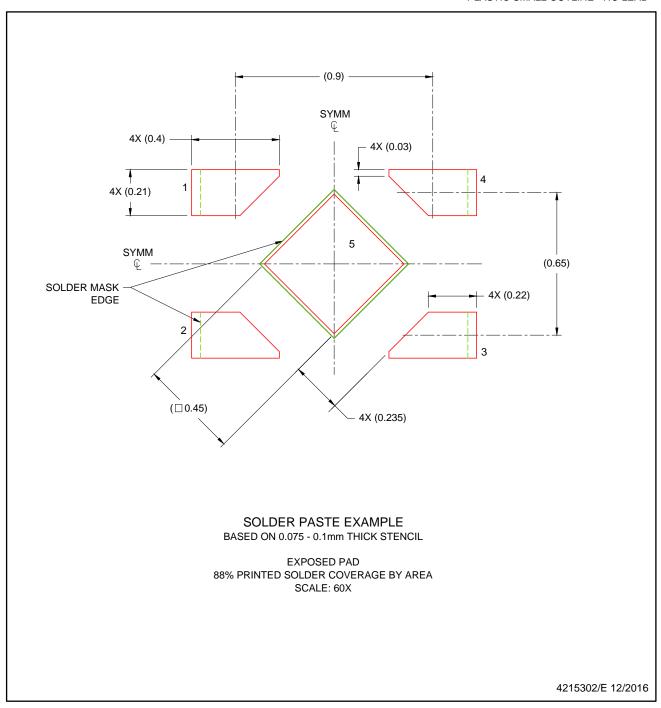


NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.



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