

Dual, 200mA, Low- I_Q Low-Dropout Regulator for Portable Devices

FEATURES

- **Very Low Dropout:**
 - 150mV at $I_{OUT} = 200mA$ and $V_{OUT} = 2.8V$
 - 75mV at $I_{OUT} = 100mA$ and $V_{OUT} = 2.8V$
 - 40mV at $I_{OUT} = 50mA$ and $V_{OUT} = 2.8V$
- **2% Accuracy Over Temperature**
- **Low I_Q of 35 μA per Regulator**
- **Multiple Fixed Output Voltage Combinations Possible from 1.2V to 4.8V**
- **High PSRR: 70dB at 1kHz**
- **Stable with Effective Capacitance of 0.1 $\mu F^{(1)}$**
- **Over-Current and Thermal Protection**
- **Dedicated V_{REF} for Each Output Minimizes Crosstalk**
- **Available in 1.5mm $\times$ 1.5mm SON-6 Package**

⁽¹⁾ See the [Input and Output Capacitor Requirements](#) in the [Application Information](#) section

APPLICATIONS

- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players and Other Handheld Products**

DESCRIPTION

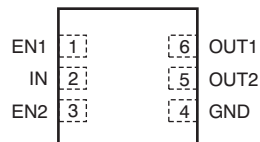
The TLV710 and TLV711 series of dual, low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. These devices provide a typical accuracy of 2% over temperature.

The TLV711 series provides an active pulldown circuit to quickly discharge the outputs.

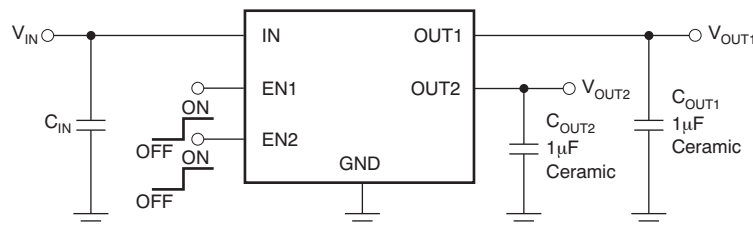
In addition, the TLV711-D series of devices have pull-down resistors at the EN pins. This design helps in disabling the device when the signal-driving EN pins are in a weak, indeterminate state (for example, the GPIO of a processor that might be three-stated during startup). The pull-down resistor pulls the voltage to the EN pins down to 0V, thus disabling the device.

The TLV710 and TLV711 series are available in a 1.5mm $\times$ 1.5mm SON-6 package, and are ideal for handheld applications.

TLV710
TLV711
1.5mm $\times$ 1.5mm SON-6
(TOP VIEW)



Typical Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾
TLV710xxyyqwwwz TLV711xxyyqwwwz	XX is nominal output voltage of channel 1 (for example 18 = 1.8V). YY is nominal output voltage of channel 2 (for example 28 = 2.8V). Q is optional. Use "U" for devices with EN pin pull-up resistor, and "D" for devices with EN pin pull-down resistor. WWW is package designator. Z is package quantity. Use "R" for reel (3000 pieces), and "T" for tape (250 pieces).

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
- (2) Output voltages from 1.2V to 4.8V in 50mV increments are available through the use of innovative factory OTP programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

At T_J = –40°C to +125°C (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage ⁽²⁾	IN	–0.3	+6.0	V
	EN	–0.3	V _{IN} + 0.3	V
	OUT	–0.3	+6.0	V
Current	OUT	Internally limited		A
Output short-circuit duration		Indefinite		s
Temperature	Operating junction, T _J	–55	+150	°C
	Storage, T _{stg}	–55	+150	°C
Electrostatic Discharge Rating	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages with respect to ground.

THERMAL INFORMATION⁽¹⁾

THERMAL METRIC ⁽²⁾	TLV710, TLV711	UNITS
	DSE	
	6 PINS	
ψ _{JT} Junction-to-top characterization parameter	6	°C/W

- (1) See the [Power Dissipation](#) section for more details.
- (2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

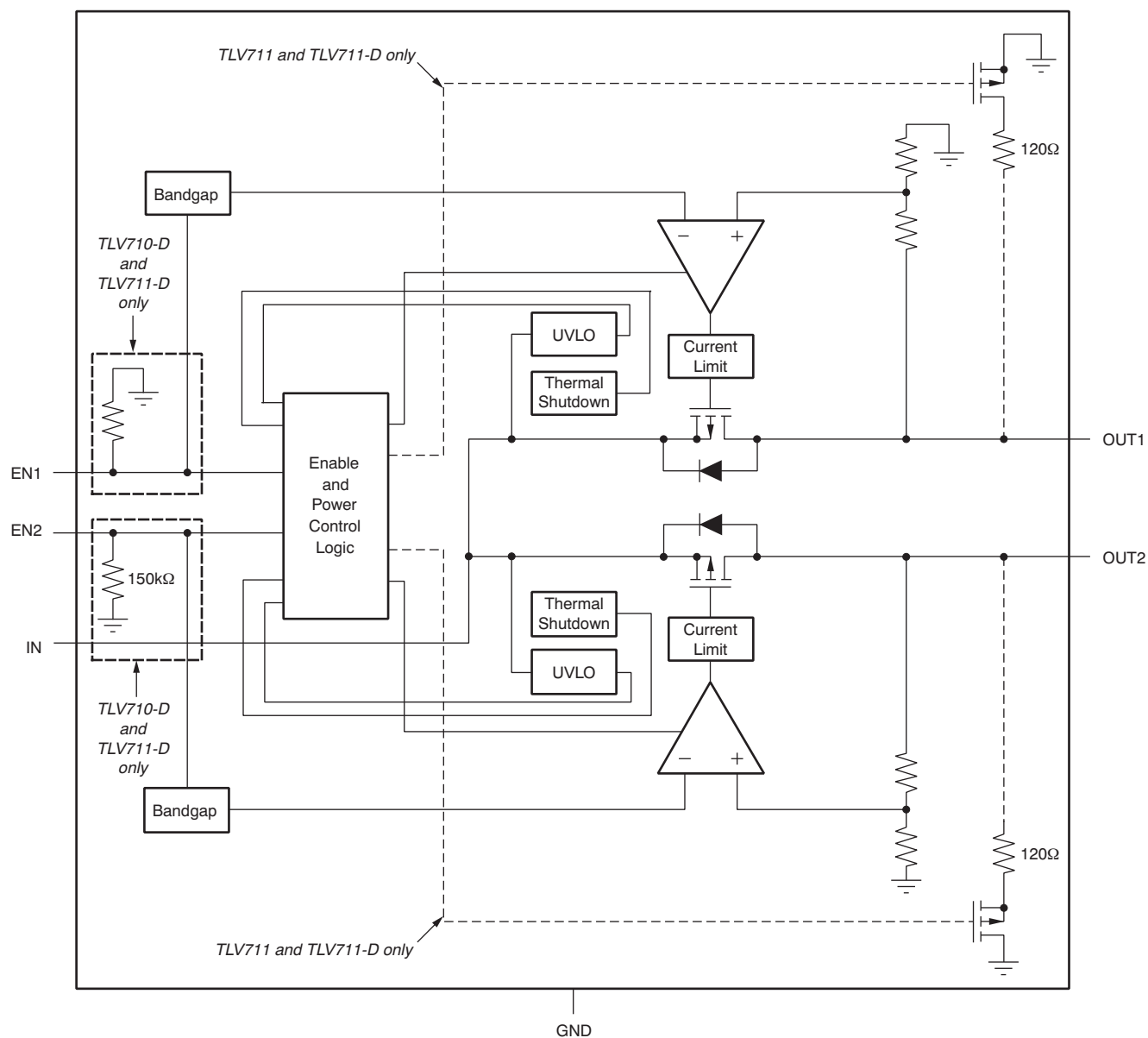
ELECTRICAL CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(TYP)} + 0.5\text{V}$ or 2.0V (whichever is greater), $I_{OUT} = 10\text{mA}$, $V_{EN1} = V_{EN2} = 0.9\text{V}$, and $C_{OUT1} = C_{OUT2} = 1\mu\text{F}$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLV710, TLV711			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		2.0		5.5	V
V_O	Output voltage range		1.2		4.8	V
V_{OUT}	DC output accuracy	$-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$	–2		+2	%
$\Delta V_O / \Delta V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.5\text{V} \leq V_{IN} \leq 5.5\text{V}$		1	5	mV
$\Delta V_O / \Delta I_{OUT}$	Load regulation	$0\text{mA} \leq I_{OUT} \leq 200\text{mA}$		5	15	mV
V_{DO}	Dropout voltage	$V_{IN} = 0.98\text{V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{mA}$, $2\text{V} \leq V_{OUT} < 2.4\text{V}$		200	285	mV
		$V_{IN} = 0.98\text{V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{mA}$, $2.4\text{V} \leq V_{OUT} < 2.8\text{V}$		175	250	mV
		$V_{IN} = 0.98\text{V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{mA}$, $2.8\text{V} \leq V_{OUT} < 3.3\text{V}$		150	215	mV
		$V_{IN} = 0.98\text{V} \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{mA}$, $3.3\text{V} \leq V_{OUT} \leq 4.8\text{V}$		140	200	mV
I_{CL}	Output current limit	$V_{OUT} = 0.9\text{V} \times V_{OUT(NOM)}$	220	350	550	mA
I_Q	Quiescent current	$V_{EN1} = \text{high}$, $V_{EN2} = \text{low}$, $I_{OUT1} = 0\text{mA}$		35		μA
		$V_{EN1} = \text{low}$, $V_{EN2} = \text{high}$, $I_{OUT2} = 0\text{mA}$		35		μA
		$V_{EN1} = \text{high}$, $V_{EN2} = \text{high}$, $I_{OUT} = 0\text{mA}$		70	110	μA
I_{GND}	Ground pin current	$I_{OUT1} = I_{OUT2} = 200\text{mA}$		360		μA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN1,2} \leq 0.4\text{V}$, $2.0\text{V} \leq V_{IN} \leq 4.5\text{V}$		2.5	4	μA
PSRR	Power-supply rejection ratio	$V_{OUT} = 1.8\text{V}$	$f = 10\text{Hz}$	80		dB
			$f = 100\text{Hz}$	75		dB
			$f = 1\text{kHz}$	70		dB
			$f = 10\text{kHz}$	70		dB
			$f = 100\text{kHz}$	50		dB
V_N	Output noise voltage	$\text{BW} = 100\text{Hz to } 100\text{kHz}$, $V_{OUT} = 1.8\text{V}$		48		μV_{RMS}
t_{STR}	Startup time ⁽¹⁾	$C_{OUT} = 1.0\mu\text{F}$, $I_{OUT} = 200\text{mA}$		100		μs
V_{HI}	Enable high (enabled)		0.9		V_{IN}	V
V_{LO}	Enable low (shutdown)		0		0.4	V
I_{EN}	Enable pin current, enabled	TLV710, TLV711		0.04		μA
		TLV710-D, TLV711-D		6		μA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_J	Operating junction temperature		–40		+125	$^\circ\text{C}$
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+165		$^\circ\text{C}$
		Reset, temperature decreasing		+145		$^\circ\text{C}$

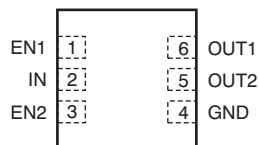
(1) Startup time = time from EN assertion to $0.98 \times V_{OUT(NOM)}$.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

DSE PACKAGE
1.5mm x 1.5mm SON-6
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
EN1	1	Enable pin for regulator 1. Driving EN1 over 0.9V turns on regulator 1. Driving EN below 0.4V puts regulator 1 into shutdown mode.
IN	2	Input pin. A small capacitor is needed from this pin to ground to assure stability. See Input and Output Capacitor Requirements in the <i>Application Information</i> section for more details.
EN2	3	Enable pin for regulator 2. Driving EN2 over 0.9V turns on regulator 2. Driving EN2 below 0.4V puts regulator2 into shutdown mode.
GND	4	Ground pin.
OUT2	5	Regulated output voltage pin. A small 1 μ F ceramic capacitor is needed from this pin to ground to assure stability. See Input and Output Capacitor Requirements in the <i>Application Information</i> section for more details.
OUT1	6	Regulated output voltage pin. A small 1 μ F ceramic capacitor is needed from this pin to ground to assure stability. See Input and Output Capacitor Requirements in the <i>Application Information</i> section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

**LINE REGULATION: V_{OUT1}
(TLV7101828)**

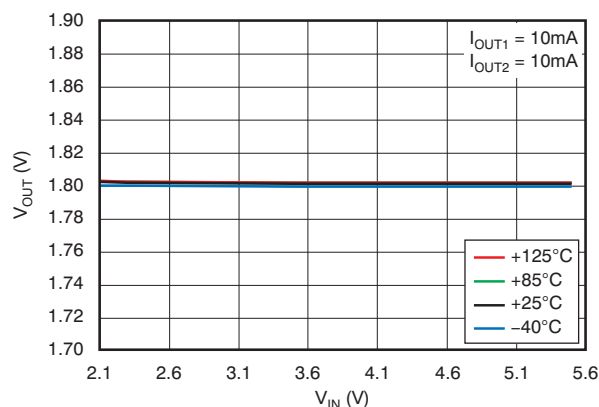


Figure 1.

**LINE REGULATION: V_{OUT2}
(TLV7101828)**

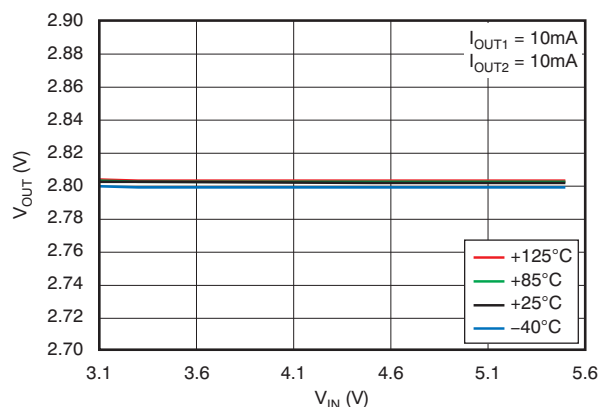


Figure 2.

**LINE REGULATION: V_{OUT1}
(TLV7101828)**

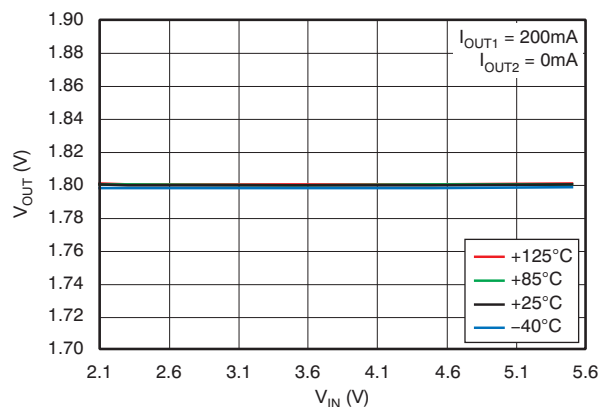


Figure 3.

**LINE REGULATION: V_{OUT2}
(TLV7101828)**

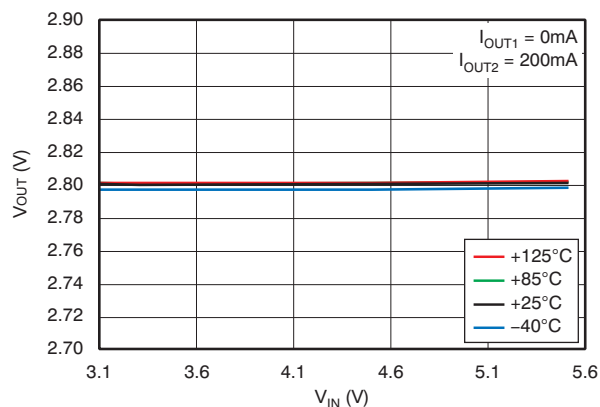


Figure 4.

**LINE REGULATION: V_{OUT1}
(TLV7103333)**

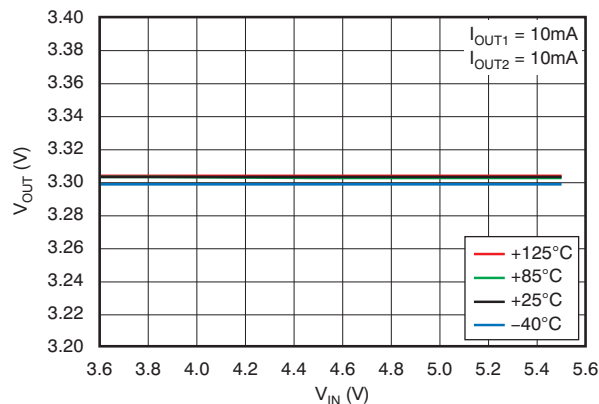


Figure 5.

**LINE REGULATION: V_{OUT2}
(TLV7103333)**

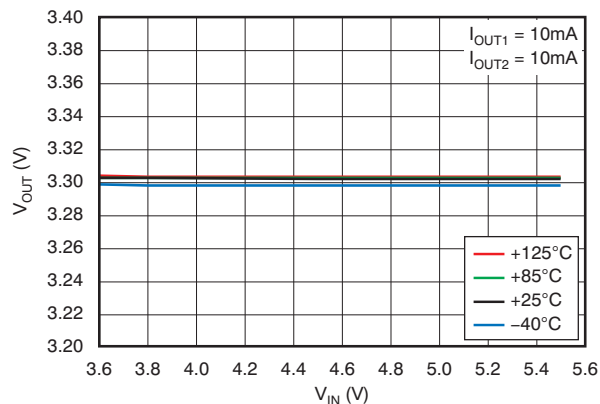


Figure 6.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

**LINE REGULATION: V_{OUT1}
(TLV7103333)**

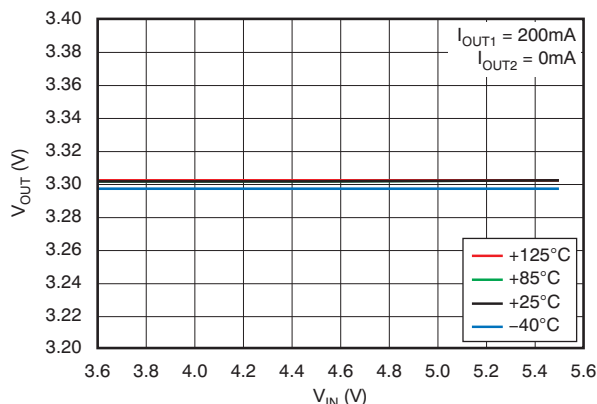


Figure 7.

**LINE REGULATION: V_{OUT2}
(TLV7103333)**

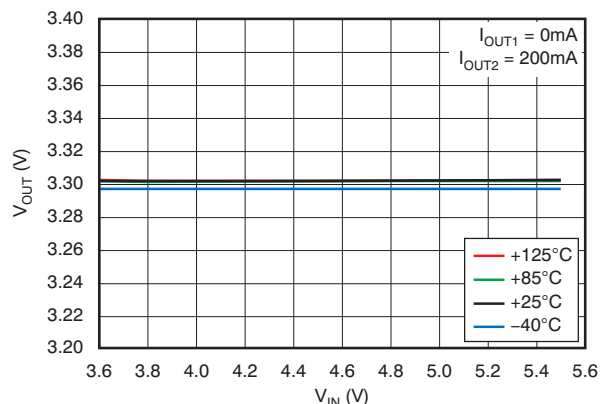


Figure 8.

**LINE REGULATION: V_{OUT1}
(TLV7111525)**

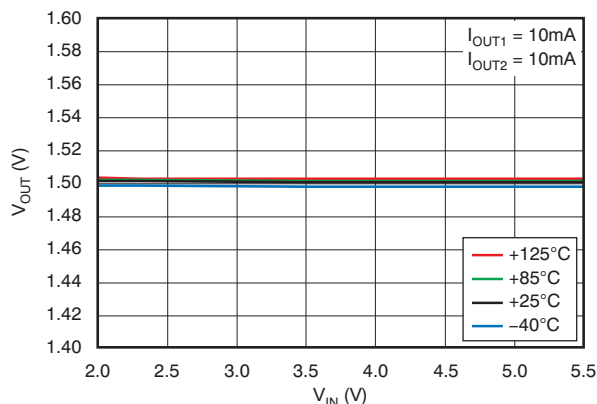


Figure 9.

**LINE REGULATION: V_{OUT2}
(TLV7111525)**

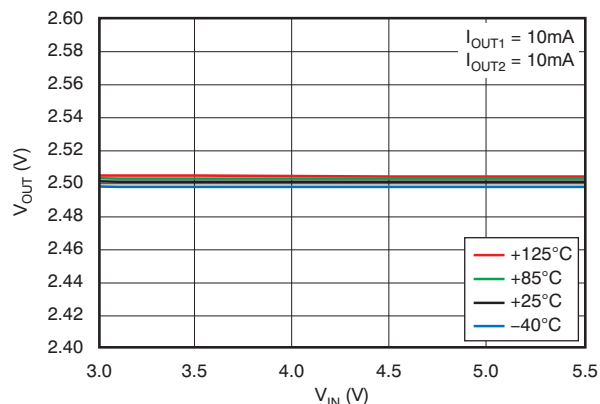


Figure 10.

**LINE REGULATION: V_{OUT1}
(TLV7111525)**

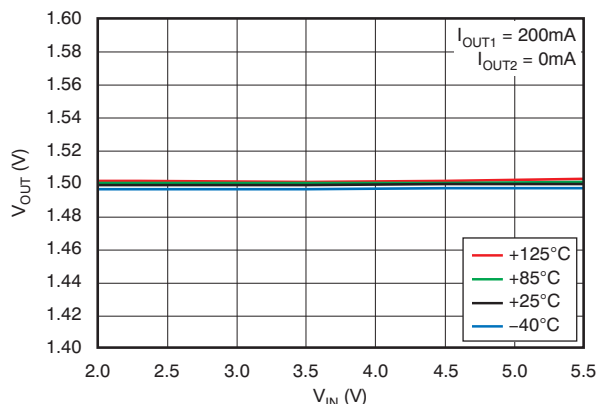


Figure 11.

**LINE REGULATION: V_{OUT2}
(TLV7111525)**

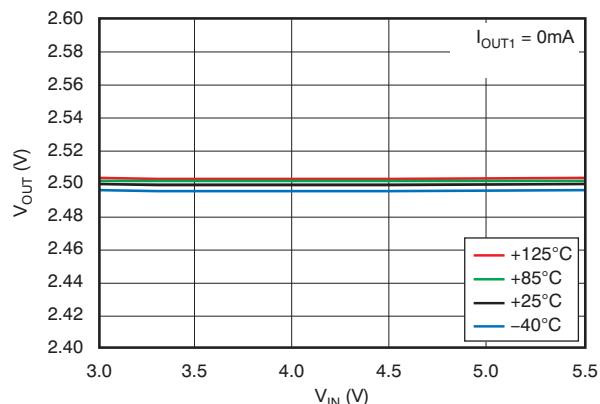


Figure 12.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

LOAD REGULATION: V_{OUT1}
(TLV7101828)

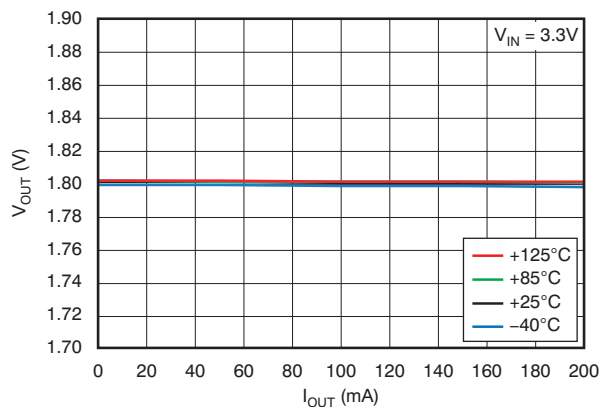


Figure 13.

LOAD REGULATION: V_{OUT2}
(TLV7101828)

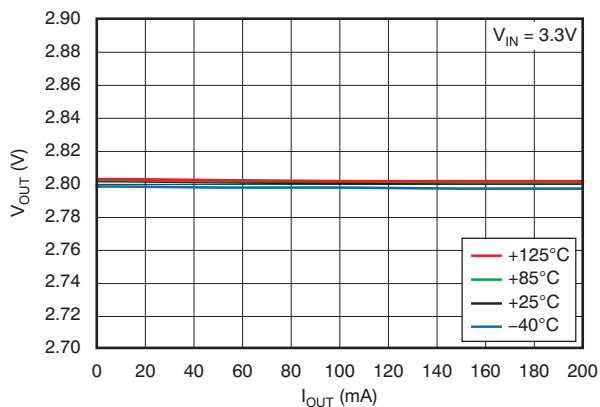


Figure 14.

LOAD REGULATION: V_{OUT1}
(TLV7103333)

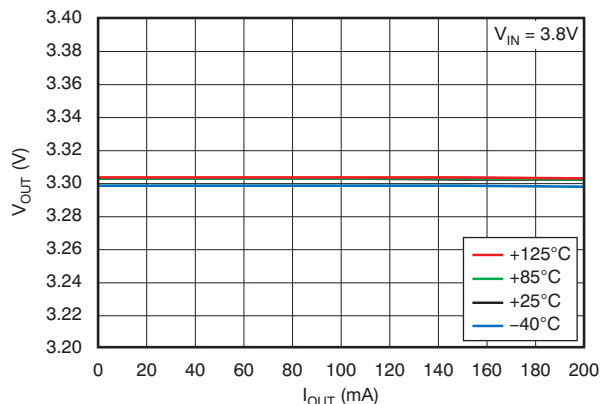


Figure 15.

LOAD REGULATION: V_{OUT2}
(TLV7103333)

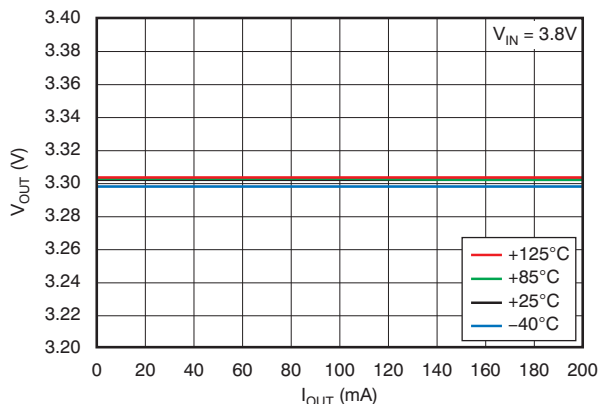


Figure 16.

LOAD REGULATION: V_{OUT1}
(TLV7111525)

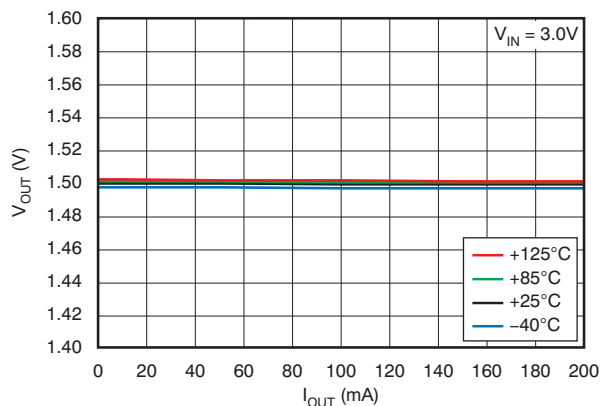


Figure 17.

LOAD REGULATION: V_{OUT2}
(TLV7111525)

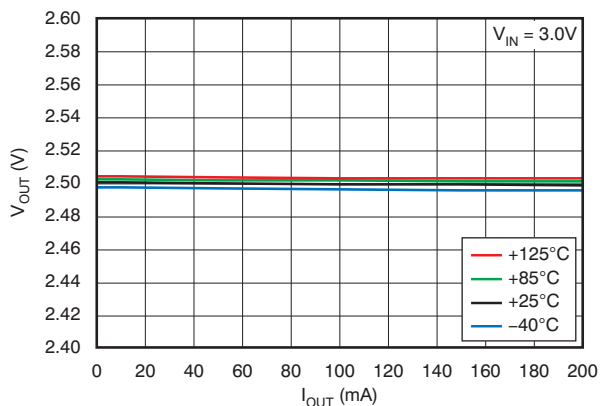


Figure 18.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

**DROPOUT VOLTAGE
vs INPUT VOLTAGE**

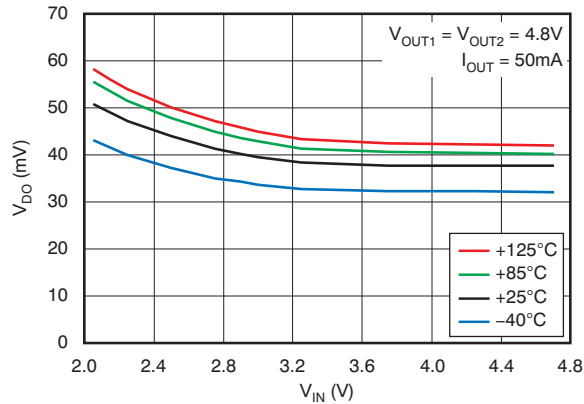


Figure 19.

**DROPOUT VOLTAGE
vs INPUT VOLTAGE**

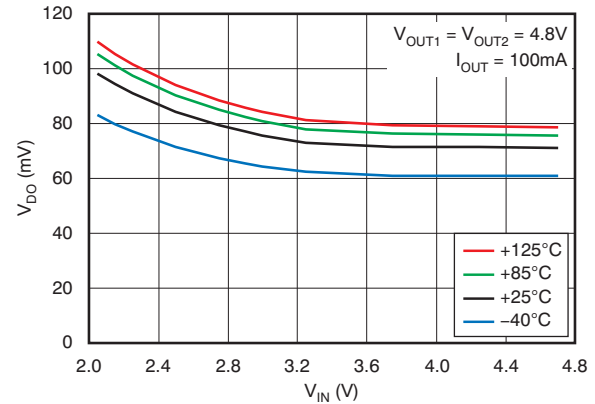


Figure 20.

**DROPOUT VOLTAGE
vs INPUT VOLTAGE**

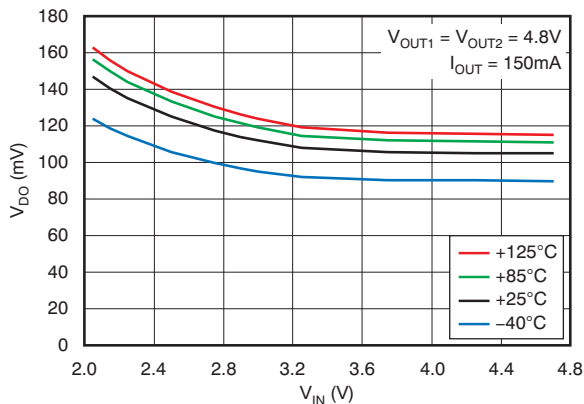


Figure 21.

**DROPOUT VOLTAGE
vs INPUT VOLTAGE**

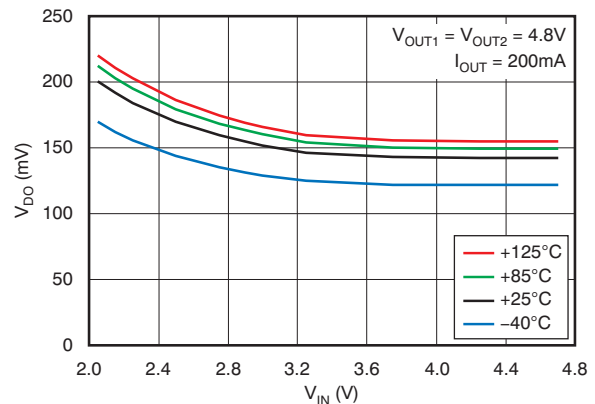


Figure 22.

**DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT2}
(TLV7101828)**

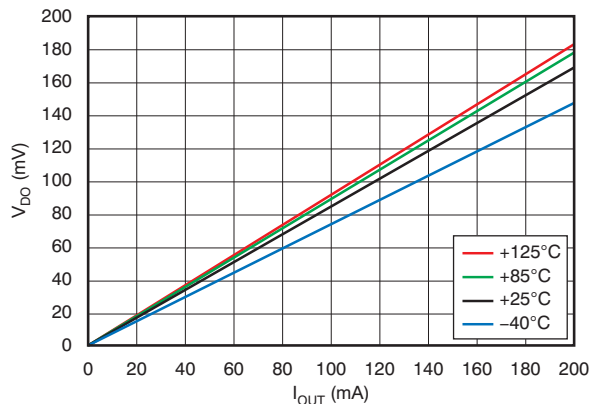


Figure 23.

**DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT1}/V_{OUT2}
(TLV7103333)**

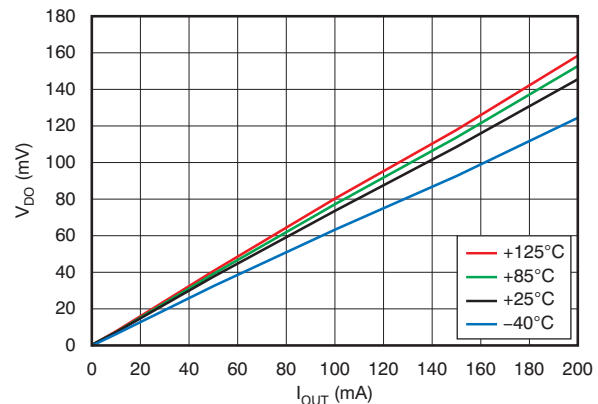


Figure 24.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT2}
(TLV7111525)

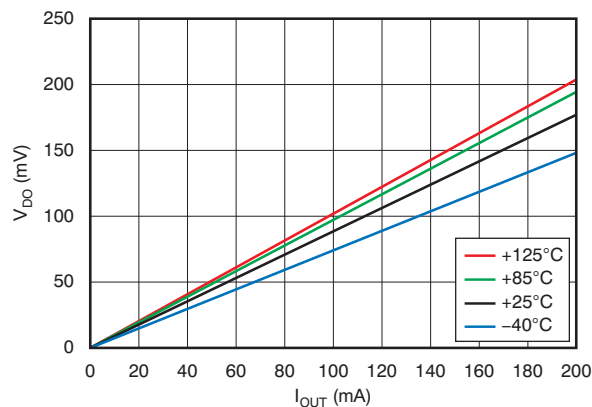


Figure 25.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1}
(TLV7101828)

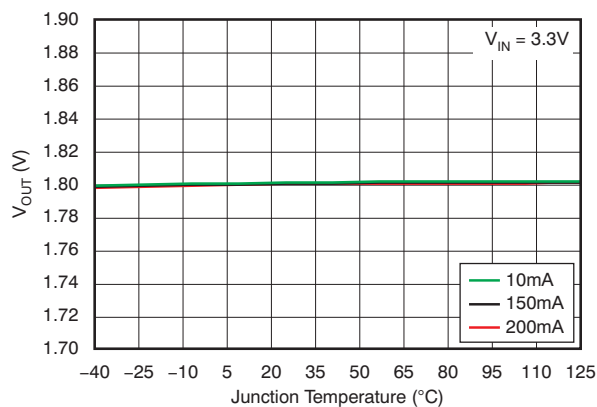


Figure 26.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2}
(TLV7101828)

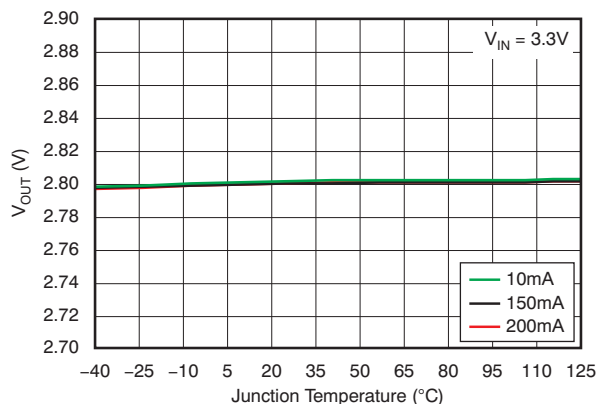


Figure 27.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1}
(TLV7103333)

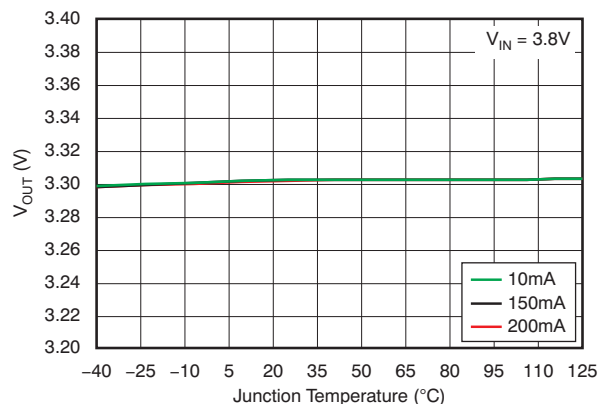


Figure 28.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2}
(TLV7103333)

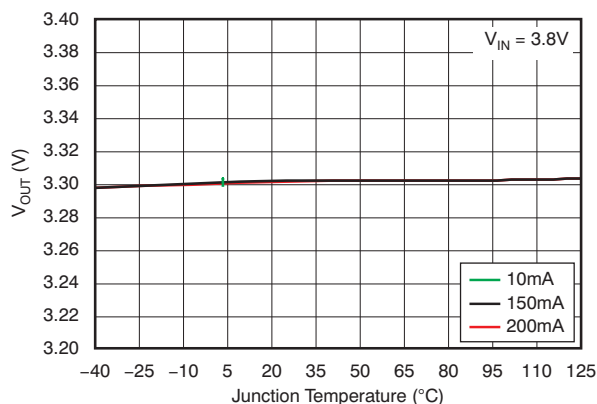


Figure 29.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1}
(TLV7111525)

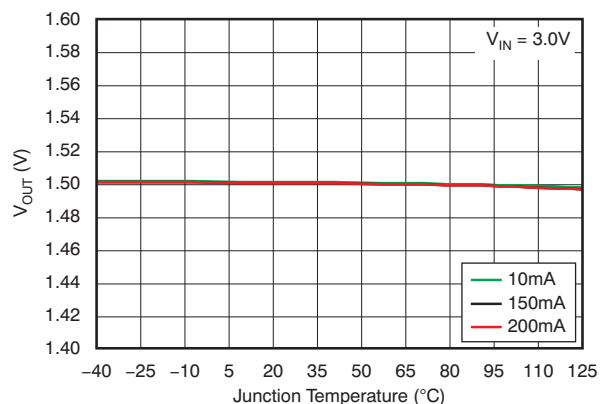


Figure 30.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2}
(TLV7111525)

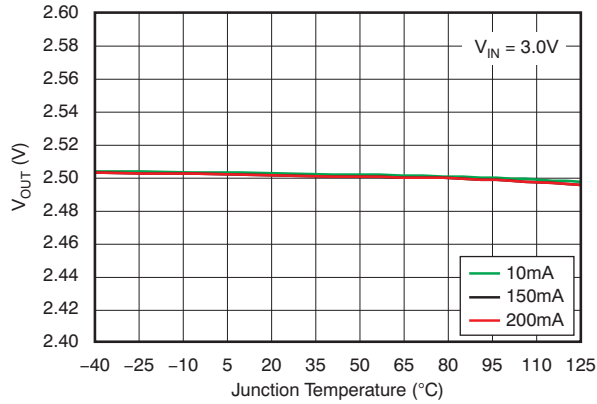


Figure 31.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1}
(TLV7101828)

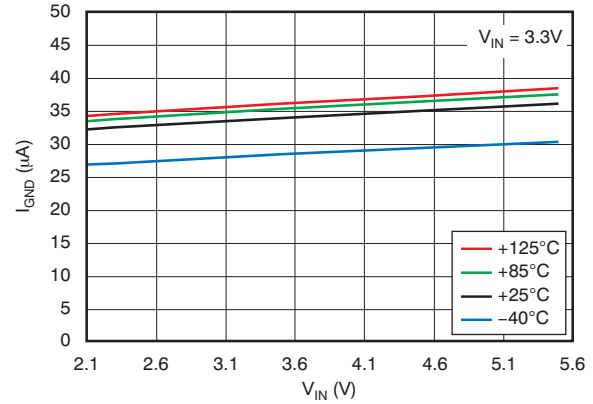


Figure 32.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2}
(TLV7101828)

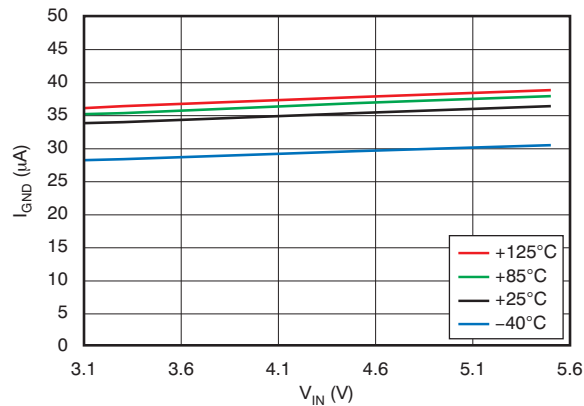


Figure 33.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1}
(TLV7103333)

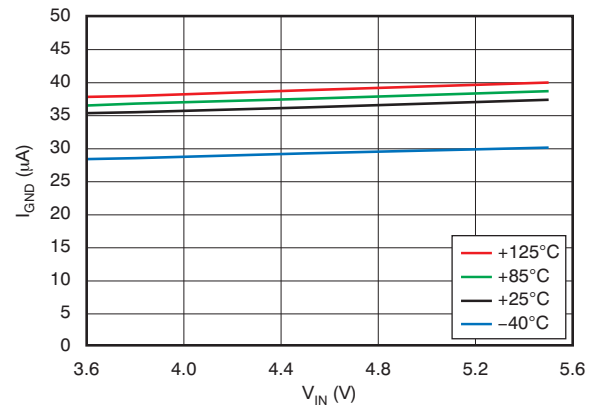


Figure 34.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2}
(TLV7103333)

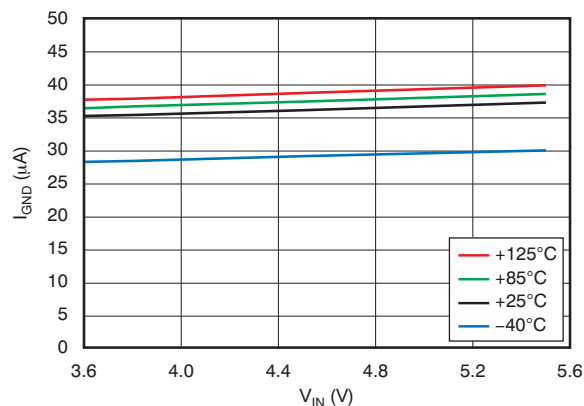


Figure 35.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1}
(TLV7111525)

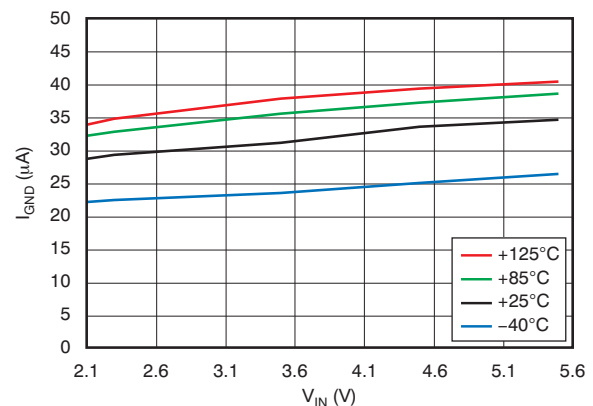


Figure 36.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2}
(TLV7111525)

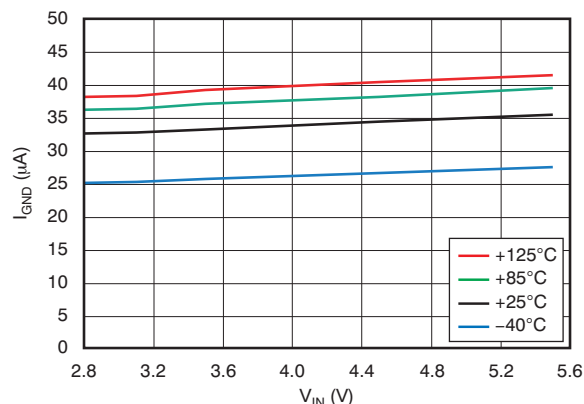


Figure 37.

GROUND PIN CURRENT vs LOAD: I_{Q1}
(TLV7101828)

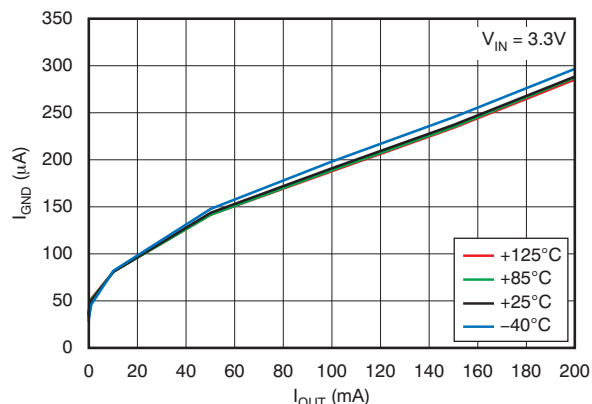


Figure 38.

GROUND PIN CURRENT vs LOAD: I_{Q2}
(TLV7103333)

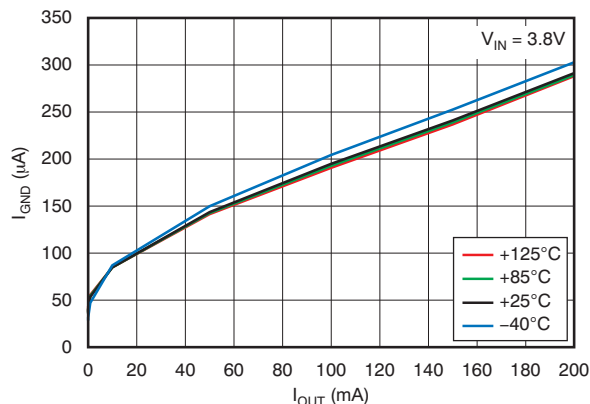


Figure 39.

GROUND PIN CURRENT vs LOAD: I_{Q1}
(TLV7111525)

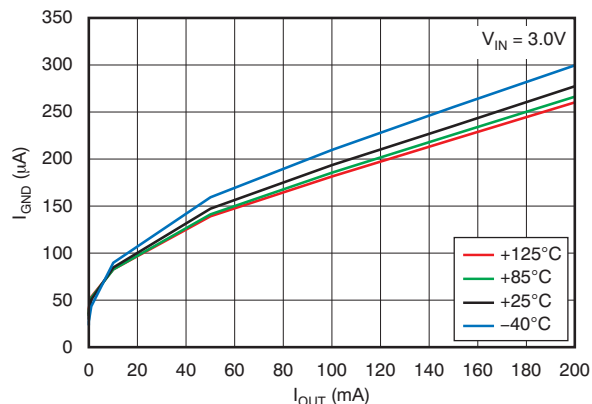


Figure 40.

SHUTDOWN CURRENT vs INPUT VOLTAGE
(TLV7101828)

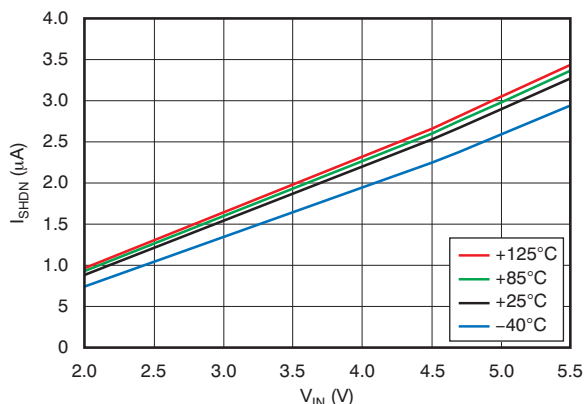


Figure 41.

SHUTDOWN CURRENT vs INPUT VOLTAGE
(TLV7103333)

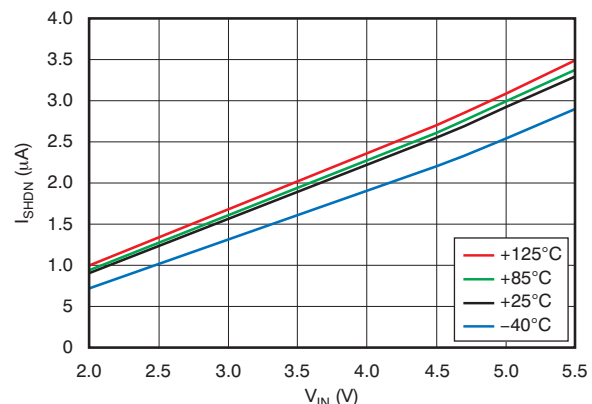


Figure 42.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^\circ\text{C}$.

**SHUTDOWN CURRENT vs INPUT VOLTAGE
(TLV7111525)**

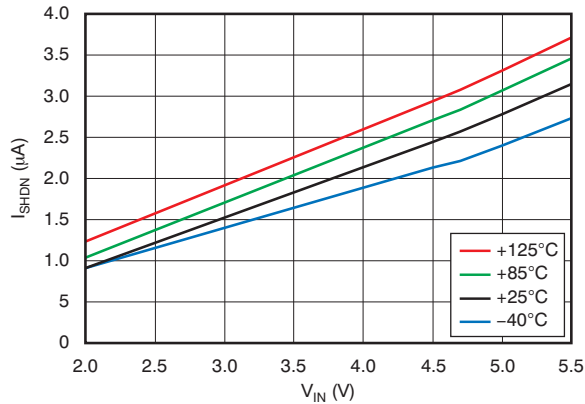


Figure 43.

**CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1}
(TLV7101828)**

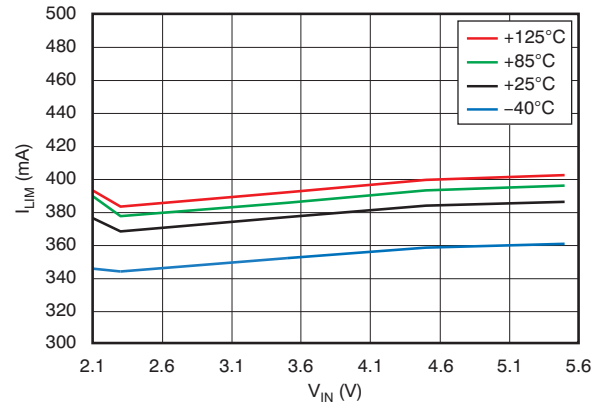


Figure 44.

**CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2}
(TLV7101828)**

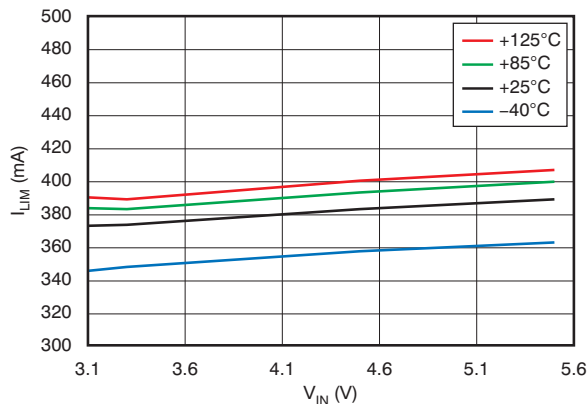


Figure 45.

**CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1}
(TLV7103333)**

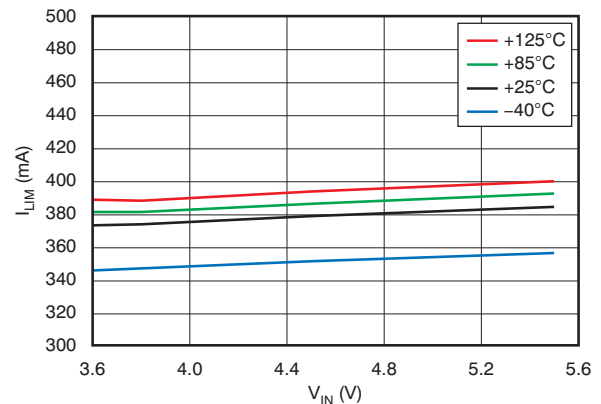


Figure 46.

**CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2}
(TLV7103333)**

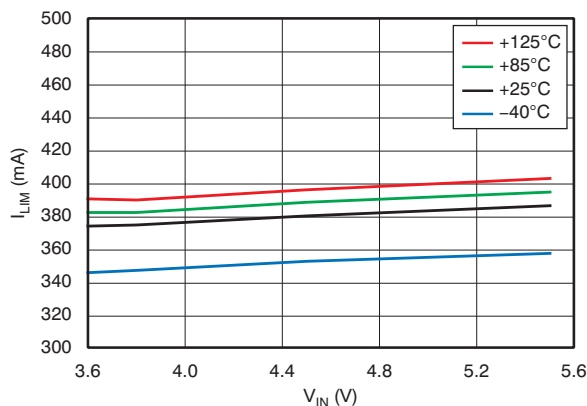


Figure 47.

**CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1}
(TLV7111525)**

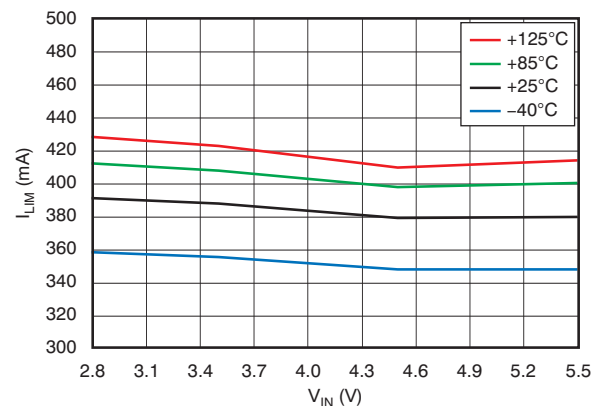


Figure 48.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2}
(TLV7111525)

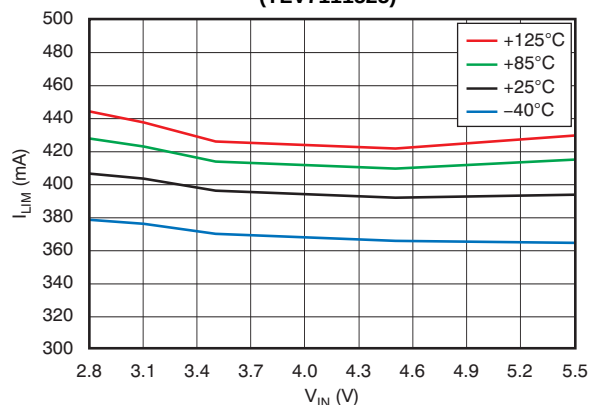


Figure 49.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(TLV7101828)

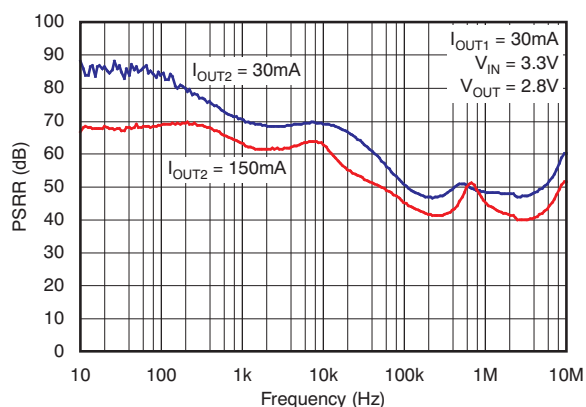


Figure 50.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(TLV7103333)

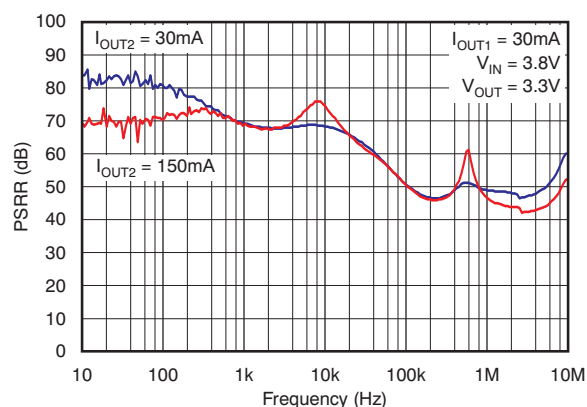


Figure 51.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY
(TLV7111525)

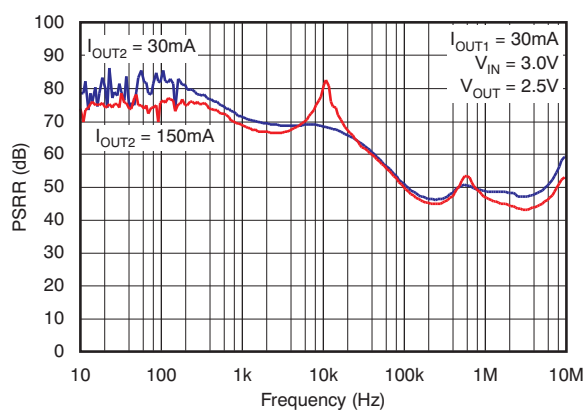


Figure 52.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY (TLV7101828)

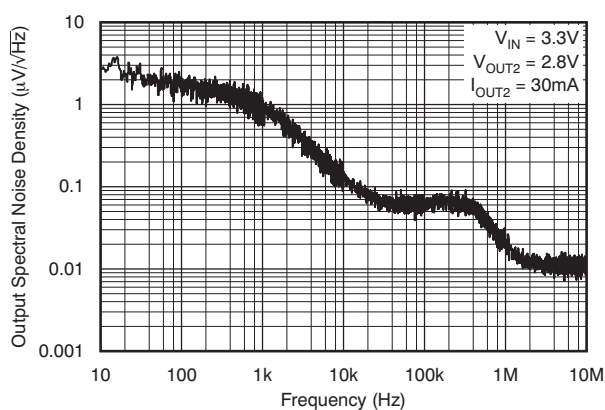


Figure 53.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

**OUTPUT SPECTRAL NOISE DENSITY
vs FREQUENCY (TLV7103333)**

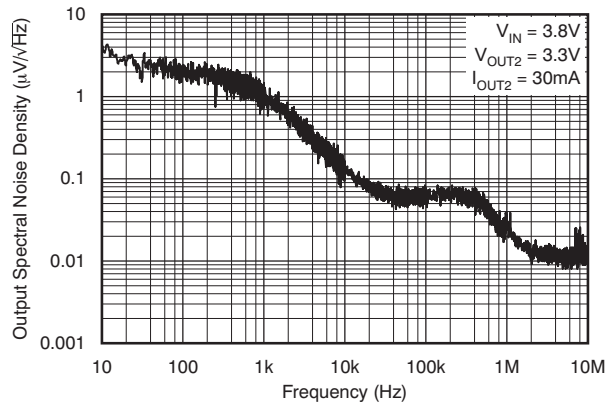


Figure 54.

**OUTPUT SPECTRAL NOISE DENSITY
vs FREQUENCY (TLV7111525)**

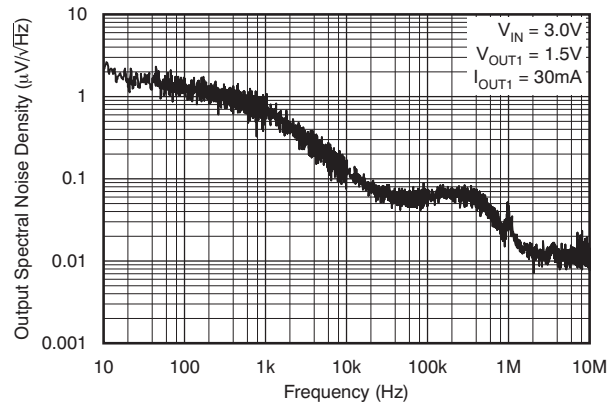


Figure 55.

**LINE TRANSIENT RESPONSE
 $V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$**

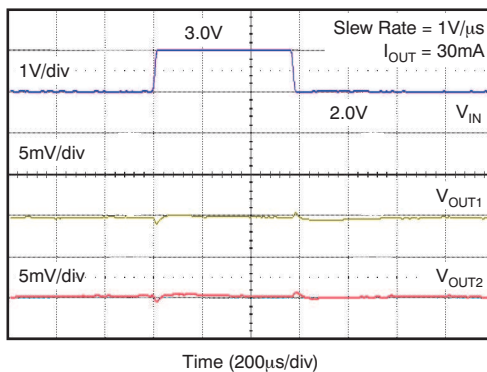


Figure 56.

**LINE TRANSIENT RESPONSE
 $V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$**

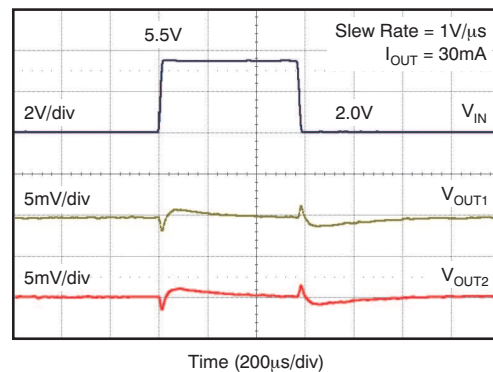


Figure 57.

**LINE TRANSIENT RESPONSE
 $V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$**

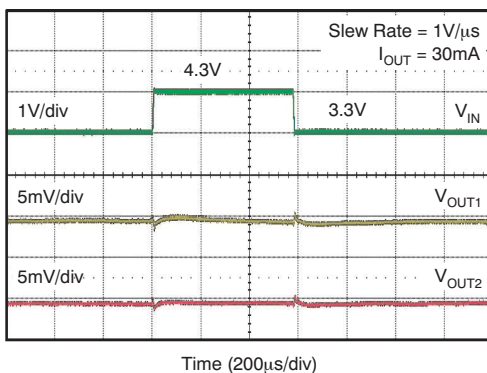


Figure 58.

**LINE TRANSIENT RESPONSE
 $V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$**

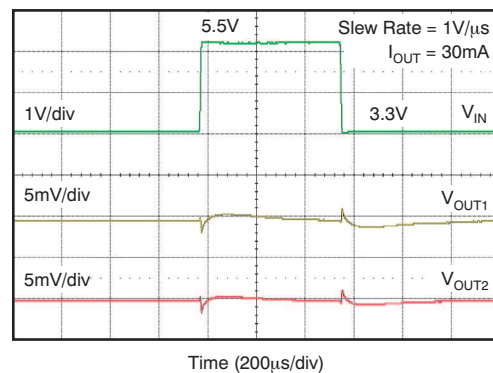


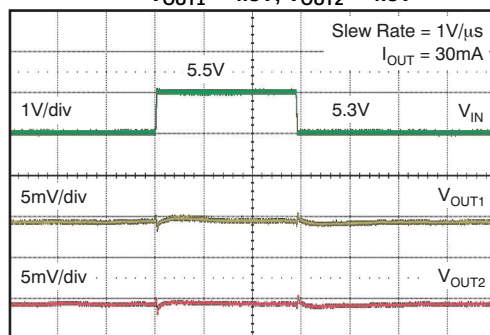
Figure 59.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

LINE TRANSIENT RESPONSE

$V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$

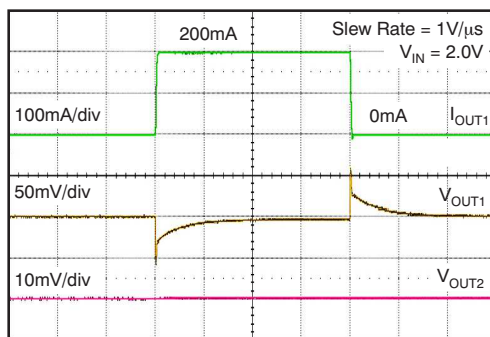


Time (200μs/div)

Figure 60.

LOAD TRANSIENT RESPONSE AND CROSSTALK

$V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$

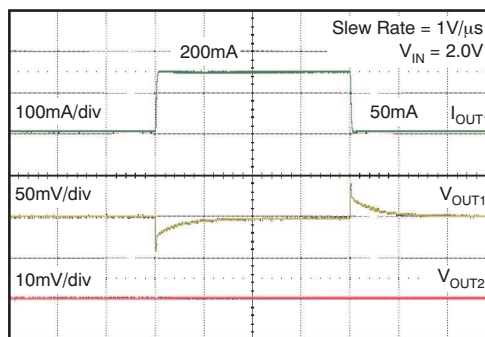


Time (50μs/div)

Figure 61.

LOAD TRANSIENT RESPONSE AND CROSSTALK

$V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$

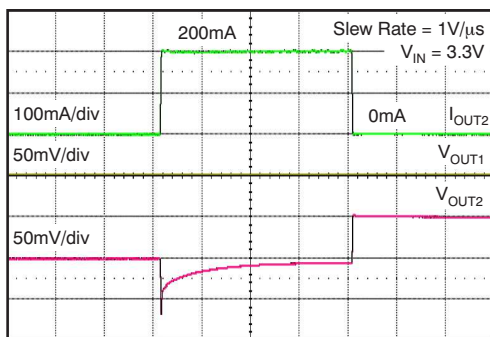


Time (50μs/div)

Figure 62.

LOAD TRANSIENT RESPONSE AND CROSSTALK

$V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$

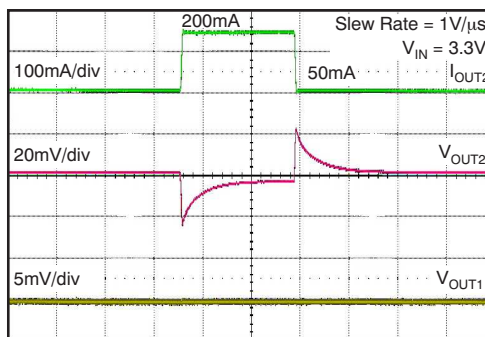


Time (50μs/div)

Figure 63.

LOAD TRANSIENT RESPONSE AND CROSSTALK

$V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$



Time (50μs/div)

Figure 64.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN1} = V_{EN2} = V_{IN}$, $C_{IN} = 1\mu\text{F}$, $C_{OUT1} = 1\mu\text{F}$, and $C_{OUT2} = 1\mu\text{F}$, unless otherwise noted. Typical values are at $T_J = +25^{\circ}\text{C}$.

LOAD TRANSIENT RESPONSE AND CROSSTALK

$V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$

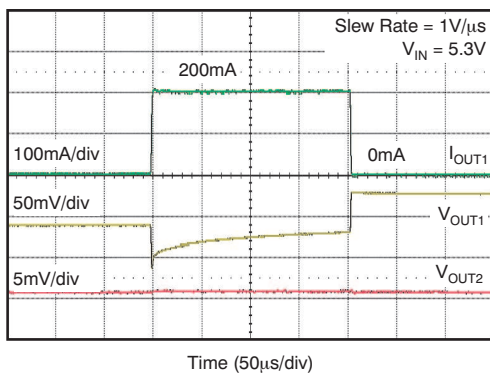


Figure 65.

LOAD TRANSIENT RESPONSE AND CROSSTALK

$V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$

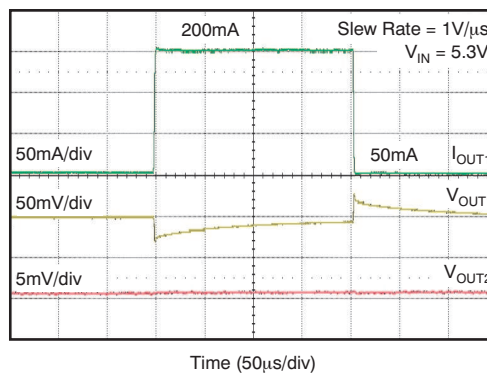


Figure 66.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

$V_{OUT1} = 1.2\text{V}$, $V_{OUT2} = 1.2\text{V}$

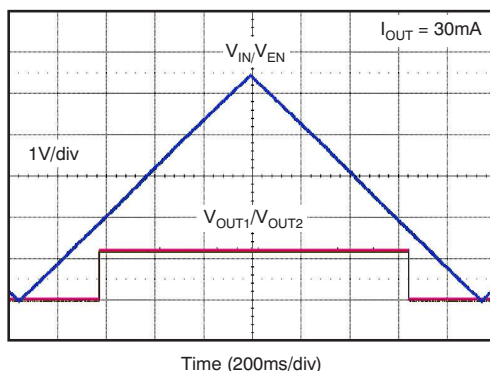


Figure 67.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

$V_{OUT1} = 1.8\text{V}$, $V_{OUT2} = 2.8\text{V}$

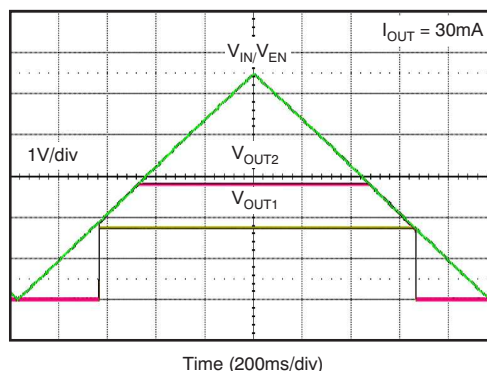


Figure 68.

V_{IN} RAMP UP, RAMP DOWN RESPONSE

$V_{OUT1} = 4.8\text{V}$, $V_{OUT2} = 4.8\text{V}$

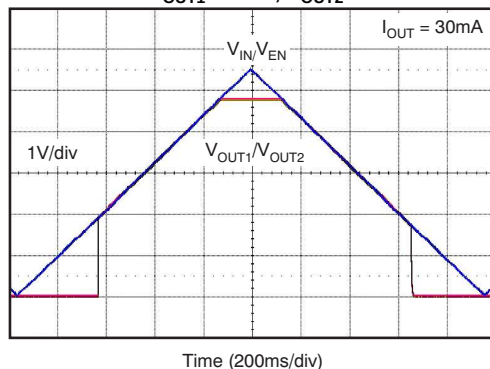


Figure 69.

APPLICATION INFORMATION

The TLV710 and TLV711 series of devices belong to a new family of next generation, value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These features, combined with low noise, very good PSRR with little (V_{IN} to V_{OUT}) headroom, make these devices ideal for RF portable applications. This family of LDO regulators offers current limit and thermal protection, and is specified from -40°C to $+125^{\circ}\text{C}$.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1.0 μF X5R- and X7R-type ceramic capacitors are recommended because they have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV710 and TLV711 are designed to be stable with an effective capacitance of 0.1 μF or larger at the output. Thus, the device would also be stable with capacitors of other dielectrics, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 μF . This effective capacitance refers to the capacitance that the device sees under operating bias voltage and temperature conditions (that is, the capacitance after taking bias voltage and temperature derating into consideration.)

In addition to allowing the use of cost-effective dielectrics, these devices also enable using smaller footprint capacitors that have a higher derating in size-constrained applications.

Note that using a 0.1 μF rating capacitor at the output of the LDO regulator does not ensure stability because the effective capacitance under operating conditions would be less than 0.1 μF . The maximum ESR should be less than 200m Ω .

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1 μF to 1.0 μF low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast-rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is more than 2 Ω , a 0.1 μF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TLV710 and TLV711 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$.

The PMOS pass transistor dissipates $(V_{IN} - V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the [Thermal Information](#) section for more details. The PMOS pass element in the TLV710 and TLV711 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when EN pin goes above 0.9V. This relatively lower value of voltage needed to turn the LDO regulator on can be used to enable the device with the GPIO of recent processors whose GPIO voltage is lower than traditional microcontrollers.

The device is turned off when the EN pin is held at less than 0.4V. When shutdown capability is not required, the EN pin can be connected to the IN pin.

The TLV711 has internal pull-down circuitry that discharges output with a time constant of:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT}$$

Where:

R_L = load resistance

C_{OUT} = output capacitor (1)

DROPOUT VOLTAGE

The TLV710 and TLV711 use a PMOS pass transistor to achieve low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} - V_{OUT})$ approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

The TLV710 and TLV711 each have a dedicated V_{REF} . Consequently, crosstalk from one channel to the other as a result of transients is close to 0V.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV710 and TLV711 use an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered;

use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV710 and TLV711 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV710/ TLV711 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from a die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for the TLV710 evaluation module (EVM) are shown in [Table 1](#). The EVM is a 2-layer board with 2 ounces of copper per side. The dimension and layout are shown in [Figure 70](#) and [Figure 71](#). Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes in the heat-dissipating layer also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV710 and TLV711 are available from the Texas Instruments Web site at www.ti.com. The recommended land pattern for the DSE (SON-6) package is shown in [Figure 72](#).

Table 1. TLV710 EVM Dissipation Ratings

PACKAGE	$R_{\theta JA}$	$T_A < +25^\circ\text{C}$	$T_A = +70^\circ\text{C}$	$T_A = +85^\circ\text{C}$
DSE	170°C/W	585mW	320mW	235mW

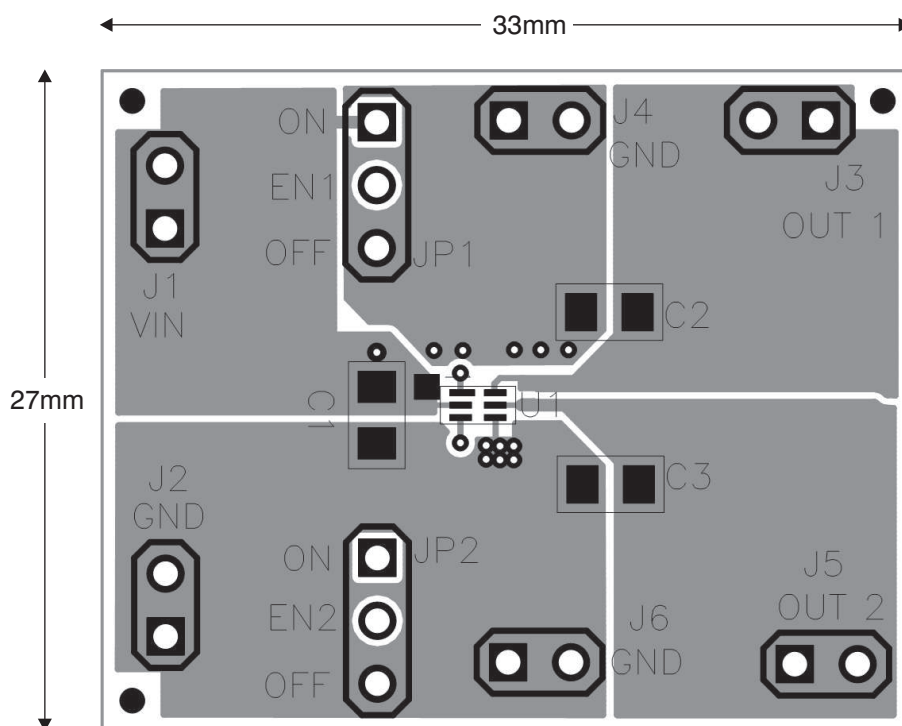


Figure 70. Top Layer

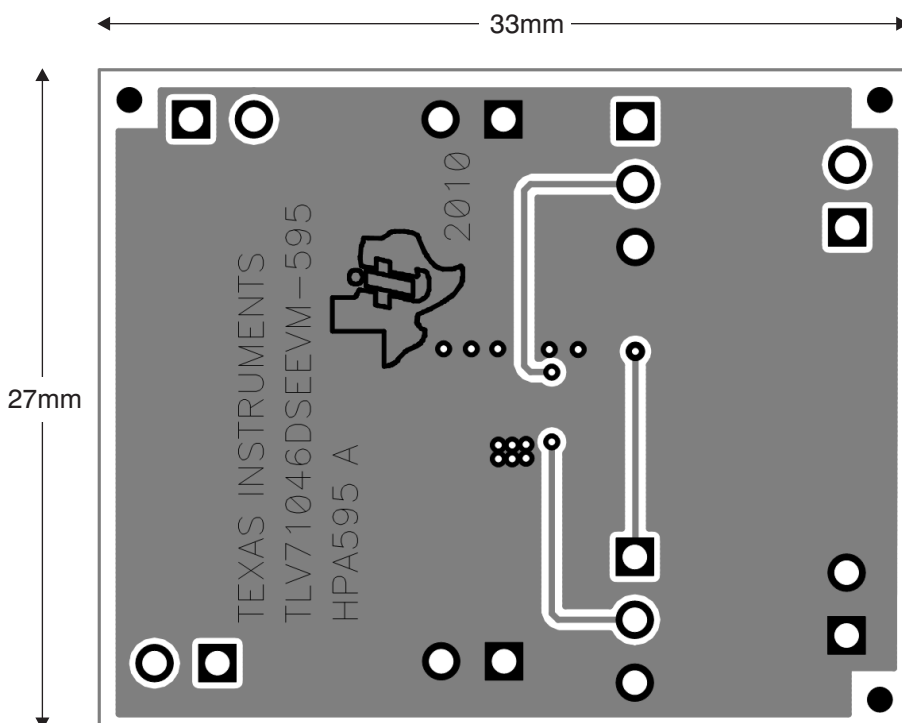
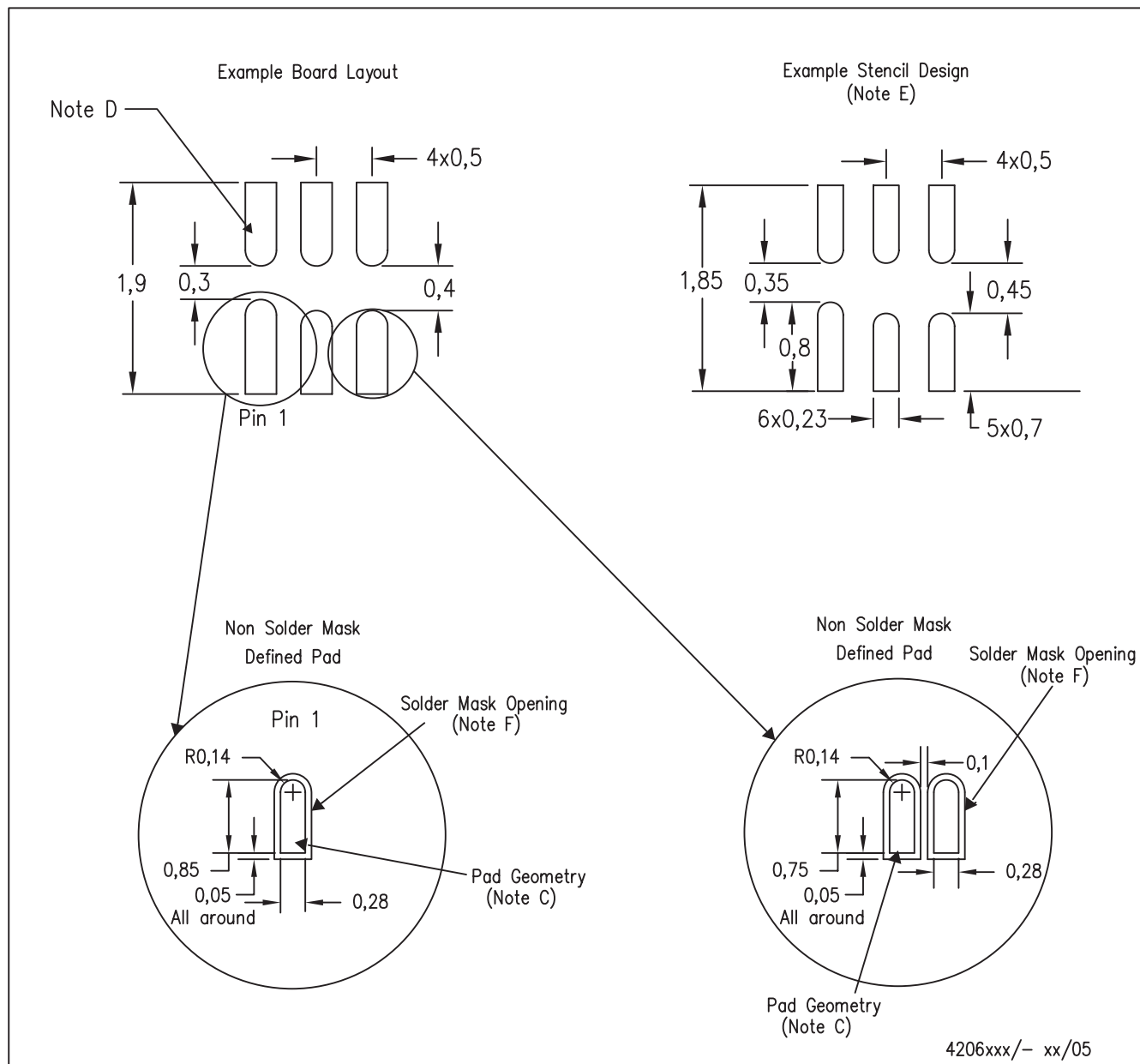


Figure 71. Bottom Layer

DSE (S–PDSO–N6)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC–7351 is recommended for alternate designs.
 - This package is a QFN that does not have a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

Figure 72. Land Pattern Drawing for DSE (SON-6) Package

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7101828DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW
TLV7101828DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW
TLV7101828DSERG4	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW
TLV7101828DSERG4.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW
TLV7101828DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW
TLV7101828DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW
TLV7103318DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UE
TLV7103318DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UE
TLV7103318DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UE
TLV7103318DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UE
TLV7111225DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BT
TLV7111225DSER.A	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BT
TLV7111225DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BT
TLV7111225DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BT
TLV7111225DSET.A	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BT
TLV7111225DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BT
TLV7111233DSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TP
TLV7111233DSER.A	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TP
TLV7111233DSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TP
TLV7111233DSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TP
TLV7111233DSET.A	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TP
TLV7111233DSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TP
TLV7111323DDSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WH
TLV7111323DDSER.B	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WH
TLV7111323DDSET	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WH
TLV7111323DDSET.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WH
TLV7111323DDSETG4	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WH
TLV7111323DDSETG4.B	Active	Production	WSO (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WH
TLV7111333DDSER	Active	Production	WSO (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YY

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7111333DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YY
TLV7111333DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YY
TLV7111333DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YY
TLV7111518DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UT
TLV7111518DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UT
TLV7111518DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UT
TLV7111518DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UT
TLV7111518DDSETG4.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	-	Call TI	Call TI	-40 to 125	
TLV7111533DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD
TLV7111533DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD
TLV7111533DDSERG4	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD
TLV7111533DDSERG4.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD
TLV7111533DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD
TLV7111533DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD
TLV7111812DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BS
TLV7111812DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BS
TLV7111812DSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BS
TLV7111812DSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BS
TLV7111812DSET.A	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BS
TLV7111812DSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BS
TLV7111830DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GB
TLV7111830DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GB
TLV7111830DSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GB
TLV7111830DSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GB
TLV7111830DSET.A	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GB
TLV7111830DSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GB
TLV7111833DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UQ
TLV7111833DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UQ
TLV7111833DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UQ
TLV7111833DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UQ
TLV7111930DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7111930DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
TLV7111930DSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
TLV7111930DSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
TLV7111930DSET.A	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
TLV7111930DSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CV
TLV71125125DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TM
TLV71125125DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TM
TLV71125125DSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TM
TLV71125125DSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TM
TLV71125125DSET.A	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TM
TLV71125125DSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TM
TLV7112525DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX
TLV7112525DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX
TLV7112525DSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX
TLV7112525DSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX
TLV7112525DSET.A	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX
TLV7112525DSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX
TLV71128512DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M
TLV71128512DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M
TLV71128512DSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M
TLV71128512DSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M
TLV71128512DSET.A	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M
TLV71128512DSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M
TLV71128518DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WV
TLV71128518DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WV
TLV71128518DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	WV
TLV71128518DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WV
TLV711285285DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UU
TLV711285285DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UU
TLV711285285DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UU
TLV711285285DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UU

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7113025DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BR
TLV7113025DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BR
TLV7113025DSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BR
TLV7113025DSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BR
TLV7113025DSET.A	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BR
TLV7113025DSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	BR
TLV7113030DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WS
TLV7113030DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WS
TLV7113030DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WS
TLV7113030DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WS
TLV7113318DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VW
TLV7113318DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VW
TLV7113318DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VW
TLV7113318DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VW
TLV71133285DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	YE
TLV71133285DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	YE
TLV71133285DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YE
TLV71133285DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YE
TLV7113330DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WZ
TLV7113330DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WZ
TLV7113330DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAU	Level-1-260C-UNLIM	-40 to 125	WZ
TLV7113330DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WZ
TLV7113333DDSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RV
TLV7113333DDSER.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RV
TLV7113333DDSERG4	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RV
TLV7113333DDSERG4.B	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	RV
TLV7113333DDSET	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RV
TLV7113333DDSET.B	Active	Production	WSON (DSE) 6	250 SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RV

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

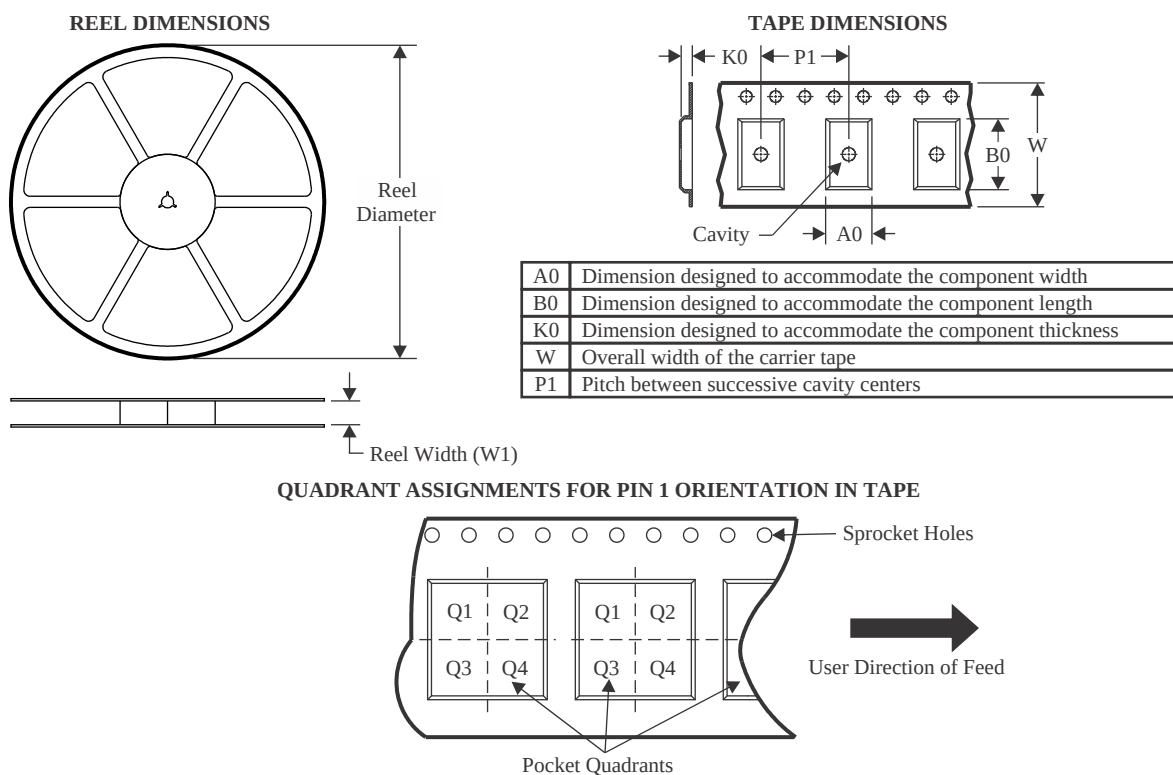
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV710 :

- Automotive : [TLV710-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION


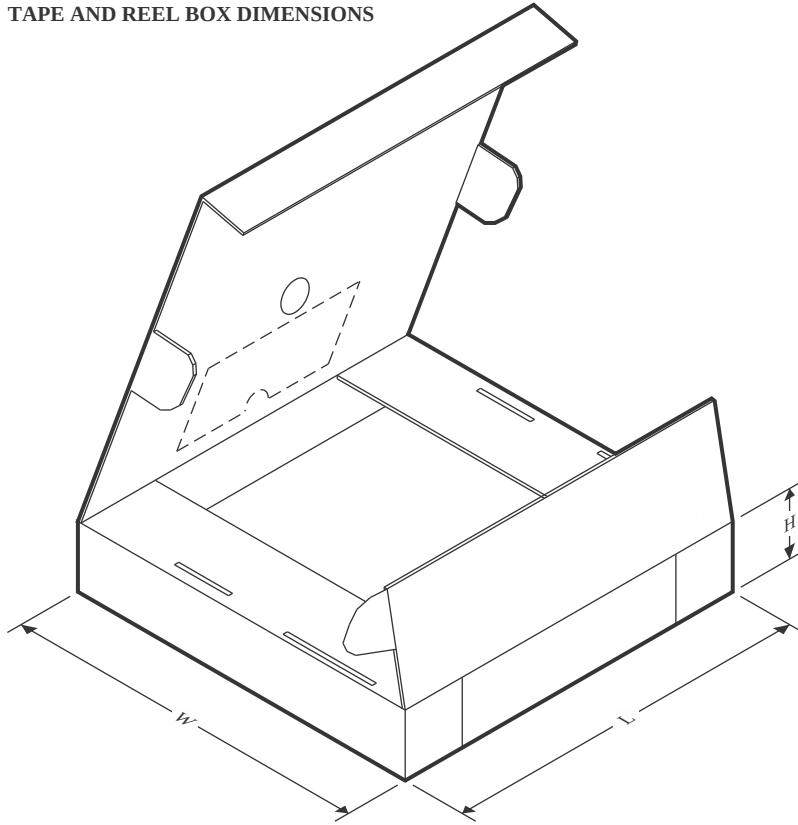
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7101828DSERG4	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7101828DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7103318DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7103318DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111225DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111225DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111233DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111233DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111323DDSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111323DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111323DDSETG4	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111333DDSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111333DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111518DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7111518DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111518DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7111533DDSERG4	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111533DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111812DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111812DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111830DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111830DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111833DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7111833DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7111930DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111930DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71125125DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71125125DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7112525DSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7112525DSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71128512DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71128512DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71128518DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV71128518DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV71128518DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV711285285DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV711285285DDSET	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV711285285DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV711285285DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113025DSER	WSO	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7113025DSET	WSO	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7113030DDSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113030DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113318DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113318DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113318DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71133285DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV71133285DDSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71133285DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71133285DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113330DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113330DDSER	WSO	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113330DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113330DDSET	WSO	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113333DDSER	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113333DDSERG4	WSO	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113333DDSET	WSO	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV711333DDSET	WSO8	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7101828DSERG4	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7101828DSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV7103318DSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7103318DSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV7111225DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV7111225DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV7111233DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV7111233DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV7111323DDSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7111323DDSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV7111323DDSETG4	WSON	DSE	6	250	200.0	183.0	25.0
TLV7111333DDSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7111333DDSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV7111518DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7111518DDSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV7111518DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7111533DDSERG4	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7111533DDSET	WSON	DSE	6	250	200.0	183.0	25.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7111812DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV7111812DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV7111830DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV7111830DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV7111833DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7111833DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7111930DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV7111930DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV71125125DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV71125125DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV7112525DSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7112525DSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV71128512DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV71128512DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV71128518DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV71128518DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV71128518DDSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV711285285DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV711285285DDSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV711285285DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV711285285DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113025DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV7113025DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV7113030DDSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7113030DDSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV7113318DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7113318DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113318DDSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV71133285DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV71133285DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV71133285DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV71133285DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113330DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7113330DDSER	WSON	DSE	6	3000	200.0	183.0	25.0
TLV7113330DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113330DDSET	WSON	DSE	6	250	200.0	183.0	25.0
TLV7113333DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7113333DDSERG4	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7113333DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113333DDSET	WSON	DSE	6	250	203.0	203.0	35.0

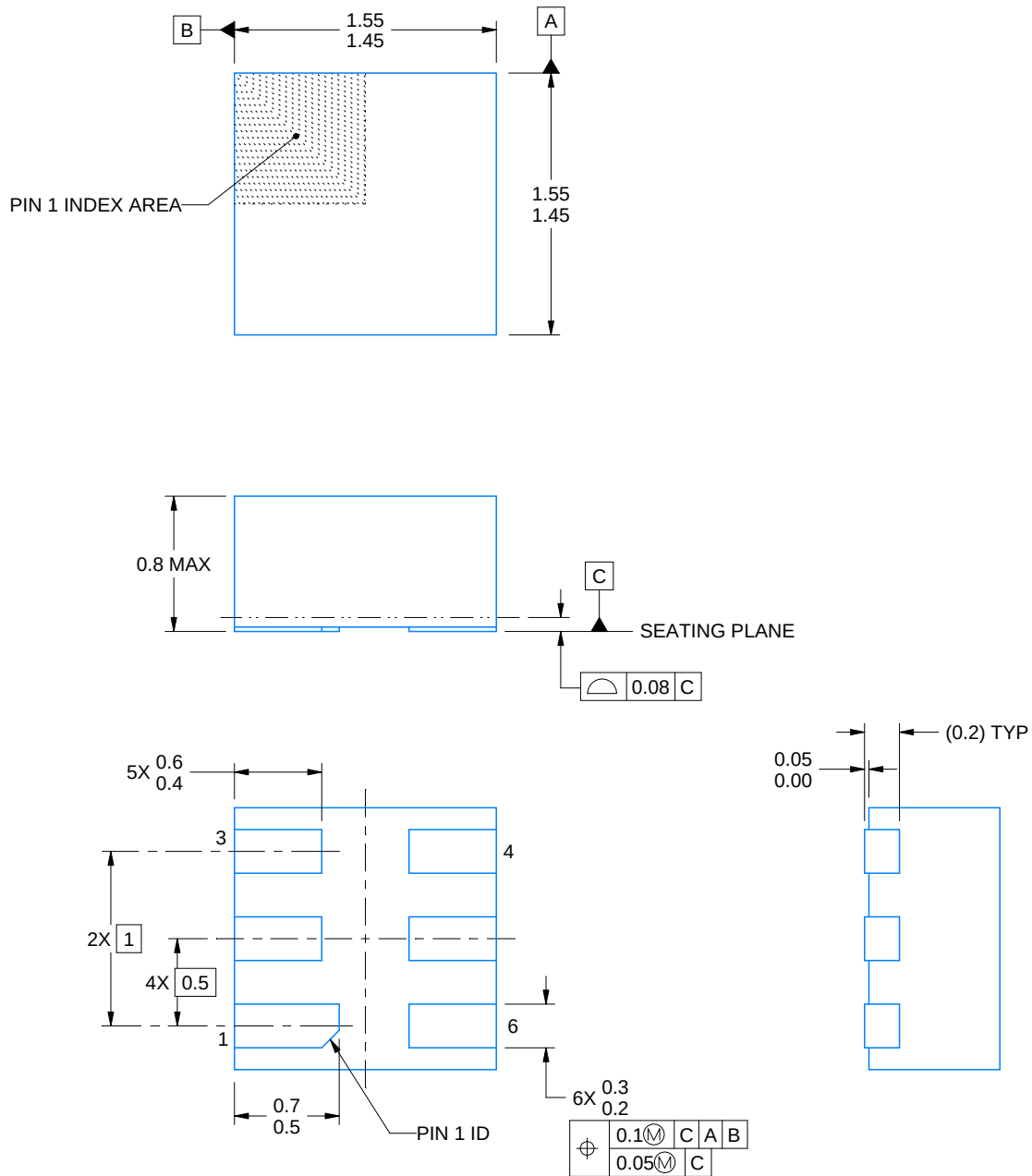
DSE0006A



PACKAGE OUTLINE

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220552/B 01/2024

NOTES:

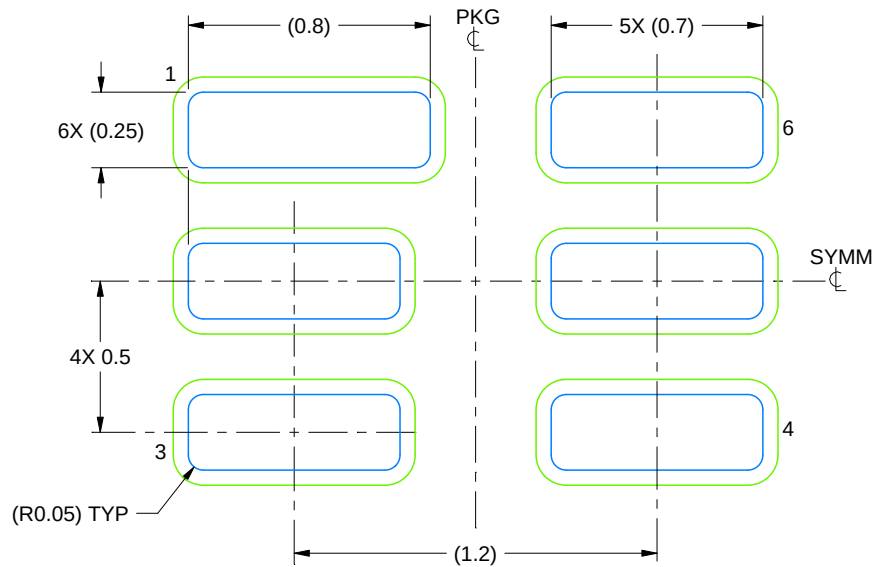
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

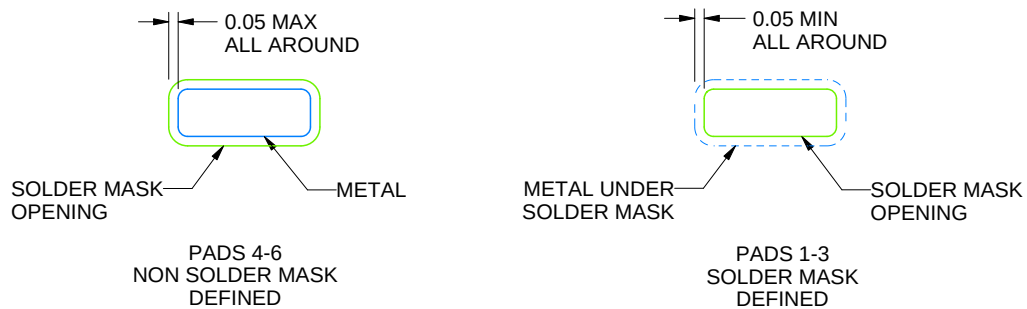
DSE0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

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NOTES: (continued)

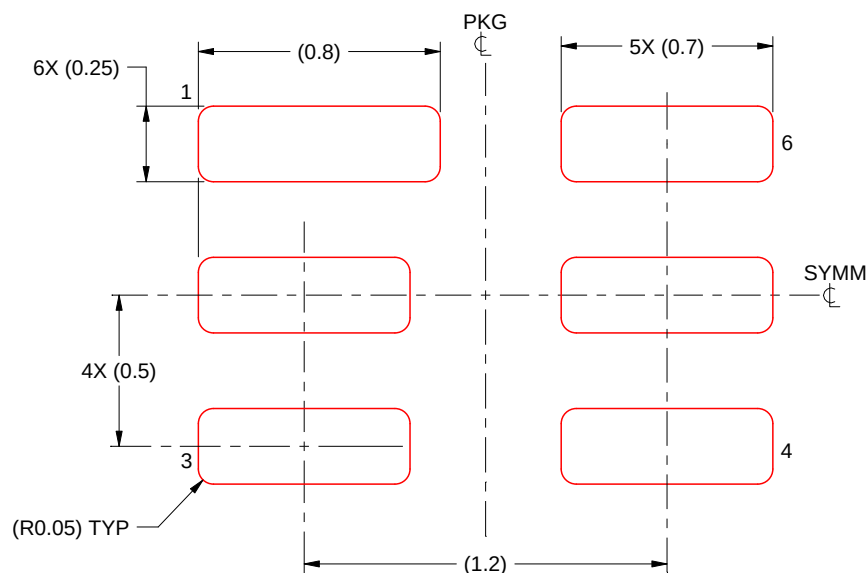
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSE0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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