











TLV6703 SBOS865B - JANUARY 2018-REVISED NOVEMBER 2019

TLV6703 Micropower, 18-V Comparator With Integrated Reference

Features

Wide supply voltage range: 1.8 V to 18 V

Adjustable threshold: down to 400 mV

High threshold accuracy:

0.5% Max at 25°C

1.0% Max over temperature

Low quiescent current: 5.5 µA (Typ)

Open-drain output

Internal hysteresis: 5.5 mV (Typ)

Temperature range: -40°C to +125°C

Package: thin SOT-23-6

WSON-6

Applications

Notebook PCs and tablets

Smartphones

Digital cameras

Video game controllers

Relays and circuit breakers

Portable medical devices

Door and window sensors

Portable- and battery-powered products

3 Description

The TLV6703 high voltage comparator operates over a 1.8-V to 18-V range. The TLV6703 has a highaccuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The monitored voltage can be set with the use of external resistors.

The OUT pin is driven low when the voltage at the SENSE pin drops below (V_{IT}-), and goes high when the voltage returns above the respective threshold (V_{IT+}). The comparator in the TLV6703 includes builtin hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering.

The TLV6703 is available in a Thin SOT-23-6 package and a leadless WSON-6; all package variants are specified over the junction temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)	
TLV6703	SOT-23 (6)	2.90 mm × 1.60 mm	
	WSON (6)	1.50 mm × 1.50 mm	

(1) For all available packages, see the package option addendum at the end of the datasheet.

Simplified Block Diagram

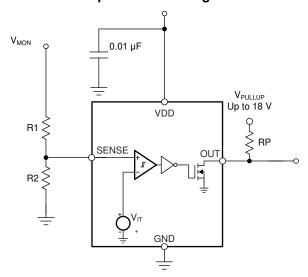




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4 Revision History

Changes from Revision A (April 2018) to Revision B	Page
Added WSON-6 package	1
Changes from Original (Jan 2018) to Revision A	Page
Changed Advance Information to Production Data	1

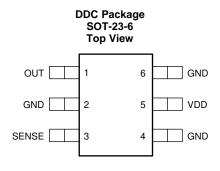
5 Device Comparison Table

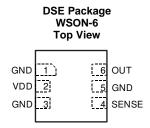
Table 1. TLV67xx Integrated Comparator Family

PART NUMBER	PART NUMBER CONFIGURATION		THRESHOLD ACCURACY OVER TEMPERATURE
TLV6700	Window	1.8 V to 18 V	1%
TLV6703	Non-Inverting Single Channel	1.8 V to 18 V	1%
TLV6710	Window	1.8 V to 36 V	0.75%
TLV6713	Non-Inverting Single Channel	1.8 V to 36 V	0.75%



6 Pin Configuration and Functions





Pin Functions

	PIN		1/0	DESCRIPTION
NAME	DDC	DSE	I/O	DESCRIPTION
GND	2, 4, 6	1, 3, 5	_	Connect all three pins to ground.
OUT	1	6	0	SENSE comparator has an open-drain output. OUT is driven low when SENSE is below (V_{IT-}) . OUT goes high when SENSE returns above the respective threshold (V_{IT+}) .
SENSE	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage ($V_{\text{IT-}}$), OUT is driven low.
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1- μ F ceramic capacitor close to this pin.



7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage ⁽²⁾	VDD	-0.3	20	
	OUT	-0.3	20	V
	SENSE	-0.3	7	
Current	OUT (output sink current)		40	mA
Temperature	Operating junction, T _J	-40	125	°C
	Storage, T _{stg}	-65	150	

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
,	,	Floatractatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	.,
,	V _(ESD)	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	V

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM MAX	UNIT
V_{DD}	Supply voltage		1.8	18	V
V_{I}	Input voltage	SENSE	0	6.5	V
Vo	Output voltage	OUT	0	18	V

7.4 Thermal Information

		TLV6	703	
	THERMAL METRIC ⁽¹⁾	DDC (SOT)	DSE (WSON)	UNIT
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.5	128.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	153.8	°C/W
ΨЈТ	Junction-to-top characterization parameter	0.8	11.9	°C/W
ΨЈВ	Junction-to-board characterization parameter	52.8	157.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor an IC Package Thermal Metrics application report.

⁽²⁾ All voltages are with respect to network ground pin.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.5 Electrical Characteristics

Over the operating temperature range of $T_J = -40^{\circ}\text{C}$ to +125°C, and 1.8 V < V_{DD} < 18 V (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$ and $V_{DD} = 5$ V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _(POR)	Power-on reset voltage (1)	V _{OL} max = 0.2 V, output sink current = 15 μA			0.8	V
	Docition and install through all districts	V _{DD} = 1.8V and 18 V, T _J = 25°C	398	400	402.5	\/
V_{IT+}	Positive-going input threshold voltage	$V_{DD} = 1.8V$ and 18 V, $T_{J} = -40^{\circ}C$ to 125°C	396		404	mV
	No matical matical district the matical district and	V _{DD} = 1.8V and 18 V, T _J = 25°C	391.6	394.5	397.5	\/
V_{IT-}	Negative-going input threshold voltage	V _{DD} = 1.8V and 18 V, T _J = -40°C to 125°C	387		400	mV
V _{hys}	Hysteresis voltage (hys = $V_{IT+} - V_{IT-}$)			5.5	12	mV
I _(SENSE)	Input current (at the SENSE pin)	V _{DD} = 1.8 V and 18 V, V _I = 6.5 V	-25	1	25	nA
		V _{DD} = 1.3 V, output sink current = 0.4 mA			250	
V_{OL}	Low-level output voltage	V _{DD} = 1.8 V, output sink current = 3 mA			250	mV
		V _{DD} = 5 V, output sink current = 5 mA			250	
		V_{DD} = 1.8 V and 18 V, V_{O} = V_{DD}			300	A
I _{lkg(OD)}	Open-drain output leakage-current	V _{DD} = 1.8 V, V _O = 18 V			300	nA
		V _{DD} = 1.8 V, no load		5.5	11	
	Complex compant	V _{DD} = 5 V		6	13	^
I _{DD}	Supply current	V _{DD} = 12 V		6	13	μA
		V _{DD} = 18 V		7	13	
UVLO	Undervoltage lockout (2)	V _{DD} falling	1.3		1.7	V

The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)} > 15 \mu s/V$. Below $V_{(POR)}$, the output cannot be determined. When V_{DD} falls below UVLO, OUT is driven low. The output cannot be determined below $V_{(POR)}$.



7.6 Timing Requirements

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
t _{pd(HL)}	High-to-low propagation delay (1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 k Ω , V_{OH} = 0.9 x V_{DD} , V_{OL} = 400 mV, see Figure 1		18		μs
t _{pd(LH)}	Low-to-high propagation delay (1)	V_{DD} = 5 V, 10-mV input overdrive, R _P = 10 k Ω , V _{OH} = 0.9 x V _{DD} , V _{OL} = 400 mV, see Figure 1		29		μs
t _{d(start)}	Start-up delay (2)			150		μs

- (1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).
- (2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs before the output is in a correct state.

7.7 Switching Characteristics

over operating temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _r	Output rise time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 k Ω , V_O = (0.1 to 0.9) × V_{DD}		2.2		μs
t _f	Output fall time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 k Ω , V_O = (0.1 to 0.9) × V_{DD}		0.22		μs

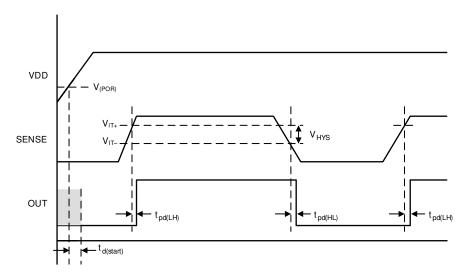
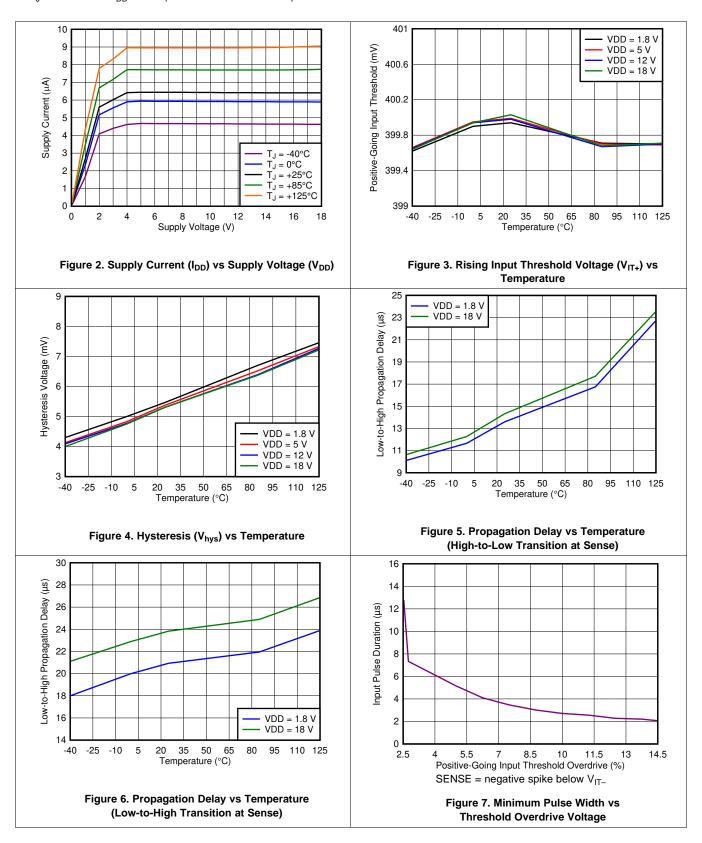


Figure 1. Timing Diagram



7.8 Typical Characteristics

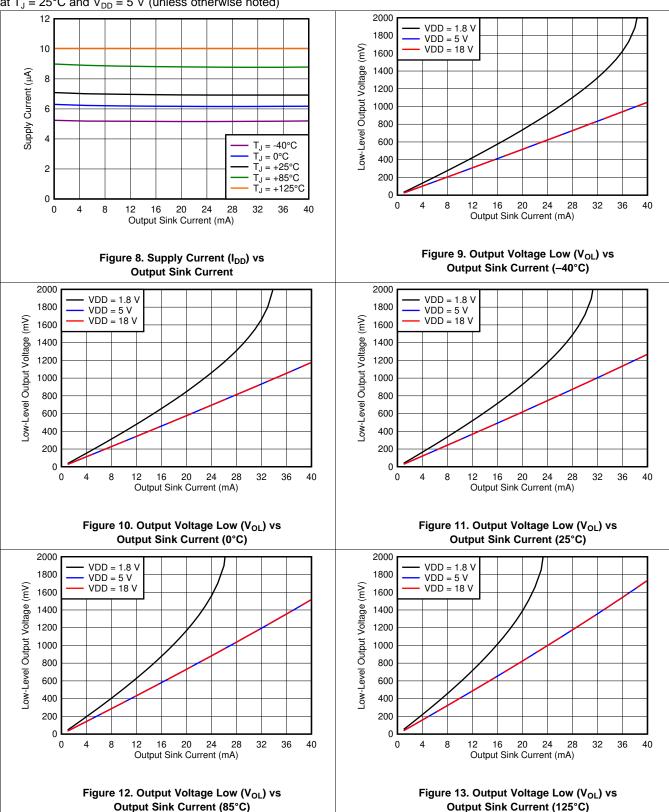
at $T_J = 25^{\circ}C$ and $V_{DD} = 5 V$ (unless otherwise noted)



NSTRUMENTS

Typical Characteristics (continued)

at $T_J = 25$ °C and $V_{DD} = 5$ V (unless otherwise noted)



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8 Detailed Description

8.1 Overview

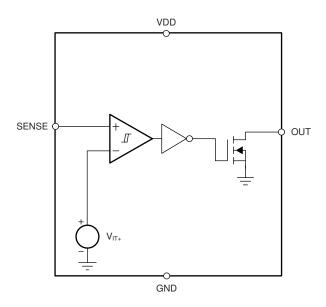
The TLV6703 provides precision voltage detection. The TLV6703 is a wide-supply voltage range (1.8 V to 18 V) comparator with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The output is also rated to 18 V, independant of supply voltage, and can sink up to 40 mA.

The TLV6703 asserts the output signal, as shown in Table 2. To monitor any voltage above 0.4 V, set the input using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

Table 2. TLV6703 Truth Table

CONDITION	OUTPUT	OUTPUT STATE
SENSE > V _{IT+}	OUT high	Output high impedance
SENSE < V _{IT} _	OUT low	Output sinking

8.2 Functional Block Diagram





8.3 Feature Description

8.3.1 Input Pin (SENSE)

The TLV6703 comparator has two inputs: one external input, and one input internally connected to the internal 400mV reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400 mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5 V, regardless of the device supply voltage. Although not required in most cases, to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below (V_{IT-}). When the voltage exceeds V_{IT+} , the output (OUT) goes to a high-impedance state; see Figure 1.

8.3.2 Output Pin (OUT)

In a typical TLV6703 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6703 device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TLV6703 output can be pulled up to 18 V, independent of the device supply voltage.

Table 2 and the *Input Pin (SENSE)* section describe how the output is asserted or de-asserted. See Figure 1 for a timing diagram that describes the relationship between threshold voltage and the respective output.

8.3.3 Immunity to Input-Pin Voltage Transients

The TLV6703 is relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see Figure 7, *Minimum Pulse Width vs Threshold Overdrive Voltage*.

8.4 Device Functional Modes

8.4.1 Normal Operation ($V_{DD} > UVLO$)

When the voltage on V_{DD} is greater than 1.8 V for at least 150 μ s, the OUT signal correspond to the voltage on SENSE as listed in Table 2.

8.4.2 Undervoltage Lockout $(V_{(POR)} < V_{DD} < UVLO)$

When the voltage on V_{DD} is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUT signal is asserted regardless of the voltage on SENSE.

8.4.3 Power-On Reset $(V_{DD} < V_{(POR)})$

When the voltage on V_{DD} is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), SENSE is in a high-impedance state.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV6703 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8 V to 18 V. The device has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

9.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The output is often tied to V_{DD} through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than V_{DD} to correctly interface with the reset and enable pins of other devices.

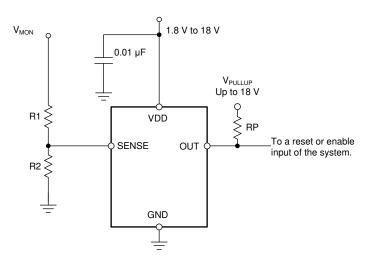


Figure 14. Interfacing to a Voltage Other Than V_{DD}

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Product Folder Links: *TLV6703*



Application Information (continued)

9.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD} . In these applications the resistor divider is simply connected to the V_{DD} rail.

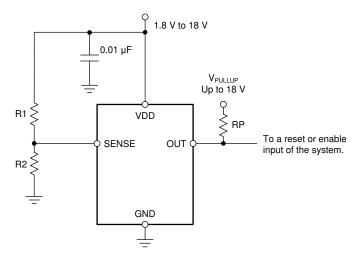
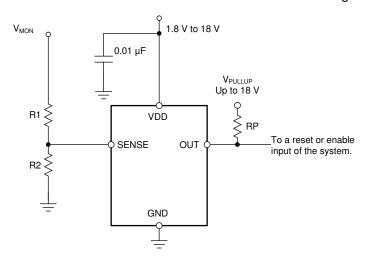


Figure 15. Monitoring the Same Voltage as V_{DD}

9.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD} . In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.



NOTE: The input can monitor a voltage greater than maximum V_{DD} with the use of an external resistor divider network.

Figure 16. Monitoring a Voltage Other Than V_{DD}



9.2 Typical Application

The TLV6703 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8 to 18 V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.

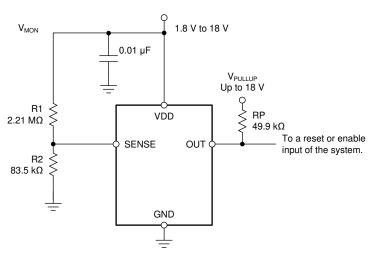


Figure 17. Wide VIN Voltage Monitor

9.2.1 Design Requirements

For this design example, use the values summarized in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT		
Monitored voltage	12-V nominal rail with maximum falling threshold of 10%	V _{MON(UV)} = 10.99 V (8.33%)		

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using Equation 1 to determine $V_{MON(UV)}$.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-}$$
(1)

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- V_{MON(UV)} is the target voltage at which an undervoltage condition is detected

Choose R_{TOTAL} (= R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report SLVA450, *Optimizing Resistor Dividers at a Comparator Input*, available for download from www.ti.com.



9.2.2.2 Pullup Resistor Selection

To ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current $(I_{lkg(OD)})$ multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the *Electrical Characteristics*.

Use Equation 2 to calculate the value of the pullup resistor.

$$\frac{\left(V_{HI} - V_{PU}\right)}{I_{lkg(OD)}} \ge R_{PU} \ge \frac{V_{PU}}{I_{O}} \tag{2}$$

9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a $0.1-\mu F$ low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

9.2.3 Application Curves

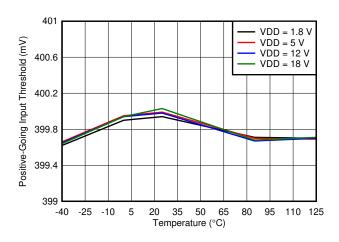


Figure 18. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

9.3 Dos and Don'ts

Do connect a 0.1-µF decoupling capacitor from V_{DD} to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}) .



10 Power-Supply Recommendations

These devices operate from an input voltage supply range between 1.8 V and 18 V.

11 Layout

11.1 Layout Guidelines

Placing a 0.1-µF capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

11.2 Layout Example

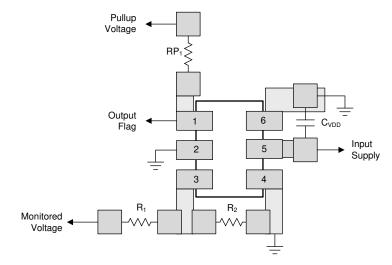


Figure 19. Layout Example



12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

The *DIP Adapter Evaluation Module* allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of protoyping and bench evaluation.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

www.ti.com

7-Oct-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	(.,	(=)			(0)	(4)	(5)		(0)
TLV6703DDCR	Active	Production	SOT-23- THIN (DDC) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1
TLV6703DDCR.A	Active	Production	SOT-23- THIN (DDC) 6	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1
TLV6703DDCT	Active	Production	SOT-23- THIN (DDC) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1
TLV6703DDCT.A	Active	Production	SOT-23- THIN (DDC) 6	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1
TLV6703DSER	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE
TLV6703DSER.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE
TLV6703DSERG4	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE
TLV6703DSERG4.A	Active	Production	WSON (DSE) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 7-Oct-2025

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OTHER QUALIFIED VERSIONS OF TLV6703:

Automotive : TLV6703-Q1

NOTE: Qualified Version Definitions:

Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6703DDCR	SOT-23- THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6703DDCT	SOT-23- THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6703DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV6703DSERG4	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

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*All dimensions are nominal

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	Device	Package Type Package Drawing		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	TLV6703DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
ı	TLV6703DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0
ı	TLV6703DSER	WSON	DSE	6	3000	205.0	200.0	33.0
	TLV6703DSERG4	WSON	DSE	6	3000	205.0	200.0	33.0



SMALL OUTLINE TRANSISTOR



NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC MO-193.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

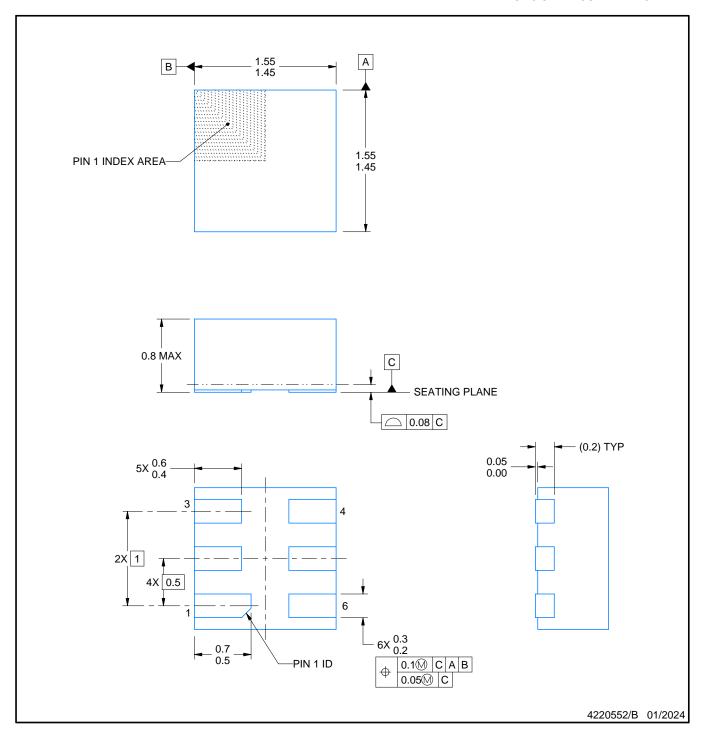
- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

 7. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE - NO LEAD

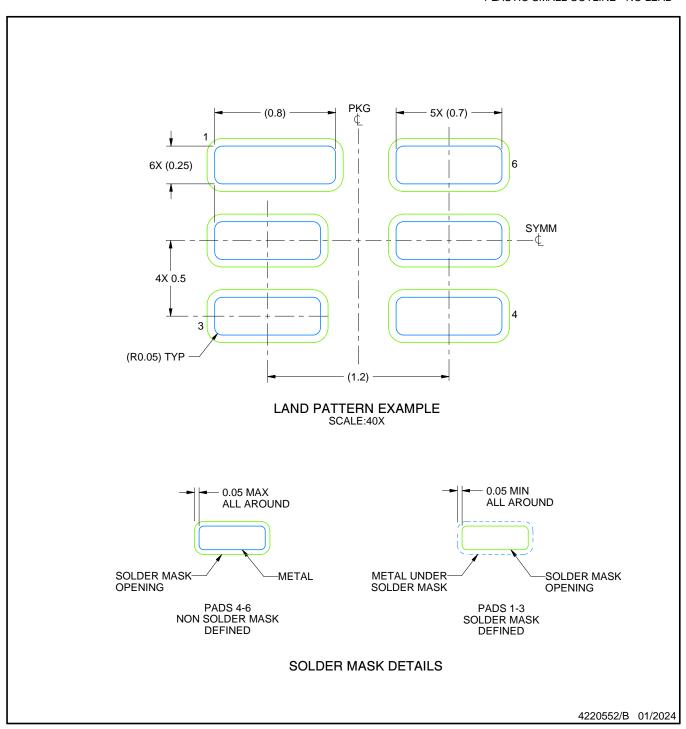


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.



PLASTIC SMALL OUTLINE - NO LEAD

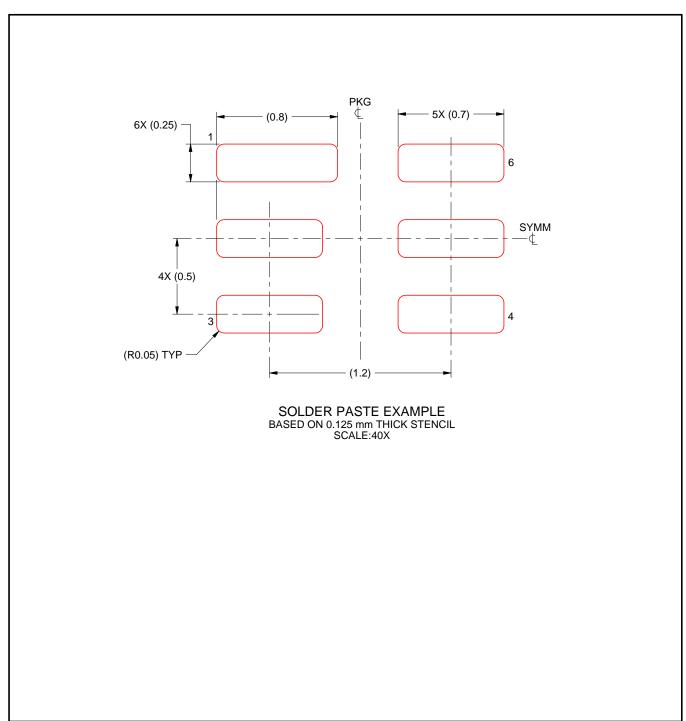


NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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