TLV61290 Wide-Voltage Battery Front-End DC/DC Converter for Single-Cell Li-Ion, Ni-Rich, Si-Anode Applications

1 Features

- Wide V_{IN} range from 2.0V to 5.0V
  - Start up input voltage: 2.2V
- Programmable average input current limit (3.5A to 8A) via I^2C
- Programmable output voltage (2.35V to 5.0V) via I^2C, default 3.4V
- 97.99% efficiency at V_{IN} = 3.3V, V_{OUT} = 3.4V, I_{OUT} = 1A
- 95.73% efficiency at V_{IN} = 3.3V, V_{OUT} = 3.4V, I_{OUT} = 3A
- <300mV undershoot at V_{IN} = 2.7V, V_{OUT} = 3.4V, I_{OUT} = 0A → 3A (0.2A/µs slew rate)
- Integrated bypass MOSFET (10mΩ), high-side MOSFET (10mΩ), low-side MOSFET (10mΩ)
- Auto bypass mode when V_{IN} > V_{OUT}
- Programmable auto PFM operation, Forced PWM operation or Ultrasonic mode operation (avoid audio band noise) during light load condition
- Spread spectrum modulation and EMI improvement
- Output discharge function when EN logic is low
- True disconnection between input and output during shutdown
- Thermal shutdown and over current protection
- I^2C compatible I/F up to 1Mbps
- 1.2V I/O logic control interface
- 16-ball WCSP package

2 Applications

- Mobile phones
- Tablet
- Optical module
- 4G, 5G Mini-module Data Card
- Satellite Communication
- RF Power Amplifier

3 Description

The TLV61290 provides a power supply solution for products powered by a nickel-rich, silicon anode, Li-ion or LiFePO4 battery. The voltage range is optimized for single-cell portable applications like in smart-phones or POS terminal.

Used as a high-power pre-regulator, the device extends the battery run-time and overcomes input current and voltage limitations of the powered system. With a wide input voltage range of 2.0V to 5.0V. Program the output voltage by I^2C up to 5.0V, and the default output voltage is 3.4V.

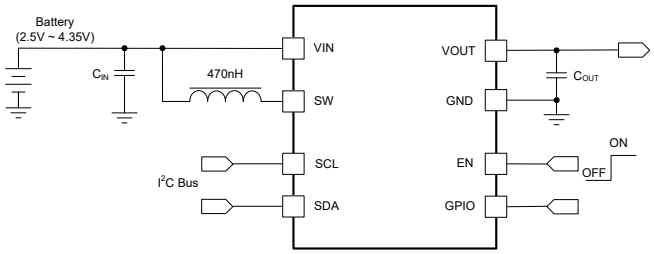
During operation, when the battery is in a good state of charge, the TLV61290 will work in bypass mode, connecting the battery to the power supply system through the bypass FET. If the battery gets to a lower state of charge and its voltage becomes lower than the desired minimum system voltage, the device seamlessly transits into boost mode to use the full battery capacity.

The TLV61290 offers a very small solution size with 16-ball YBG package.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TLV61290x	YBG (16)	1.58mm x 1.58mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Circuit

Table of Contents

4 Device Comparison Table

PART NUMBER	DEFAULT GPIO CONFIGURATION
TLV61290	GPIO = ADDR, I^2C address selection pin(75h when ADDR is low, 76h when ADDR is high, 77h when ADDR is floating). The address is locked when the start-up sequence is successfully completed.
TLV612901 (1)	GPIO = VSEL, DC/DC boost or bypass threshold selection pin(VOUTFLOORSET when VSEL is low, VOUTROOFSET when VSEL is high)

(1) Product preview. Contact TI factory for more information.

5 Pin Configuration and Functions

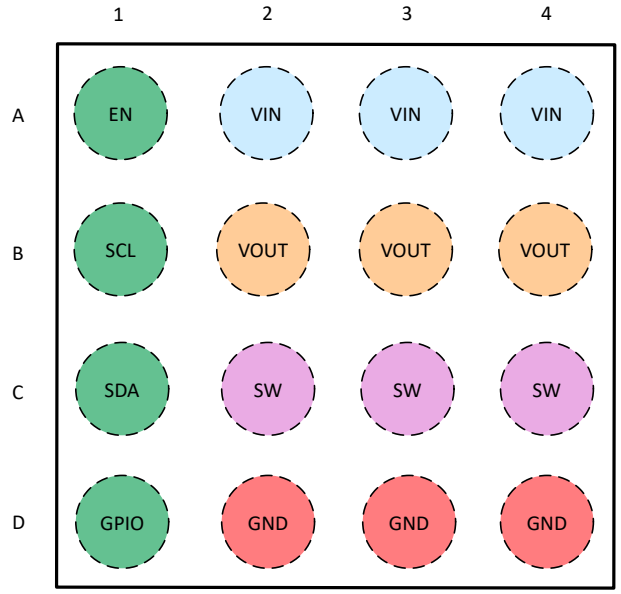


Figure 5-1. TLV61290 YBG Package, 16-Pin (Top View)

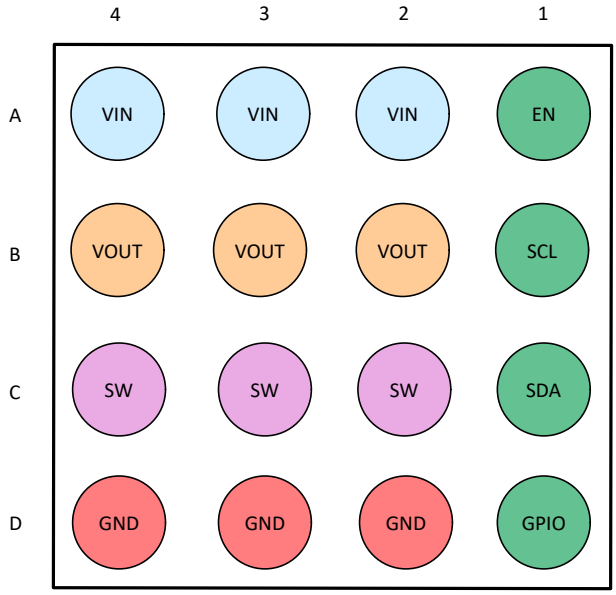


Figure 5-2. TLV61290 YBG Package, 16-Pin (Bottom View)

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	A1	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode. Logic high voltage while setting ENABLE_bit = 11 through I^2C also disables the device and turns it into shutdown mode.
SCL	B1	I	Serial interface clock line. Terminate this pin and do not leave it floating.
SDA	C1	I	Serial interface address/data line. Terminate this pin and do not leave it floating.
GPIO	D1	I/O	Configure the pin as ADDR or VSEL function. For TLV61290, the default configuration is ADDR function. For TLV612901, the default configuration is VSEL function.
			ADDR: I^2C target address selection. I^2C target address is 75h when ADDR is low, I^2C target address is 76h when ADDR is high, I^2C target address is 77h when ADDR is floating. The address is locked when the start-up sequence is successfully completed.
			VSEL: DC/DC boost or bypass threshold selection pin. (refer to Section 7.3.1)
VIN	A2, A3, A4	PWR	Power supply input.
VOUT	B2, B3, B4	PWR	Boost converter output.
SW	C2, C3, C4	PWR	The switch pin of the converter. This pin is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
GND	D2, D3, D4	PWR	Ground pin of the IC. The GND pad of output capacitor must be close to the GND pin. Layout example is shown in Layout Example.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input voltage	VIN, SW, EN, VOUT, SCL, SDA, GPIO(2)	DC	-0.3	7	V
Input voltage	SW spike at 10ns(2)	AC	-0.7	8	V
Input voltage	SW spike at 1ns(2)	AC	-0.7	8.5	V
Temperature range	Operating virtual junction, T_J		-40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.0		5	V
V_{OUT}	Output voltage setting range	2.35		5	V
L	Effective inductance range	330	470	560	nH
C_{in}	Effective input capacitance range		5		µF
C_O	Effective output capacitance range, $I_{out} \le 4A$	10(1)	14		µF
	Effective output capacitance range, $6A \ge I_{out} > 4A$(2)	20(1)			µF
T_J	Operating junction temperature	-40		125	°C

(1) The minimum value only apply to a typical device with input voltage is higher than 2.7V, it is not specified by simulation at corner case.
(2) TI recommends to increase the output capacitance when the output curren is higher than 4A.

6.4 Thermal Information

THERMAL METRIC(1)		TLV61290 YBG (16 PINS) Standard	TLV61290 YBG (16 PINS) EVM(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78	40.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	0.6	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.4	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13	16.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Measured on TLV61290VM-076, 4-layer, 2oz copper 92.2 mm×59.2 mm PCB.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 2.0V to 5.0V, V_{OUT} = 3.4V (or V_{IN}, whichever is higher), EN = 1.2V, GPIO= 1.2V. Typical values are at V_{IN} = 3.2V, V_{OUT} = 3.4V, EN = 1.2V, T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2		5	V
V_{UVLO}	Undervoltage lockout threshold	Rising		2.1	2.2	V
		Falling		1.9	2	V
		Hysteresis		0.2		V
I_Q	Operating quiescent current into V_{IN}	DC/DC boost mode. Device not switching EN = VIN, ENABLE_bit = 01 –40°C ≤ T_J ≤ 85°C		40	52	µA
	Operating quiescent current into V_{OUT}	DC/DC boost mode. Device not switching EN = VIN, ENABLE_bit = 01 –40°C ≤ T_J ≤ 85°C		9	20	µA
	Operating quiescent current in auto bypass mode	True bypass mode (auto) EN = VIN, ENABLE_bit = 01, VIN=3.6V –40°C ≤ T_J ≤ 85°C		30	40	µA
	Operating quiescent current in forced bypass mode	True bypass mode (forced) EN = VIN, ENABLE_bit = 10 –40°C ≤ T_J ≤ 85°C		30	42	µA
I_{SD}	Shutdown current	Shutdown mode EN = GND, VOUT = GND –40°C ≤ T_J ≤ 85°C		0.8		µA
		Shutdown mode, but I^2C block is active. EN = VIN, ENABLE_bit = 11 –40°C ≤ T_J ≤ 85°C		16	31	µA
EN, SDA, SCL, GPIO						
V_{IL}	Low-level input voltage		0.33			V
V_{IH}	High-level input voltage				0.82	V
V_{OL}	Low-level output voltage (SDA)	I_{OL} = 8mA			0.36	V
R_{PD}	EN pull-down resistance	Applied voltage < 0.4V		800		kΩ
I_{lkg}	Input leakage current	–40°C ≤ T_J ≤ 85°C			0.1	µA
OUTPUT						
V_{OUT}	Output voltage setting range		2.35		5	V
V_{OUT_PWM}	DC voltage accuracy	2.2V ≤ V_{IN} ≤ V_{OUT_TAR} - 150mV PWM/PFM operation.	-1.5		1.5	%
$V_{OUT\_BP\_ENTER}$	Enter bypass mode threshold	MODE_CTRL = 01 or 11, PFM or Ultrasonic mode		V_{OUT_PWM}*(1+1%)		%
$V_{OUT\_BP\_ENTER}$	Enter bypass mode threshold	MODE_CTRL = 10, FPWM mode		V_{OUT_PWM}*(1+2%)		%
$V_{OUT\_BP\_EXIT}$	Exit bypass mode threshold			V_{OUT_PWM}-50 mV		mV
POWER SWITCH						

6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 2.0V to 5.0V, V_{OUT} = 3.4V (or V_{IN}, whichever is higher), EN = 1.2V, GPIO= 1.2V. Typical values are at V_{IN} = 3.2V, V_{OUT} = 3.4V, EN = 1.2V, T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Low-side switch MOSFET on resistance	V_{OUT} = 4.5V		8	16	mΩ
	High-side rectifier MOSFET on resistance	V_{OUT} = 4.5V		8	16	mΩ
	Low-side switch MOSFET on resistance	V_{OUT} = 3.4V		10	20	mΩ
	High-side rectifier MOSFET on resistance	V_{OUT} = 3.4V		10	20	mΩ
	High-side bypass MOSFET on resistance	V_{OUT} = 2.35V to 5V		10	20	mΩ
I_{LIM_SW}	Average Inductor current limit	ILIM_BOOST = 0110(default), 2.7V ≤ V_{IN} ≤ 4.85V	6	8	9	A
	Average Inductor current limit adjustable range via I^2C	Typical value, 2.7V ≤ V_{IN} ≤ 4.85V	3.5		8	A
$I_{LIM\_REVERSE}$	Reverse current limit (FPWM operation)	MODE_CTRL = 10		-1		A
I_{LIM_BP}	Bypass mode current limit (Forced)	ENABLE_bit = 10, ILIM_FPT = 011 (default)		10		A
	Bypass mode current limit (Auto)	ENABLE_bit = 01, ILIM_APT = 011 (default)		10		A
I_{LIM_DOWN2}	Down mode inductor valley current limit	0.6V < V_{OUT} <= V_{IN} - 2V		1		A
I_{LIM_DOWN3}	Down mode inductor valley current limit	V_{IN} - 2V < V_{OUT} <= V_{IN}		50%		$I_{LIM\_SW\_VALLEY}$
I_{lkg}	Reverse leakage current into SW-GND	EN = GND, V_{IN} = V_{OUT} = V_{SW} = 5V, T_J = 25°C		0.1	1	µA
		EN = GND, V_{IN} = V_{OUT} = V_{SW} = 5V –40°C ≤ T_J ≤ 85°C		0.1	40	µA
	Reverse leakage current into SW-VOUT	EN = GND, V_{IN} = V_{SW} = 5V, V_{OUT}=GND, T_J = 25°C		0.1	1	µA
		EN = GND, V_{IN} = V_{SW} = 5V, V_{OUT}=GND –40°C ≤ T_J ≤ 85°C		0.1	40	µA
	Reverse leakage current into VIN-VOUT	EN = GND, V_{IN} = V_{SW} = 5V, V_{OUT}=GND, T_J = 25°C		0.1	1	µA
		EN = GND, V_{IN} = V_{SW} = 5V, V_{OUT}=GND –40°C ≤ T_J ≤ 85°C		0.1	40	µA
OSCILLATOR						
T_{ON_MIN}	Minimum On time	PWM mode		50		ns
$F_{sw\_min\_fpwm}$	Minimum switching frequency in FPWM	MODE_CTRL = 10, FPWM operation	200			kHz
$F_{sw\_min\_pfm}$	Minimum switching frequency in Ultrasonic mode	MODE_CTRL = 11, Ultrasonic operation	23			kHz
F_{DITHER}	Spread Spectrum dithering frequency	V_{IN}= 3.2V, V_{OUT}=3.4V, MODE_CTRL = 10, SSFM = 1		±8%		F_{sw}
$F_{PATTERN}$	Spread Spectrum pattern frequency	V_{IN}= 3.2V, V_{OUT}=3.4V, MODE_CTRL = 10, SSFM = 1		0.5%		F_{sw}
THERMAL SHUTDOWN, HOT DIE DETECTOR						
T_{SD}	Thermal shutdown	T_J rising		165		°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		
TIMING						
t_{ss}	Soft startup time	Internal SS ramp time		400		µs

6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 2.0V to 5.0V, V_{OUT} = 3.4V (or V_{IN}, whichever is higher), EN = 1.2V, GPIO= 1.2V. Typical values are at V_{IN} = 3.2V, V_{OUT} = 3.4V, EN = 1.2V, T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{hiccup_on}	Hiccup on time	HICCUP_MODE bit = 1		1		ms
t_{hiccup_off}	Hiccup off time	HICCUP_MODE bit = 1		19		ms

6.6 System Characteristics

The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to T_A = 25℃ only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_A = –40℃ to 85℃ (unless otherwise noted). These specifications are not specified by production testing.

PARAMETERS		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{OUT}	Adjustable output voltage load regulation(1)	PFM/PWM operation, don't include USM, T_A=25°C	-1		+1.5	%
	Adjustable output voltage line regulation(2)	PFM/PWM operation, don't include USM, T_A=25°C	-0.25		+1.1	%
I_{SUPPLY}	Input supply current with no load	V_{IN} = 2.7V, V_{OUT} = 3.4V, PFM		66		µA
		V_{IN} = 3.3V, V_{OUT} = 3.4V, USM		1.4		mA
		V_{IN} = 3.3V, V_{OUT} = 3.4V, FPWM		5.3		mA
t_{RAMPUP}	Output voltage ramp up time when changing by I^2C(3)	VIN=2.7V, VOUT = 3.4V -> 5V, I_{OUT} = 100mA, $f_{(SCL)}$ = 100kHz, C_{OUT} is 2pcs 22uF/ 0603/6.3V/X5R		350		µs
$t_{RAMPDOWN}$	Output voltage ramp down time when changing by I^2C(3)	VIN=2.7V, VOUT = 5V -> 3.4V, I_{OUT} = 100mA, $f_{(SCL)}$ = 100kHz, C_{OUT} is 2pcs 22uF/ 0603/6.3V/X5R		600		µs
$t_{STARTUP}$	Start-up time with 0V pre-bias voltage	V_{IN} = 2.7V, V_{OUT} = 3.4V, I_{OUT} = 0A, C_{OUT} is 2pcs 22uF/ 0603/6.3V/X5R		400		µs

(1) Deviation in VOUT from nominal output voltage value at V_{IN} = 2.7V, V_{OUT} = 3.4V, I_{OUT} = 1mA to 4A with default I^2C register value. The max value is calculated by (V_{OUT_MAX} - V_{OUT_SET}) / V_{OUT_SET} * 100%, the min value is calculated by (V_{OUT_MIN} - V_{OUT_SET}) / V_{OUT_SET} * 100%.
(2) Deviation in VOUT from nominal output voltage value at V_{OUT} = 3.4V, I_{OUT} = 1A V_{IN} = 2.0V to 3.3V. The max value is calculated by (V_{OUT_MAX} - V_{OUT_SET}) / V_{OUT_SET} * 100%, the min value is calculated by (V_{OUT_MIN} - V_{OUT_SET}) / V_{OUT_SET} * 100%.
(3) The result includes I^2C communication time.

6.7 I²C Interface Timing Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
$f_{(SCL)}$	SCL Clock Frequency	Fast mode		400	kHz
$f_{(SCL)}$	SCL Clock Frequency	Fast mode plus		1	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Fast mode plus	0.5		µs
t_{HD}, t_{STA}	Hold Time (Repeated) START Condition		260		ns
t_{LOW}	LOW Period of the SCL Clock		0.5		µs
t_{HIGH}	HIGH Period of the SCL Clock		260		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition		260		ns
t_{SU}, t_{DAT}	Data Setup Time		50		ns
t_{HD}, t_{DAT}	Data Hold Time		0		µs
t_{RCL}	Rise Time of SCL Signal			120	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT			120	ns
t_{FCL}	Fall Time of SCL Signal			120	ns
t_{RDA}	Rise Time of SDA Signal			120	ns
t_{FDA}	Fall Time of SDA Signal			120	ns
$t_{SU,}$ t_{STO}	Setup Time of STOP Condition		260		ns
C_B	Capacitive Load for SDA and SCL			200	pF

(1) Specified by design. Not tested in production.

6.8 Typical Characteristics

V_{IN} = 2.7V, V_{OUT} = 3.4V, Normal Mode, T_J = 25°C, unless otherwise noted

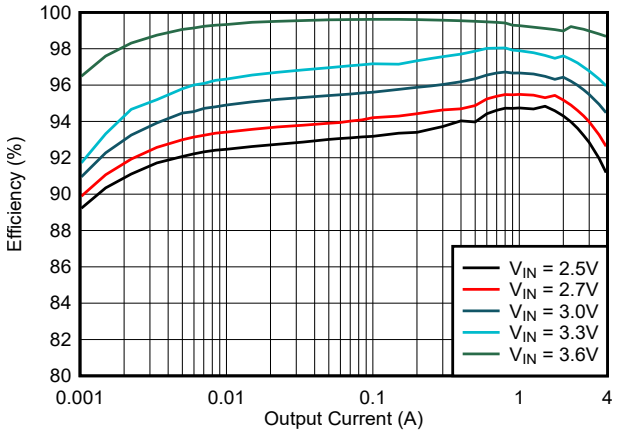


Figure 6-1. Efficiency vs Output Current

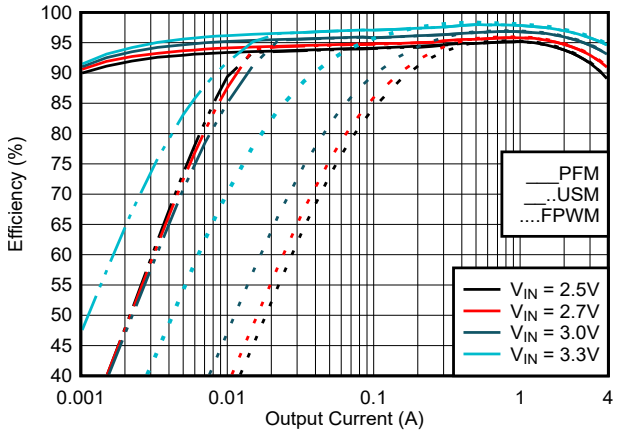


Figure 6-2. Efficiency vs Output Current

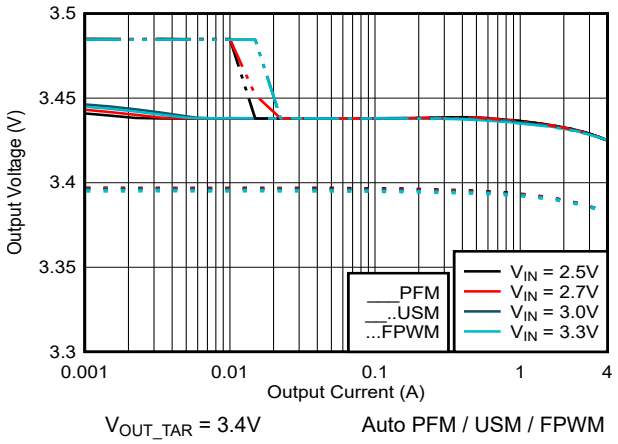


Figure 6-3. DC Output Voltage vs Output Current

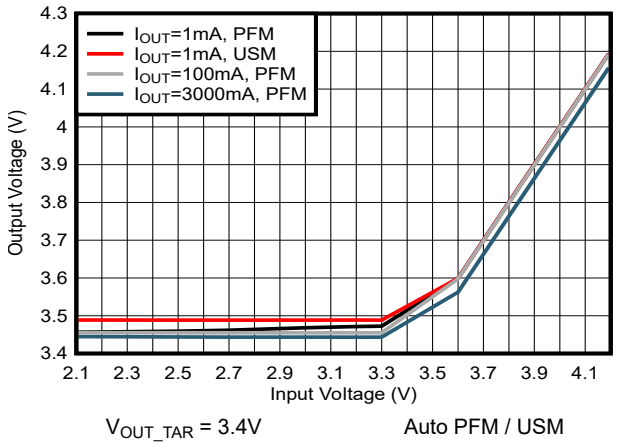


Figure 6-4. DC Output Voltage vs Input Voltage

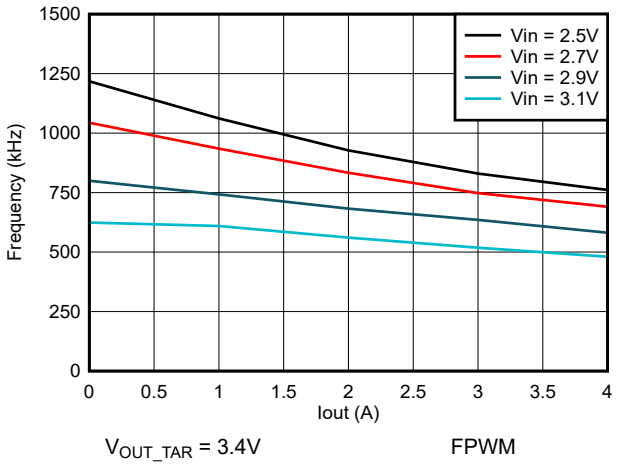


Figure 6-5. Switching Frequency vs Output Current

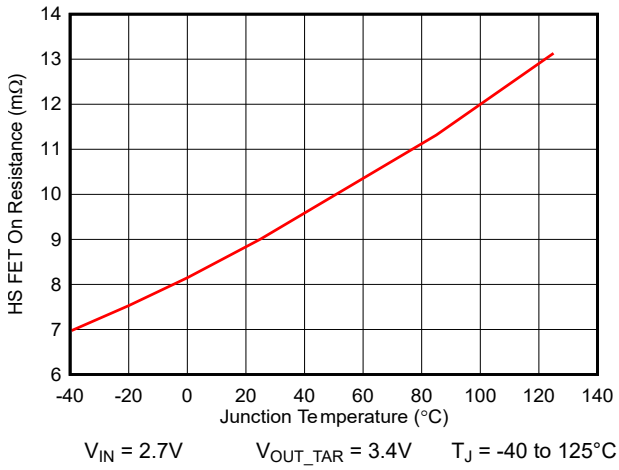


Figure 6-6. High side $R_{ds(on)}$ vs Junction Temperature

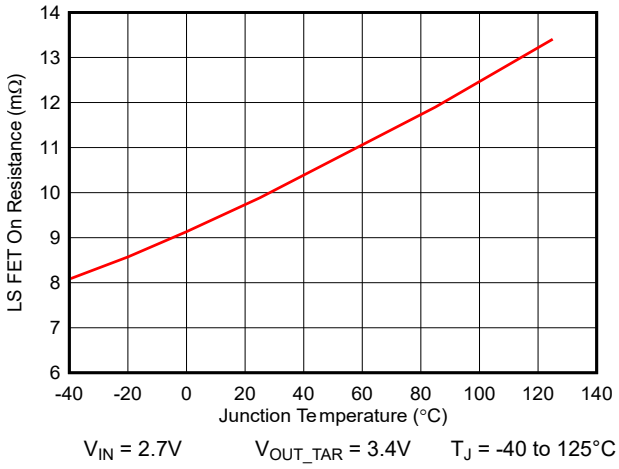


Figure 6-7. Low side $R_{ds(on)}$ vs Junction Temperature

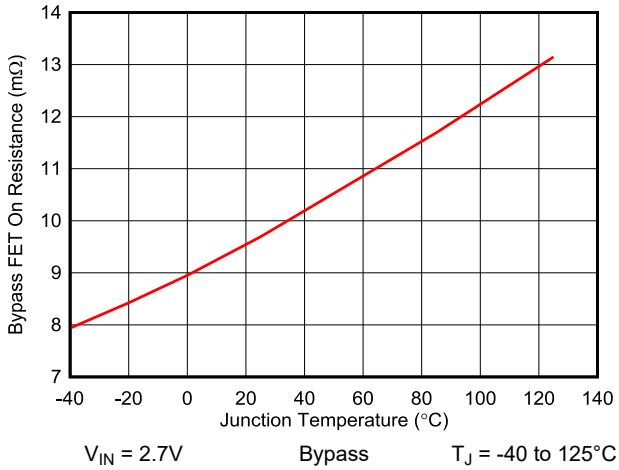


Figure 6-8. Bypass FET $R_{ds(on)}$ vs Junction Temperature

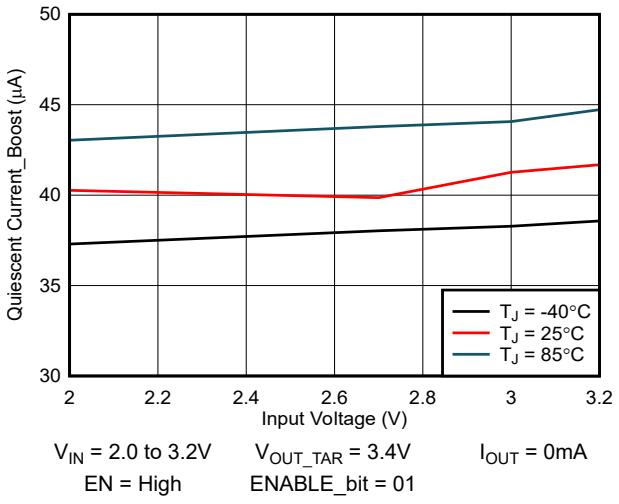


Figure 6-9. Quiescent Current at Boost Mode vs Input Voltage

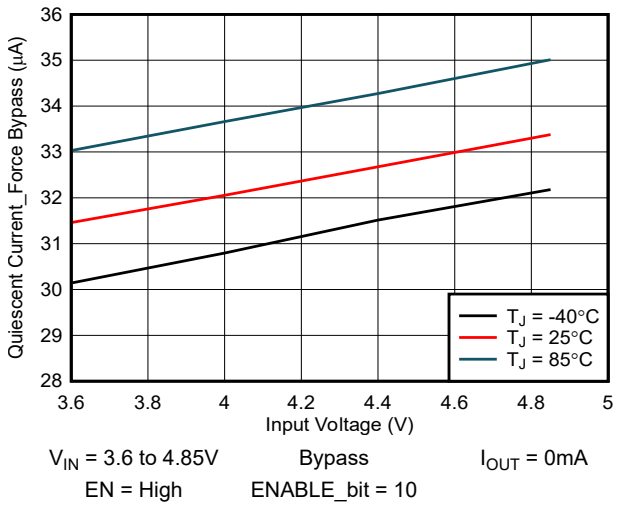


Figure 6-10. Quiescent Current at Forced Bypass Mode vs Input Voltage

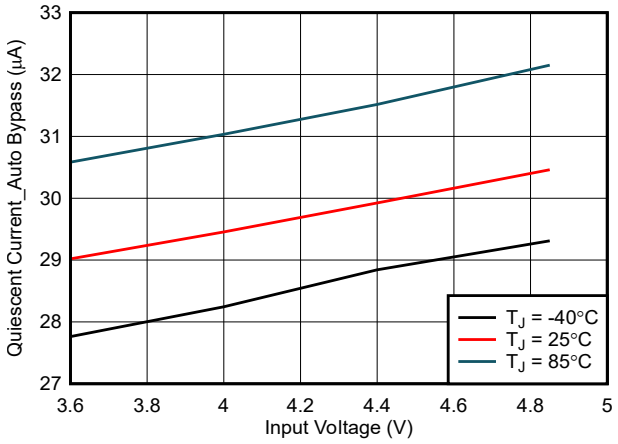


Figure 6-11. Quiescent Current at Auto Bypass Mode vs Input Voltage

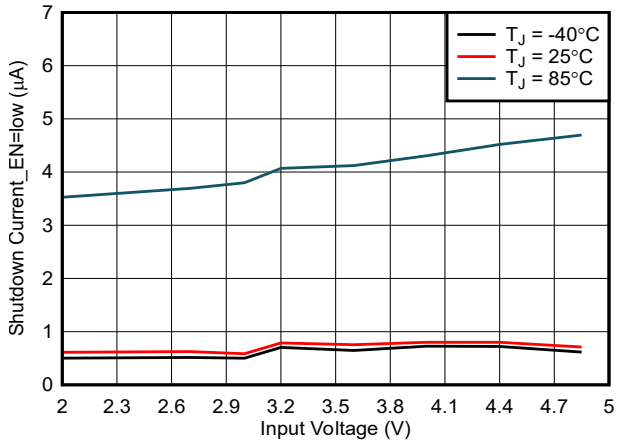


Figure 6-12. Shutdown Current at EN = Low vs Input Voltage

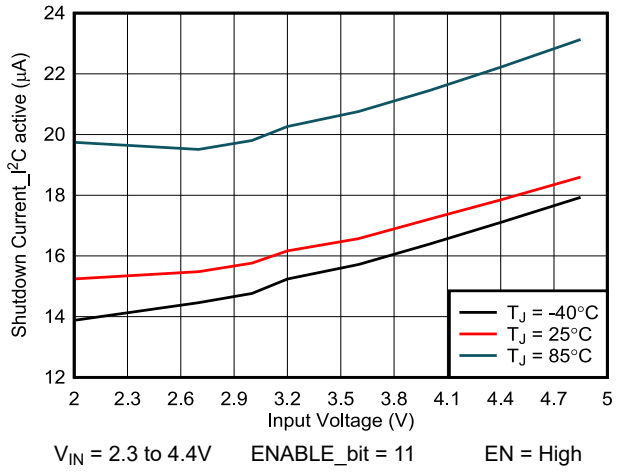


Figure 6-13. Shutdown Current with Active I²C Block vs Input Voltage

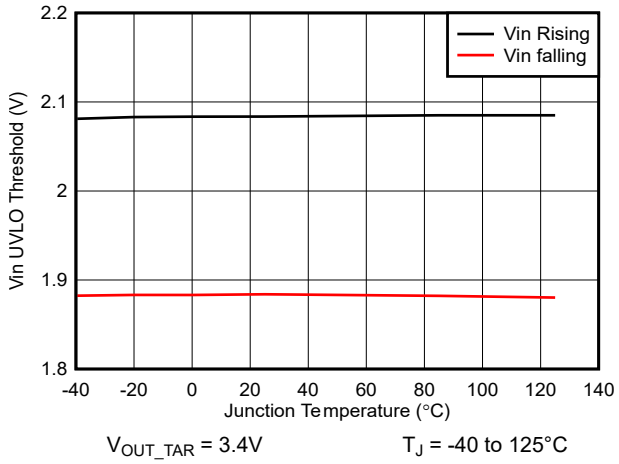


Figure 6-14. V_{IN} UVLO Threshold Rising/Falling vs Junction Temperature

7 Detailed Description

7.1 Overview

The TLV61290 is a high-efficiency step-up converter featuring bypass mode optimized to provide low-noise voltage supply for 2G RF power amplifiers (PAs) in mobile phones and/or to pre-regulate voltage for supplying subsystem like eMMC memory, audio codec, LCD bias, antenna switches, RF engine PMIC and so on. This device is designed to allow the system to operate at maximum efficiency for a wide range of power consumption levels from a low-I_Q, wide-voltage battery cell.

The capability of the TLV61290 to step-up the voltage as well as to bypass the input battery voltage when its level is high enough allow systems to operate at maximum performance over a wide range of battery voltages, thereby extending the battery life between charges. The device also addresses brownouts caused by the peak currents drawn by the APU and GPU which causes the battery rail to drop momentarily. Using the TLV61290 device as a pre-regulator eliminates system brownout condition while maintaining a stable supply rail for critical sub-system to function properly.

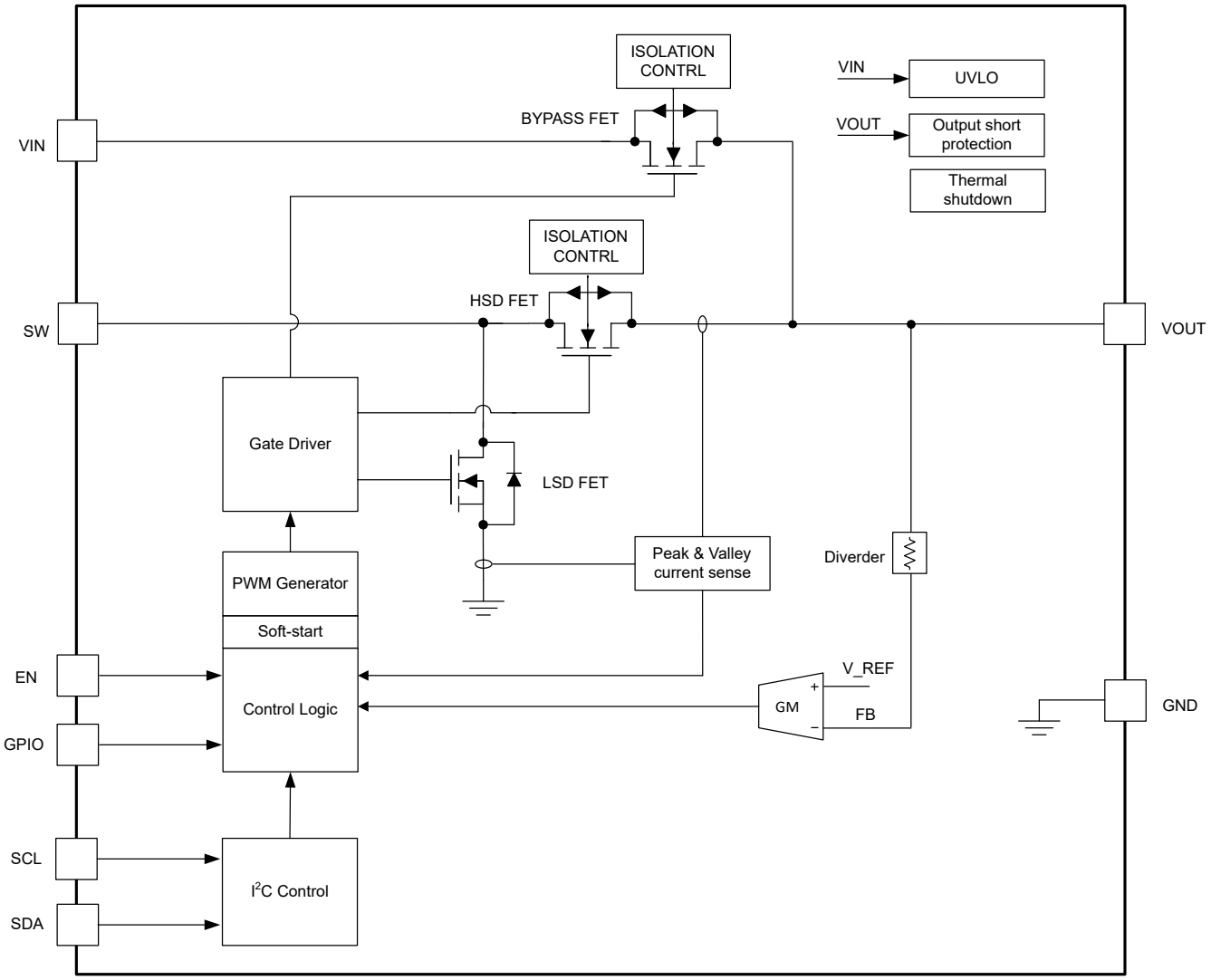
During auto PWM operation, the TLV61290 uses a hysteretic control scheme. At light load, the TLV61290 converter operates in power save mode with pulse frequency modulation (auto PFM), or forced PWM or Ultrasonic mode, which is programmable by I^2C.

In general, a DC/DC step-up converter only operates in "true" boost mode, that is the output “boosted” by a certain amount above the input voltage. The TLV61290 device operates differently as it smoothly transitions in and out of zero duty cycle operation. Depending upon the input voltage, output voltage threshold and load current, the integrated bypass switch automatically transitions the converter into so called true bypass mode to maintain low-dropout and high-efficiency. The device exits true bypass mode (0% duty cycle operation) if the total dropout resistance in true bypass mode is insufficient to maintain the output voltage at the nominal level.

Dynamically adjust the output voltage by VSEL function (TLV612901). Use this feature to either raise the output voltage in anticipation of a positive load transient or to dynamically change the PA supply voltage depending on its mode of operation and/or transmitting power.

The TLV61290 integrates an I^2C compatible interface allowing transfers up to 1Mbps. Use this communication interface to set the output voltage threshold at which the converter transitions between boost and bypass mode, for reprogramming the mode of operation (auto PFM or forced PWM or Ultrasonic mode), for settings the average current limit or resetting the output voltage for instance. The I^2C compatible interface address can be adjusted by ADDR function (TLV61290). Use this ADDR function feature when there are one more units per one I^2C bus.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage Setting

In order to maintain a certain minimum output voltage under heavy load transients, dynamically increase the output voltage set point by I^2C register. The functionality also helps to mitigate undershoot during severe line transients, while minimizing the output voltage during more bengin operating conditions to save power.

The output voltage ramps up at pre-defined rate defined by the average input current limit setting. The required time to ramp down the voltage largely depends on the amount of capacitance present at the output of the converter as well as on the load current. In auto PFM and Ultrasonic mode the output capacitance is being discharged (solely) by the load current drawn. So under very light load conditions, the actual output voltage of auto PFM is around $(1+1\%)V_{OUT\_TAR}$, and the actual output voltage of Ultrasonic mode is around $(1+2\%)V_{OUT\_TAR}$. As the load increases, the actual output voltage of both mode is around $(1+1\%)V_{OUT\_TAR}$. In forced PWM, the output capacitance is being discharged at a rate of approximately 100mA (or higher) constant current in addition to the load current drawn. So the actual output voltage is V_{OUT_TAR}.

For TLV61290, the GPIO is configured as ADDR function, only set the output voltage by VOUTFLOORSET (default 3.4V). For TLV612901, the GPIO is configured as VSEL function, set the output voltage by VOUTFLOORSET Register (VSEL = low) and VOUTROOFSET (VSEL = high).

It is not recommended to ramp up setting output voltage by a step that is larger than 200mV when setting output voltage is higher than 4.5V, otherwise the overshoot during output voltage ramping up possibly exceeds the recommended operation condition.

7.3.2 Switching frequency and Spread Spectrum Function

The TLV61290 boost converter does not have fixed frequency and it keeps the inductor ripple current in the range of approximately 1.0A, so the frequency is changed and determined by the operation condition.

In auto PFM operation, the minimum switching frequency is not limited, the switching frequency is approximately 20Hz (or even lower) with open load.

In Ultrasonic mode, the minimum switching frequency is limited to 25kHz (min.) to avoid audio band noise. In forced PWM operation, minimum switching frequency is limited to approximately 300 kHz. With this unique feature, the TLV61290 avoids the low frequency switching and prevents the application against the low frequency noise sensitive range.

Switching regulators are particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The TLV61290 provides a spread spectrum feature. The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with the power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

The spread spectrum architecture varies the switching frequency by ca. ±8% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

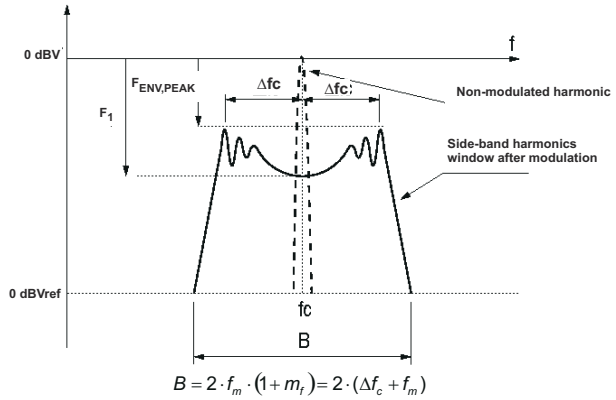


Figure 7-1. Spectrum of a Frequency Modulated Sin. Wave with Sinusoidal Variation in Time

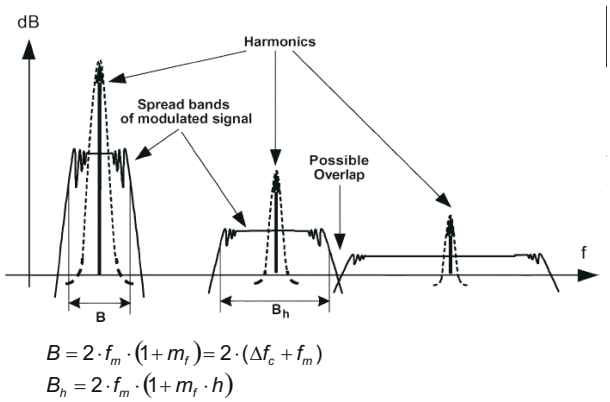


Figure 7-2. Spread Bands of Harmonics in Modulated Square Signals [1]

The above figures show that after modulation the sideband harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \quad (1)$$

where

- f_c is the carrier frequency (switching frequency)
- f_m is the modulating frequency (approximately 0.5%*f_c)
- δ is the modulation ratio (approximately 8%)

$$\delta = \frac{\Delta f_c}{f_c} \quad (2)$$

The maximum switching frequency f_c is limited by the process and finally the parameter modulation ratio (δ), together with f_m, which is the side-band harmonics bandwidth around the carrier frequency f_c. The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule and can be summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \quad (3)$$

f_m < RBW: The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

[1] Spectrum illustrations and formulae (Figure 7-1 and Figure 7-2) copyright IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005.

7.4 Device Functional Modes

7.4.1 Enable and Start-up

The TLV61290 automatically powers-up once an input voltage greater than 2.2V and less than 5V is applied. After start-up, the input voltage can be reduced to 2.0V. The device has an internal soft-start circuit that limits the inrush current during start-up. The first phase in the start-up procedure is to bias the output node close to the input level (also called down mode pre-charge phase). In this operation mode, when output voltage is lower than 0.6V, the inductor average current is limited to approximately 500mA. When the output voltage is higher than 0.6V but lower than the input voltage minus 2.0V, the inductor average current limit is increased to approx 1.5A. And when the output voltage is higher than the input voltage minus 2V but lower than the input voltage, the input average current limit is increased to the half of the value setted by ILIM_BOOST.

When output voltage is higher than input voltage, the device exits down mode pre-charge phase and enter Boost switching phase, the input average current limit is increased to Boost current limit (default value is 8A). Using this method the loading capability during start-up is improved and this is helpful to reduce the input current overshoot during start-up. Table 7-1shows the relationship between input current limit and output voltage in start-up phase.

Table 7-1. Average Current Limit Setting During Start-up (VIN ≤ 2.6V)

Phase	Inductor Average Current Limit	Output Voltage
Down mode pre-charge phase	500mA (typ.)	VOUT ≤ 0.6V
	ILIM_BOOST / 2	VIN - 2V < VOUT ≤ VIN
Boost switching phase	ILIM_BOOST	VIN < VOUT

Table 7-2. Average Current Limit Setting During Startup (VIN > 2.6V)

Phase	Inductor Average Current Limit	Output Voltage
Down mode pre-charge phase	500mA (typ.)	VOUT ≤ 0.6V
	1.5A (typ.)	0.6V < VOUT ≤ VIN- 2V
	ILIM_BOOST / 2	VIN - 2V < VOUT ≤ VIN
Boost switching phase	ILIM_BOOST	VIN < VOUT

In down mode pre-charge phase, if the output voltage fails to reach input voltage after 1ms, a fault condition is declared. After waiting 19ms, a restart is attempted, this operation mode is also called hiccup mode. Disable the hiccup mode via I^2C.

The TLV61290 is able to start up with 2.2V UVLO rising threshold with larger than 10Ω load. However, if the load during start-up is so heavy or the output capacitance is so large that the TLV61290 fails to charge the output voltage to target value, the TLV61290 does not start up successfully until the input voltage is increased or the load current is reduced. The total start-up time depends on input voltage, output capacitance and load current.

7.4.2 Operation Mode Setting

The TLV61290 device can be configured (via the Section 7.6.5) to select the operating mode of the device.

When the EN pin is set to logic high, ENABLE bit (CONFIG[5:6]) = 01 (default value), the device enters normal mode(that is, automatic boost/bypass mode) and enables the output voltage to remain above a pre-defined target voltage.

When the EN pin is set to logic high, ENABLE bit (CONFIG[5:6]) = 10, the device enters forced bypass mode. In this mode, the synchronous rectifier is current limited to ca. 10A (programmable via I^2C) allowing an external load (for example audio amplifier) to be powered with a restricted supply. The output voltage is slightly reduced due to voltage drop across the bypass MOSFET. The device consumes only a standby current of 30µA (typ).

When the EN pin is set to logic high, and ENABLE bit (CONFIG[5:6]) = 11 forces the device in shutdown mode, but I^2C block works, with a standby current of typically 16µA. In this mode, true load disconnect between the battery and load prevents current flow from VIN to VOUT, as well as reverse current flow from VOUT to VIN.

When the EN pin is set to logic low forces the device in shutdown mode (regardless of what ENABLE bit is), with a shutdown current of typically 0.8µA. In this mode, true load disconnect between the battery and load prevents current flow from VIN to VOUT, as well as reverse current flow from VOUT to VIN.

Table 7-3. Mode of Operation

EN pin	ENABLE bit	Operation Mode
Low	xx	Shutdown mode. True load disconnection and no V_{OUT}. The device shutdown current is approximately 0.8µA typ.
High	11	I^2C shutdown mode. Power stage is turned off and no V_{OUT}, but I^2C is active. True load disconnection. The device standby current in this mode is approximately 16µA typ.
High	10	Forced bypass mode. V_{OUT} follows V_{IN}. The device standby current is approximately 30µA typ.
High	00/01 (default 01)	Automatic boost/bypass mode. In boost mode, V_{OUT} = V_{OUT_TAR} (default 3.4V). In bypass mode, V_{OUT} follows V_{IN}.

7.4.3 Bypass Mode

The TLV61290 contains an internal switch for bypassing the dc/dc boost converter during bypass mode. When the input voltage is larger than the preset output voltage, the converter seamlessly transitions into 0% duty cycle operation and the bypass FET is fully turned on.

In auto PFM or Ultrasonic mode, entry in bypass mode is triggered by condition where V_{OUT} >(1+1%)* V_{OUT_TAR} and V_{IN} > V_{OUT}.

In forced PWM operation, the device enters into bypass mode from either of these two conditions:

- V_{OUT} >(1+2%)* V_{OUT_TAR}.
- Seven (7) consecutive cycle of maximum clamped off-time occurs (typical t_{OFF} is 2.25µs of each cycle and total 16µs).

Bypass mode exit is triggered when V_{OUT} < V_{OUT_TAR}-50mV.

In bypass mode operation, the load (2G RF PA for instance) is directly supplied from the battery for maximum RF output power, highest efficiency and lowest possible input-to-output voltage difference. The device consumes only a standby current of 30µA (typ). In bypass mode, the device is protected from short-circuit by a very fast current limit detection scheme.

During this operation, the output voltage follows the input voltage and does not fall below the programmed output voltage threshold as the input voltage decreases. The output voltage drop during bypass mode depends on the load current and input voltage, the resulting output voltage is calculated as:

$$V_{OUT} = V_{IN} - \left(R_{DSON(BP)} \times I_{OUT}\right) \quad (4)$$

Conversely, the efficiency in bypass mode is defined as:

$$\eta = 1 - R_{DSON(BP)} \frac{I_{OUT}}{V_{IN}} \quad (5)$$

- in which $R_{DSON(BP)}$ is the typical on-resistance of the bypass FET

During bypass mode, the TLV61290 device has overcurrent and short-circuit protection by a fast current limit detection scheme. If the current in the bypass FET exceeds approximately 10A (programmable via I^2C), the bypass FET is turned off, then the TLV61290 enters into output short-to-ground protection mode. Once the overcurrent or short-circuit is released, the TLV61290 goes through the start-up procedure again.

During bypass mode, the device is also protected by a reverse current protection. If the V_{OUT} is higher than V_{IN} + 20mV, after approximately 4µs delay, the bypass FET is turned off to block reverse current from V_{OUT} to V_{IN}. This protection scheme protects the battery from overcharging.

7.4.4 Boost Control Operation

The TLV61290 boost converter is controlled by a hysteretic current mode. This controller regulates the output voltage by keeping the inductor ripple current constant around 1.0A and adjusting the offset of this inductor current depending on the output load. Since the input voltage, output voltage and inductor value all affect the rising and falling slopes of inductor ripple current, the switching frequency is not fixed and is determined by the operation condition. At light load, the TLV61290 implements three operating modes, auto PFM, forced PWM and Ultrasonic mode, to meet different application requirements. The operating mode is set by changing the state of the MODE_CTRL bit via I^2C. When MODE_CTRL = 00, the device operates in auto PFM mode. When MODE_CTRL = 01, the device operates in Ultrasonic mode. When MODE_CTRL = 10 or 11, the device operates in forced PWM mode. For this device, the recommended inductance range is 330nH to 560nH.

7.4.5 Auto PFM Mode

The TLV61290 integrates the power save mode with pulse frequency modulation (Auto PFM) to improve the efficiency at the light load. In this mode, if the required average input current is lower than the average inductor current defined by this constant ripple, the inductor current goes discontinuously to keep the efficiency high under light load condition. The peak inductor current and the valley inductor is limited by approximately 1.0A and 0A separately. If the output current in auto PFM mode is no longer be supported, the TLV61290 exits auto PFM mode and enter PWM mode.

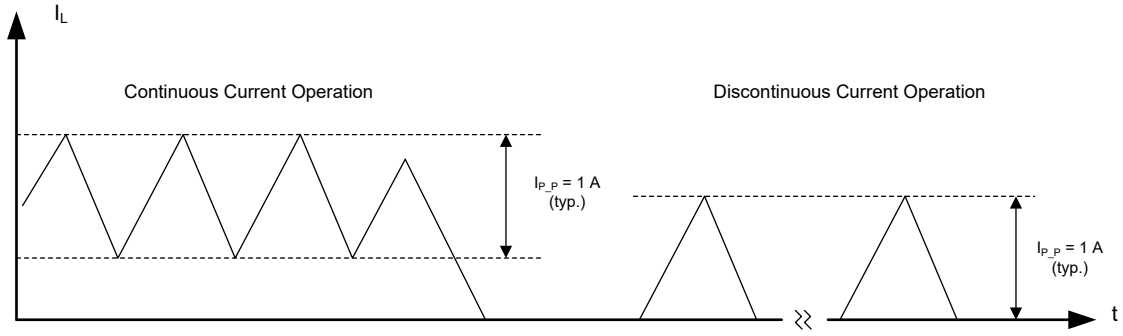


Figure 7-3. Auto PFM Mode

7.4.6 Forced PWM Mode

In forced PWM mode, the TLV61290 keeps the inductor current being continuous for the whole load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and delivers less power from input to output. The high-side FET is not turned off even if the current through the FET goes negative to keep the switching frequency being the same as that of the heavy load. In this mode, the minimal switching frequency in this mode is limited to 300kHz (typ.) when input voltage is close to output voltage.

7.4.7 Ultrasonic Mode

The Ultrasonic mode is an unique control feature that keeps the switching frequency above the acoustic audible frequency toward no load and light load condition. The Ultrasonic mode control circuit monitors the switching frequency and keeps the switching frequency above 23kHz to avoid the acoustic band. The output voltage becomes typically 1% higher than PWM operation.

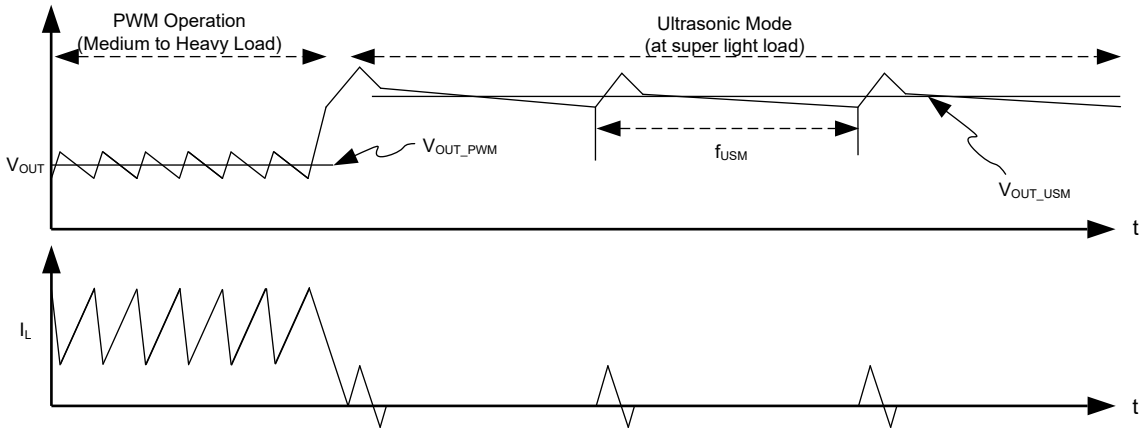


Figure 7-4. Ultrasonic Mode Operation

7.4.8 Output Discharge

TLV61290 provides an active pull down current to quickly discharge output when the EN is logic low or device in I^{2}C shutdown mode. With this function, the output voltage is connected to ground through internal circuitry, preventing the output from “floating” or entering into an undetermined state. The output discharge function makes the power on and off sequencing smooth. Pay attention to the output discharge function if use this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground.

TLV61290 can modify the status of this function by writing the value of the DISCHG bit via I^{2}C. When DISCHG = 0, disable output discharge function in I^{2}C shutdown mode. When DISCHG = 1, enable output discharge function in shutdown mode. The default value of this bit is 1.

7.4.9 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. The I^{2}C control interface and the output stage of the converter are disabled once the falling V_{IN} trips the undervoltage lockout threshold $V_{UVLO\_falling}$ (2.0V max). The device starts operation once the rising V_{IN} trips V_{UVLO_rising} threshold (2.2V max).

7.4.10 Current Limit Operation

The TLV61290 device features an average inductor current limit scheme.

In dc/dc boost mode, the TLV61290 device employs a current limit detection scheme in which the voltage drop across the synchronous rectifier is sensed during the off-time. The average current limit threshold is set via an I^{2}C register. The default average current limit in boost mode is approximately 8A, when it hits the current limit, the device works in constant current mode. The output voltage is reduced as the power stage of the device operates in a constant current mode.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(max)}$), before entering current limit (CL) operation, is defined by Equation 6.

$$I_{OUT(max)} = I_{LIMIT} \times \left(\frac{V_{IN}}{V_{OUT}}\right) \times \eta \quad (6)$$

where

- η is the efficiency
- $I_{OUT(max)}$ is the maximum output current
- I_{LIMIT} is the current limit of the input side
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

The output current, I_{OUT}, is the average of the rectifier ripple current waveform. When the load current is increased such that the trough is above the current limit threshold, the off-time is increased to allow the current to decrease this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached the output voltage decreases during further load increase.

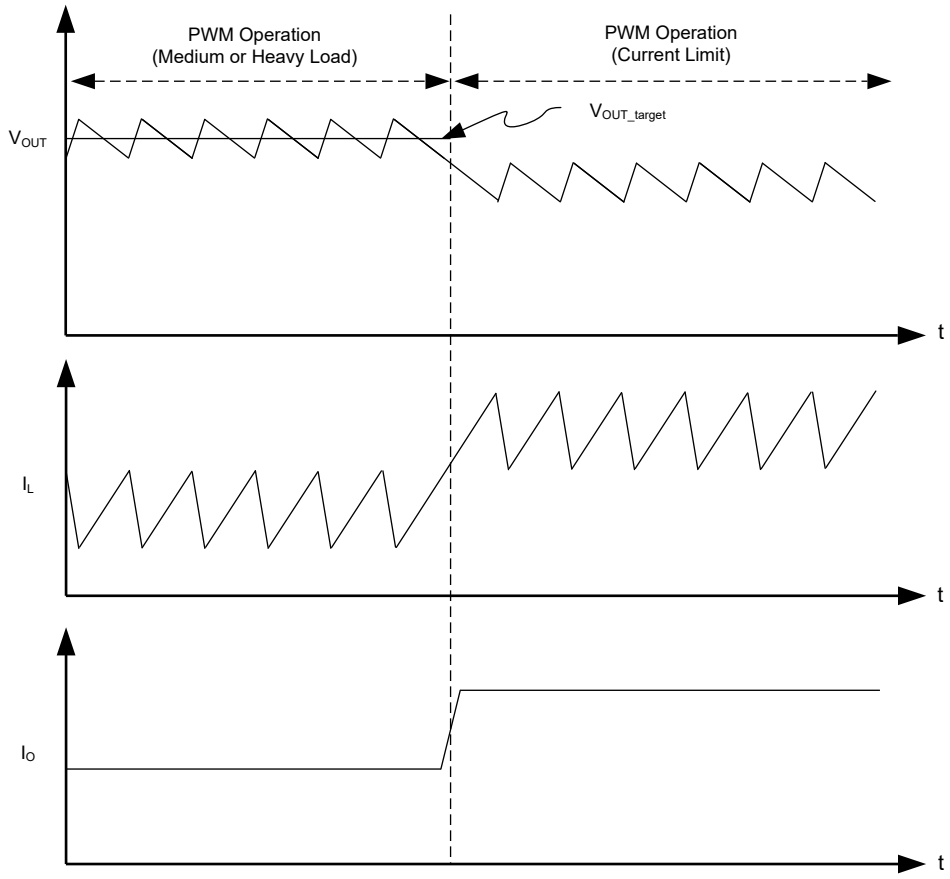


Figure 7-5. Operation scheme of current limit in dc/dc boost mode

In true bypass mode, the TLV61290 device employs a hiccup protection scheme. The current limit threshold is set using an I^2C register. The default current limit in true bypass mode is 10A, when it hits the current limit, the device turns off the bypass FET after a small delay, ca. 200ns, then the device enters into hiccup mode. Once the short-circuit is released, the TLV61290 goes through the soft start-up again.

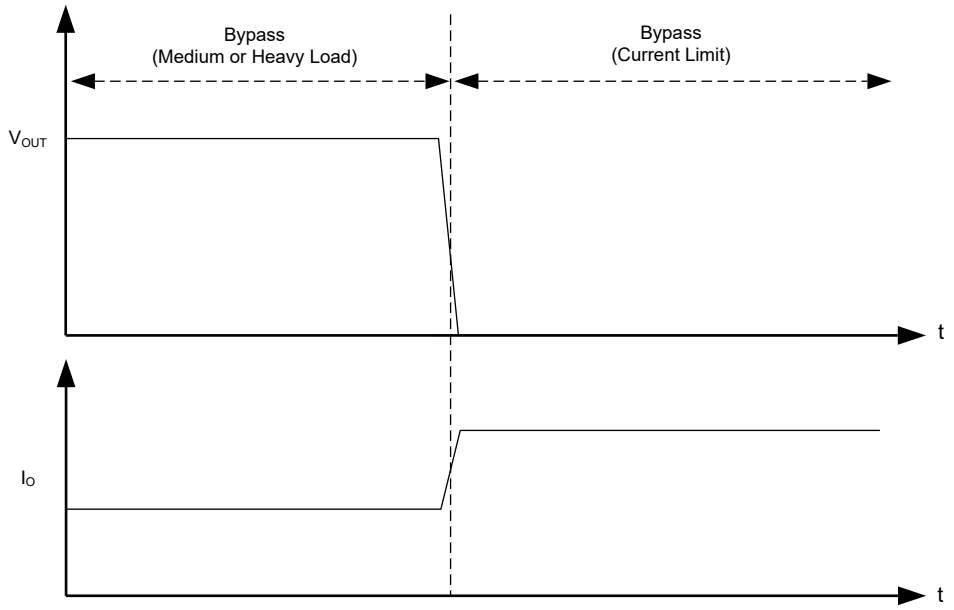


Figure 7-6. Operation scheme of current limit in true bypass mode

7.4.11 Output Short-to-Ground Protection

The device TLV61290 works in hiccup mode when output short-to-ground. The scheme of output short-to-ground protection (OSGP) is same as the scheme in start-up phase.

When output is short, the TLV61290 enters into hiccup mode. Once the overcurrent or short-circuit is released, the TLV61290 goes through the soft start-up again to regulated the output voltage.

The hiccup protection mode is disabled using I^2C.

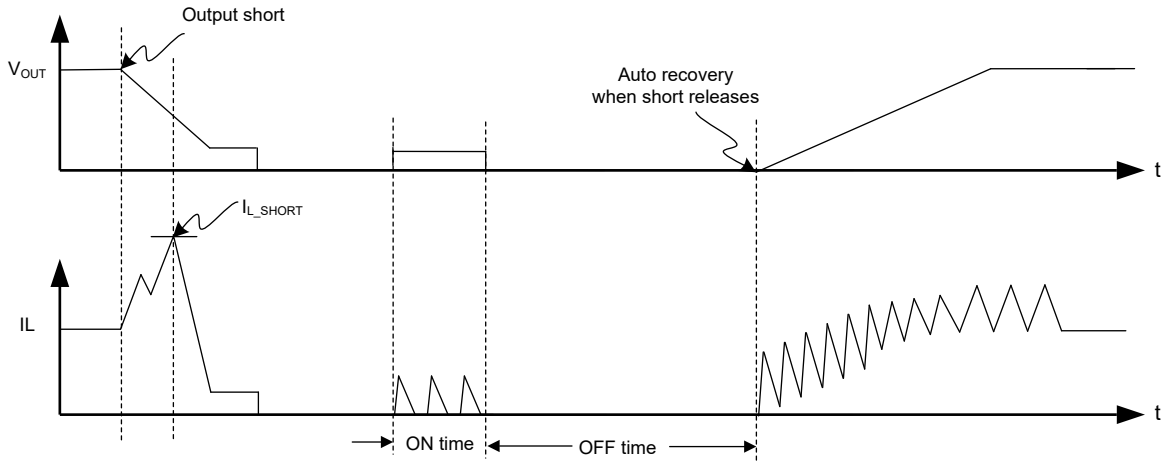


Figure 7-7. Hiccup Mode in OSGP

7.4.12 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 165°C (typ.) the device goes into thermal shutdown. In this mode the bypass, high-side and low-side MOSFETs are turned-off, the I^2C block is active. When the junction temperature falls below the thermal shutdown minus its hysteresis (20°C typ.), the device continuous to re-startup and regulate the output voltage.

7.4.13 Power-Good Indication Status

The TLV61290 also provide a power-good output bit(PG bit in I^2C) for signaling the system when the regulator has successfully completed start-up and no faults have occurred. Power-good also functions as an early warning flag for excessive die temperature and overload conditions.

- PG is set (bit = 1) when the start-up sequence is successfully completed.
- PG is reset (bit = 0) when the output voltage falls approximately 50mV below its regulation level in Boost mode.
- PG is set (bit = 1) when the device is operating in auto bypass mode (that is ENABLE bit = 00 or 01 and $V_{IN}>V_{OUT}$).
- PG is not defined when the device is operating in forced bypass mode (that is ENABLE bit = 10).
- PG is reset (bit = 0) when the device is in shutdown mode (that is ENABLE bit = 11).
- PG is reset (bit = 0) when the device is in short protection mode, thermal shutdown mode.

7.5 Programming

The TLV61290 uses I^2C interface for flexible converter parameter programming. I^2C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). I^2C devices can be considered as controllers or targets when performing data transfers. A controller is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The TLV61290 operates as a target device with address 75h. Receiving control inputs from the controller device like a microcontroller or a digital signal processor reads and writes the internal registers 00h through 07h. The I^2C interface of the TLV61290 supports both standard mode (up to 100kbit/s) and fast mode plus (up to 1000kbit/s). Both SDA and SCL must be connected to the positive supply voltage through current sources or pullup resistors. When the bus is free, both lines are in high voltage.

7.5.1 Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high level or low level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

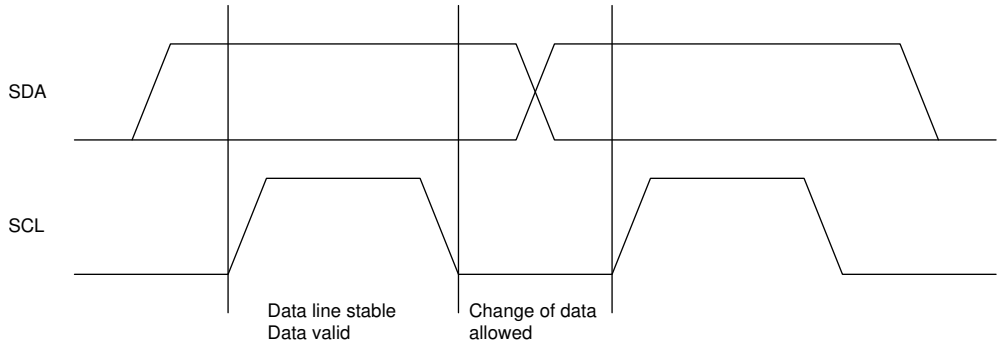


Figure 7-8. I^2C Data Validity

7.5.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high level to low level transition on the SDA line while SCL is at high level defines a START condition. A low level to high level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition, and free after the STOP condition.

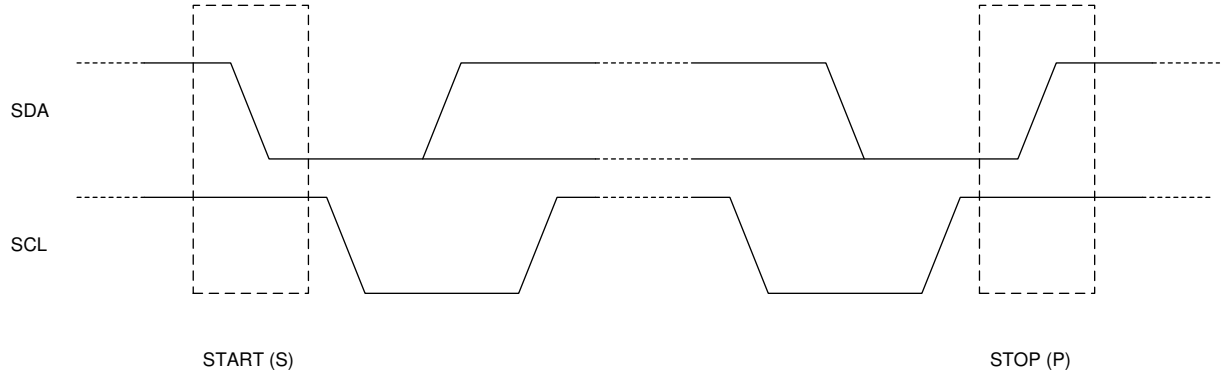


Figure 7-9. I²C START and STOP Conditions

7.5.3 Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a target cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

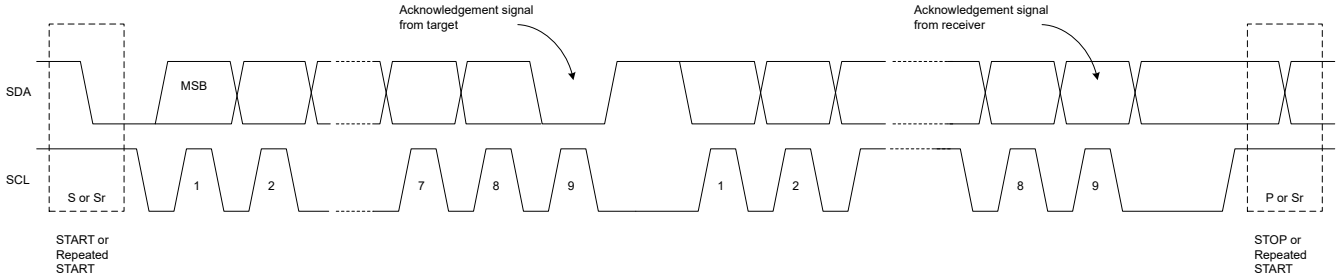


Figure 7-10. Byte Format

7.5.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line to low level and it remains stable low level during the high level period of this clock pulse.

The Not Acknowledge signal is when SDA remains high level during the 9th clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.5.5 Target Address and Data Direction Bit

After the START, a target address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

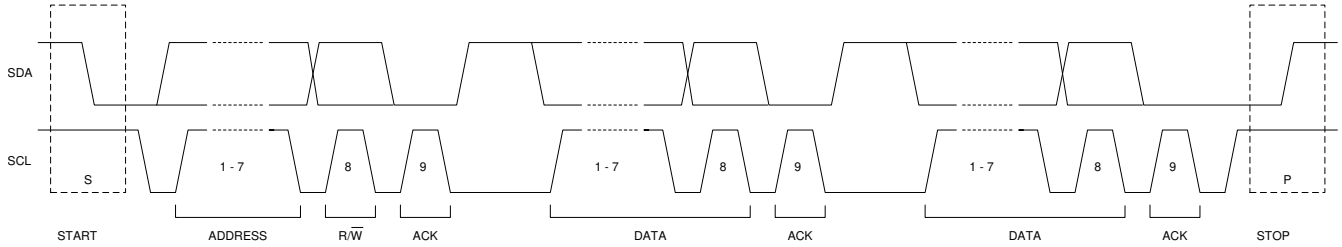


Figure 7-11. Target Address and Data Direction

7.5.6 Single Read and Write

Figure 7-12 and Figure 7-13 show the single-byte write and single-byte read format of the I^{2}C communication.

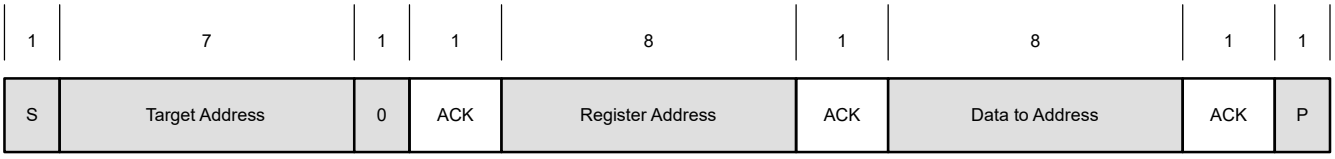


Figure 7-12. Single-byte Write

Figure 7-13. Single-byte Read

If the register address is not defined, the TLV61290 sends back NACK and goes back to the idle state.

7.5.7 Multi-Read and Multi-Write

The TLV61290 supports multi-read and multi-write.

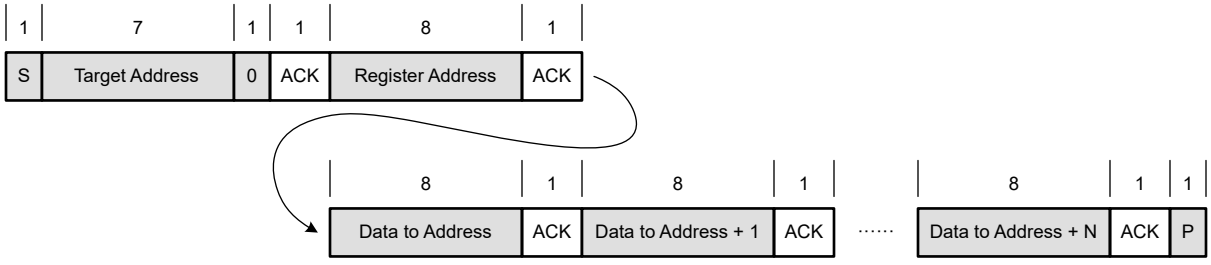


Figure 7-14. Multi-byte Write

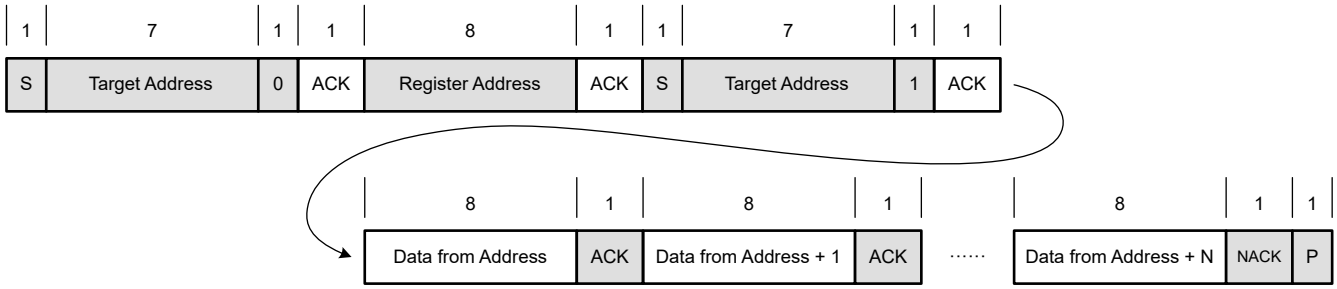


Figure 7-15. Multi-byte Read

7.6 Register Maps

The Configuration Memory Map lists the memory-mapped registers for the device registers. All register offset addresses not listed in The Configuration Memory Map should be considered as reserved locations, and the register contents should not be modified.

Table 7-4. Device Registers

Register Address	Register Name	Description
00h	DeviceID Register	Sets Manufacturer ID & Device version ID
01h	CONFIG Register	Sets miscellaneous configuration bits
02h	VOUTFLOORSET Register	Sets the floor output voltage threshold boost / bypass mode change
03h	ILIMBSTSET Register	Sets the input current limit in dc/dc boost mode
04h	VOUTROOFSET Register	Sets the roof output voltage threshold boost / bypass mode change (only valid when GPIO is configured as VSEL function)
05h	STATUS Register	Returns status flags
06h	ILIMPTSET Register	Sets the input current limit in bypass mode
07h	BSTLOOP Register	Sets the internal compensation loop

7.6.1 DeviceID Register

Memory location: 0x00

Table 7-5. VersionID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Manufacture ID	R	0111	Manufacturer ID.
3:0	Device ID	R	0000	Device version ID.

7.6.2 CONFIG Register

Memory location: 0x01

Table 7-6. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0	Device reset bit. 0: Normal operation. or line breaks 1: Default values are set to all internal registers. The device operation is cycled (ON-OFF-ON), that is, the converter is disabled for a short period of time and the output is reset.
6:5	ENABLE	R/W	01	Device enable bit (refer to Operation Mode Setting). 00 or 01: Device operates in automatic boost mode. 10: Device forced in true bypass mode. 11: Device is in shutdown mode but I^2C active.
4	HICCUP_MODE	R/W	1	Hiccup mode enable bit. 0 : Hiccup mode disable 1 : Hiccup mode enable
3	DISCHG	R/W	1	Output discharge enable bit. 0: Disable VOUT discharge when the device is in I^2C shutdown mode. 1: Enable VOUT discharge when the device is in shutdown mode. (refer to Output Discharge)
2	SSFM	R/W	0	Spread modulation control. 0: Spread spectrum modulation is disabled. 1: Spread spectrum modulation is enabled in forced PWM mode
1:0	MODE_CTRL	R/W	00	Device light load functional modes bits. 00: Device operates in Auto PFM Mode. 01: Device operates in Ultrasonic Mode. 10 or 11: Device operates in Forced PWM Mode.

7.6.3 VOUTFLOORSET Register

Memory location: 0x02

Table 7-7. VOUTFLOORSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0	Reserved bit. This bits is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
5:0	VOUTFLOOR_TH	R/W	0	Output voltage threshold, dc/dc boost / bypass mode change.
		R/W	0	
		R/W	1	000000: 2.85V 000001: 2.90V 000010: 2.95V 000011: 3.00V 000100: 3.05V 000101: 3.10V 000110: 3.15V 000111: 3.20V 001000: 3.25V 001001: 3.30V 001010: 3.35V 001011: 3.40V 001100: 3.45V 001101: 3.50V 001110: 3.55V 001111: 3.60V 010000: 3.65V 010001: 3.70V 010010: 3.75V 010011: 3.80V 010100: 3.85V 010101: 3.90V 010110: 3.95V 010111: 4.00V 011000: 4.05V 011001: 4.10V 011010: 4.15V 011011: 4.20V 011100: 4.25V 011101: 4.30V 011110: 4.35V 011111: 4.40V 100000: 4.45V 100001: 4.50V 100010: 4.55V 100011: 4.60V 100100: 4.65V 100101: 4.70V 100110: 4.75V 100111: 4.80V 101000: 4.85V 101001: 4.90V 101010: 4.95V 101011: 5.00V 110110: 2.80V 110111: 2.75V 111000: 2.70V 111001: 2.65V 111010: 2.60V 111011: 2.55V 111100: 2.50V 111101: 2.45V 111110: 2.40V 111111: 2.35V 101100 ~ 110101: Not Defined.
		R/W	0	
		R/W	1	

7.6.4 ILIMBSTSET Register

Memory location: 0x03

Table 7-8. ILIMBSTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
6	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
5	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
4	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
3:0	ILIM_BOOST	R/W	0	Inductor average current limit in dc/dc boost mode. 0000: 5A 0001: 5.5A 0010: 6A 0011: 6.5A 0100: 7A 0101: 7.5A 0110: 8A 1101: 3.5A 1110: 4A 1111: 4.5A 0111 ~ 1100: Not Defined.
		R/W	1	
		R/W	1	
		R/W	0	

7.6.5 VOUTROOFSET Register

Memory location: 0x04

Table 7-9. VOUTROOFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
5:0	VOUTROOF_TH	R/W	0	Output voltage threshold, dc/dc boost / bypass mode change. 000000: 2.85V 000001: 2.90V 000010: 2.95V 000011: 3.00V 000100: 3.05V 000101: 3.10V 000110: 3.15V 000111: 3.20V 001000: 3.25V 001001: 3.30V 001010: 3.35V 001011: 3.40V 001100: 3.45V 001101: 3.50V 001110: 3.55V 001111: 3.60V 010000: 3.65V 010001: 3.70V 010010: 3.75V 010011: 3.80V 010100: 3.85V 010101: 3.90V 010110: 3.95V 010111: 4.00V 011000: 4.05V 011001: 4.10V 011010: 4.15V 011011: 4.20V 011100: 4.25V 011101: 4.30V 011110: 4.35V 011111: 4.40V 100000: 4.45V 100001: 4.50V 100010: 4.55V 100011: 4.60V 100100: 4.65V 100101: 4.70V 100110: 4.75V 100111: 4.80V 101000: 4.85V 101001: 4.90V 101010: 4.95V 101011: 5.00V 110110: 2.80V 110111: 2.75V 111000: 2.70V 111001: 2.65V 111010: 2.60V 111011: 2.55V 111100: 2.50V 111101: 2.45V 111110: 2.40V 111111: 2.35V 101100 ~ 110101: Not Defined.

7.6.6 STATUS Register

Memory location: 0x05

Table 7-10. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSD	R	0	Thermal shutdown status bit. 0: Normal operation. 1: Thermal shutdown tripped. This flag is reset after readout.
6	CRC_PASS	R	1	OTP test status bit. 0: OTP test failed. This bit is reserved for Test Engineers in TI. 1: Normal operation. This flag is reset after readout.
5	VOUT_START	R	1	Vout status bit. 0: Vout < 0.6V. 1: Vout > 0.6V. This flag is reset after readout.
4	OPMODE	R	1	Device mode of operation status bit. 0: Device operates in bypass mode. 1: Device operates in boost mode.
3	ILIMPT	R	0	Current limit status bit (bypass mode). 0: Normal operation. 1: Indicates that the bypass FET current limit has triggered. This flag is reset after readout.
2	ILIMBST	R	0	Current limit status bit (dc/dc boost mode). 0: Normal operation. 1: Indicates that the average input current limit has triggered for 4ms in dc/dc boost mode. This flag is reset after readout.
1	FL_LD	R	0	Current limit status bit (dc/dc boost mode). 0: Normal operation. 1: Indicates that the average input current limit has triggered in dc/dc boost mode. This flag is reset after readout.
0	PGOOD	R	1	Power Good status bit. 0: Indicates the output voltage is out of regulation. 1: Indicates the output voltage is within its nominal range. This bit is set to 1 if the converter operates in auto bypass mode.

7.6.7 ILIMPTSET Register

Memory location: 0x06

Table 7-11. ILIMPTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
6	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
5:3	ILIM_FPT	R/W	0	Current limit in forced true bypass mode. 000: 16A 001: 6A 010: 8A 011: 10A 100: 12A 101: 14A 110: 4A 111: 18A
		R/W	1	
		R/W	1	
2:0	ILIM_APT	R/W	0	Current limit in automatic true bypass mode. 000: 16A 001: 6A 010: 8A 011: 10A 100: 12A 101: 14A 110: 4A 111: 18A
		R/W	1	
		R/W	1	

7.6.8 BSTLOOP Register

Memory location: 0x07

Table 7-12. BSTLOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	TI_internal	R/W	01000	TI internal use. Do not read or write.
2:0	RC	R/W	000	Compensation resistor set bit. 000: 200k 001: 250k 010: 100k 011: 150k 100: 400k 101: 450k 110: 300k 111: 350k

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The devices are step up dc/dc converters with true bypass function integrated. They are typically used as pre-regulators with input voltage ranges from 2.0V to 5.0V, extend the battery run time and overcome input current and input voltage limitations of the system being powered.

While the input voltage higher than boost/bypass threshold, the high-efficient integrated bypass path connects the battery to the powered system directly.

If the input voltage becomes lower than boost/bypass threshold, the device seamlessly transitions into the boost mode operation.

Use the following design procedure to select component values for the both TLV61290 and TLV612901.

8.2 Typical Application

8.2.1 TLV61290 with 2.5V-4.35V V_{IN}, 3.4V V_{OUT}, 4A Output Current

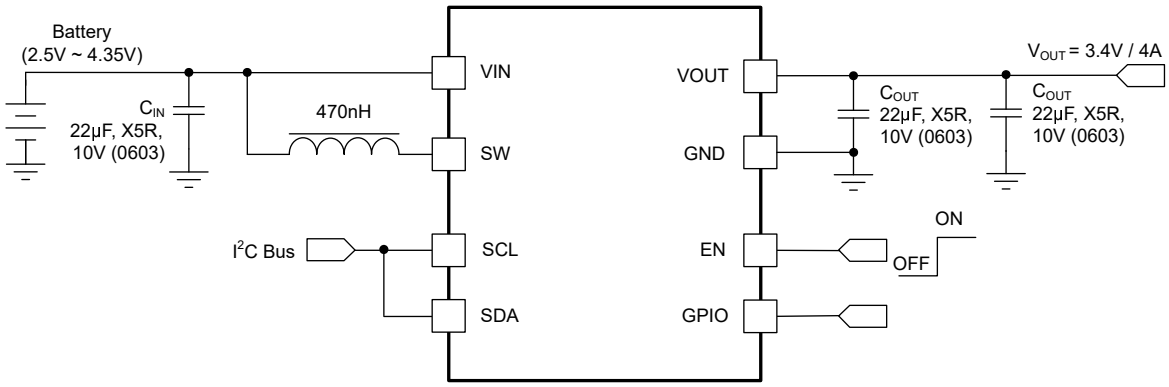


Figure 8-1. TLV61290 with 2.5V-4.35V V_{IN}, 3.4V V_{OUT}, 4A Output Current

8.2.1.1 Design Requirement

Table 8-1. Design Parameters

REFERENCE	DESCRIPTION	SAMPLE VALUES
V_{IN}	Input voltage range	2.5V-4.35V
V_{OUT}	Output voltage range at Boost Mode	V_{OUT} = 3.4V
	Output voltage range Bypass Mode	$V_{OUT}= V_{IN} - I_{OUT} * R_{DS(ON)\_BYP}$
I_{OUT}	Output current	4A

8.2.1.2 Detailed Design Parameters

8.2.1.2.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor are required. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches.

The inductor peak current varies as a function of the load, the input and output voltages and is estimated using Equation 7.

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times \eta} \text{ with } D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (7)$$

Selecting an inductor with insufficient saturation performance leads to excessive peak current in the converter. This current could eventually harm the device and reduce the reliability of the device.

When selecting the inductor, as well as the inductance, parameters of importance are: maximum current rating, series resistance, and operating temperature. Enable the inductor DC current rating to be greater than the maximum input average current, refer to the *Section 7.4.10* section for more details.

$$I_{L(DC)} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta} \times I_{OUT} \quad (8)$$

The TLV61290 series of step-up converters have been optimized to operate with a effective inductance in the range of 330nH to 560nH. Larger or smaller inductor values are used to optimize the performance of the device for specific operating conditions. For more details, see the *Section 8.2.1.2.4* section.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

For good efficiency, enable the inductor DC resistance to be less than 30mΩ. The following inductor series from different suppliers have recommended with the TLV61290 converters.

Table 8-2. List of Inductors

SERIES	L (nH)	DIMENSIONS (in mm)	DC INPUT CURRENT LIMIT SETTING	MANUFACTURER(1)
HTTO32251T-R47MMR	470	3.2 x 2.5 x 1.0 max. height	≤8600mA	Cyntec
744383340047	470	3.4 x 3.4 x 1.2 max. height	≤9400mA	Wurth Elektronik
XGL4012-451	450	4.0 x 4.0 x 1.2 max. height	≤9900mA	Coilcraft
DFE32CAHR47MR0	470	3.2 x 2.5 x 2.0 max. height	≤8700mA	Murata

(1) See *Third-Party Products Disclaimer*

8.2.1.2.2 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors that do not fit close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. To get an estimate of the recommended minimum output capacitance, use Equation 9.

$$C_{MIN} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (9)$$

where f is the switching frequency and ΔV is the maximum allowed output ripple.

The total ripple will be larger due to the ESR and ESL of the output capacitor. Calculate this additional component of the ripple using:

$$\Delta V_{OUT(ESR)} = ESR \times \left(\frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2} \right) \quad (10)$$

$$\Delta V_{OUT(ESL)} = ESL \times \left(\frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2} - I_{OUT} \right) \times \frac{1}{t_{SW(RISE)}} \quad (11)$$

$$\Delta V_{OUT(ESL)} = ESL \times \left(\frac{I_{OUT}}{1 - D} - \frac{\Delta I_L}{2} - I_{OUT} \right) \times \frac{1}{t_{SW(FALL)}} \quad (12)$$

where

- I_{OUT} = output current of the application
- D = duty cycle
- ΔI_L = inductor ripple current
- $t_{SW(RISE)}$ = switch node rise time
- $t_{SW(FALL)}$ = switch node fall time
- ESR = equivalent series resistance of the used output capacitor
- ESL = equivalent series inductance of the used output capacitor

Use an MLCC capacitor with twice the value of the calculated minimum because of the DC bias effects. This capacitor is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

For most of the application cases, 2pcs 22µF X5R 10V (0603) MLCC capacitors is recommended to use.

In applications featuring high (pulsed) load currents (for example: ≥ 3.4V / 4A), it is recommended to run the converter with a reasonable amount of effective output capacitance and low-ESL device, for instance 3pcs 22µF X5R 10V (0603) MLCC capacitors.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the effective capacitance of the device. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and effective capacitance of the capacitor. For instance, a 22µF X5R 6.3V (0603) MLCC capacitor typically shows an effective capacitance of less than 10µF (under 3.4V DC bias and 20mV AC bias condition).

For RF Power Amplifier applications, the output capacitor loading is combined between the DC/DC converter and the RF Power Amplifier + PA input capacitors.

High values of output capacitance are mainly achieved by putting capacitors in parallel. This reduces the overall series resistance (ESR) to very low values. This results in almost no voltage ripple at the output and therefore the regulation circuit has no voltage drop to react on. Nevertheless, for accurate output voltage regulation even with low ESR, the regulation loop switches to a pure comparator regulation scheme.

8.2.1.2.3 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Place capacitors as close as possible to the device. While a 22µF input capacitor is sufficient for most applications. To further reduce input current ripple without limitations, use larger values.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output induces ringing at the V_{IN} pin. This ringing couples to the output and be mistaken as loop instability or damage the part. To reduce ringing that occurs between the inductance of the power source leads and C_I, place "bulk" capacitance (electrolytic or tantalum) between C_I and the power source.

8.2.1.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. Signs of instability in the regulation loop include switching waveforms showing large duty cycle jitter, or the output voltage or inductor current showing oscillations. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, enable the output capacitor to supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, monitor V_{OUT} for settling time, overshoot or ringing that helps judge the stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (that is, MOSFET $r_{DS(on)}$) that are temperature dependent, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

The TLV61290 series of step-up converters have been optimized to operate with a effective inductance in the range of 330nH to 560nH and with output capacitors in the range of 11µF to 100µF. The internal compensation is optimized for an output filter of L = 0.47µH and effective C_O = 14µF.

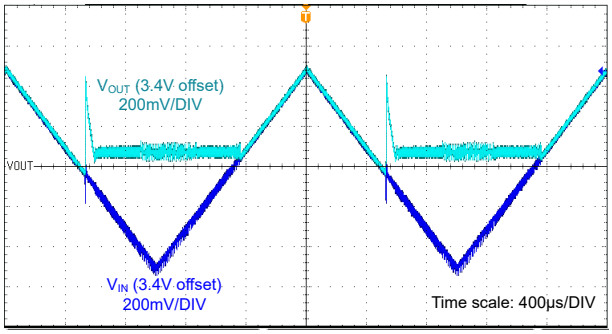
Table 8-3. Component List

REFERENCE	DESCRIPTION	PART NUMBER, MANUFACTURER(1)
C_{IN}	22µF, 10V, 0603, X5R ceramic	GRM187R61A226ME15D
C_{OUT}	2 x 22µF, 10V, 0603, X5R ceramic	2 x GRM187R61A226ME15D
L	450nH, 13.8mΩ, 4.0mm x 4.0mm x 1.2mm	XGL4012-451

(1) See *Third-Party Products Disclaimer*

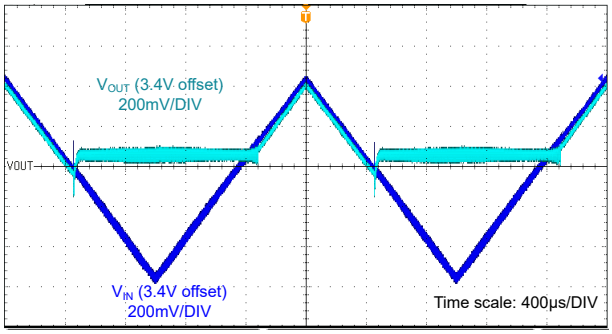
8.2.1.3 Application Curves

Typical condition V_{IN} = 2.5V to 4.35V, V_{OUT_TAR} = 3.4V, T_J = 25°C, unless otherwise noted



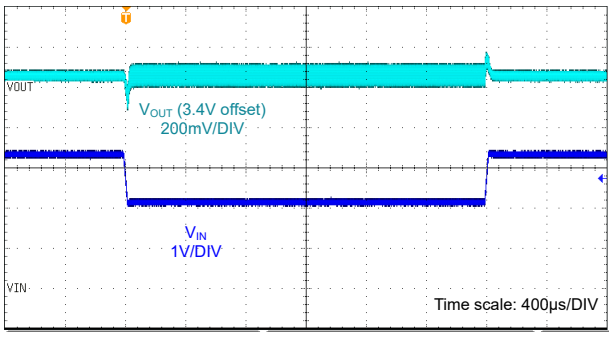
V_{OUT_TAR} = 3.4V T_A = 25°C Auto PFM Load = 100mA

Figure 8-2. Boost to bypass Mode Exit / Entry



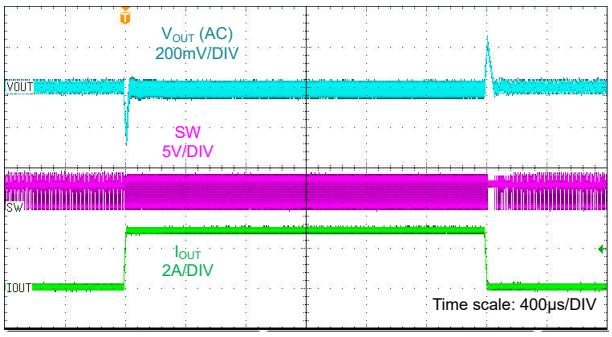
V_{OUT_TAR} = 3.4V T_A = 25°C Auto PFM Load = 3A

Figure 8-3. Boost to bypass Mode Exit / Entry



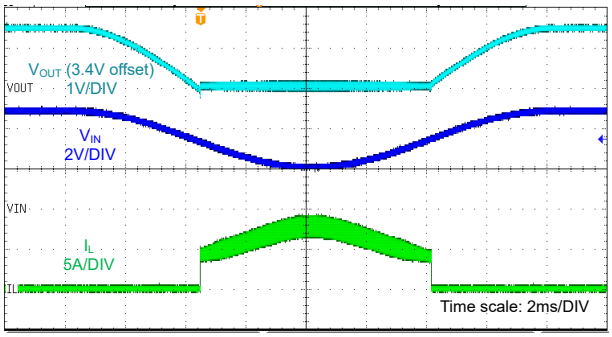
V_{OUT_TAR} = 3.4V T_A = 25°C Auto PFM Load = 4A
VIN = 2V to 3.4V with 20µs slew rate

Figure 8-4. Line Transient Response



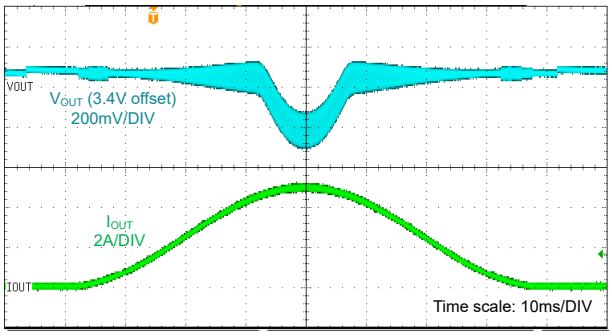
V_{OUT_TAR} = 3.4V V_{IN} = 2.7V Auto PFM
Load = 0.1A - 3A, 0.2A/µs slew rate

Figure 8-5. Load Transient Response



V_{OUT_TAR} = 3.4V T_A = 25°C Auto PFM Load = 4A
VIN = 5V to 2.2V sweep

Figure 8-6. Line Sweep



V_{OUT_TAR} = 3.4V V_{IN} = 2.7V Auto PFM
Load = 0A to 5A sweep

Figure 8-7. Load Sweep

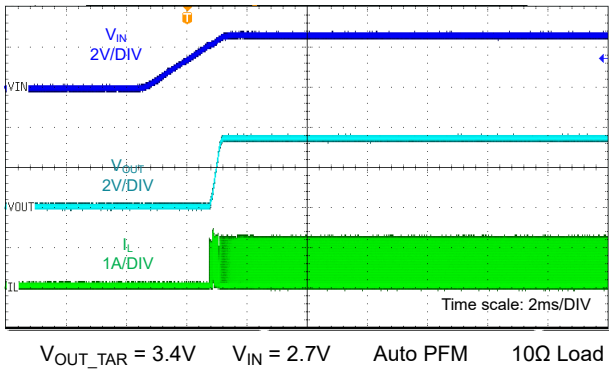


Figure 8-8. Start-Up by V_{IN}

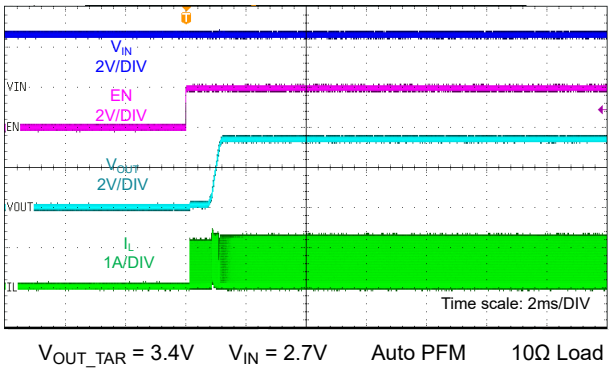


Figure 8-9. Start-Up by EN

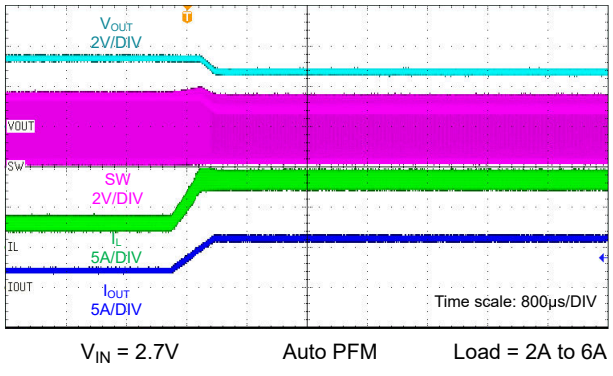


Figure 8-10. Current Limit Operation at Boost Mode

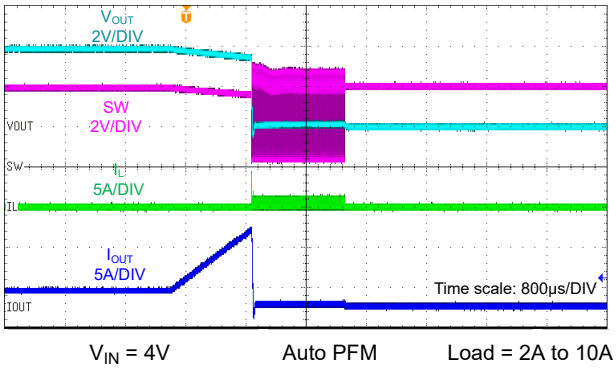


Figure 8-11. Current Limit Operation at Bypass Mode

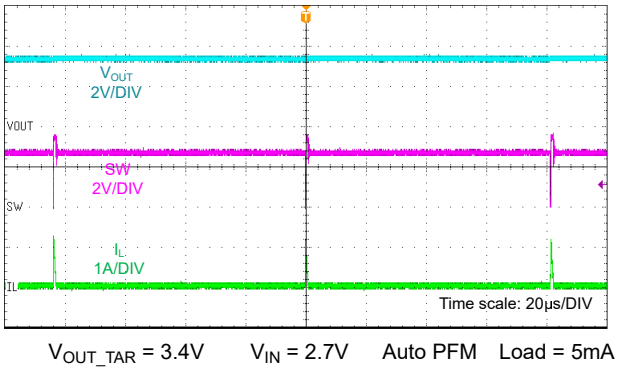


Figure 8-12. Switching Waveform at Light Load

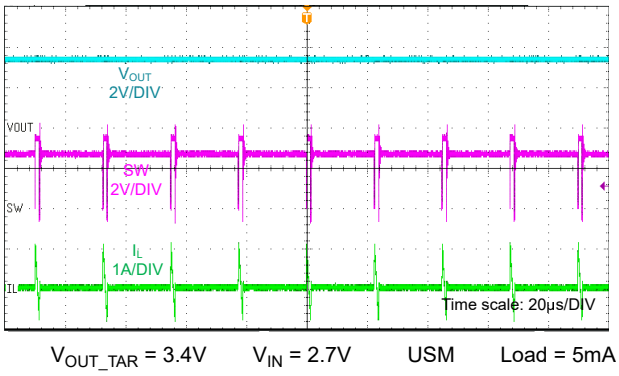


Figure 8-13. Switching Waveform at Light Load

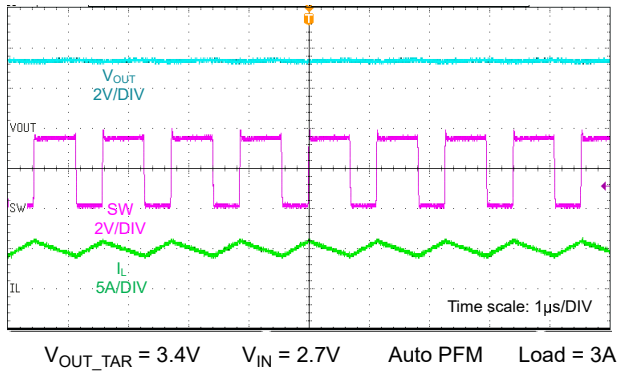


Figure 8-14. Switching Waveform at Heavy Load

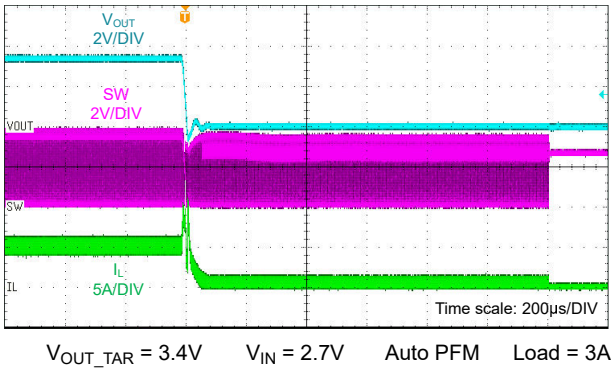


Figure 8-15. Output Short to Ground Protection

8.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 2.0V and 5.0V. Well regulate this input supply. If the input supply is located more than a few inches from the TLV61290 converter, additional bulk capacitance is required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47µF is a typical choice.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high current, layout is an important design step. If the layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switching rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

The input capacitor needs to be close to the VIN pin and PGND pin in order to reduce the I_{input} supply ripple.

The power paths of VOUT, output capacitor and PGND should be as small as possible, in order to reduce parasitic inductance.

The layout should also be done with well consideration of the thermal as this is a high power density device. The SW, VOUT and PGND pins that improves the thermal capabilities of the package should be soldered with the large polygon, using thermal vias underneath the SW pin could improve thermal performance.

8.4.2 Layout Example

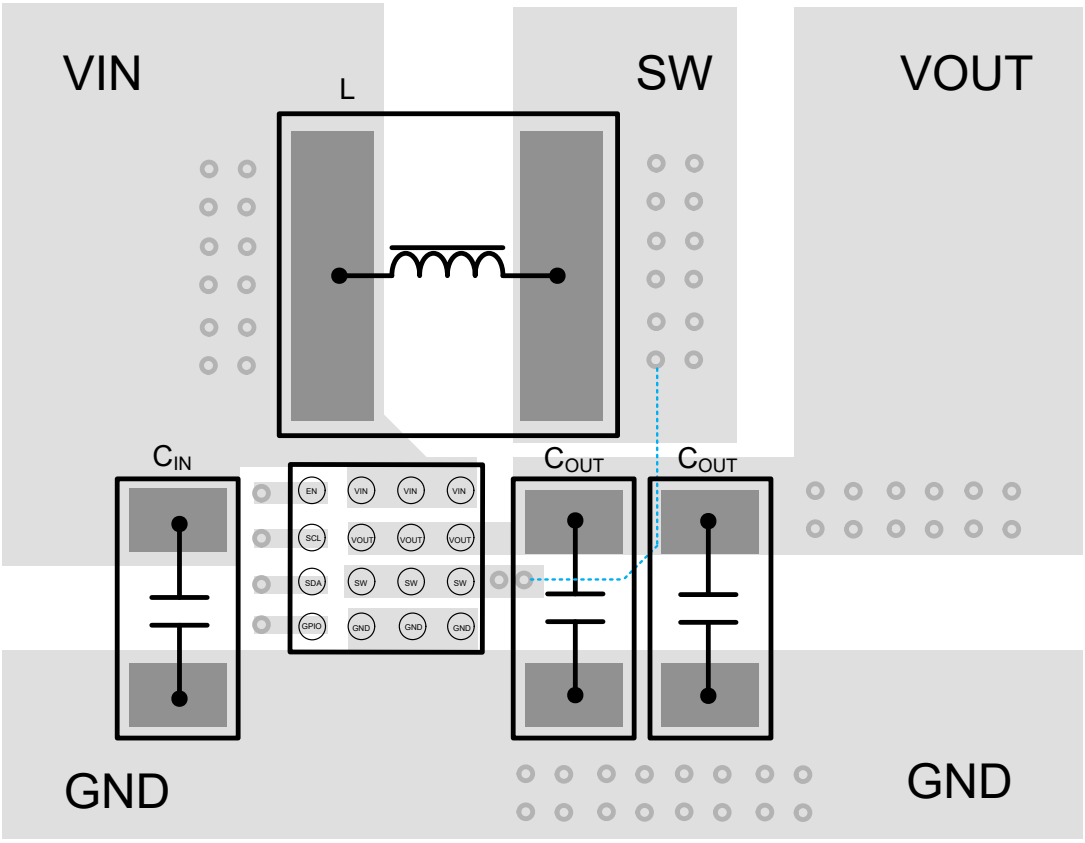


Figure 8-16. Suggested Layout (Top)

8.4.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The importance of power demand in portable designs is ever-growing, leading designers to choose what is best between efficiency, power dissipation, and solution size. Due to integration and miniaturization, junction temperature increases significantly which could lead to bad application behaviors (that is, premature thermal shutdown or worst case reduce device reliability).

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, pay special attention to thermal dissipation issues in board design. Keep the device operating junction temperature (T_J) below 125°C.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

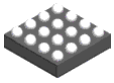
DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

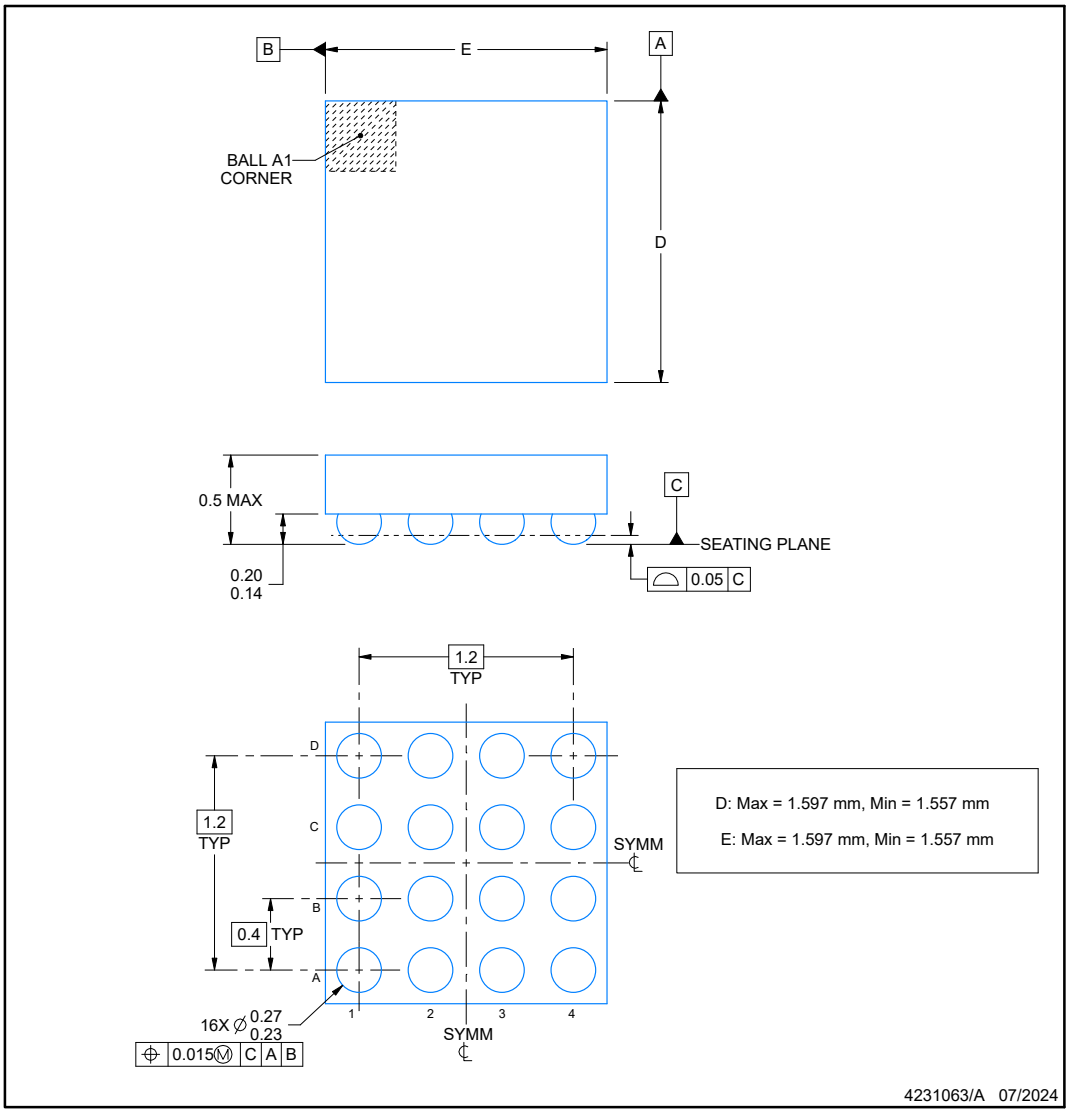
PACKAGE OUTLINE

YBG0016-C01



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

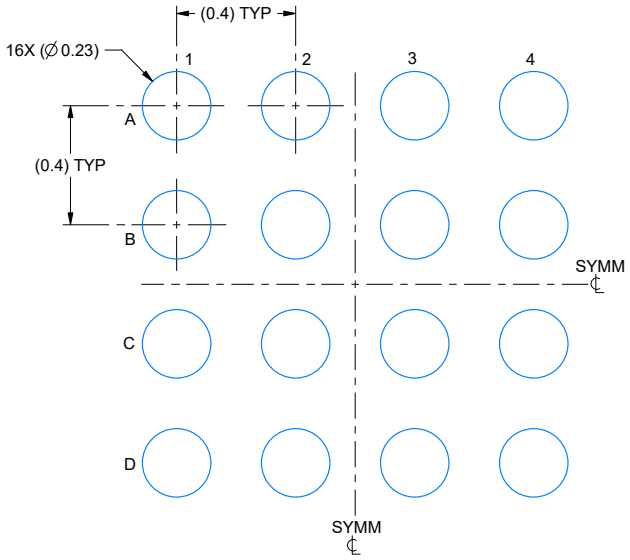
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

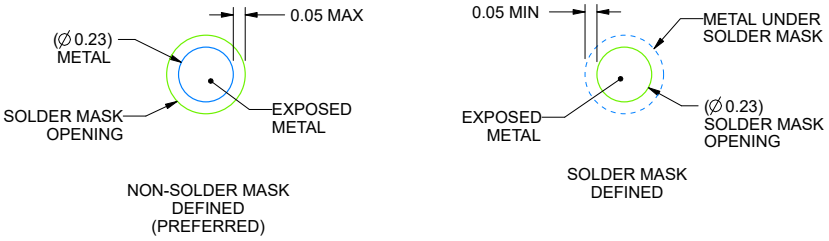
YBG0016-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4231063/A 07/2024

NOTES: (continued)

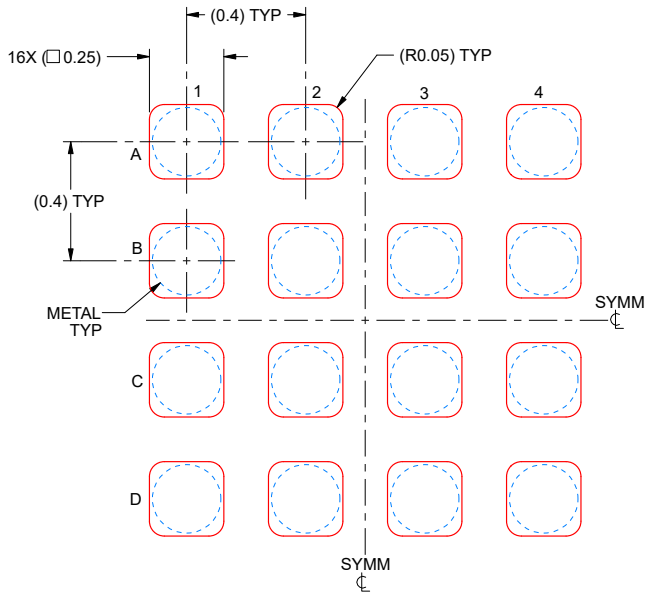
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0016-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4231063/A 07/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV61290YBGR	Active	Production	DSBGA (YBG) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	1ZG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

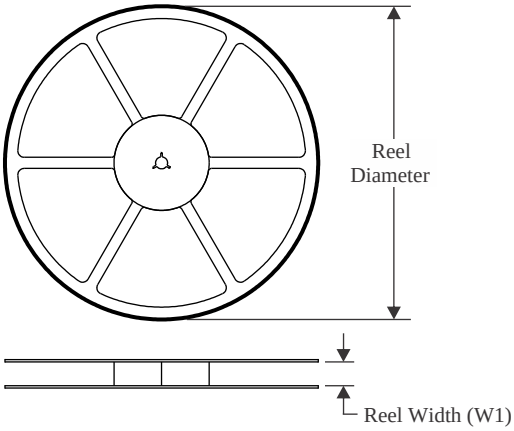
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

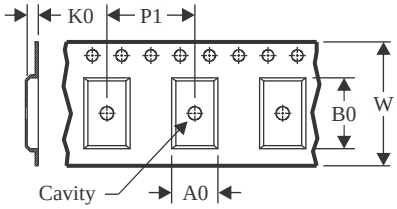
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

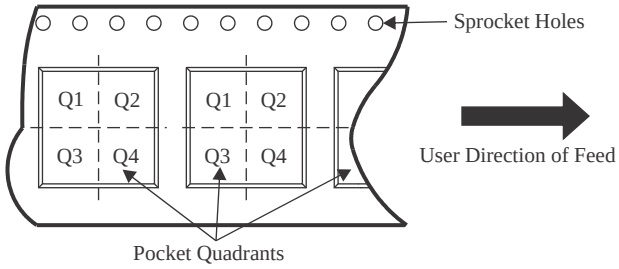


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

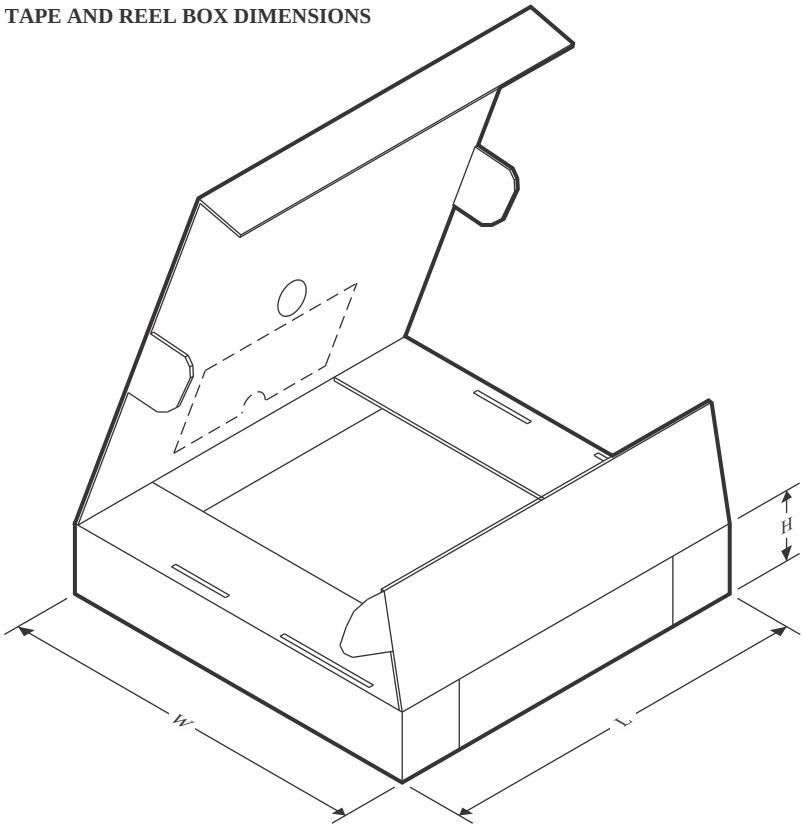
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV61290YBGR	DSBGA	YBG	16	3000	180.0	8.4	1.68	1.72	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV61290YBGR	DSBGA	YBG	16	3000	182.0	182.0	20.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265