- **2.7-V to 5.5-V Single-Supply Operation**
- **Four 8-Bit Voltage Output DACs**
- **One-Half Power 8-Bit Voltage Output DAC**
- **Fast Serial Interface . . . 1 MHz Max**
- **Simple Two-Wire Interface In Single Buffered Mode**
- **High-Impedance Reference Inputs For Each DAC**
- **Programmable for 1 or 2 Times Output Range**
- **Simultaneous-Update Facility In Double-Buffered Mode**
- **Internal Power-On Reset**
- **Industry Temperature Range**
- **Low Power Consumption**
- **Half-Buffered Output**
- **Power-Down Mode**

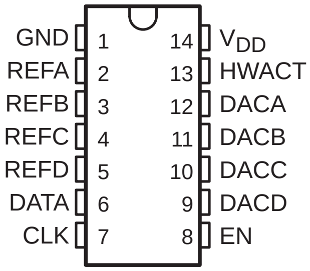
applications

- **Programmable Voltage Sources**
- **Digitally-Controlled Amplifiers/Attenuators**
- **Cordless/Wireless Communications**
- **Automatic Test Equipment**
- **Portable Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLV5621I is a quadruple 8-bit voltage output digital-to-analog converter (DAC) with buffered reference inputs (high impedance). The DAC produces an output voltage that ranges between either one or two times the reference voltages and GND, and the DAC is monotonic. The device is simple to use since it operates from a single supply of 2.7 V to 5.5 V. A power-on reset function is incorporated to provide repeatable start-up conditions. A global hardware shut-down terminal and the capability to shut down each individual DAC with software are provided to minimize power consumption.

D PACKAGE
(TOP VIEW)



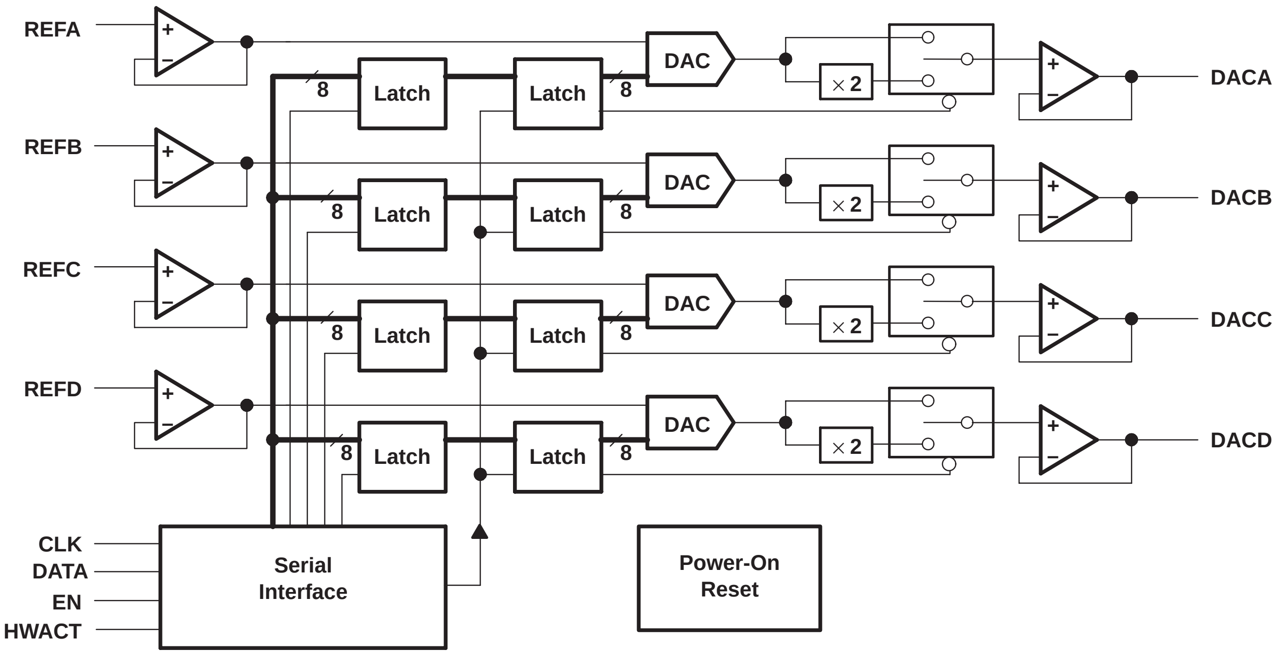
Digital control of the TLV5621I is over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. A TLV5621I 11-bit command word consists of eight bits of data, two DAC select bits, and a range bit for selection between the times one or times two output range. The TLV5621I digital inputs feature Schmitt triggers for high noise immunity. The DAC registers are double buffered which allows a complete set of new values to be written to the device, and then under control of the HWACT signal, all of the DAC outputs are updated simultaneously.

The 14-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLV5621I does not require external trimming. The TLV5621I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

PACKAGE	
T_A	SMALL OUTLINE (D)
–40°C to 85°C	TLV5621ID

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock, data enters on the negative edge
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial-interface digital-data input
EN	8	I	Input enable
GND	1		Ground return and reference
HWACT	13	I	Global hardware activate
REFA	2	I	Reference voltage input to DACA
REFB	3	I	Reference voltage input to DACB
REFC	4	I	Reference voltage input to DACC
REFD	5	I	Reference voltage input to DACD
V_{DD}	14		Positive supply voltage

detailed description

The TLV5621 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to GND and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always present a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times one or times two gain.

On power-up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\mathrm{DACA|B|C|D}) = \mathrm{REF} \times \frac{\mathrm{CODE}}{256} \times (1 + \mathrm{RNG\ bit\ value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial control word.

Table 1. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

data interface

The data interface has two modes of operation; single and double buffered. Both modes serially clock in bits of data using DATA and CLK whenever EN is high. When EN is low, CLK is disabled and data cannot be loaded into the buffers.

In the single buffered mode, the DAC outputs are updated on the last/twelfth falling edge of CLK, so this mode only requires a two-wire interface with EN tied high (see Figure 1 and Figure 2).

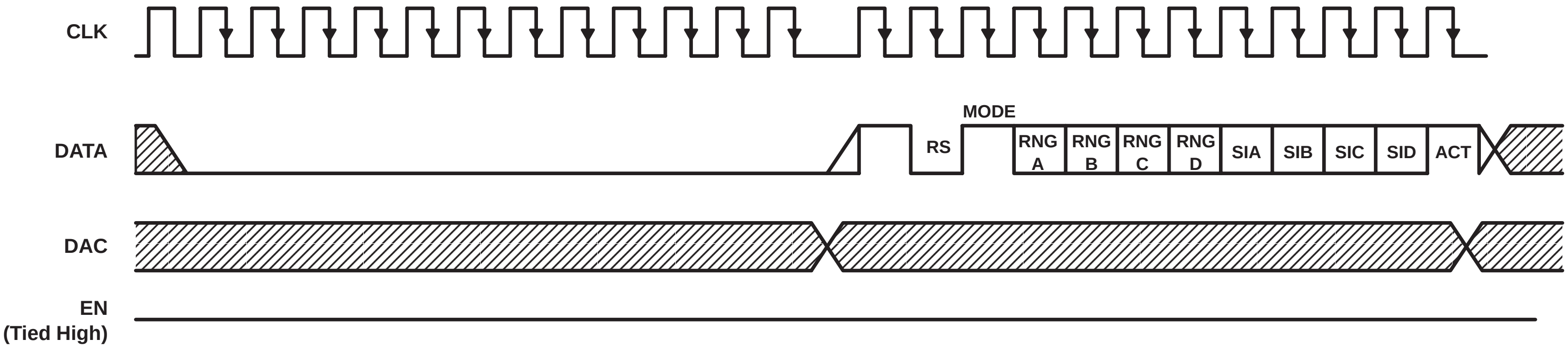
In the double buffered mode (startup default), the outputs of the DACs are updated on the falling edge of the EN strobe (see Figure 3 and Figure 4). This allows multiple devices to share data and clock lines by having only separate EN lines.

single-buffer mode (MODE = 1)

When a two wire interface is used, EN is tied high and the input to the device is always active; therefore, random data can be clocked into the input latch. In order to regain word synchronization, twelve zeros are clocked in as shown in Figure 1, and then a data or control word is clocked in. In Figure 1, the MODE bit is set to one, and a control word is clocked in with the DAC outputs becoming active after the last falling edge of the control word.

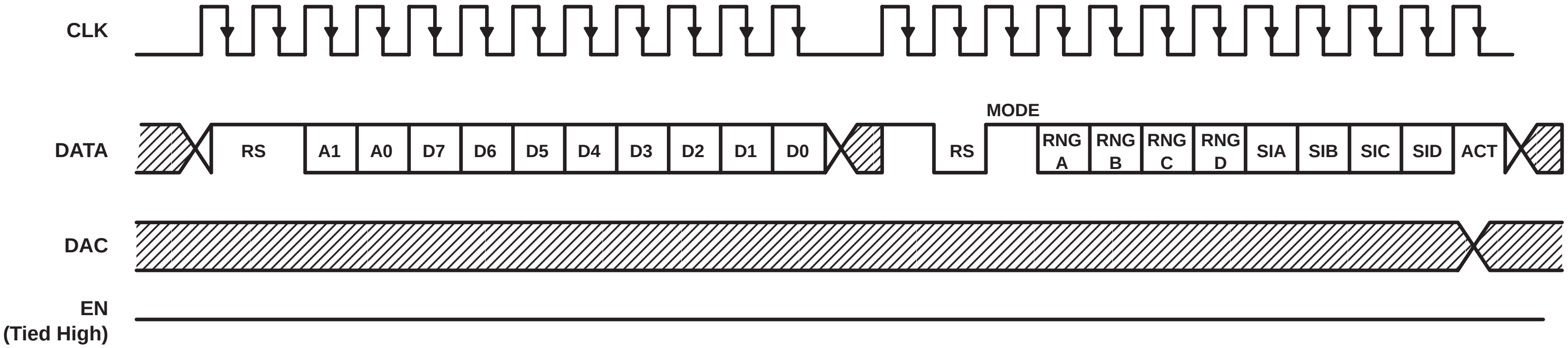
Figure 2 shows valid data being written to a DAC, note that CLK is held low while the data is invalid. Data can be written to all four DACs and then the control word is clocked in which sets the MODE bit to 1. At the end of the control word, the data is latched to the inputs of the DACs.

Note that once the MODE bit has been set, it is not possible to clear it, i.e., it is not possible to move from single to double-buffered mode.



NOTE A: Twelve zeros enable word synchronization and the output can change after the leading edge of CLK depending on the data in the latches.

Figure 1. Register Write Operation Following Noise or Undefined Levels on DATA or CLK (Single-Buffer Mode)



NOTE A: EN is held high and data is written to a DAC register. The data is latched to the output of the DAC on the falling edge of the last CLK of the control word, where the mode is set.

Figure 2. First Nonzero Write Operation After Startup (EN = High)

double-buffered mode (MODE = 0)

In this mode, data is only latched to the output of the DACs on the falling edge of the EN strobe. Therefore, all four DACs can be written to before updating their outputs.

Any number of input data blocks can be written with all having the same length. Subsequent data blocks simply overwrite previous ones with the same address until EN goes low.

Multiple data blocks can be written in any sequence provided signal timing limits are met. The negative going edge of EN terminates and latches all data.

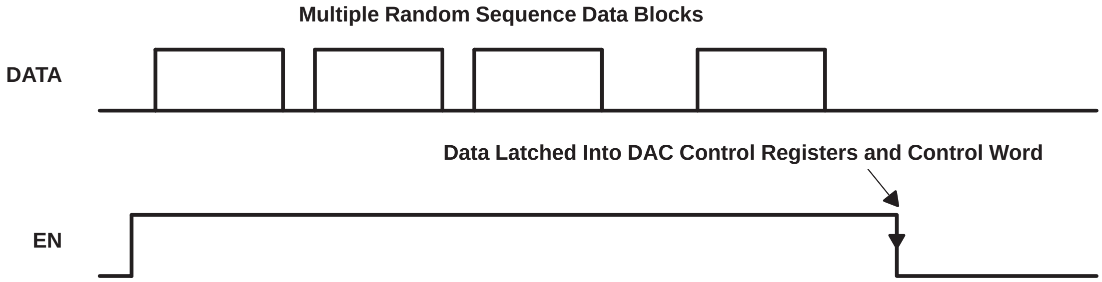
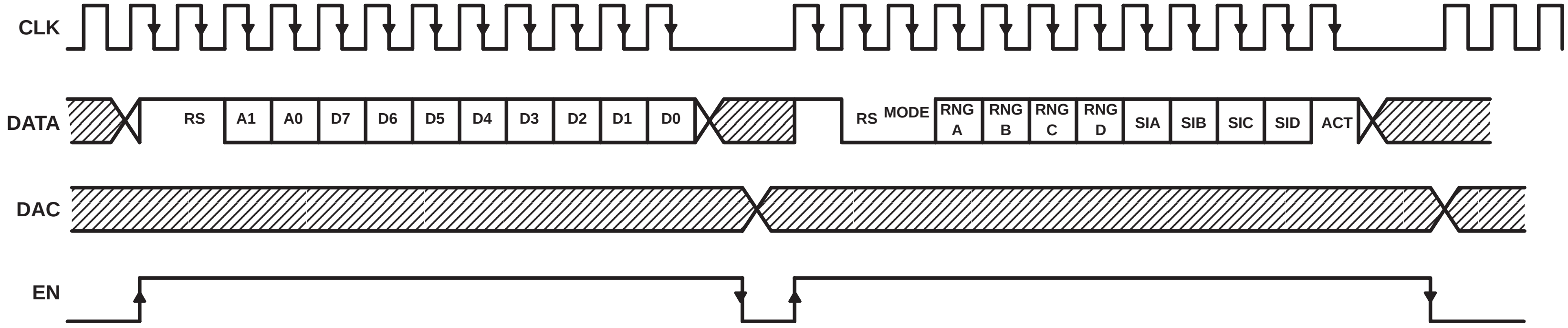


Figure 3. Data and Control Serial Control



NOTE A: Data is written to the output of a DAC, and the data is latched to the output on the falling edge of EN. A control word then selects double-buffered mode. When the range is changed, the output changes on the falling edge of EN.

Figure 4. First Nonzero Write Operation After Startup

control register

The control register contains ten active bits. Four bits are range select bits as on the TLC5620. The register also contains a software shutdown bit (ACT) and four shutdown inhibit bits (SIA, SIB, SIC, SID). The shutdown inhibit bits act on each DAC (DACA through DACD). The mode select bit is used to change between single and double buffered modes. The bits in the control register are listed in Table 2.

Table 2. Control Register Bits

BIT	FUNCTION
MODE	Selection bit for type of interface (see data interface section)
RNG A	Range select bit for DACA, 0 = ×1, 1 = ×2
RNG B	Range select bit for DACB, 0 = ×1, 1 = ×2
RNG C	Range select bit for DACC, 0 = ×1, 1 = ×2
RNG D	Range select bit for DACD, 0 = ×1, 1 = ×2
SIA	Shutdown inhibit bit for DACA
SIB	Shutdown inhibit bit for DACB
SIC	Shutdown inhibit bit for DACC
SID	Shutdown inhibit bit for DACD
ACT	Software shutdown bit

The SIx bits inhibit the actions of the shutdown bits as shown in Table 3. When the ACT bit is 1 or the HWACT signal is high (active), the inhibit bits act as enable bits in inverse logic terms. The ACT software shutdown bit and HWACT (asynchronously acting hardware terminal) are logically ORed together.

This configuration allows any combination of DACs to be shut down to save power.

Table 3. Shutdown Inhibit Bits and HWACT Signal

SIx	ACT	HWACT	DACx STATUS
0	0	L	Shutdown (see Note 1)
0	0	H	Shutdown
0	1	L	Shutdown
0	1	H	Active (see Note 1)
1	0	L	Active
1	0	H	Active
1	1	L	Active
1	1	H	Active

NOTE 1: Sense of HWACT terminal and ACT bit were changed from early versions of this specification.

The values of the input address select bits, A0 and A1, and the updated DAC are listed in Table 4.

Table 4. Serial Input Decode

INPUT ADDRESS SELECT BITS		DAC UPDATED
A1	A0	
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

power-on reset

Power-on reset circuitry is available on the TLV5621I. The threshold to trigger a power-on reset is 1.95 V typical (1.4 V min and 2.5 V max). For a power-on reset, all DACs are shut down. The control register bit values and states after a power-on reset are listed in Table 5.

Table 5. Control Register Bit Values and States After Power-On Reset

BIT	VALUE	STATE AFTER POWER-ON RESET
MODE	0	Double buffer mode selected
RNG A	1	Range ×2
RNG B	1	Range ×2
RNG C	1	Range ×2
RNG D	1	Range ×2
SIA	0	Shutdown affects DACA according to ACT state
SIB	0	Shutdown affects DACB according to ACT state
SIC	0	Shutdown affects DACC according to ACT state
SID	0	Shutdown affects DACD according to ACT state
ACT	0	DACs in shutdown state

linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

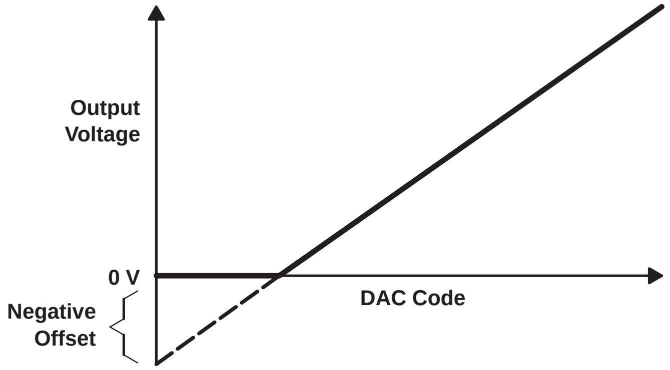
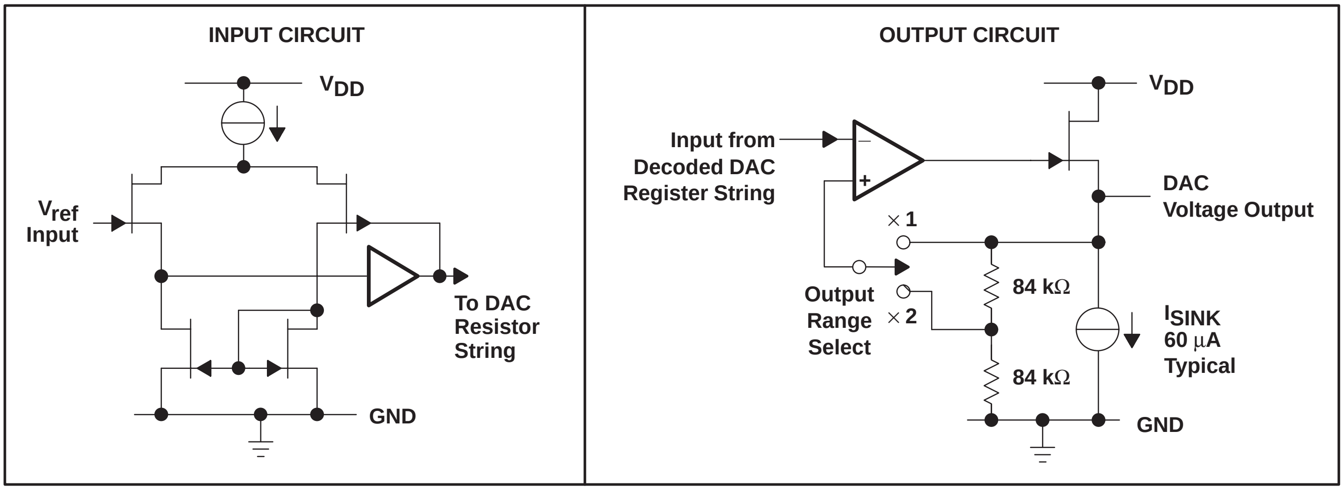


Figure 5. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset.

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND)	7 V
Digital input voltage range	GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID}	GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 2)	2.7	3.3	5.5	V
High-level digital input voltage, V_{IH}	0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}			0.2 V_{DD}	V
Reference voltage, V_{ref} [A|B|C|D], x1 gain	GND		$V_{DD}-1.5$	V
Load resistance, R_L	10			kΩ
Setup time, data input, $t_{su(DATA\text{-}CLK)}$ (see Figure 6)	50			ns
Hold time, data input valid after CLK↓, $t_{h(DATA\text{-}CLK)}$ (see Figure 6)	50			ns
Setup time, CLK↓ to EN↓, $t_{su(CLK\text{-}EN)}$ (see Figure 7)	100			ns
Setup time, EN↑ to CLK↓, $t_{su(EN\text{-}CLK)}$ (see Figure 7) (see Note 3)	100			ns
Pulse duration, EN low, $t_{w(EN)}$ (see Figure 7) (see Note 3)	200			ns
Pulse duration, CLK high, $t_{w(CLK)}$ (see Figure 6) (see Note 3)	400			ns
CLK frequency			1	MHz
Operating free-air temperature, T_A	–40		85	°C

NOTES: 2. The device operates over the supply voltage range of 2.7 V to 5.5 V. Over this voltage range the device responds correctly to data input by changing the output voltage but conversion accuracy is not specified over this extended range.

3. This is specified by design but is not production tested.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 1.25 V, GND = 0 V, R_L = 10 kΩ, C_L = 100 pF, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_O$max	Maximum full-scale output voltage	V_{ref} = 1.5 V, open circuit output, × 2 gain	V_{DD} – 100	2		mV
$I_{IH(digital)}$	High-level digital input current	$V_I = V_{DD}$			±10	μA
$I_{IL(digital)}$	Low-level digital input current	V_I = 0 V			±10	μA
$I_{O(sink)}$	Output sink current, DACA	DAC code 0	5			μA
	Output sink current, DACB, DACC, DACD	DAC code 0	20			μA
$I_{O(source)}$	Output source current	Each DAC output, DAC code 255	1			mA
C_i	Input capacitance			15		pF
	Reference input capacitance	A, B, C, D inputs		15		
I_{DD}	Supply current	V_{DD} = 3.6 V		1	1.5	mA
		V_{DD} = 5 V		1	1.5	mA
$I_{DD(active)}$	Supply current, one low power DAC active	V_{DD} = 3.6 V, See Note 4		150	250	μA
$I_{DD(shutdown)}$	Supply current, all DACs shut down	V_{DD} = 3.6 V, See Note 4		50	100	μA
I_{ref}	Reference input current	A, B, C, D inputs			±10	μA
E_L	Integral linearity error	V_{ref} = 1.25 V, × 2 gain, See Notes 5 and 13			±1	LSB
E_D	Differential linearity error	V_{ref} = 1.25 V, × 2 gain, See Notes 6 and 13		±0.1	±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 1.25 V, × 2 gain, See Note 7	0		30	mV
	Zero-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain, See Note 8		10		μV/°C
	Zero-scale error supply rejection			2		mV/V
E_{FS}	Full-scale error	V_{ref} = 1.25 V, × 2 gain, See Note 9			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain, See Note 10		±25		μV/°C
	Full-scale error supply rejection			2		mV/V
PSRR	Power-supply sensitivity	See Notes 11 and 12		0.5		mV/V
	Feedback resistor network resistance			168		kΩ

NOTES:
4. This is measured with no load (open circuit output), V_{ref} = 1.25 V, range = × 2.
5. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
6. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
7. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
8. Zero-scale error temperature coefficient is given by: ZSETC = $[ZSE(T_{max}) – ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
9. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
10. Full-scale temperature coefficient is given by: FSETC = $[FSE(T_{max}) – FSE (T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
11. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the effect of this signal on the zero-code output voltage.
12. Full-scale error rejection ratio (FSE-RR) is measured by varing the V_{DD} voltage from 3 V to 3.6 V dc and measuring the effect of this signal on the full-scale output voltage.
13. Linearity is only specified for DAC codes 1 through 255.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 1.25 V, GND = 0 V, R_L = 10 kΩ, C_L = 100 pF, × 1 gain output range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate, rising (DACA)			0.8		V/µs
Output slew rate, falling (DACA)			0.5		V/µs
Output slew rate (DACB, DACC, DACD)			1		V/µs
Output settling time, rising (DACA)	To 1/2 LSB, V_{DD} = 3 V		20		µs
Output settling time, falling (DACA)	To 1/2 LSB, V_{DD} = 3 V		75		µs
Output settling time, rising (DACB, DACC, DACD)	To 1/2 LSB, V_{DD} = 3 V		10		µs
Output settling time, falling (DACB, DACC, DACD)	To 1/2 LSB, V_{DD} = 3 V		75		µs
Output settling time, HWACT or ACT↑ to output volts (DACA) (see Note 14)	To 1/2 LSB, V_{DD} = 3 V		40	120†	µs
Output settling time, HWACT or ACT↑ to output volts (DACB, DACC, DACD) (see Note 14)	To 1/2 LSB, V_{DD} = 3 V		25	75†	µs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA–DACD		–50		dB
Reference feedthrough	A, B, C, D inputs, See Note 15		–60		dB
Channel-to-channel isolation	A, B, C, D inputs, See Note 16		–60		dB
Channel-to-channel isolation when in shutdown	A, B, C, D inputs		–40		dB
Reference bandwidth (DACA)	See Note 17		20		kHz
Reference bandwidth (DACB, DACC, DACD)	See Note 17		100		kHz

† This is specified by characterization but is not production tested.

NOTES: 14. The ACT bit is latched on EN↓.

15. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz.
16. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz.
17. Reference bandwidth is the –3 dB bandwidth with an ideal input at V_{ref} = 1.25 V dc + 2 V_{PP} and with a digital input code of full-scale (range set to × 1 and V_{DD} = 5 V).

PARAMETER MEASUREMENT INFORMATION

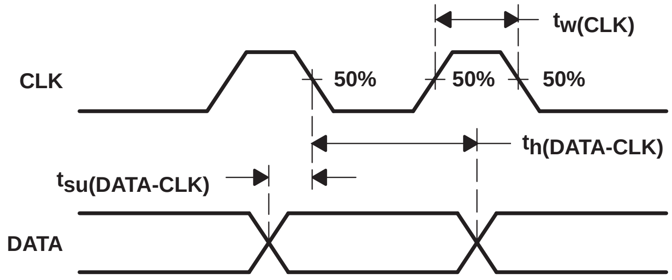


Figure 6. Timing of DATA Relative to CLK

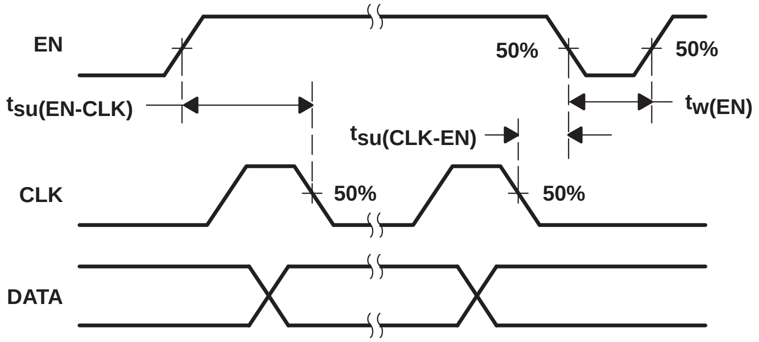


Figure 7. Timing of CLK Relative to EN

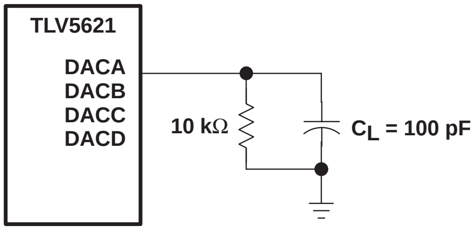
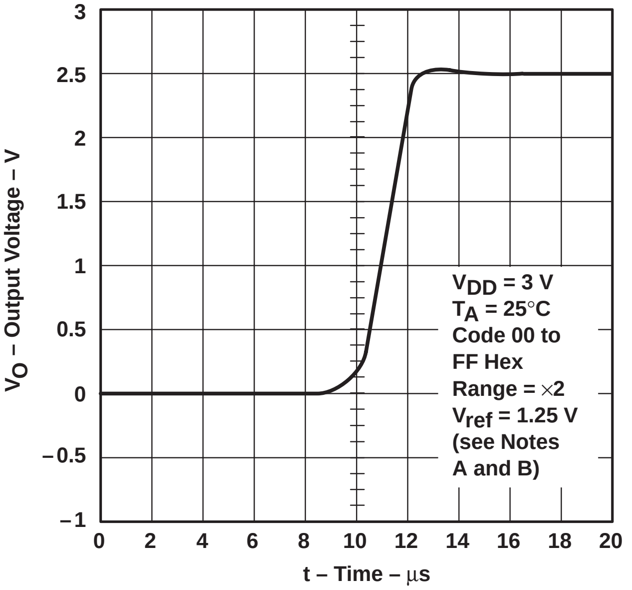


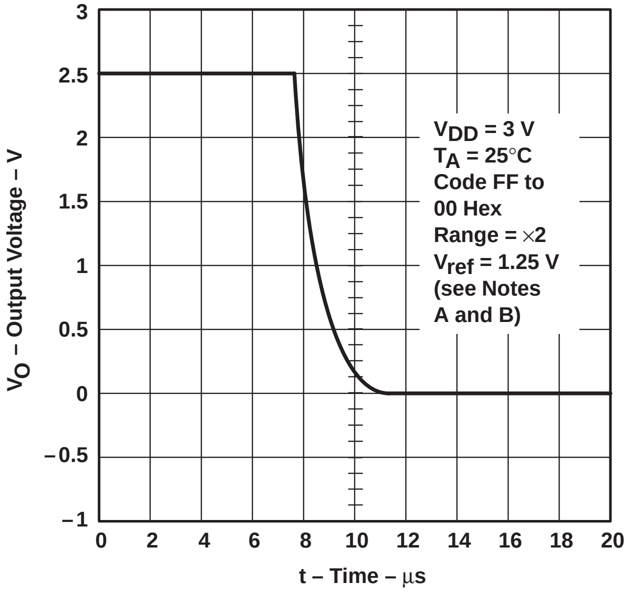
Figure 8. Slewing Settling Time and Linearity Measurements

TYPICAL CHARACTERISTICS


POSITIVE RISE TIME AND SETTLING TIME

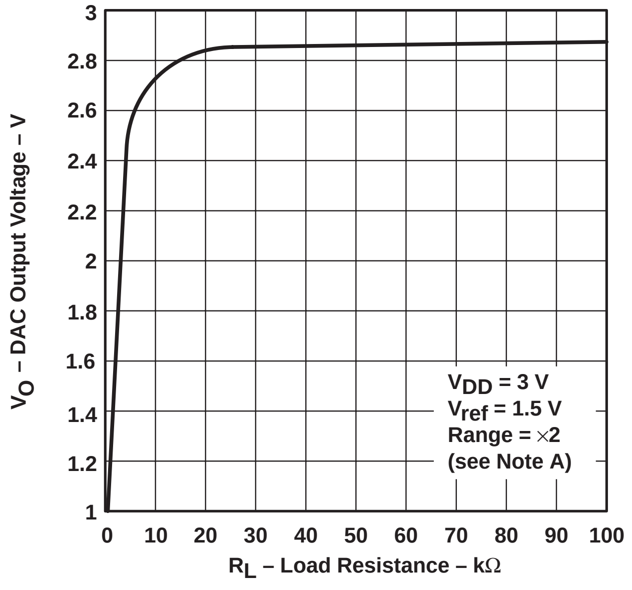
NOTES: A. Rise time = 2.05 µs, positive slew rate = 0.96 V/µs, settling time = 4.5 µs.
B. For DACB, DACC, and DACD

Figure 9


NEGATIVE FALL TIME AND SETTLING TIME

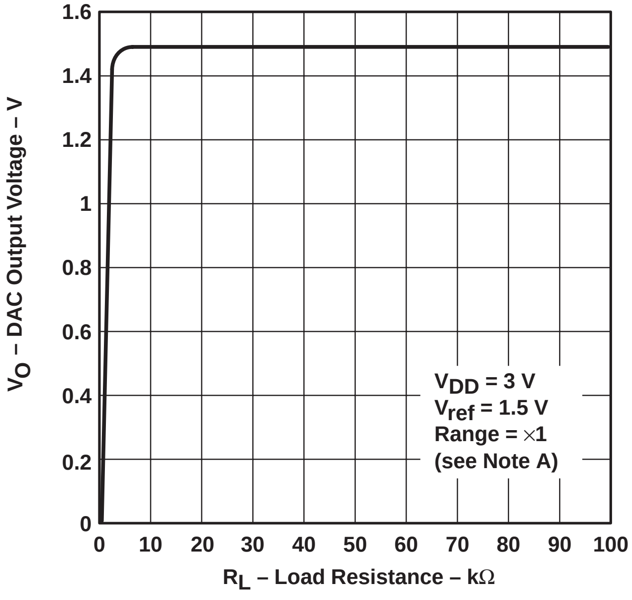
NOTES: A. Fall time = 4.25 µs, negative slew rate = 0.46 V/µs, settling time = 8.5 µs.
B. For DACB, DACC, and DACD

Figure 10


DAC OUTPUT VOLTAGE
vs
LOAD RESISTANCE

NOTE A: For DACB, DACC, and DACD

Figure 11


DAC OUTPUT VOLTAGE
vs
LOAD RESISTANCE

NOTE A: For DACB, DACC, and DACD

Figure 12

TYPICAL CHARACTERISTICS

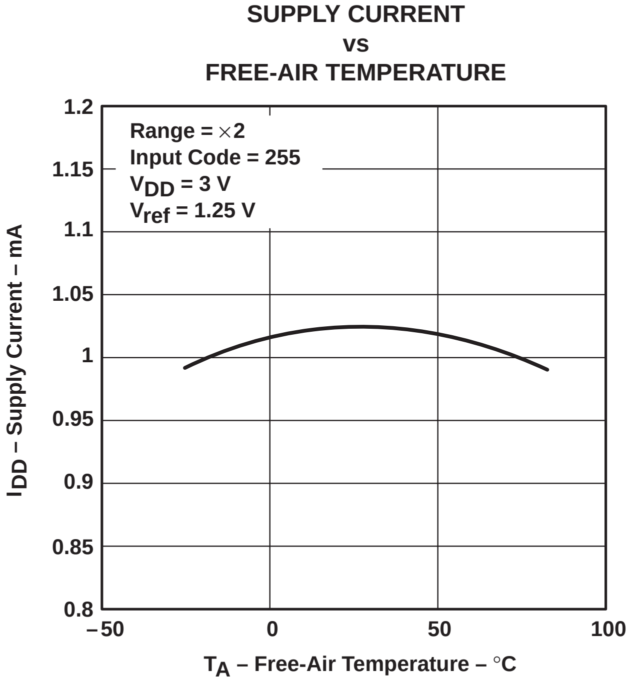
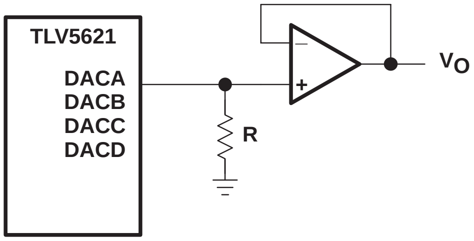


Figure 13

APPLICATION INFORMATION



NOTE A: Resistor R ≥ 10 kΩ

Figure 14. Output Buffering Scheme

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV5621ED	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5621E
TLV5621ED.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5621E
TLV5621ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5621I
TLV5621ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5621I
TLV5621IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5621I
TLV5621IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5621I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

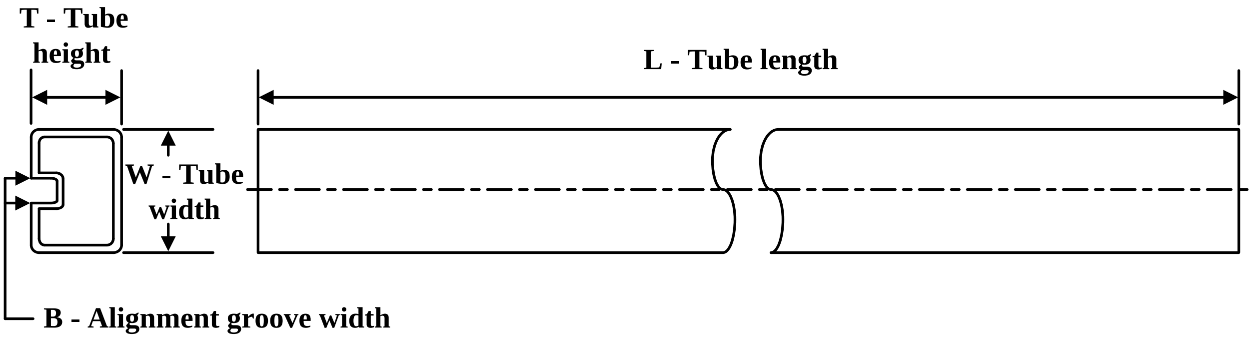
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

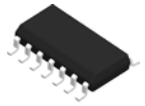
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5621ED	D	SOIC	14	50	505.46	6.76	3810	4
TLV5621ED.A	D	SOIC	14	50	505.46	6.76	3810	4
TLV5621ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV5621ID.A	D	SOIC	14	50	505.46	6.76	3810	4

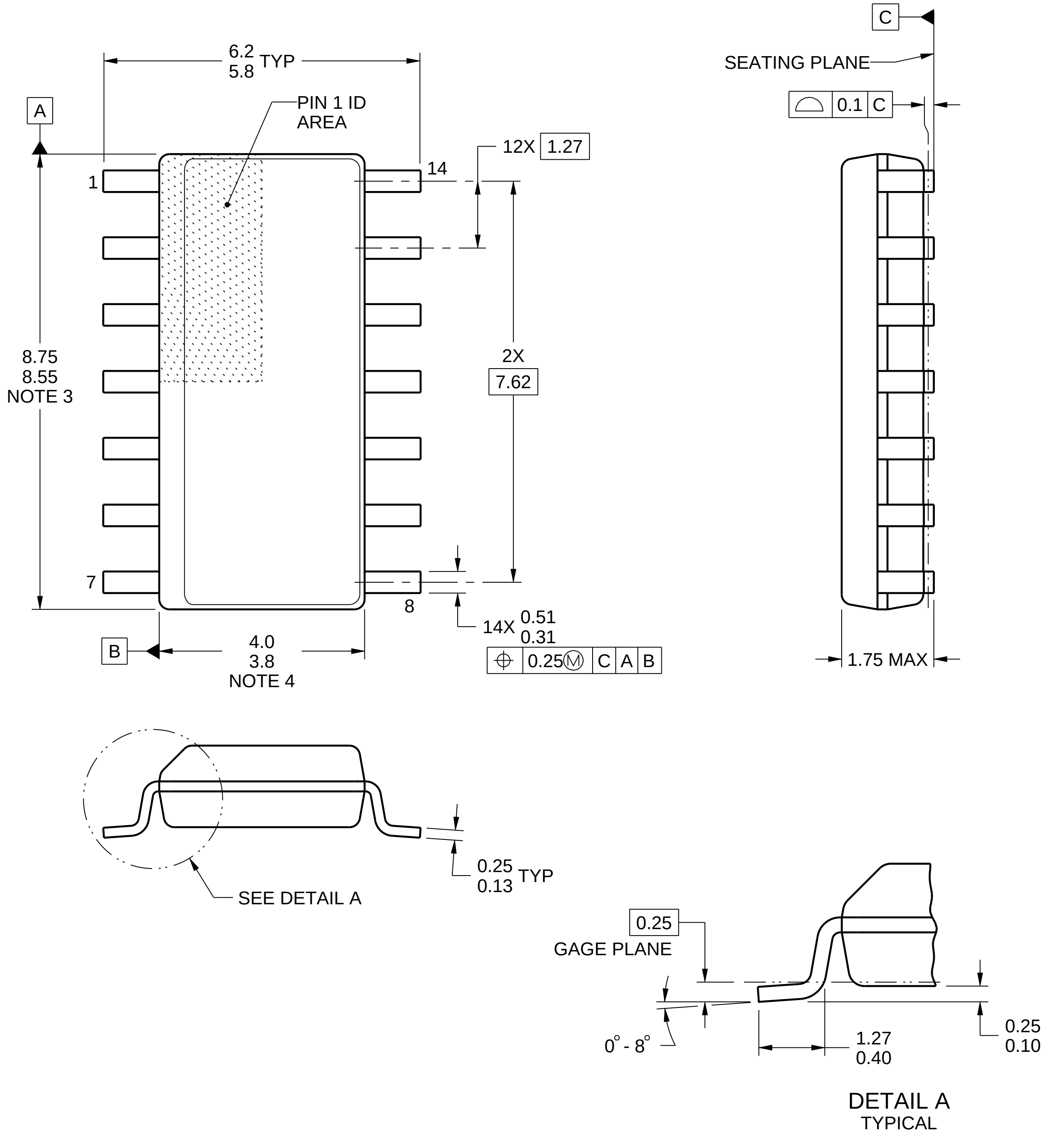


PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

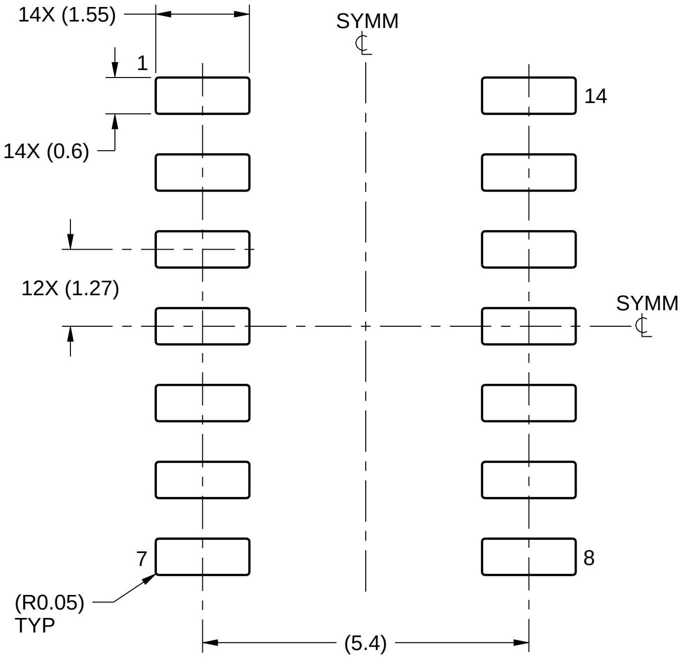
SMALL OUTLINE INTEGRATED CIRCUIT



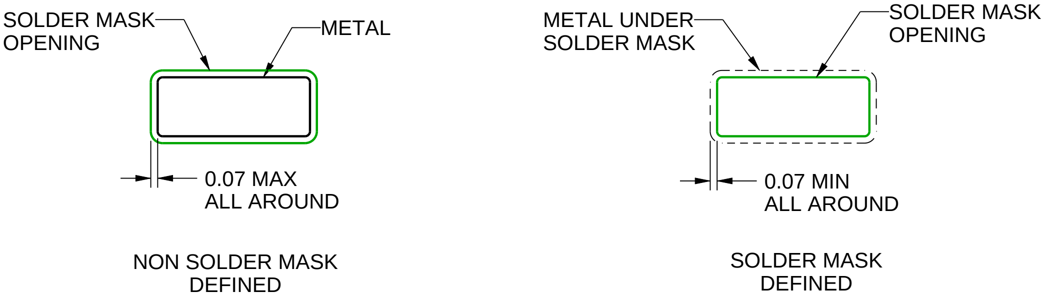
4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

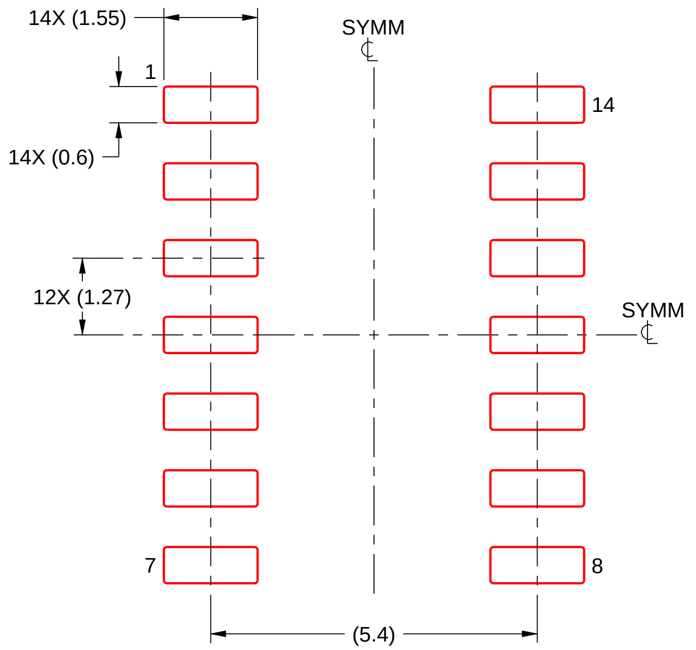


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated