

## TLVx314-Q1 3-MHz, low-power, internal EMI filter, RRIO, operational amplifier

### 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 3A
  - Device CDM ESD Classification Level C6
- Low Offset Voltage: 0.75 mV (Typical)
- Low Input Bias Current: 1 pA (Typical)
- Wide Supply Range: 1.8 V to 5.5 V
- Rail-to-Rail Input and Output
- Gain Bandwidth: 3 MHz
- Low  $I_Q$ : 250  $\mu\text{A}/\text{Ch}$  (Maximum)
- Low Noise: 16 nV/ $\sqrt{\text{Hz}}$  at 1 kHz
- Internal RF and EMI Filter
- Number of Channels:
  - TLV314-Q1: 1
  - TLV2314-Q1: 2
  - TLV4314-Q1: 4
- Extended Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### 2 Applications

- Low-Side Sensing
- Battery Management Systems
- Passive Safety
- Capacitive Sensing
- Fuel Pumps

### 3 Description

The TLVx314-Q1 family of single-, dual-, and quad-channel operational amplifiers represents a new generation of low-power, general-purpose operational amplifiers. Rail-to-rail input and output swings (RRIO), low quiescent current (150  $\mu\text{A}$  typically at 5 V) combine with a wide bandwidth of 3 MHz to make this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. The TLVx314-Q1 family achieves a low-input bias current of 1 pA, making it an excellent choice for high impedance sensors.

The robust design of the TLVx314-Q1 devices provides ease-of-use to the circuit designer: unity-gain stability, RRIO, capacitive loads of up to 300-pF, an integrated RF and EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

These devices are optimized for low-voltage operation as low as 1.8 V ( $\pm 0.9$  V) and up to 5.5 V ( $\pm 2.75$  V), and are specified over the extended industrial temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

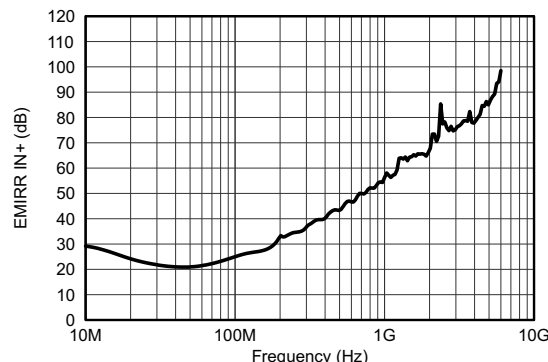
The TLV314-Q1 (single) is available in both 5-pin SC70 and SOT-23 packages. The TLV2314-Q1 (dual) is offered in 8-pin SOIC and VSSOP packages. The quad-channel TLV4314-Q1 is offered in a 14-pin TSSOP package.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV314-Q1	SOT-23 (5)	2.90 mm $\times$ 1.60 mm
	SC70 (5)	2.00 mm $\times$ 1.25 mm
TLV2314-Q1	SOIC (8)	4.90 mm $\times$ 3.91 mm
TLV4314-Q1	TSSOP (14)	5.00 mm $\times$ 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### EMIRR vs Frequency



## Table of Contents

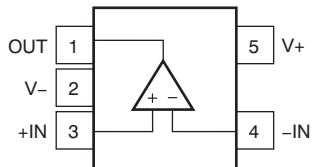
<b>1 Features</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>15</b>
<b>2 Applications</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>16</b>
<b>3 Description</b> .....	<b>1</b>	8.1 Application Information.....	<b>16</b>
<b>4 Revision History</b> .....	<b>2</b>	8.2 Typical Application .....	<b>16</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.3 System Examples .....	<b>17</b>
<b>6 Specifications</b> .....	<b>6</b>	<b>9 Power Supply Recommendations</b> .....	<b>19</b>
6.1 Absolute Maximum Ratings .....	<b>6</b>	9.1 Input and ESD Protection .....	<b>19</b>
6.2 ESD Ratings .....	<b>6</b>	<b>10 Layout</b> .....	<b>20</b>
6.3 Recommended Operating Conditions.....	<b>6</b>	10.1 Layout Guidelines .....	<b>20</b>
6.4 Thermal Information: TLV314-Q1 .....	<b>7</b>	10.2 Layout Example .....	<b>20</b>
6.5 Thermal Information: TLV2314-Q1 .....	<b>7</b>	<b>11 Device and Documentation Support</b> .....	<b>21</b>
6.6 Thermal Information: TLV4314-Q1 .....	<b>7</b>	11.1 Device Support.....	<b>21</b>
6.7 Electrical Characteristics.....	<b>8</b>	11.2 Documentation Support .....	<b>21</b>
6.8 Typical Characteristics.....	<b>9</b>	11.3 Related Links .....	<b>21</b>
6.9 Typical Characteristics.....	<b>10</b>	11.4 Community Resources.....	<b>21</b>
<b>7 Detailed Description</b> .....	<b>13</b>	11.5 Trademarks .....	<b>21</b>
7.1 Overview .....	<b>13</b>	11.6 Electrostatic Discharge Caution.....	<b>21</b>
7.2 Functional Block Diagram .....	<b>13</b>	11.7 Glossary .....	<b>21</b>
7.3 Feature Description.....	<b>14</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>22</b>

## 4 Revision History

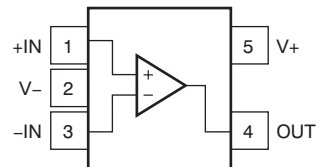
Changes from Original (November 2016) to Revision A	Page
• Deleted TLV2314-Q1 Preview notation in <i>Device Information</i> .....	<b>1</b>
• Deleted VSSOP (8) package from <i>Device Information</i> .....	<b>1</b>
• Deleted VSSOP package information and preview notation for 8-Pin SOIC in <i>Pin Functions</i> .....	<b>4</b>
• Deleted DGK (VSSOP) thermal information .....	<b>7</b>

## 5 Pin Configuration and Functions

**TLV314-Q1 DBV Package  
5-Pin SOT-23  
Top View**



**TLV314-Q1 DCK Package  
5-Pin SC70  
Top View**



**Pin Functions: TLV314-Q1**

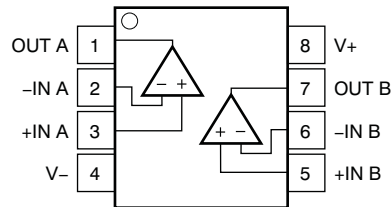
PIN			I/O	DESCRIPTION
NAME	DBV (SOT-23)	DCK (SC70)		
-IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V-	2	2	—	Negative (lowest) supply
V+	5	5	—	Positive (highest) supply

**TLV314-Q1, TLV2314-Q1, TLV4314-Q1**

SBOS837A –NOVEMBER 2016–REVISED JANUARY 2019

[www.ti.com](http://www.ti.com)

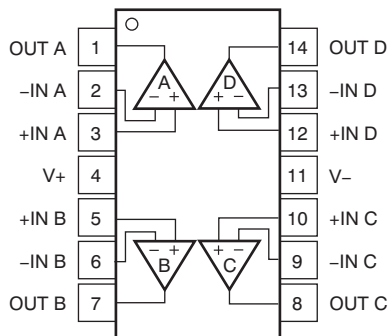
**TLV2314-Q1 D Package  
8-Pin SOIC  
Top View**



**Pin Functions: TLV2314-Q1**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V-	4	—	Negative (lowest) supply
V+	8	—	Positive (highest) supply

**TLV4314-Q1 PW Package  
14-Pin TSSOP  
Top View**



**Pin Functions: TLV4314-Q1**

PIN		I/O	DESCRIPTION
NAME	NO.		
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
-IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
-IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
-IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V-	11	—	Negative (lowest) supply
V+	4	—	Positive (highest) supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage $V_S = (V+) - (V-)$			7	V
Signal input pins	Voltage <sup>(2)</sup>	(V-) – 0.5	(V+) + 0.5	V
	Current <sup>(2)</sup>	–10	10	mA
Output short-circuit <sup>(3)</sup>		Continuous		mA
Temperature	Specified, $T_A$	–40	125	°C
	Junction, $T_J$		150	
	Storage, $T_{stg}$	–65	150	

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
	Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_S$ Supply voltage	Single-supply	1.8		5.5	V
	Dual-supply	±0.9		±2.75	
Specified temperature range		–40		125	°C

## 6.4 Thermal Information: TLV314-Q1

THERMAL METRIC <sup>(1)</sup>		TLV314-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	281.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	99.1	91.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	59.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	7.7	1.5	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	53.8	58.8	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

## 6.5 Thermal Information: TLV2314-Q1

THERMAL METRIC <sup>(1)</sup>		TLV2314-Q1	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	89.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	29.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	78.1	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

## 6.6 Thermal Information: TLV4314-Q1

THERMAL METRIC <sup>(1)</sup>		TLV4314-Q1	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	5.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	62.2	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#) (SPRA953).

## 6.7 Electrical Characteristics

$V_S = 1.8\text{ V to }5.5\text{ V}$ ; at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V <sub>OS</sub>	Input offset voltage	V <sub>CM</sub> = (V <sub>S</sub> +) − 1.3 V, T <sub>A</sub> = 25°C		±0.75	±3	mV
dV <sub>OS</sub> /dT	V <sub>OS</sub> vs temperature	T <sub>A</sub> = −40°C to +125°C		2		μV/°C
PSRR	Power-supply rejection ratio	V <sub>CM</sub> = (V <sub>S</sub> +) − 1.3 V, T <sub>A</sub> = 25°C		±30	±135	μV/V
	Channel separation, dc	At dc, T <sub>A</sub> = 25°C		100		dB
INPUT VOLTAGE RANGE						
V <sub>CM</sub>	Common-mode voltage range	T <sub>A</sub> = 25°C	(V−) − 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V <sub>S</sub> = 5.5 V, (V <sub>S</sub> −) − 0.2 V < V <sub>CM</sub> < (V <sub>S</sub> +) − 1.3 V, T <sub>A</sub> = 25°C	72	96		dB
		V <sub>S</sub> = 5.5 V, V <sub>CM</sub> = −0.2 V to 5.7 V <sup>(2)</sup> , T <sub>A</sub> = 25°C		75		
INPUT BIAS CURRENT						
I <sub>B</sub>	Input bias current	T <sub>A</sub> = 25°C		±1.0		pA
I <sub>OS</sub>	Input offset current	T <sub>A</sub> = 25°C		±1.0		pA
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz, T <sub>A</sub> = 25°C		5		μV <sub>PP</sub>
e <sub>n</sub>	Input voltage noise density	f = 10 kHz, T <sub>A</sub> = 25°C		15		nV/√Hz
		f = 1 kHz, T <sub>A</sub> = 25°C		16		
i <sub>n</sub>	Input current noise density	f = 1 kHz, T <sub>A</sub> = 25°C		6		fA/√Hz
INPUT CAPACITANCE						
C <sub>IN</sub>	Input capacitance	Differential	V <sub>S</sub> = 5 V, T <sub>A</sub> = 25°C		1	pF
		Common-mode	V <sub>S</sub> = 5 V, T <sub>A</sub> = 25°C		5	
OPEN-LOOP GAIN						
A <sub>OL</sub>	Open-loop voltage gain	V <sub>S</sub> = 1.8 V to 5.5 V, 0.2 V < V <sub>O</sub> < (V+) − 0.2 V, R <sub>L</sub> = 10 kΩ, T <sub>A</sub> = 25°C	85	115		dB
		V <sub>S</sub> = 1.8 V to 5.5 V, 0.5 V < V <sub>O</sub> < (V+) − 0.5 V, R <sub>L</sub> = 2 kΩ <sup>(2)</sup> , T <sub>A</sub> = 25°C	85	100		
	Phase margin	V <sub>S</sub> = 5 V, G = 1, R <sub>L</sub> = 10 kΩ, T <sub>A</sub> = 25°C		65		°
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	V <sub>S</sub> = 1.8 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF, T <sub>A</sub> = 25°C		2.7		MHz
		V <sub>S</sub> = 5 V, R <sub>L</sub> = 10 kΩ, C <sub>L</sub> = 10 pF, T <sub>A</sub> = 25°C		3		
SR	Slew rate <sup>(3)</sup>	V <sub>S</sub> = 5 V, G = 1, T <sub>A</sub> = 25°C		1.5		V/μs
t <sub>S</sub>	Settling time	To 0.1%, V <sub>S</sub> = 5 V, 2-V step , G = 1, T <sub>A</sub> = 25°C		3		μs
	Overload recovery time	V <sub>S</sub> = 5 V, V <sub>IN</sub> × gain > V <sub>S</sub> , T <sub>A</sub> = 25°C		8		μs
THD+N	Total harmonic distortion + noise <sup>(4)</sup>	V <sub>S</sub> = 5 V, V <sub>O</sub> = 1 V <sub>RMS</sub> , G = 1, f = 1 kHz, R <sub>L</sub> = 10 kΩ, T <sub>A</sub> = 25°C		0.005%		
OUTPUT						
V <sub>O</sub>	Voltage output swing from supply rails	V <sub>S</sub> = 1.8 V to 5.5 V, R <sub>L</sub> = 10 kΩ, T <sub>A</sub> = 25°C		5	25	mV
		V <sub>S</sub> = 1.8 V to 5.5 V, R <sub>L</sub> = 2 kΩ, T <sub>A</sub> = 25°C		22	45	
I <sub>SC</sub>	Short-circuit current	V <sub>S</sub> = 5 V, T <sub>A</sub> = 25°C		±20		mA
R <sub>O</sub>	Open-loop output impedance	V <sub>S</sub> = 5.5 V, f = 100 Hz, T <sub>A</sub> = 25°C		570		Ω
POWER SUPPLY						
V <sub>S</sub>	Specified voltage range		1.8		5.5	V
I <sub>Q</sub>	Quiescent current per amplifier, over temperature	V <sub>S</sub> = 5 V, I <sub>O</sub> = 0 mA, T <sub>A</sub> = −40°C to +125°C		150	250	μA
TEMPERATURE						
	Specified range		−40		125	°C
T <sub>stg</sub>	Storage range		−65		150	°C

(1) Parameters with minimum or maximum specification limits are 100% production tested at  $25^\circ\text{C}$ , unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.

(2) Specified by design and characterization; not production tested.

(3) Signifies the slower value of the positive or negative slew rate.

(4) Third-order filter; bandwidth = 80 kHz at -3 dB.



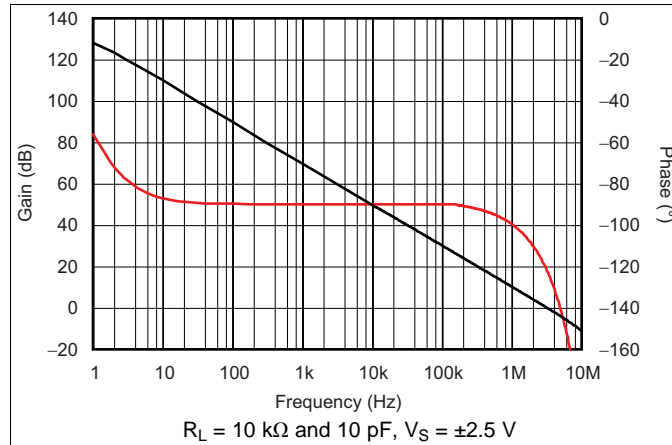
## 6.8 Typical Characteristics

**Table 1. Table of Graphs**

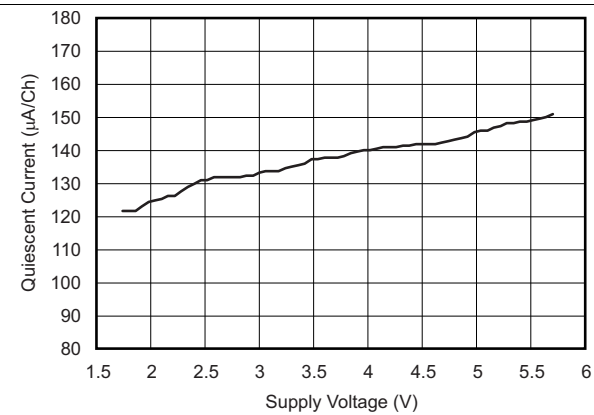
TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	<a href="#">Figure 1</a>
Quiescent Current vs Supply Voltage	<a href="#">Figure 2</a>
Offset Voltage Production Distribution	<a href="#">Figure 3</a>
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	<a href="#">Figure 4</a>
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	<a href="#">Figure 5</a>
Input Bias and Offset Current vs Temperature	<a href="#">Figure 6</a>
Output Voltage Swing vs Output Current (Overtemperature)	<a href="#">Figure 7</a>
Small-Signal Overshoot vs Load Capacitance	<a href="#">Figure 8</a>
Small-Signal Step Response, Noninverting (1.8 V)	<a href="#">Figure 9</a>
Large-Signal Step Response, Noninverting (1.8 V)	<a href="#">Figure 10</a>
No Phase Reversal	<a href="#">Figure 11</a>
Channel Separation vs Frequency (Dual)	<a href="#">Figure 12</a>
EMIRR	<a href="#">Figure 13</a>

## 6.9 Typical Characteristics

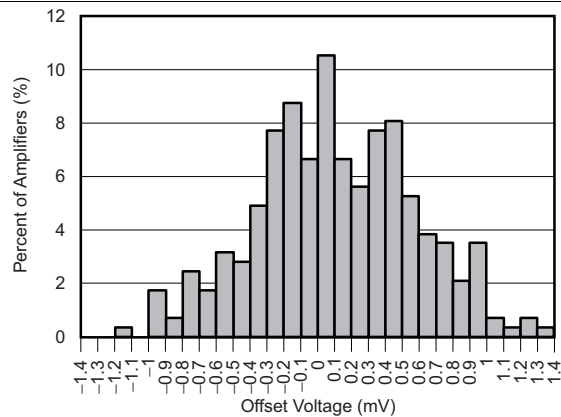
at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



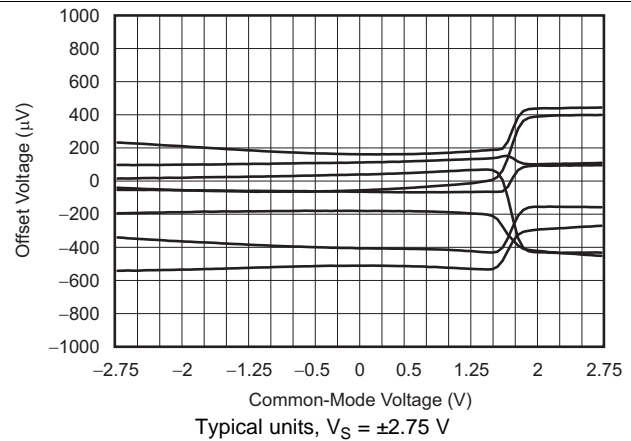
**Figure 1. Open-Loop Gain and Phase vs Frequency**



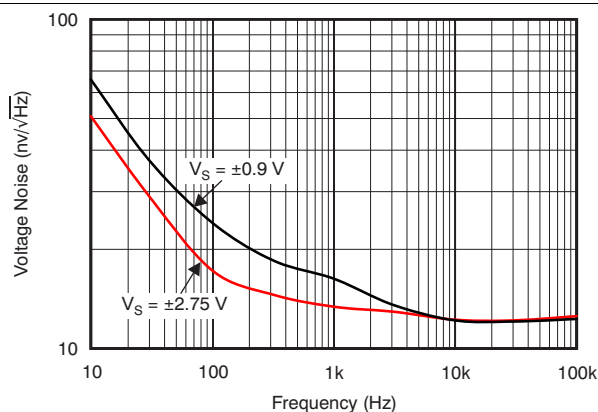
**Figure 2. Quiescent Current vs Supply**



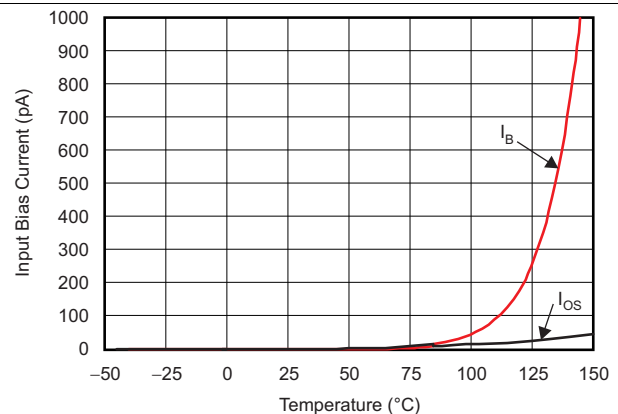
**Figure 3. Offset Voltage Production Distribution**



**Figure 4. Offset Voltage vs Common-Mode Voltage**



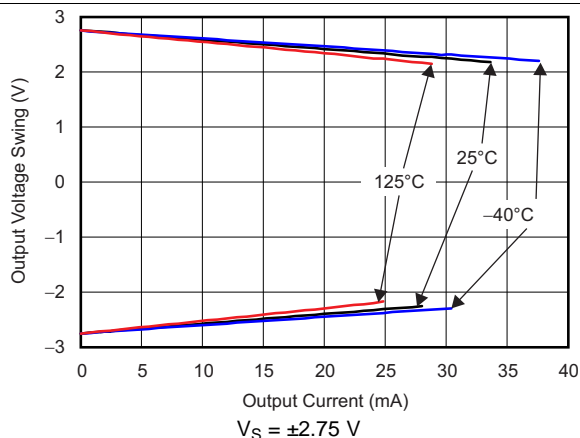
**Figure 5. Input Voltage Noise Spectral Density vs Frequency**



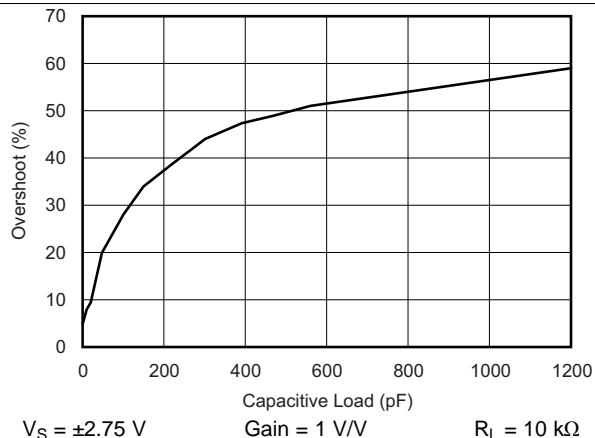
**Figure 6. Input Bias and Offset Current vs Temperature**

## Typical Characteristics (continued)

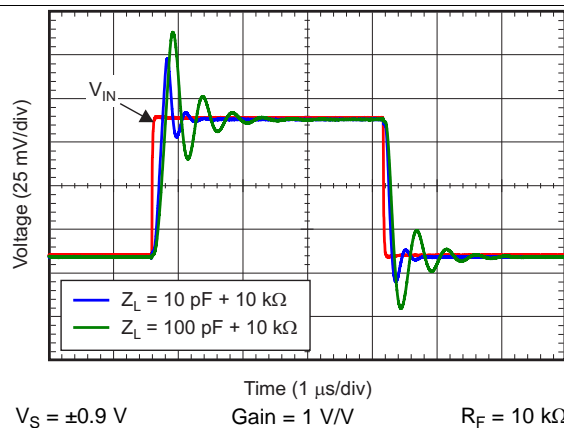
at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



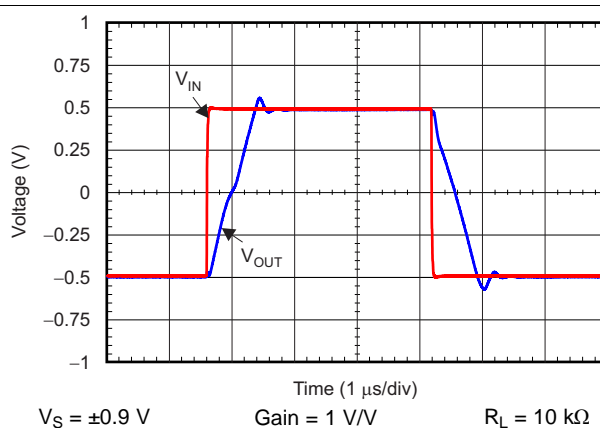
**Figure 7. Output Voltage Swing vs Output Current (Overtemperature)**



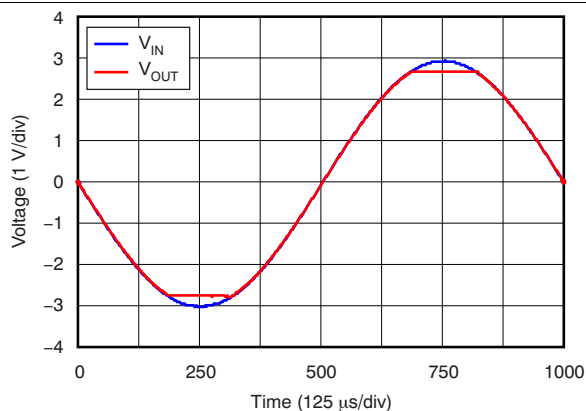
**Figure 8. Small-Signal Overshoot vs Load Capacitance**



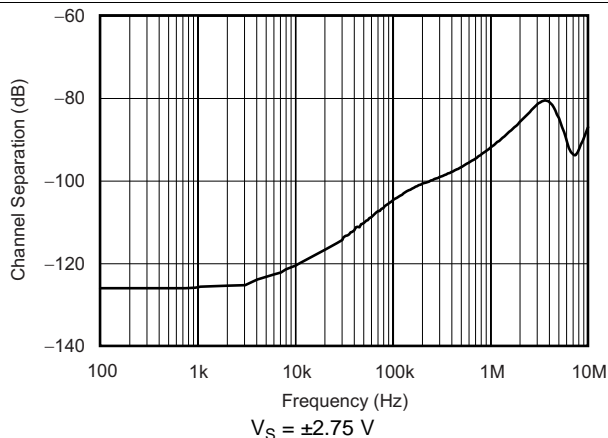
**Figure 9. Small-Signal Pulse Response (Noninverting)**



**Figure 10. Large-Signal Pulse Response (Noninverting)**



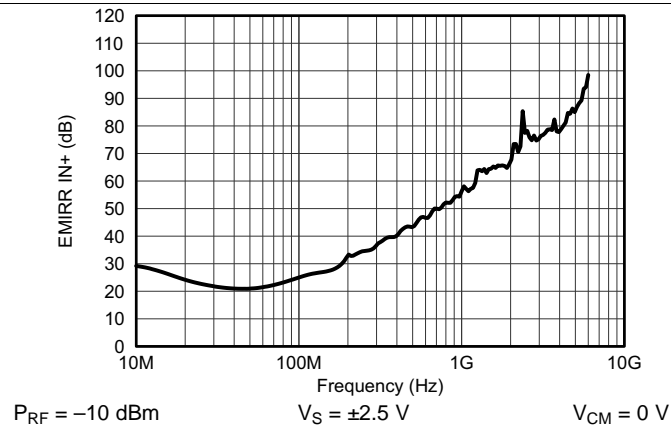
**Figure 11. No Phase Reversal**



**Figure 12. Channel Separation vs Frequency (TLV2314)**

## Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



**Figure 13. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR IN+) vs Frequency**

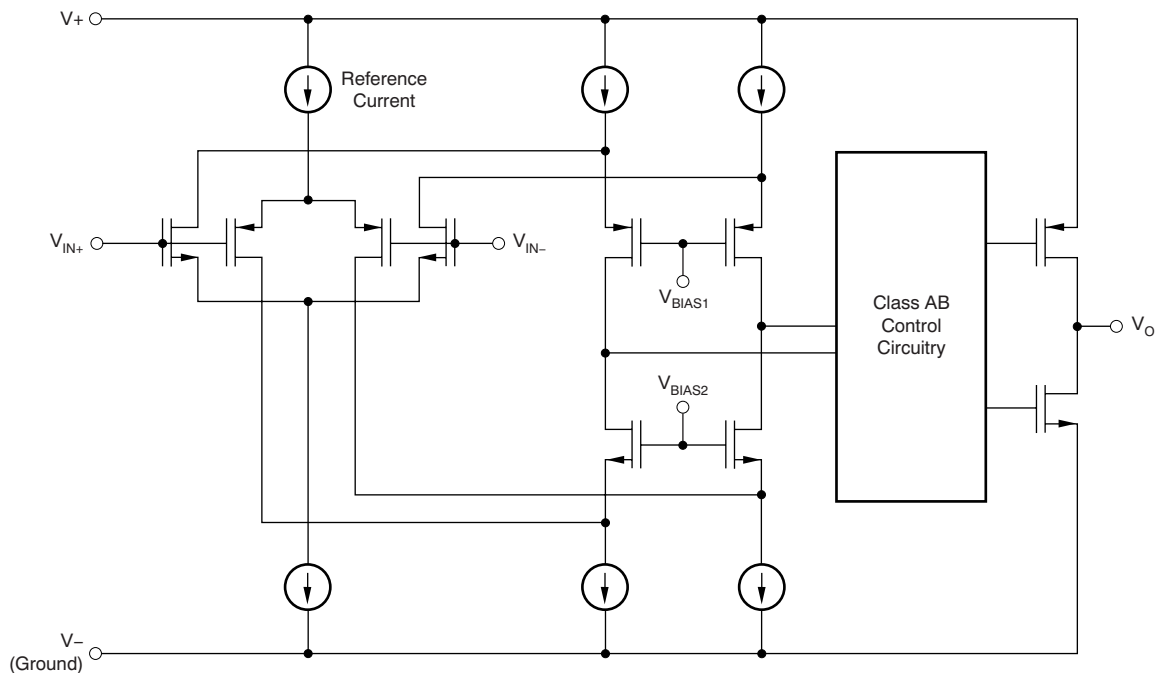
## 7 Detailed Description

### 7.1 Overview

The TLVx314-Q1 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving  $\leq 10\text{-k}\Omega$  loads connected to any point between  $V_+$  and ground. The input common-mode voltage range includes both rails, and allows the TLVx314-Q1 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx314-Q1 family features 3-MHz bandwidth and  $1.5\text{-V}/\mu\text{s}$  slew rate with only  $150\text{-}\mu\text{A}$  supply current per channel, providing good ac performance at very-low-power consumption. DC applications are also well served with a very low input noise voltage of  $14\text{ nV} / \sqrt{\text{Hz}}$  at 1 kHz, low input bias current ( $0.2\text{-pA}$ ), and a typical input offset voltage of  $0.5\text{ mV}$ .

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Operating Voltage

The TLVx314-Q1 series of operational amplifiers is fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are provided in the [Typical Characteristics](#) section. Bypass power-supply pins with 0.01- $\mu\text{F}$  ceramic capacitors.

### 7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLVx314-Q1 extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [Functional Block Diagram](#). The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.3\text{ V}$  to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately  $(V+) - 1.3\text{ V}$ . There is a small transition region, typically  $(V+) - 1.4\text{ V}$  to  $(V+) - 1.2\text{ V}$ , in which both pairs are on. This 200-mV transition region may vary up to 300 mV with process variation. Thus, the transition region (with both stages on) ranges from  $(V+) - 1.7\text{ V}$  to  $(V+) - 1.5\text{ V}$  on the low end, up to  $(V+) - 1.1\text{ V}$  to  $(V+) - 0.9\text{ V}$  on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

### 7.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLVx314-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads up to 10-k $\Omega$ , the output typically swings to within 5 mV of either supply rail regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails, as shown in [Figure 7](#).

### 7.3.4 Common-Mode Rejection Ratio (CMRR)

The CMRR for the TLVx314-Q1 is specified in several ways so the best match for a given application can be used; see the [Electrical Characteristics](#) table. First, the CMRR of the device in the common-mode range below the transition region [ $V_{\text{CM}} < (V+) - 1.3\text{ V}$ ] is given. This specification is the best indicator of the capability of the device when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at  $(V_{\text{CM}} = -0.2\text{ V to } 5.7\text{ V})$ . This last value includes the variations measured through the transition region, as shown in [Figure 4](#).

## Feature Description (continued)

### 7.3.5 Capacitive Load and Stability

The TLVx314-Q1 is designed for applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLVx314-Q1 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLVx314-Q1 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors ( $C_L$  capacitors with a value greater than 1  $\mu$ F) is sufficient to alter the phase characteristics in the feedback loop so the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains, as shown in Figure 8.

Inserting a small resistor (typically 10- $\Omega$  to 20- $\Omega$ ) can increase the capacitive load drive of the amplifier in a unity-gain configuration, as shown in Figure 14. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

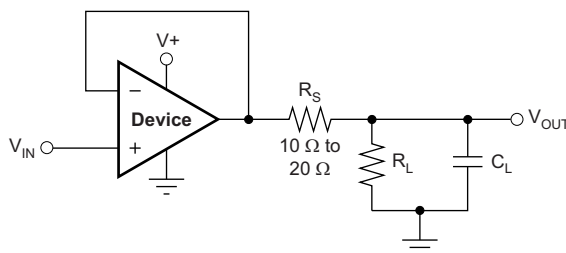


Figure 14. Improving Capacitive Load Drive

### 7.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from the nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although EMI can affect all operational amplifier pin functions, the signal input pins are likely to be the most susceptible. The TLVx314-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. The filter provides common-mode and differential mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared to the EMI immunity. Figure 13 illustrates the testing results on the TLVx314-Q1. For more detailed information, see *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from [www.ti.com](http://www.ti.com).

## 7.4 Device Functional Modes

The TLVx314-Q1 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V ( $\pm 0.9$  V) and 5.5 V ( $\pm 2.75$  V).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

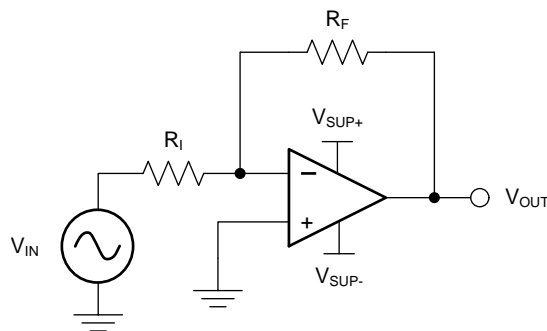
### 8.1 Application Information

The TLVx314-Q1 device is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving  $\leq 10\text{-k}\Omega$  loads connected to any point between  $V_+$  and ground. The input common-mode voltage range includes both rails, and allows the TLVx314-Q1 family to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device suitable for driving sampling analog-to-digital converters (ADCs).

The TLVx314-Q1 features a 3-MHz bandwidth and 1.5-V/ $\mu\text{s}$  slew rate with only 150- $\mu\text{A}$  supply current per channel, providing good ac performance at very-low-power consumption. DC applications are also well served with a very-low input noise voltage of 14 nV/ $\sqrt{\text{Hz}}$  at 1 kHz, low-input bias current (0.2 pA), and a typical input offset voltage of 0.5 mV.

### 8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 15. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor ( $R_I$ ) and the feedback resistor ( $R_F$ ).



**Figure 15. Application Schematic**

#### 8.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range ( $V_{CM}$ ) and the output voltage swing to the rails ( $V_O$ ) must also be considered. For instance, this application scales a signal of  $\pm 0.5\text{ V}$  (1 V) to  $\pm 1.8\text{ V}$  (3.6 V). Setting the supply at  $\pm 2.5\text{ V}$  is sufficient to accommodate this application.

#### 8.2.2 Detailed Design Procedure

Calculate the gain required by the inverting amplifier using Equation 1 and Equation 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

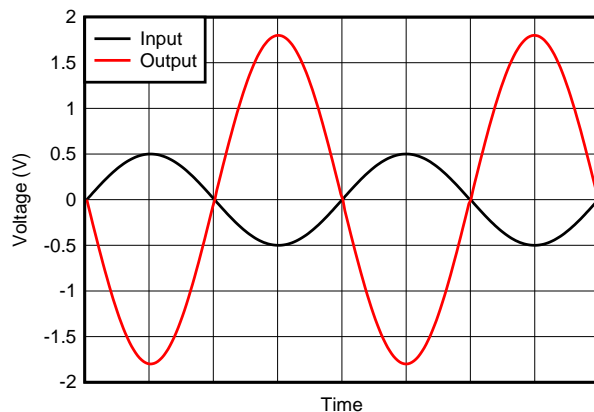


## Typical Application (continued)

When the desired gain is determined, select a value for  $R_I$  or  $R_F$ . Selecting a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (hundreds of kilohms) draw the smallest current, but generate the highest noise. Very small resistors (hundreds of ohms) generate low noise but draw high current. This example uses 10 k $\Omega$  for  $R_I$ , and  $R_F$  uses 36 k $\Omega$ . These values are calculated using [Equation 3](#):

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

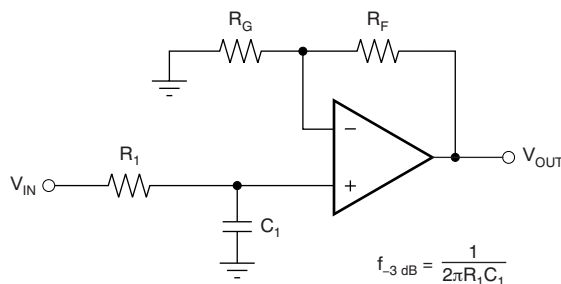
### 8.2.3 Application Curve



**Figure 16. Inverting Amplifier Input and Output**

## 8.3 System Examples

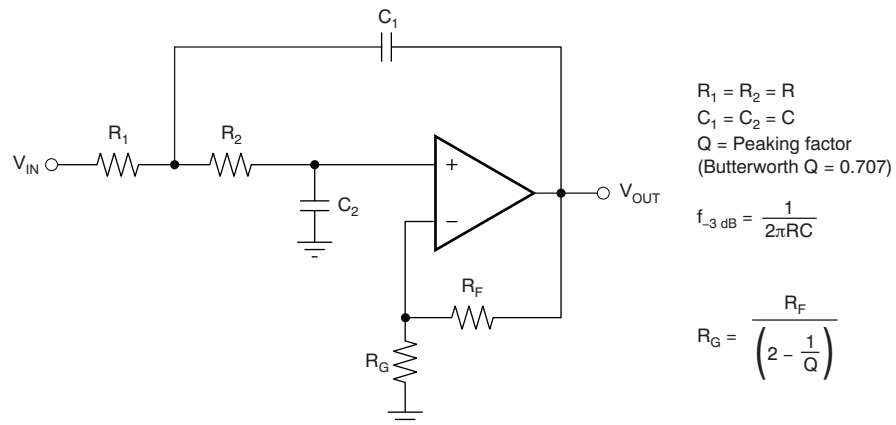
When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as [Figure 17](#) shows.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_I C_1}\right)$$

**Figure 17. Single-Pole, Low-Pass Filter**

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as [Figure 18](#) shows. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

**System Examples (continued)**

**Figure 18. Two-Pole, Low-Pass, Sallen-Key Filter**

## 9 Power Supply Recommendations

The TLVx314-Q1 family is specified for operation from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . [Typical Characteristics](#) presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

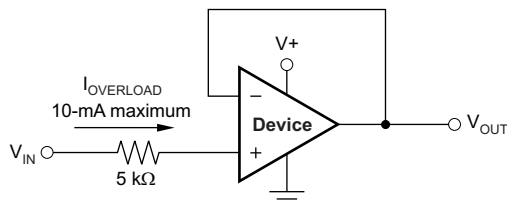
### CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#) table).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see [Layout Guidelines](#).

### 9.1 Input and ESD Protection

The TLVx314-Q1 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as stated in the [Absolute Maximum Ratings](#) table. [Figure 19](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input, which must be kept to a minimum in noise-sensitive applications.



**Figure 19. Input Current Protection**

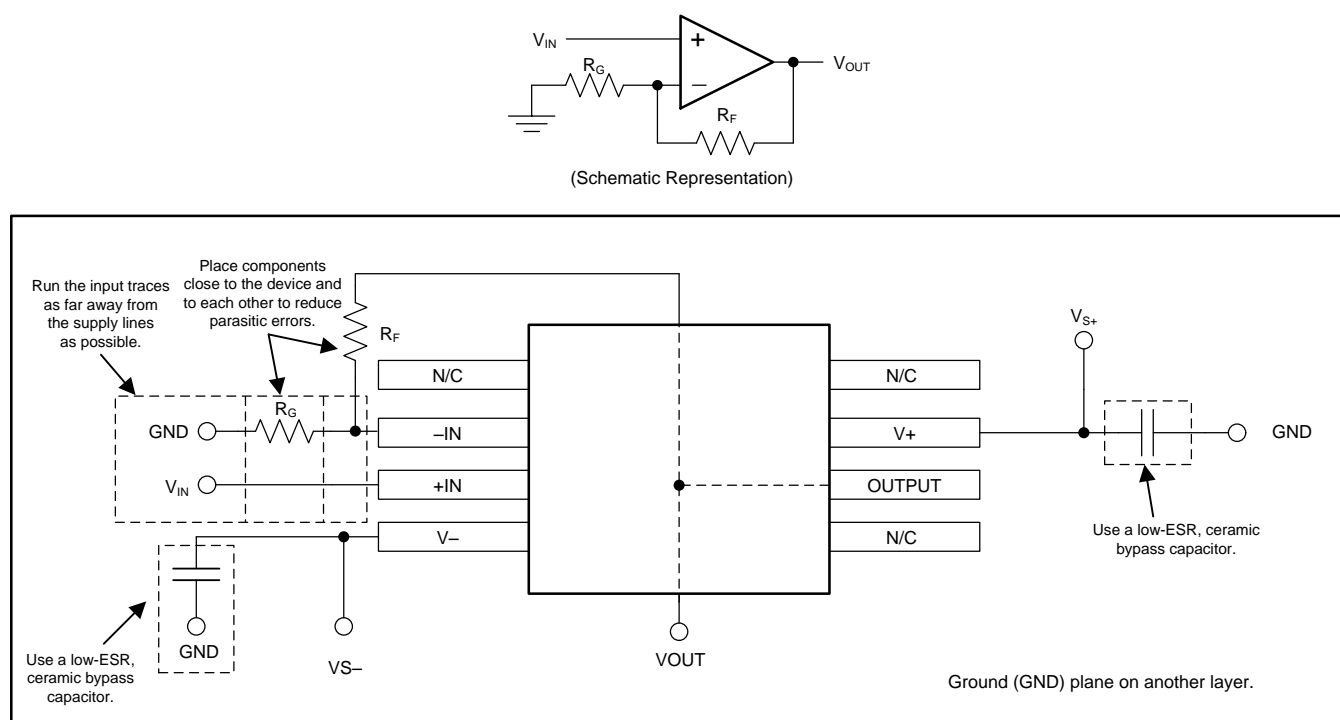
## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from  $V_+$  to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#) (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep  $R_F$  and  $R_G$  close to the inverting input in order to minimize parasitic capacitance, as shown in [Figure 20](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 10.2 Layout Example



**Figure 20. Operational Amplifier Board Layout for Noninverting Configuration**

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- [EMI Rejection Ratio of Operational Amplifiers](#) (SBOA128).
- [Circuit Board Layout Techniques](#) (SLOA089).
- [QFN/SON PCB Attachment](#) (SLUA271).
- [Quad Flatpack No-Lead Logic Packages](#) (SCBA017).

### 11.3 Related Links

[Table 2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV314-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV2314-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TLV4314-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2314QDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2314Q
TLV2314QDRQ1.B	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2314Q
<a href="#">TLV314QDBVRQ1</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	16SD
TLV314QDBVRQ1.B	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	16SD
<a href="#">TLV314QDBVTQ1</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	16SD
TLV314QDBVTQ1.B	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	16SD
<a href="#">TLV4314QPWRQ1</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V4314Q1
TLV4314QPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V4314Q1

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV2314-Q1, TLV314-Q1, TLV4314-Q1 :**

- Catalog : [TLV2314](#), [TLV314](#), [TLV4314](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2314QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV314QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV314QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV314QDBVTQ1	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV4314QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2314QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TLV314QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV314QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV314QDBVTQ1	SOT-23	DBV	5	250	210.0	185.0	35.0
TLV4314QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0



## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

## SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220202/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



**DBV0005A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2025, Texas Instruments Incorporated