TLV3901 125ps High-Speed RRI Comparator With CML Output

1 Features

- Low propagation delay: 125ps
- Low overdrive dispersion: 5ps
- Quiescent current: 53mA
- High toggle frequency: 10GHz / 20Gbps
- Narrow pulse width detection capability: 60ps
- CML output
- Separate input and output supplies
- Single supply voltage: 3.1V to 5.25V
- Low input offset voltage: ±1mV
- On-chip terminations at both input pins
- Resistor programmable hysteresis
- Differential latch control

2 Applications

- Distance sensing in LIDAR
- Time-of-Flight sensors
- High speed trigger function in oscilloscope and logic analyzer
- High speed differential line receiver
- Drone vision

3 Description

The TLV3901 is a 125ps high speed comparator with a wide power supply range and a high toggle frequency of 10GHz. Along with an operating supply voltage range of 3.1V to 5.25V, the TLV3901 comes in an industry-standard small packages, making this comparator well suited for Time-of-Flight (ToF) applications such as LIDAR, differential line receivers, and test and measurement systems.

The TLV3901 has a strong input overdrive performance of 5ps and narrow pulse width capabilities of just 60ps. In addition to excellent performance specifications, the TLV3901 offers optional 50Ω on-chip termination resistors at both inputs along with latching function and programmable hysteresis features.

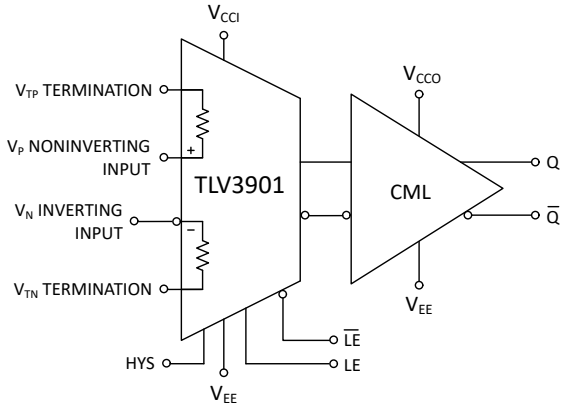
The Current-Mode-Logic (CML) output of the TLV3901 helps increase data throughput and optimizes power consumption. Likewise, the complementary outputs help to reduce EMI by suppressing common mode noise on each output. The CML output is designed to drive and interface directly with other devices that accept a standard CML input, such as most FPGAs and CPUs downstream in an application.

The TLV3901 is available in a 16-pin WQFN package which is desirable for space sensitive applications such as an optical sensor module.

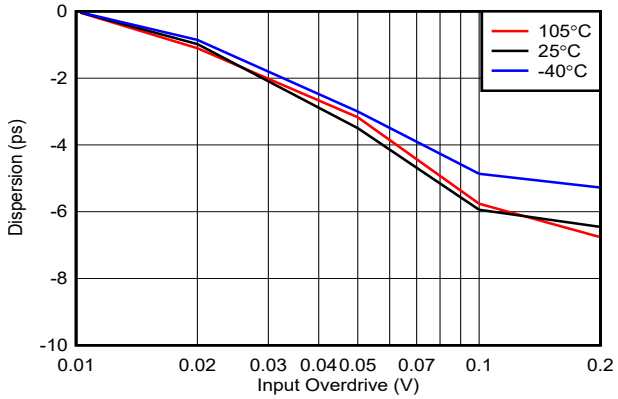
Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TLV3901	RTE (WQFN, 16)	3.00mm × 3.00mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



Dispersion vs. Overdrive

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4 Pin Configuration and Functions

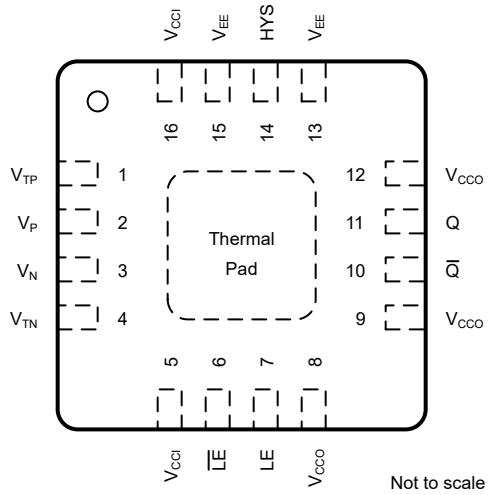


Figure 4-1. RTE Package
16-Pad WQFN With Exposed Thermal Pad
Top View

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	TLV3901		
V_{TP}	1	-	Termination Resistor Return Pin for V_P
V_P	2	I	Noninverting Analog Input
V_N	3	I	Inverting Analog Input
V_{TN}	4	-	Termination Resistor Return Pin For V_N Input
V_{CCI}	5, 16	-	Positive Supply Voltage for Input Stage
$\overline{LE}$	6	I	Latch Enable Pin, Inverting Side
LE	7	I	Latch Enable Input Pin
V_{CCO}	8	-	Termination Return Pin LE/$\overline{LE}$ Input Pins
V_{CCO}	9, 12	-	Positive Supply Voltage for CML Output Stage
$\overline{Q}$	10	O	Inverting Output
Q	11	O	Noninverting Output
V_{EE}	13, 15	-	Negative power supply (If using single supply, connect to GND)
HYS	14	I	Hysteresis Control Pin
Thermal PAD	-	-	Connect directly to VEE

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input supply voltage $V_S = V_{CCI} - V_{EE}$	–0.3	5.5	V
Output supply voltage $V_S = V_{CCO} - V_{EE}$	–0.3	5.5	V
Difference from V_{CCI} to V_{CCO}	–0.2	2.4	V
Differential input voltage, VID	–2.5	+2.5	V
Input pins (IN+, IN–) from (V-)(2)	V_{EE} – 0.3	V_{CCI} + 0.3	V
Current into input pins (IN+, IN-)(2) (3)	–10	10	mA
V_P to V_{TP}, V_N to V_{TN} pins	–1.25	1.25	V
LE/$\overline{LE}$ to V_{CCO}		1.5	V
Output current	–20	+20	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode clamped to V_{EE} and V_{CC}
(3) When V_{TP} and V_{TN} pins are left floating

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Input supply voltage $V_{CCI} - V_{EE}$	3.1	5.25	V
Output supply voltage $V_{CCO} - V_{EE}$	3.1	5.25	V
Difference from V_{CCI} to V_{CCO}	–0.2	2.15	V
Input voltage range	V_{EE} – 0.2	V_{CCI} + 0.2	V
Differential Input voltage range	–1.5	1.5	V
Ambient temperature, T_A	–40	105	°C
Junction temperature, T_J	–40	125	°C

5.4 Thermal Information

THERMAL METRIC (1)		TLV3901 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	35.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	19.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

V_S = 3.3V to 5V, V_{CM} = V_S / 2; at T_A = 25°C (unless otherwise noted).
Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input Offset Voltage	V_S = 5V, V_{CM} = V_S / 2		±1	±4	mV
V_{IO}	Input Offset Voltage	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 105℃			±5	mV
dV_{OS}/dT	Input Offset Voltage Drift	V_{CM} = V_S / 2, T_A = -40 to 105℃		±10		µV/°C
V_{CM}	Common-mode voltage range		V_{EE} – 0.1		V_{CCI} + 0.1	V
I_B	Input bias current	V_S = 5V, V_{CM} = V_S / 2	–10	–5		µA
I_B	Input bias current	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 105℃	–15			µA
I_{OS}	Input offset current	V_S = 5V, V_{CM} = V_S / 2		±1		µA
C_{IN}	Input capacitance			2		pF
R_{DM}	Input differential mode resistance			1		MΩ
R_{CM}	Input common mode resistance			5		MΩ
CMRR	Common-mode rejection ratio	V_{CM} = V_{EE} – 0.1V to V_{CCI} + 0.1V		76		dB
DC Output Characteristics						
V_{OH}	Output Voltage Swing High Level from V_{CCO}	50Ω terminate to V_{CCO}	100	50	0	mV
V_{OL}	Output Voltage Swing Low Level from V_{CCO}	50Ω terminate to V_{CCO}	575	425	275	mV
V_{ODIFF}	Output Voltage Differential	50Ω terminate to V_{CCO}	275	375	475	mV
Power Supply						
I_{CC}	Supply current / Channel(1)	V_S = 3.3V and 5V, no load		53		mA
I_{CC}	Supply current / Channel(1)	V_S = 3.3V and 5V, no load, T_A = -40 to 105℃			65	mA
PSRR	Power Supply Rejection Ratio	V_S = 3.3V to 5V, no load, T_A = -40 to 105℃		74		dB

(1) Does not include I_{TT}

5.6 Switching Characteristics

For V_S = 5V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low	Midpoint of input to midpoint of output, V_{OD} = 50mV		125		ps
dt_{PHL}/dT	Propagation delay time, high to-low, vs temperature	Midpoint of input to midpoint of output, V_{OD} = 50mV, -40 to 105C		0.08		ps/°C
t_{PLH}	Propagation delay time, low-to high	Midpoint of input to midpoint of output, V_{OD} = 50mV		125		ps
dt_{PLH}/dT	Propagation delay time, low-to high, vs temperature	Midpoint of input to midpoint of output, V_{OD} = 50mV, -40 to 105C		0.08		ps/°C
t_{PD} skew	Skew between t_{PLH} and t_{PHL}	V_{CM} = V_{CCI} /2, V_{OD} = V_{UD} = 50mV, 5MHz Squarewave		7		ps

For V_S = 5V, V_{CM} = V_S / 2 at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 20mV to 100mV, 600mV Vpp		5		ps
$t_{OD\_DISPERSION}$	Overdrive dispersion	Overdrive varied from 10mV to 200mV, 600mV Vpp		7		ps
R_{Jitter}	Random Jitter (RMS)	V_{OD} = V_{UD} = 200mV, 5V/ns, 1.25GHz		2		ps
D_{Jitter}	Deterministic Jitter	V_{OD} = V_{UD} = 200mV, 5V/ns, 1.25GHz		15		ps
Min_Pulse	Minimum allowed input pulse width	$V_{OVERDRIVE}$ = $V_{UNDERDRIVE}$ = 50mV PW_{OUT} = 90% of PW_{IN}		60		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200mV_{PP} Sine Wave, 50% Output swing		10		GHz
TR	Toggle Rate	V_{IN} = 200mV_{PP} Sine Wave, 50% Output swing		20		Gbps
t_R	Rise time	Measured from 20% to 80%		40		ps
t_F	Fall time	Measured from 20% to 80%		40		ps
t_{ON}	Power-up time	During power on, (V+) must exceed 2V for 3µs before the output reflects the input.		3		µs

5.7 Latching/Adjustable Hysteresis

V_S = 3.3V to 5V, V_{CM} = V_S / 2; at T_A = 25°C (unless otherwise noted).
Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Latching/Adjustable Hysteresis						
V_{HYST}	Input hysteresis voltage	V_S = 5V, R_{HYST} ≧ 4kΩ		1		mV
V_{HYST}	Input hysteresis voltage	V_S = 5V, R_{HYST} = 0.8kΩ		16.5		mV
V_{HYST}	Input hysteresis voltage	V_S = 5V, R_{HYST} = 0kΩ		47.5		mV
V_{LE}	LE pin input voltage range	V_{CCI} = V_{CCO} = 3.1V and 5.25V T_A = –40°C to +105°C	V_{CCO} - 1		V_{CCO}	V
V_{LE_DIFF}	LE pin input differential	V_{CCI} = V_{CCO} = 3.1V and 5.25V T_A = –40°C to +105°C	0.2		1	V
t_{SETUP}	Latch setup time			55		ps
t_{HOLD}	Latch hold time			12		ps
t_{PL}	Latch to output delay			155		ps
t_{PW}	Latch minimum pulse width			60		ps

5.8 Timing Diagrams

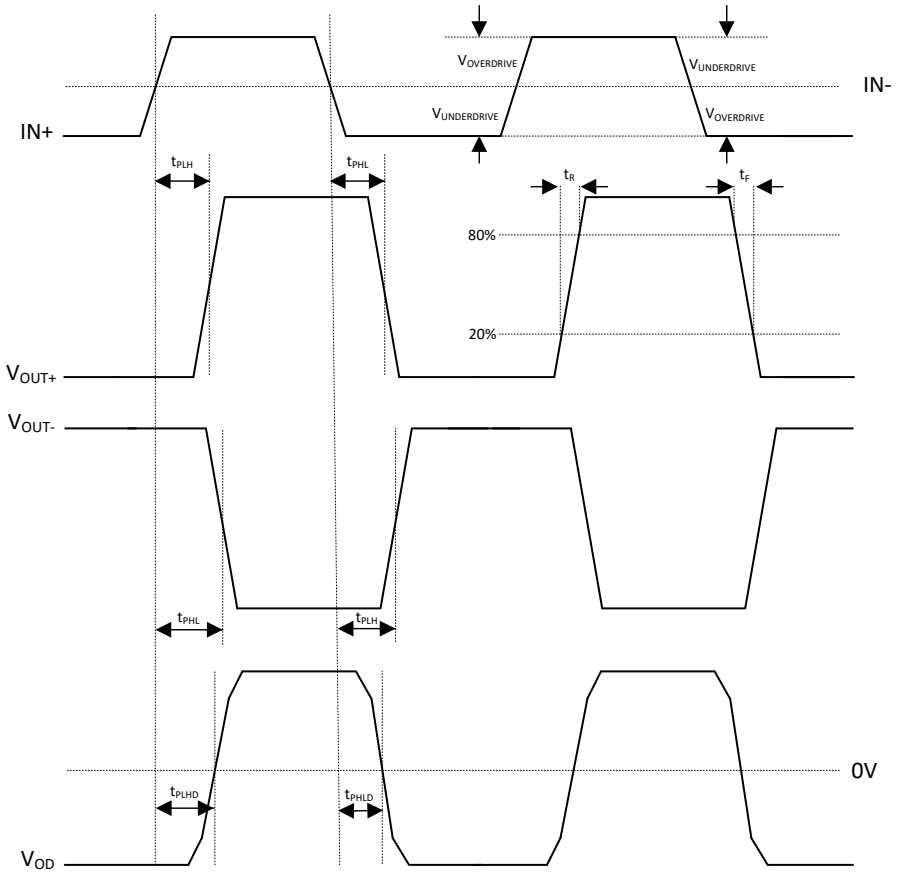


Figure 5-1. General Timing Diagram

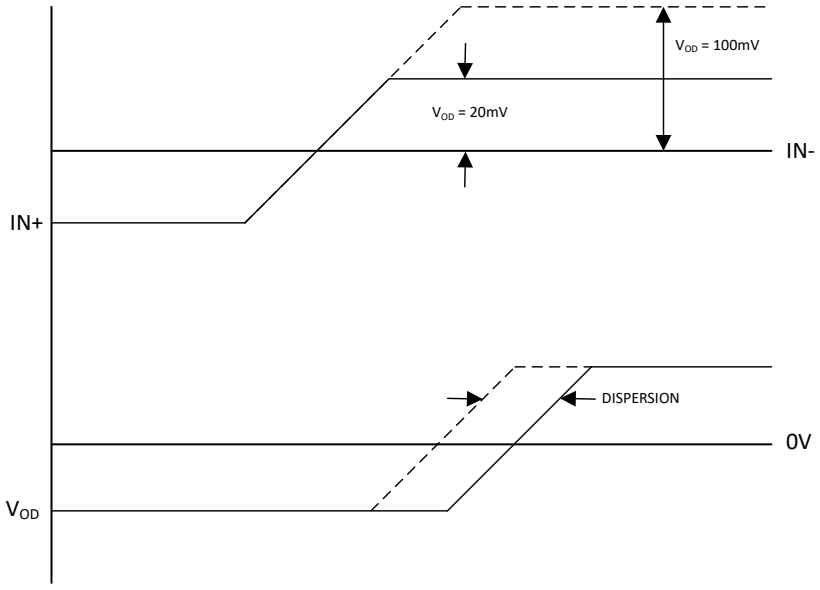


Figure 5-2. Overdrive Dispersion

5.9 Typical Characteristics

At T_A = 25°C, V_{CCI} = V_{CCO} = 3.3V to 5V while V_{EE} = GND = 0, V_{CM} = 0.5 × V_{CCI}, R_{HYS} = 4000Ω, and input overdrive/underdrive = 50mV, unless otherwise noted.

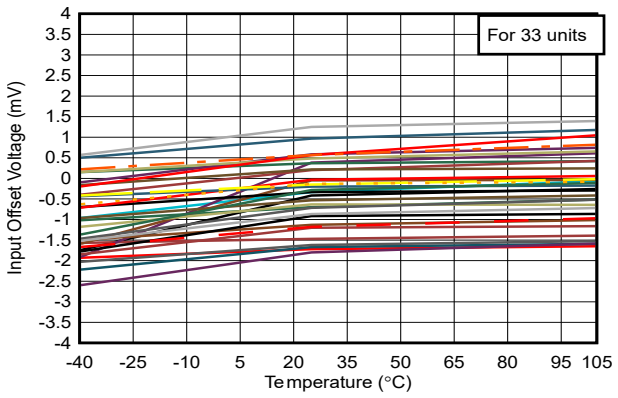


Figure 5-3. Offset vs. Temperature at 3.3V

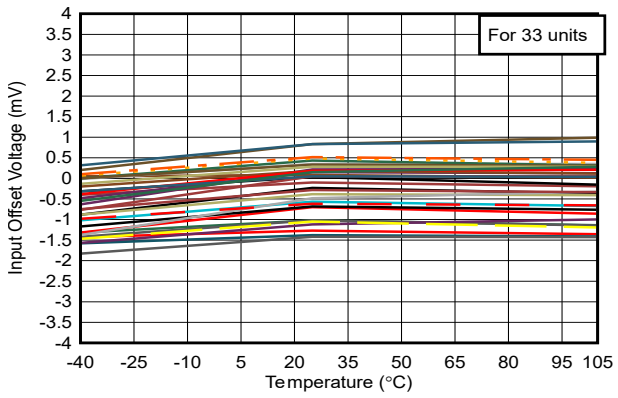


Figure 5-4. Offset vs. Temperature at 5V

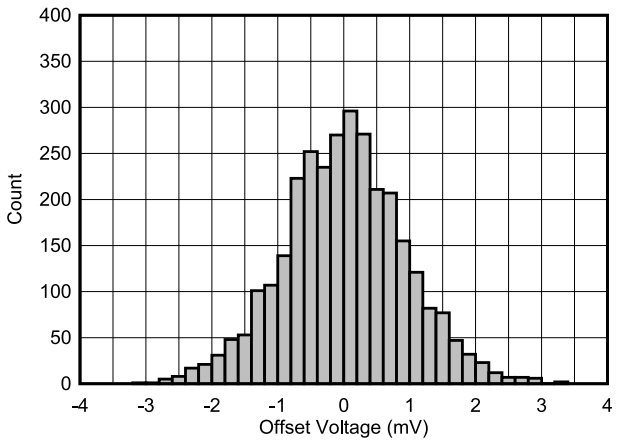


Figure 5-5. Offset Histogram at 3.3V

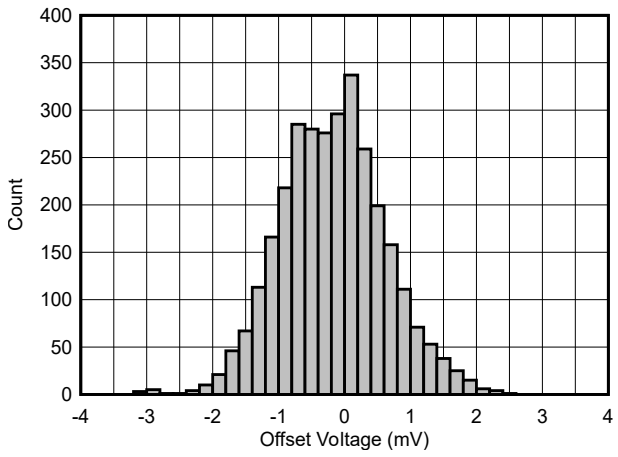


Figure 5-6. Offset Histogram at 5V

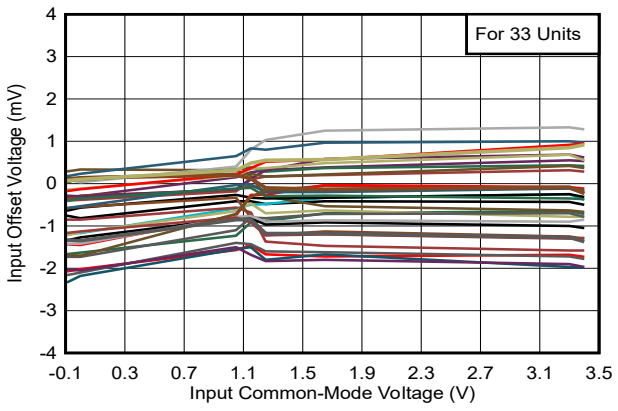


Figure 5-7. Offset vs. Common-Mode at 3.3V

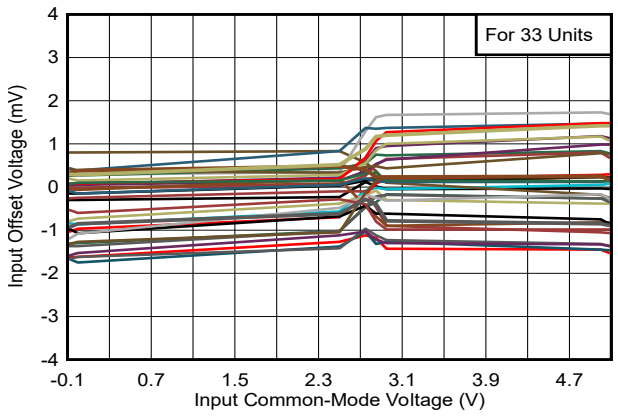


Figure 5-8. Offset vs. Common-Mode at 5V

5.9 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} = V_{CCO} = 3.3V to 5V while V_{EE} = GND = 0, V_{CM} = 0.5 × V_{CCI}, R_{HYS} = 4000Ω, and input overdrive/underdrive = 50mV, unless otherwise noted.

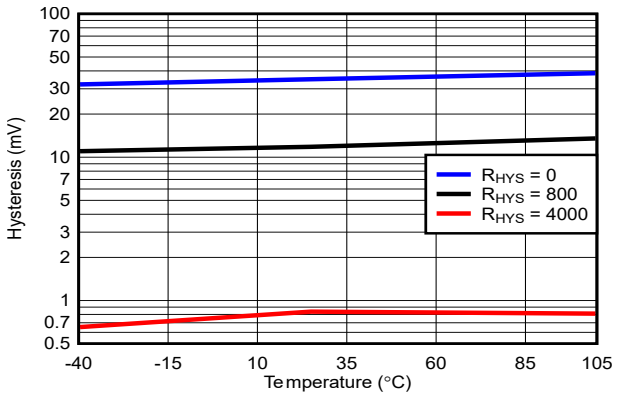


Figure 5-9. Hysteresis vs. Temperature at 3.3V

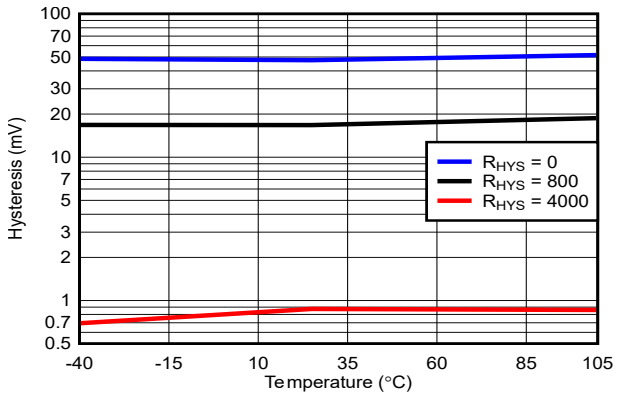


Figure 5-10. Hysteresis vs. Temperature at 5V

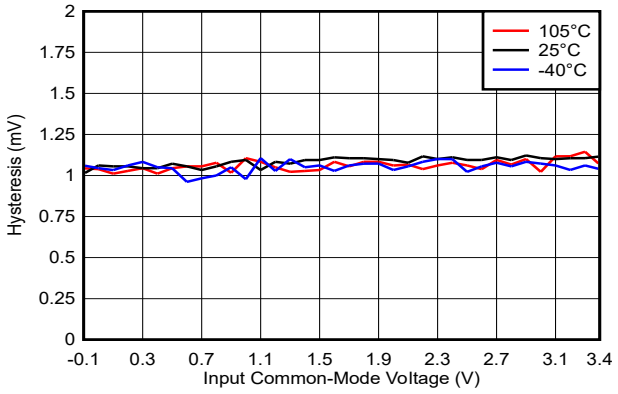


Figure 5-11. Hysteresis vs. VCM at 3.3V with RHYS = 4000

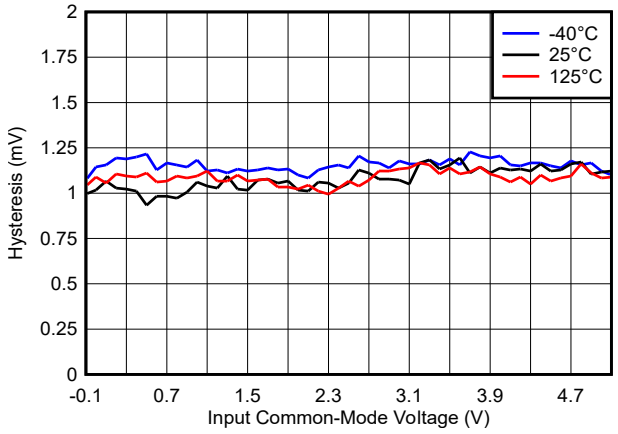


Figure 5-12. Hysteresis vs. VCM at 5V with RHYS = 4000

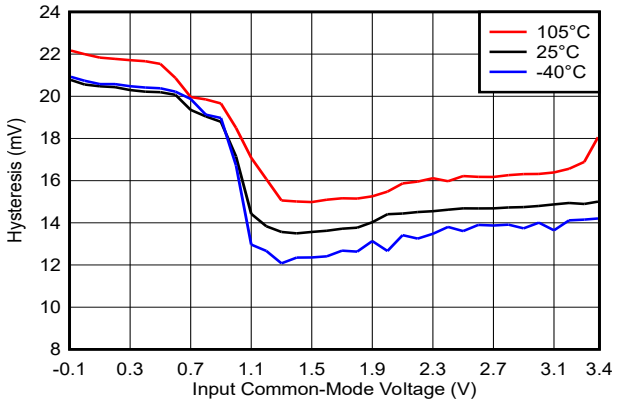


Figure 5-13. Hysteresis vs. VCM at 3.3V with RHYS = 800

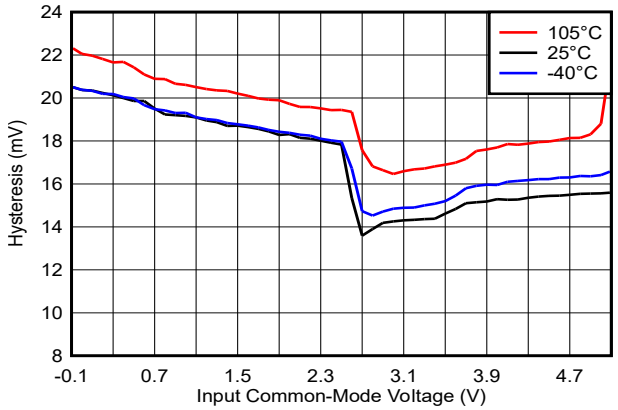


Figure 5-14. Hysteresis vs. VCM at 5V with RHYS = 800

5.9 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} = V_{CCO} = 3.3V to 5V while V_{EE} = GND = 0, V_{CM} = 0.5 × V_{CCI}, R_{HYS} = 4000Ω, and input overdrive/underdrive = 50mV, unless otherwise noted.

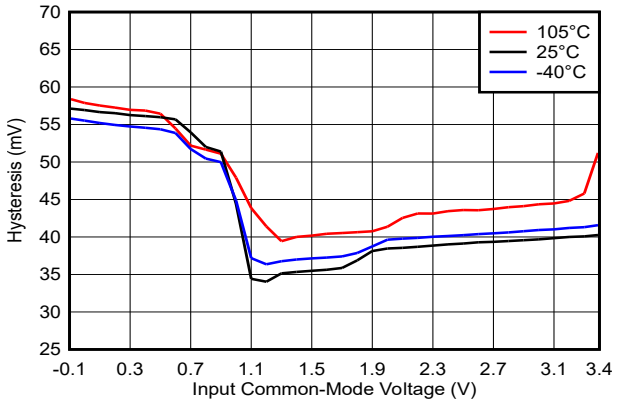


Figure 5-15. Hysteresis vs. VCM at 3.3V with RHYS = 0

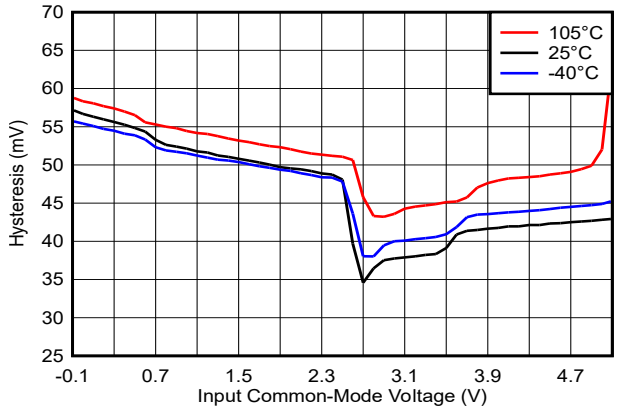


Figure 5-16. Hysteresis vs. VCM at 5V with RHYS = 0

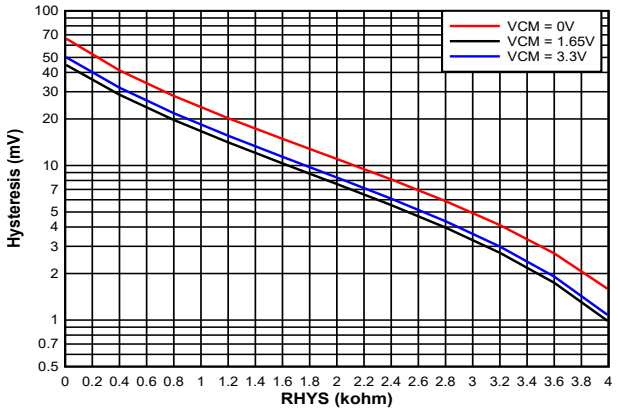


Figure 5-17. Hysteresis vs. RHYS at 3.3V

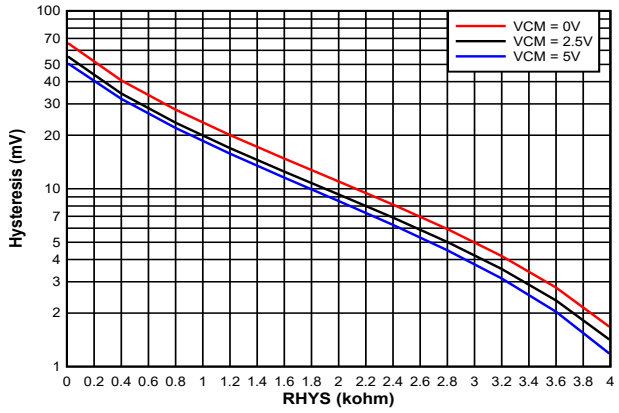


Figure 5-18. Hysteresis vs. RHYS at 5V

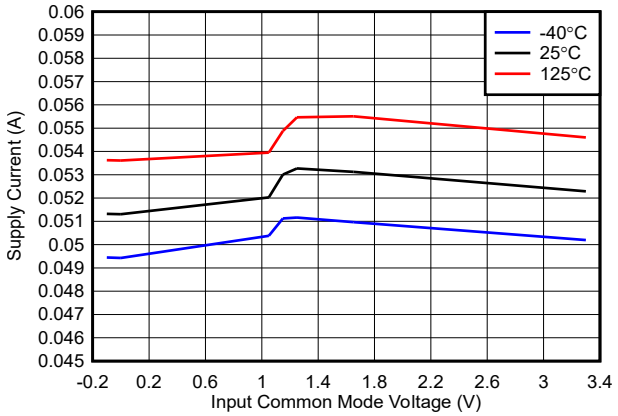


Figure 5-19. Supply Current vs. Common-Mode, Output High at 3.3V

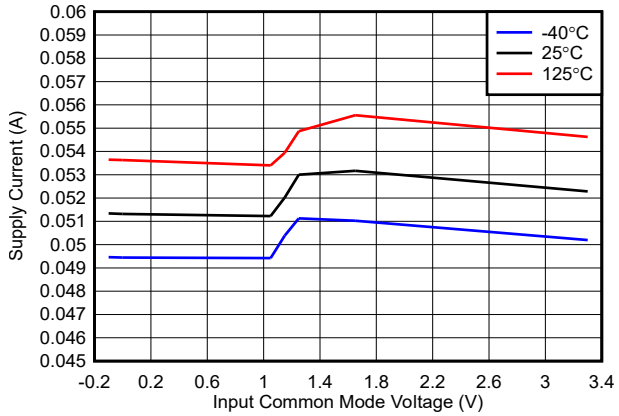


Figure 5-20. Supply Current vs. Common-Mode, Output Low at 3.3V

5.9 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} = V_{CCO} = 3.3V to 5V while V_{EE} = GND = 0, V_{CM} = 0.5 × V_{CCI}, R_{HYS} = 4000Ω, and input overdrive/underdrive = 50mV, unless otherwise noted.

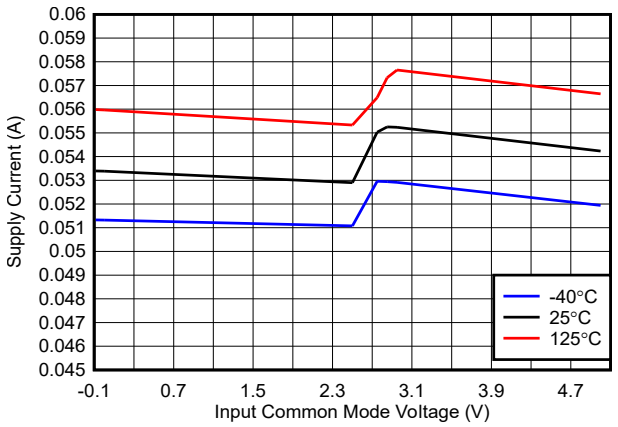


Figure 5-21. Supply Current vs. Common-Mode, Output High at 5V

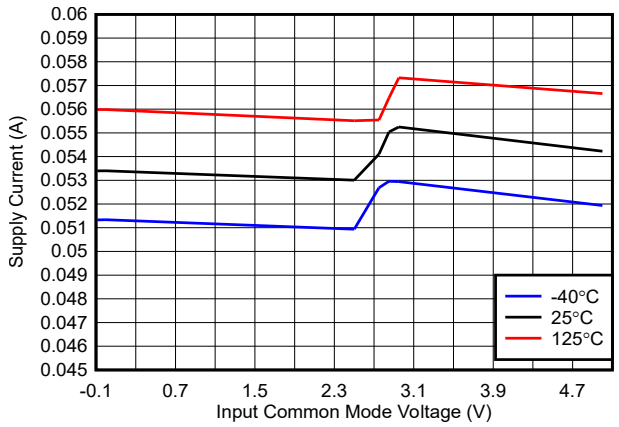


Figure 5-22. Supply Current vs. Common-Mode, Output Low at 5V

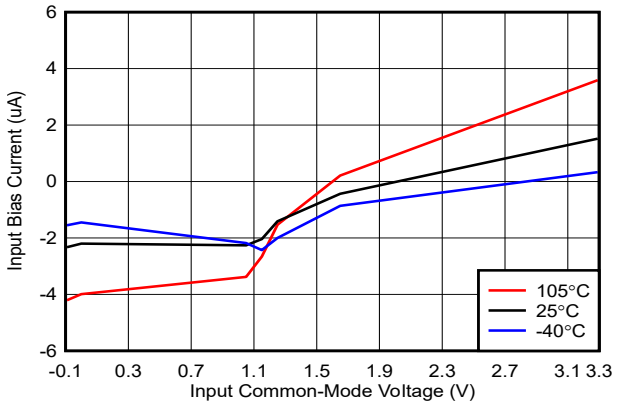


Figure 5-23. Bias Current vs. Common-Mode at 3.3V

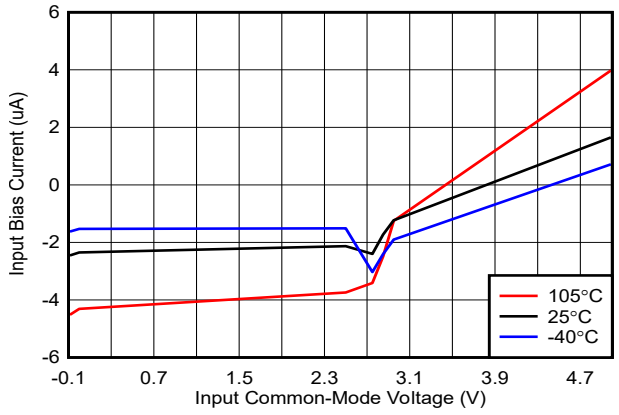


Figure 5-24. Bias Current vs. Common-Mode at 5V

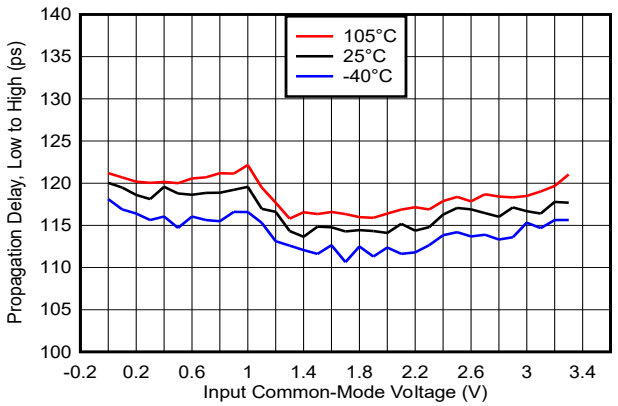


Figure 5-25. Propagation Delay vs. Common-Mode at 3.3V

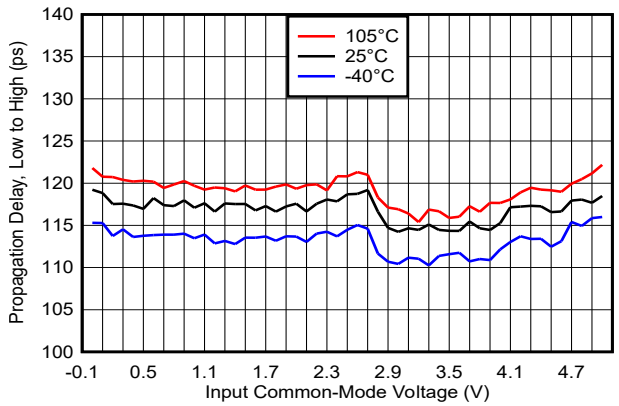


Figure 5-26. Propagation Delay vs. Common-Mode at 5V

5.9 Typical Characteristics (continued)

At T_A = 25°C, V_{CCI} = V_{CCO} = 3.3V to 5V while V_{EE} = GND = 0, V_{CM} = 0.5 × V_{CCI}, R_{HYS} = 4000Ω, and input overdrive/underdrive = 50mV, unless otherwise noted.

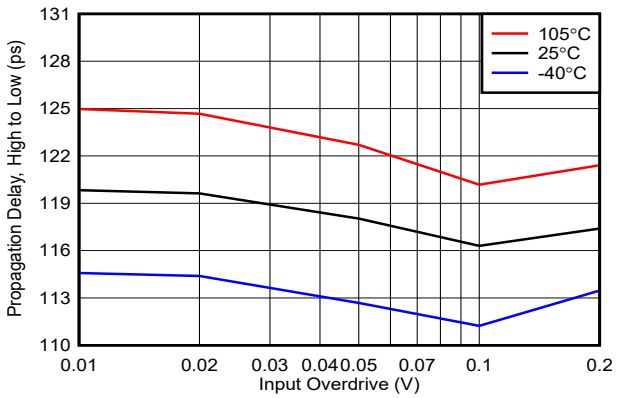


Figure 5-27. Propagation Delay High-to-Low vs. Overdrive at 3.3V

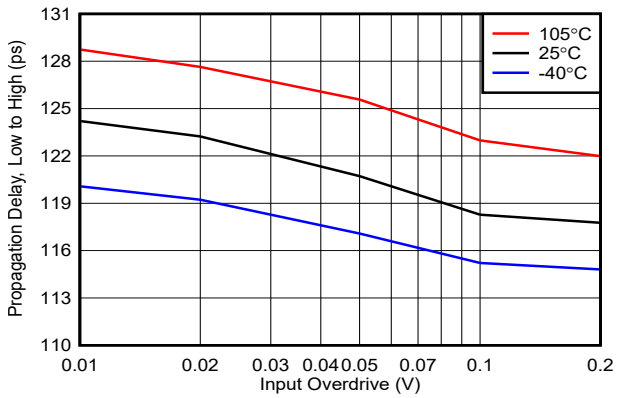


Figure 5-28. Propagation Delay Low-to-High vs. Overdrive at 3.3V

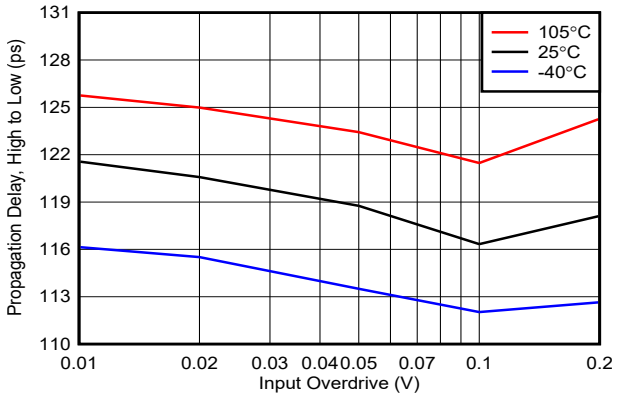


Figure 5-29. Propagation Delay High-to-Low vs. Overdrive, 5V

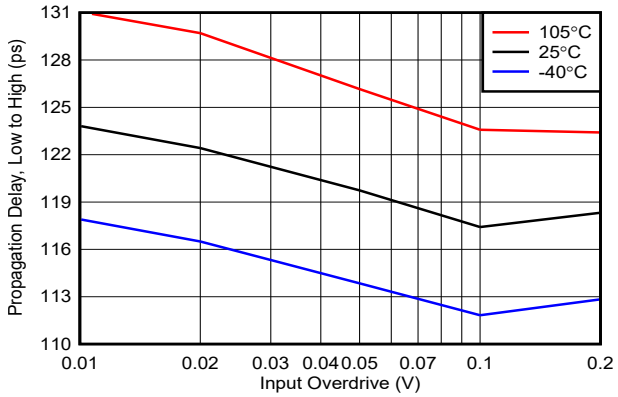


Figure 5-30. Propagation Delay Low-to-High vs. Overdrive, 5V

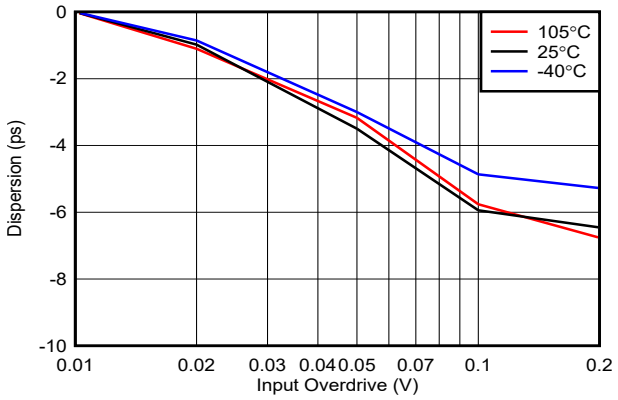


Figure 5-31. Dispersion vs. Overdrive, 3.3V

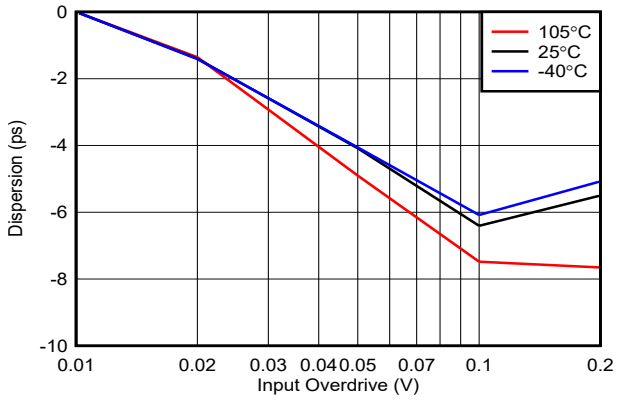


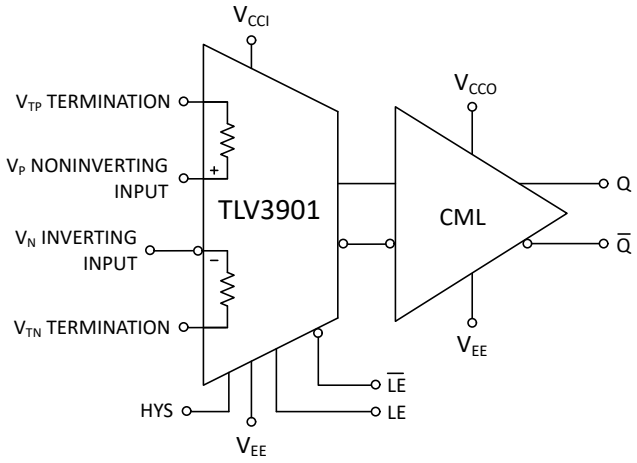
Figure 5-32. Dispersion vs. Overdrive, 5V

6 Detailed Description

6.1 Overview

The TLV3901 is a high-speed comparator with CML output. The fast response time makes the comparator well suited for applications that require narrow pulse width detection or high toggle frequencies. The TLV3901 is available in a 16-pin WQFN package.

6.2 Functional Block Diagram



6.3 Feature Description

The TLV3901 comparator features a typical propagation delay of 125ps and CML outputs. The minimum pulse width detection capability is 60ps and the typical toggle frequency is 10GHz (20Gbps). The TLV3901 has two separate power rails for the input and output blocks. This allows the input to be referenced from either single or split supplies (VCCI and VEE), while the output is referenced from VCCO and VEE.

6.4 Device Functional Modes

The TLV3901 can be operated from a single power supply or from split (bipolar) supplies and has two features that alter the function of the comparator. The first is the latch function and the other is adjustable hysteresis.

6.4.1 Inputs

The TLV3901 features a differential input stage capable of operating 0.1V below VEE to 0.1V above VCCI, making the comparator fully rail-to-rail on the input. Integrated at the inputs is a protection circuit that includes two pairs of front-to-back diodes between VP and VN as well as two 25Ω resistors, as shown in Figure 6-1. By limiting the input differential voltage to less than 1.5V, damage to the input differential input pair is prevented.

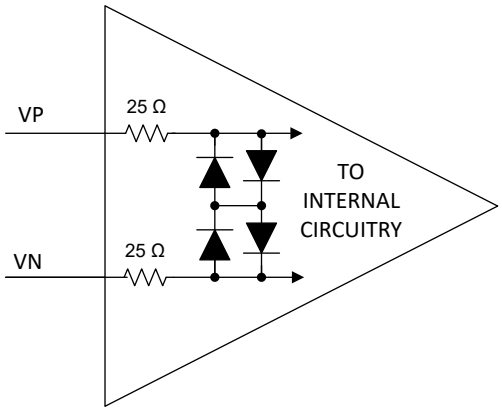


Figure 6-1. Input Protection Circuitry

Bipolar technology comparators, like TLV3901, feature higher bias currents than CMOS comparators, often in the low µA range instead of pAs. In the Electrical Characteristic table, IBIAS is specified at mid-supply over temperature where the differential input signal is close to 0V (VP = VN). Since IBIAS also varies over input common mode voltage, IBIAS versus input common mode data is available in the Typical Performance plots. When operating with the VN and VP pins apart, IBIAS shifts primarily to either the VP pin when VP >> VN or to the VN pin when VN >> VP. This results from one half of the input differential pair being turned fully ON while the other is fully OFF, causing the tail current that biases the input differential pair to be unevenly shared.

In addition to the input protection circuitry, the TLV3901 features optional, internal 50Ω termination resistors (see image below). When VP and VN are driven by a 50Ω source, connect the Termination Resistor Return Pins (VTP and VTN) to system ground or the common mode voltage of the upstream device. However, when not driven by a 50Ω source, no termination resistor is required and VTP or VTN are left unconnected (floating). Likewise, when the TLV3901 is used as a CML repeater, VTP and VTN are connected to the VCCO of the upstream device (note that VCCO must be less than VCCI of the TLV3901).

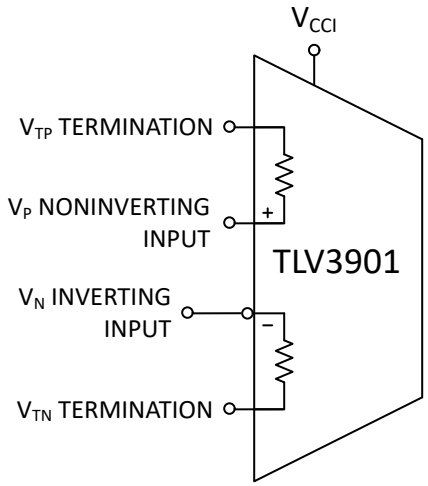


Figure 6-2. Input Termination Resistors

6.4.2 CML Output

The TLV3901 outputs are CML compliant. Each comparator output is terminated with a 50Ω resistor to the output supply voltage (VCCO), generating a 375mV swing from VCCO. The fully differential nature of the CML outputs enables fast digital toggling and reduces EMI compared to single-ended output standards.

6.4.3 Latch Functionality

TLV3901 features an integrated latch function for holding the CML outputs in a fixed state. CML input pins Latch Enable (LE) and Latch Enable Bar (LEB) control the latch functionality and the pins are internally terminated with 50Ω to VCCO. When LE is high (VCCO) and LEB is low (VCCO-1), the comparator output is latched.

An important consideration of the latch functionality is the latch hold time. Latch hold time is the minimum time after latch mode is asserted for properly latching the comparator output. Likewise, latch setup time is defined as the time that the input must be stable before the latch mode is asserted. The figure below illustrates when LE and LEB can transition for a valid latch.

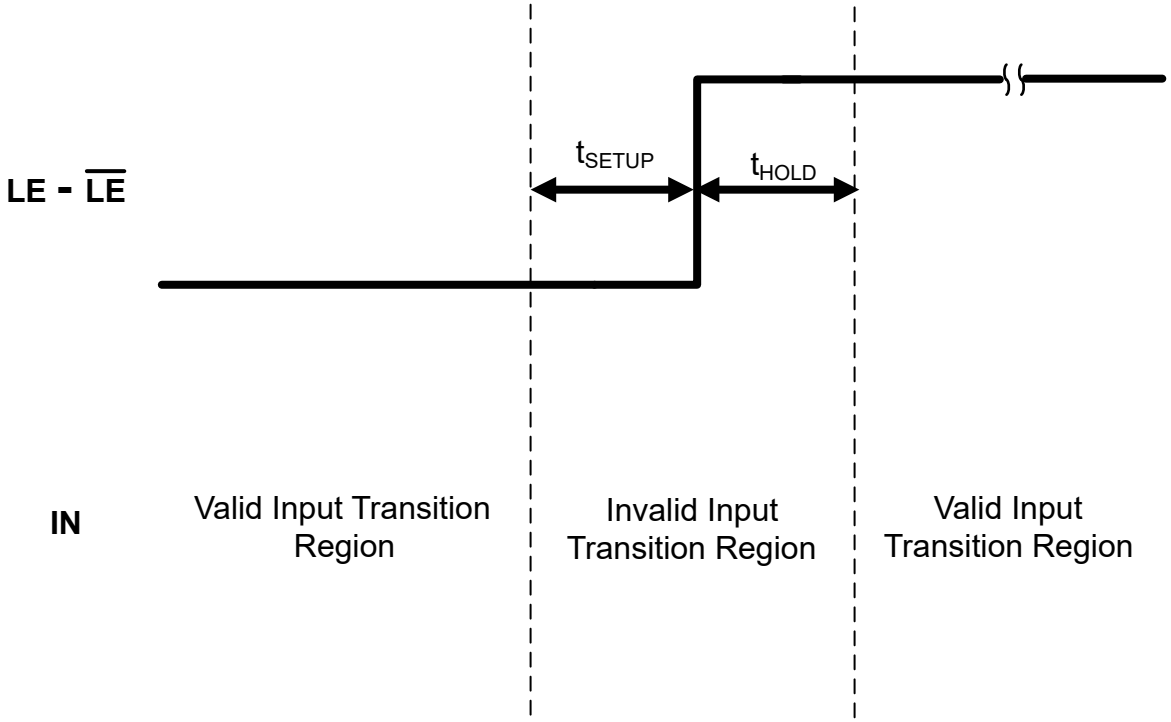


Figure 6-3. Valid Latch Diagram

A small delay (tPL) in the output response is shown below when the TLV3901 exits a latched output state.

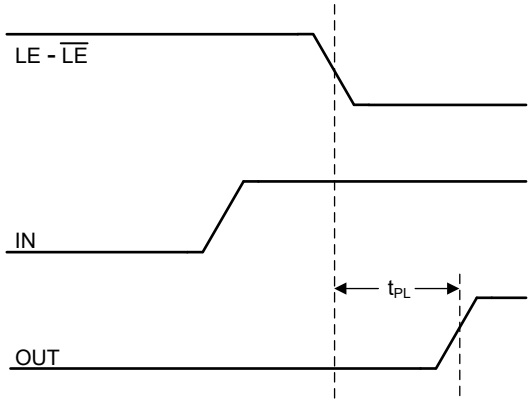


Figure 6-4. Latch Disable with Input Change

Latch mode is disabled by connecting LE to a voltage that is a minimum of 200mV below VCCO, while LEB is left unconnected (floating). Note that the acceptable range for either LE or LEB is VCCO to VCCO - 1V with a minimum difference voltage of 200mV.

6.4.4 Adjustable Hysteresis

As a result of a comparator's high open loop gain, there is a small band of input differential voltage where the output can toggle back and forth between "logic high" and "logic low" states. This can cause design challenges for inputs with slow rise and fall times or systems with excessive noise. These challenges can be overcome by adding hysteresis to the comparator.

The TLV3901 features a hysteresis control pin (HYS) that is used to increase the internal hysteresis of the comparator. To change the internal hysteresis of the TLV3901, connect a single resistor as shown in the Figure 6-5 between the HYS pin and VEE. Curves of hysteresis versus resistance at VCCI of 3.3V and 5V

provide guidance in setting the desired amount of hysteresis. Drive the HYS pin directly with a Digital-to-Analog Converter if the system requires the hysteresis to be fine tuned or vary during the application.

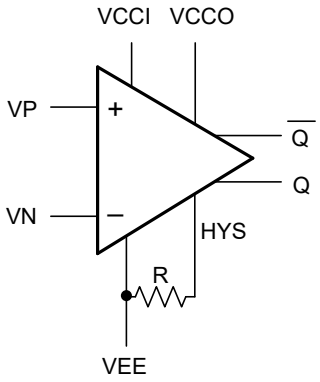


Figure 6-5. Adjusting Hysteresis with an External Resistor (R)

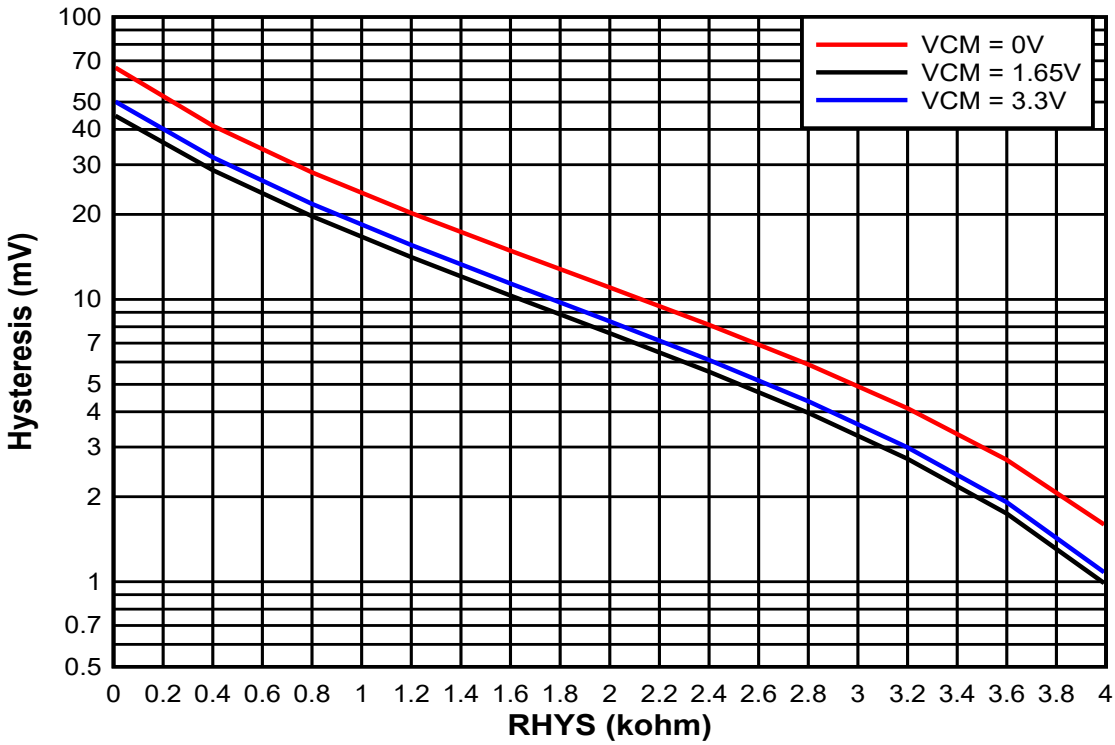


Figure 6-6. Hysteresis vs RHYS at VCC = 3.3V

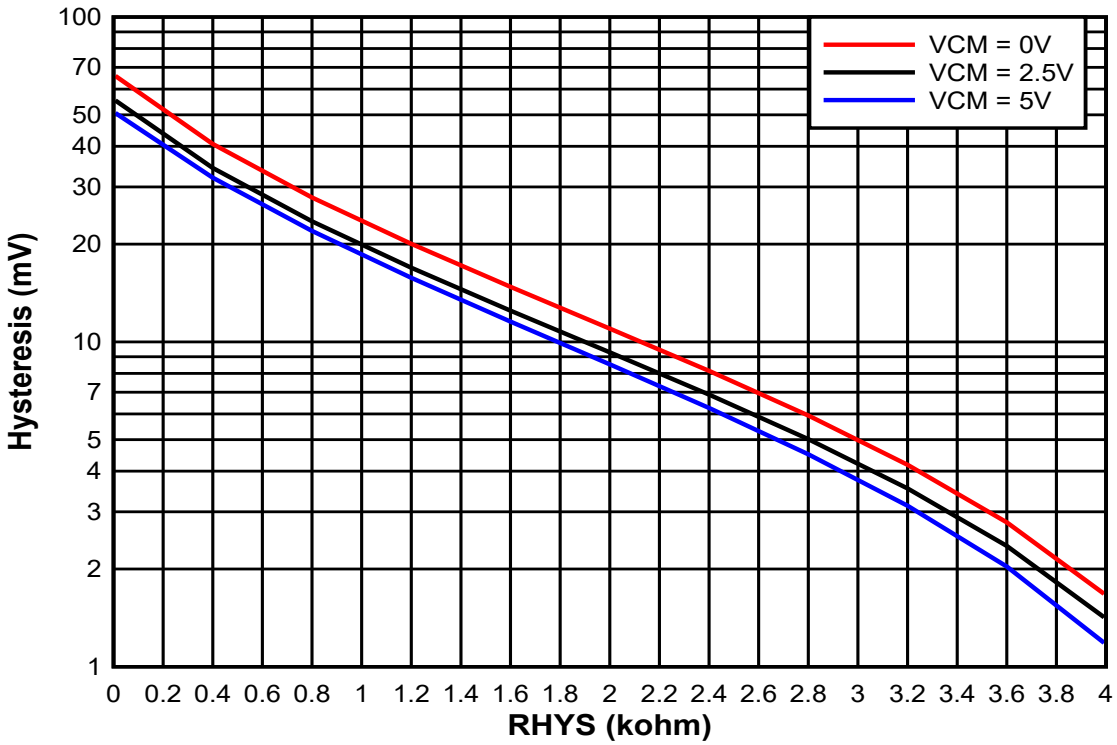


Figure 6-7. Hysteresis vs RHYS at VCC = 5V

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Application Overview

The TLV3901 comparator features rail-to-rail inputs, separate input and output power supply pins, latch functionality, external hysteresis control, along with a CML output stage for high speed applications. The 125ps propagation delay of the comparator improves performance and extends the range for applications involving optical reception (proximity sensing and LIDAR), triggers for test and measurement systems, and transceivers that require a high speed signal to be carried over a certain distance.

7.2 Typical Application

7.2.1 Optical Receiver

The TLV3901 in conjunction with a high-speed amplifier such as the OPA858 creates an optical receiver as shown in the Figure 7-1. The photodiode operates in photoconductive mode where exposure to light causes a reverse current through the photodiode. A bias voltage is applied to the op amp's non-inverting input to prevent saturation at the negative power supply and also serves as a negative bias for the photodiode, effectively reducing the parasitic capacitance. The OPA858 converts the current conducting through the diode into a voltage for the high-speed comparator to detect. The TLV3901 outputs the proper CML signal according to the threshold set by V_{REF}.

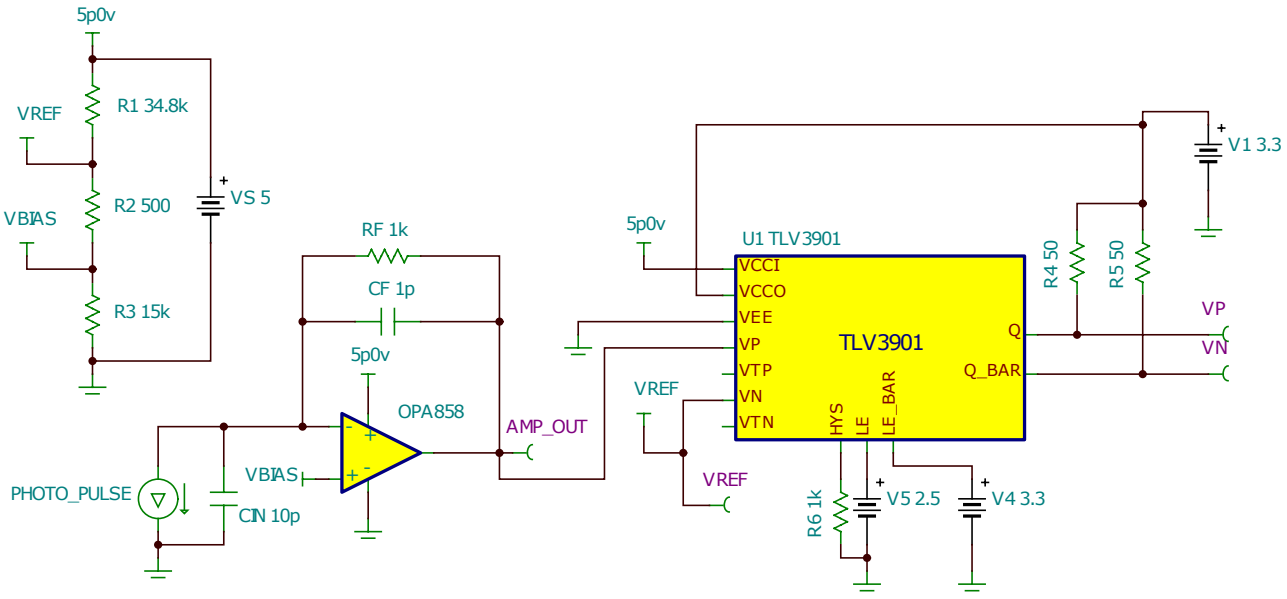


Figure 7-1. Optical Receiver

7.2.1.1 Design Requirements

Table 7-1. Design Parameters

PARAMETER	VALUE
V_{CC}	+5V
V_{EE}	0V
$V_{OUT, SWING}$	100mV
I_{DIODE}	100µA
f_p	159MHz

7.2.1.2 Detailed Design Procedure

Set V_{BIAS} to be in the recommended common-mode voltage range of the OPA858. This is also the minimum output voltage of the op amp $V_{OUT, MIN}$ as the op amp attempts to settle at the voltage applied to the non-inverting input.

The maximum output voltage of the op amp $V_{OUT, MAX}$ can be calculated from the desired output voltage swing $V_{OUT, SWING}$ and $V_{OUT, MIN}$, as shown in Equation 1

$$V_{OUT, MAX} = V_{OUT, SWING} + V_{OUT, MIN} \quad (1)$$

The gain resistor R_F is determined by the desired $V_{OUT, MAX}$ and $V_{OUT, MIN}$ and the maximum current I_{DIODE} through the diode, as shown in Equation 2.

$$R_F = (V_{OUT, MAX} - V_{OUT, MIN}) / I_{DIODE} \quad (2)$$

The feedback capacitor, in combination with the gain resistor, forms a pole in the frequency response of the amplifier. The feedback capacitor can be determined by the gain resistor and the desired pole frequency f_p, as shown in Equation 3.

$$C_F = 1 / (2 \times \pi \times R_F \times f_p) \quad (3)$$

Set V_{REF} to be the switching threshold voltage between $V_{OUT, MAX}$ and $V_{OUT, MIN}$.

Select values for V_{BIAS} and V_{REF}. Plug in given values for $V_{OUT, MAX}$, I_{DIODE}, and f_p. In the example, V_{BIAS} = 1.5V, V_{REF} = 1.55V, and R_F, C_F is solved as 1kΩ and 1pF, respectively.

For more information, please refer to the op amp tutorials for stability analysis on the transimpedance amplifier Spice Stability Analysis and Op Amp Stability. See the application note, Transimpedance Amplifier Circuit for more detailed procedures.

7.2.1.3 Application Performance Plots

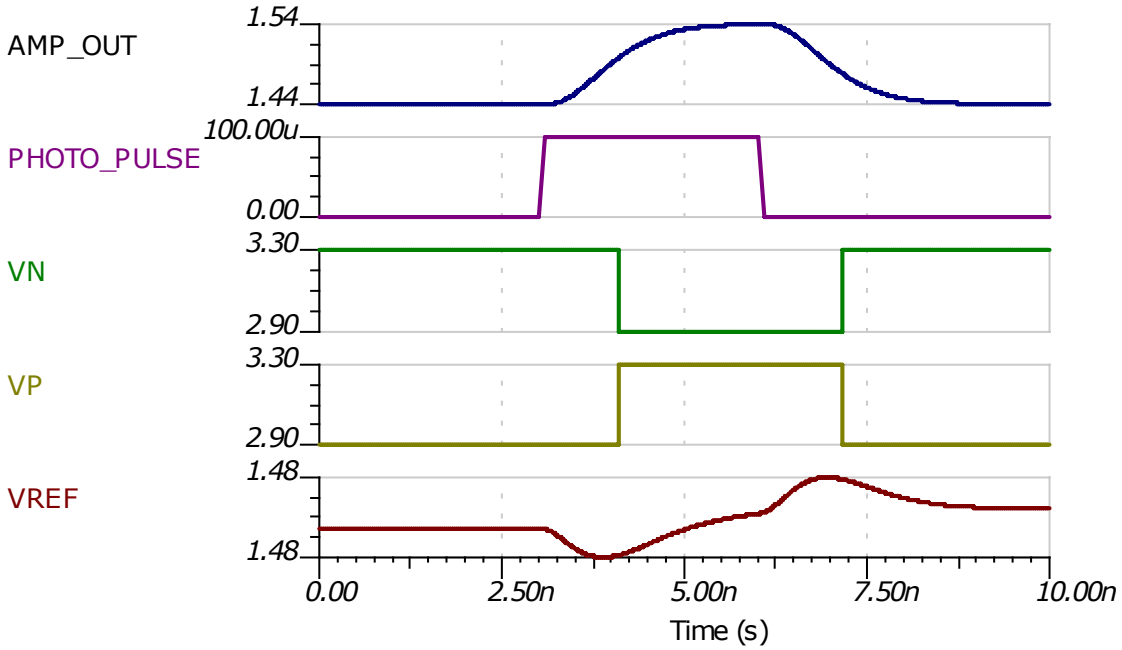


Figure 7-2. Optical Receiver Output Waveforms

7.2.2 External Trigger Function for Oscilloscopes

Figure 7-3 is a typical configuration for creating an external trigger on oscilloscopes. The user adjusts the trigger level, and a DAC converts this trigger level to a voltage the TLV3901 can use as a reference. The input voltage from an oscilloscope channel is then compared to the trigger reference voltage, and the TLV3901 sends a CML signal to a downstream FPGA to begin a capture. Since bipolar inputs are common in test and measurement systems such as oscilloscopes, the TLV3901 can be configured in split supply so that the inputs are within the allowable input voltage range. Since the outputs are CML, 50ohm pullup resistors are utilized. Please note that the pullup voltage needs to be less than or equal to VCCI.

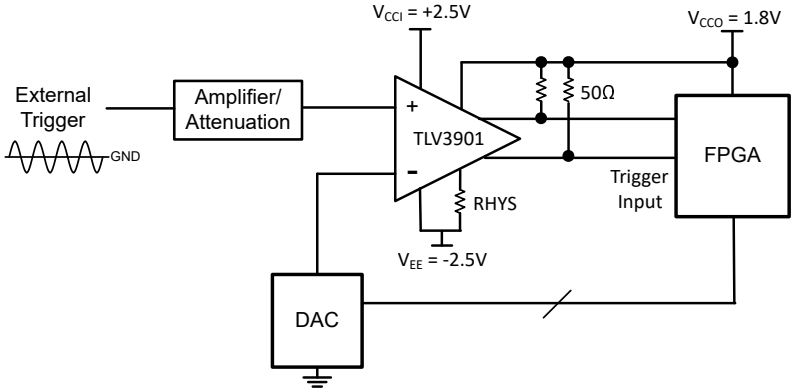


Figure 7-3. External Trigger Function

7.2.3 Logic Clock Source to CML Transceiver

The Figure 7-4 shows a logic clock source being terminated and driven with the TLV3901 across a CAT6 Cable to receive an equivalent CML clock signal at the receiver end. Utilizing a comparator which implements an analog differential amplifier on the input allows more sensitivity to attenuated (distorted) signals than a traditional CML buffer.

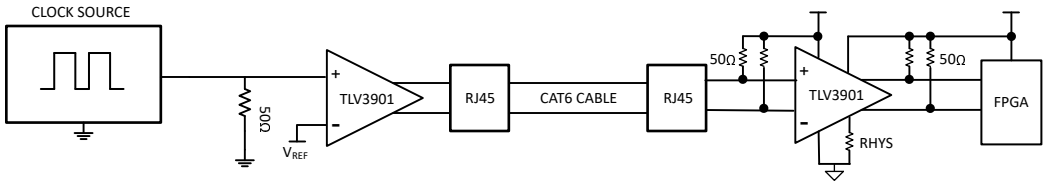


Figure 7-4. CML Clock Transceiver

7.3 Power Supply Recommendations

The TLV3901 has two separate power rails: VCCI - VEE for the input stage and VCCO - VEE for the output stage. This allows for both single and split supply operation for the input stage. Split supply operation allows users to apply both positive and negative (bipolar) voltages to the rail-to-rail input stage. Similarly, having dedicated pins for VCCO, allows the CML output stage to be compatible with the downstream receiver by making VCCO and the receiver supply the same voltage. Note that the CML output 50Ω pull-up resistors are connected to VCCO to meet data sheet specification.

Regardless of single supply or split supply operation, proper decoupling capacitors are required. Use a scheme of multiple, low-ESR ceramic capacitors from the supply pins to the ground plane for optimum performance. A good combination is 100pF, 10nF, and 1µF with the lowest value capacitor closest to the comparator.

7.4 Layout

7.4.1 Layout Guidelines

Comparators are very sensitive to input noise. For best results, adhere to the following layout guidelines.

1. Use a printed-circuit-board (PCB) with a good, unbroken, low-inductance ground plane. Proper grounding (use of a ground plane) helps maintain specified device performance.
2. To minimize supply noise for single and split supply, place decoupling capacitor arrays as close as possible to V_{CC}.
3. On the inputs and the output, keep lead lengths as short as possible to avoid unwanted feedback around the comparator (keep input traces away from the outputs) and minimize parasitic capacitance by eliminating ground pours around the inputs and outputs.
4. Solder the device directly to the PCB rather than using a socket.
5. Each output requires a 50Ω termination to VCCO.
6. Use higher performance substrate materials such as Rogers.

7.4.2 Layout Example

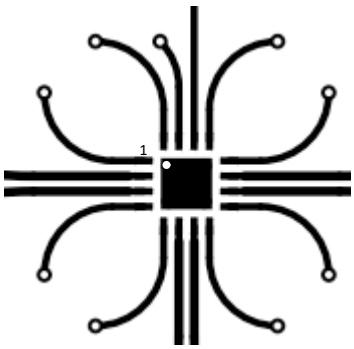


Figure 7-5. TLV3901EVM Layout Example

8 Device and Documentation Support

8.1 Device Support

8.1.1 Related Documentation

Texas Instruments, *LIDAR Pulsed Time of Flight Reference Design*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (December 2025)	Page
• Change preview to RTM for TLV3811	1
• Changed the device status from Advanced to Production	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3901RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL3901

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

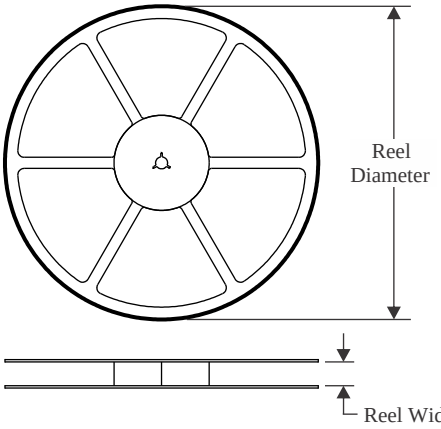
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

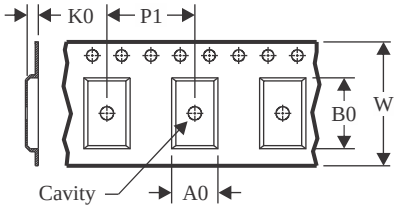
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

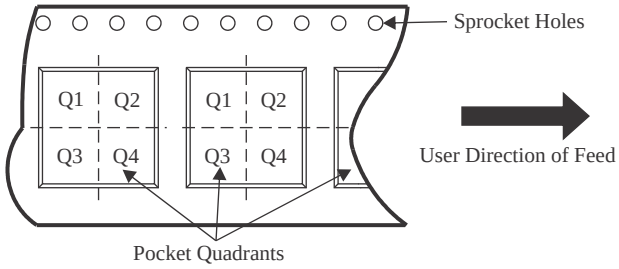


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

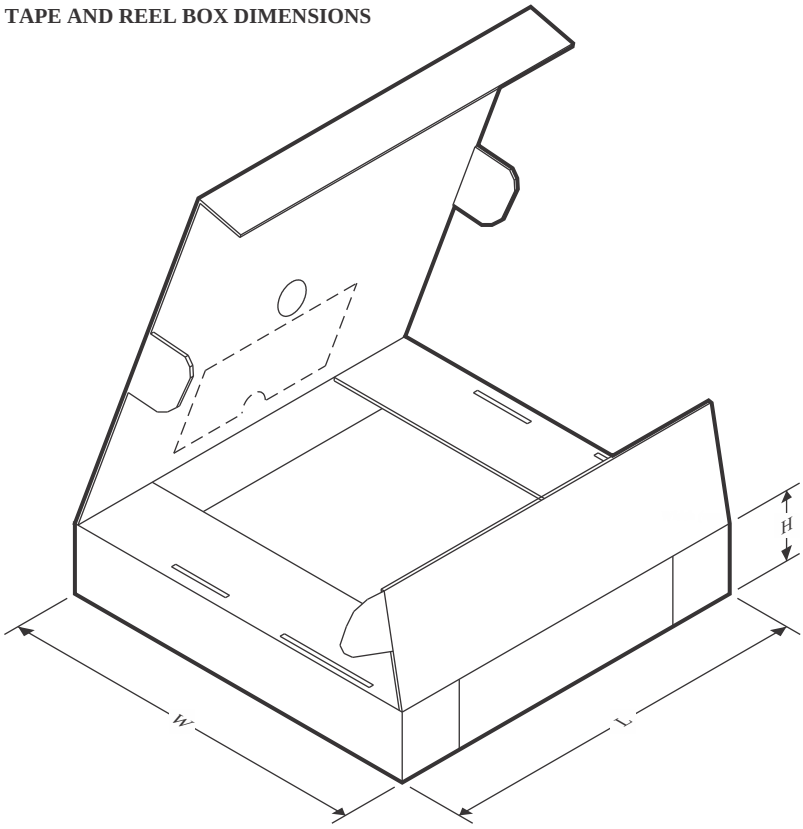
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3901RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3901RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

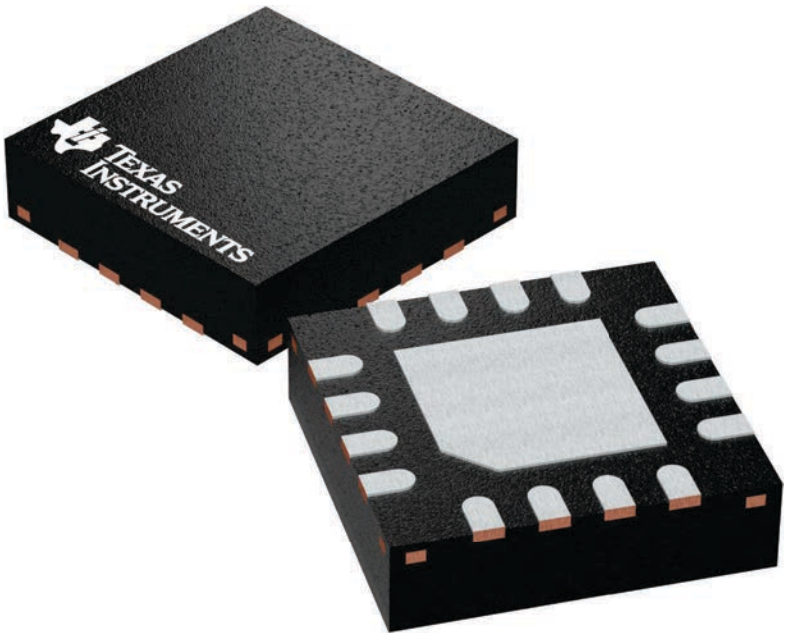
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

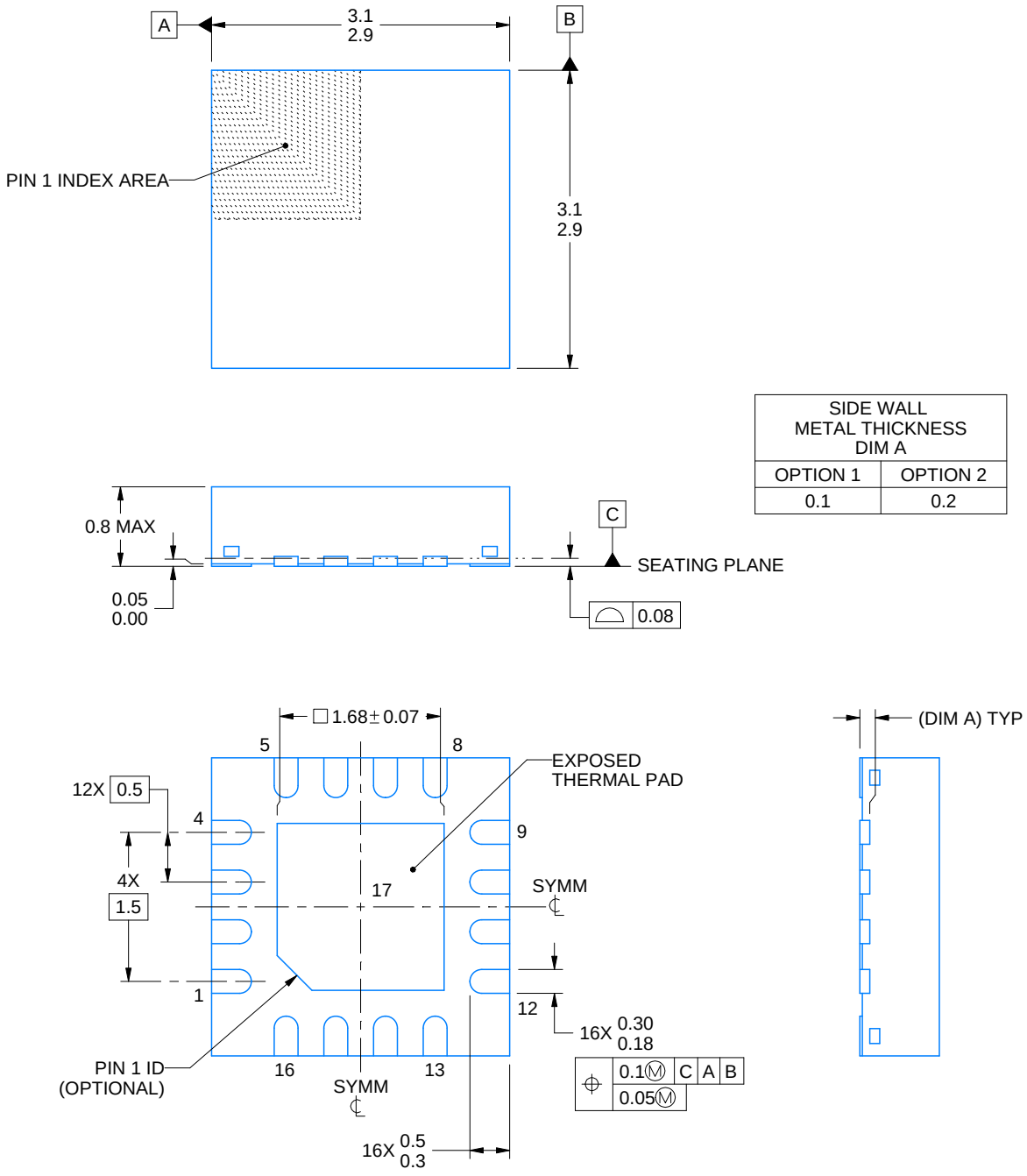


RTE0016C

PACKAGE OUTLINE

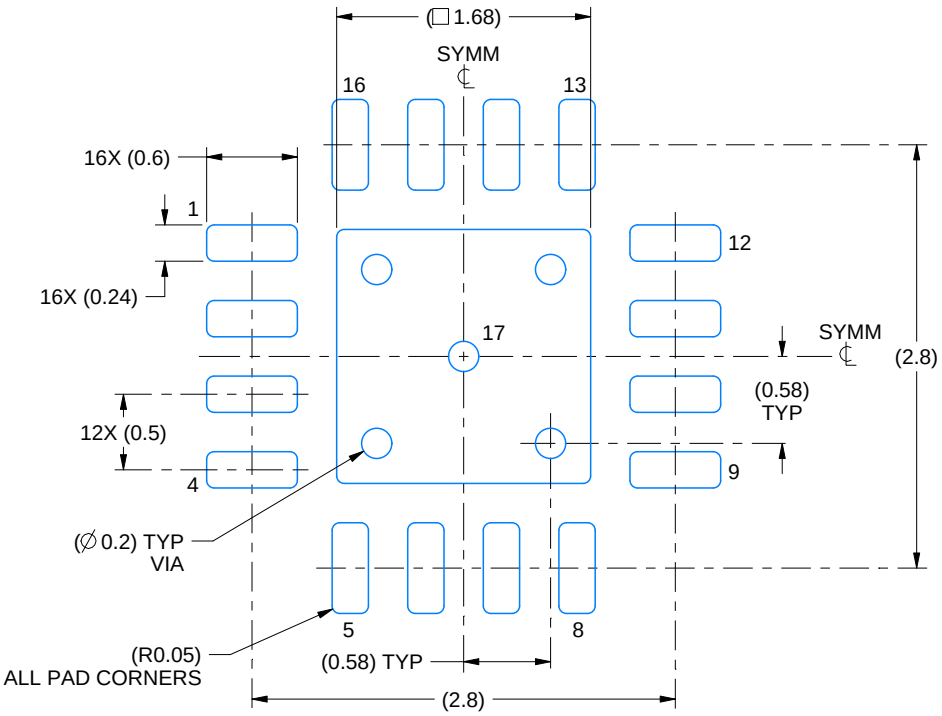
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

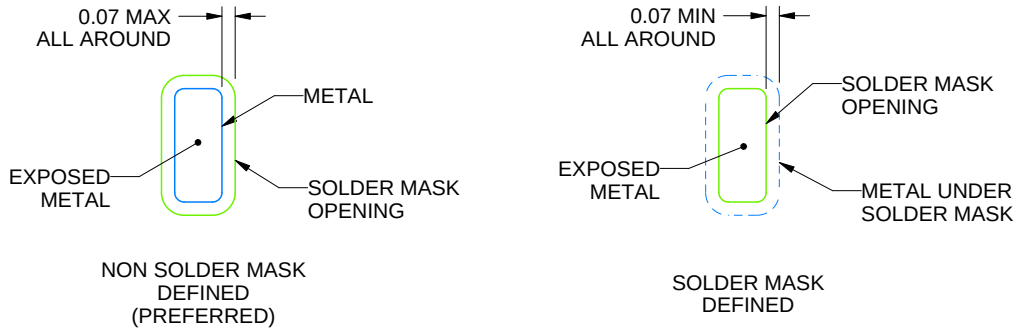


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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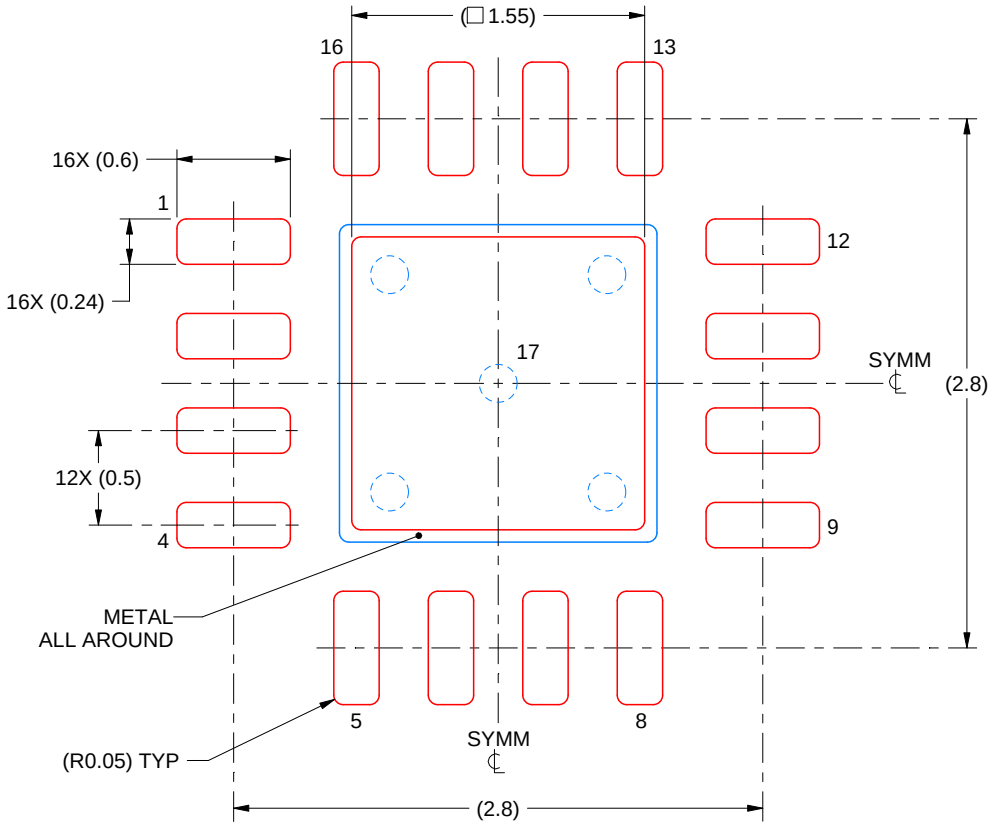
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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