TLV2460A-EP TLV2461A-EP TLV2462A-EP TLV2463A-EP TLV2464A-EP FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

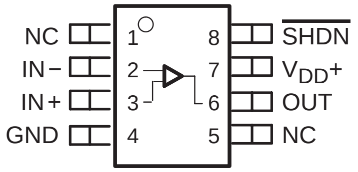
SGLS132C − AUGUST 2002 − REVISED OCTOBER 2005

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree**[†]
- **Rail-to-Rail Output Swing**
- **Gain Bandwidth Product . . . 6.4 MHz**
- **±80 mA Output Drive Capability**

[†] Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **Supply Current . . . 500 μA/channel**
- **Input Offset Voltage . . . 100 μV**
- **Input Noise Voltage . . . 11 nV/√Hz**
- **Slew Rate . . . 1.6 V/μs**
- **Micropower Shutdown Mode (TLV2460/3) . . . 0.3 μA/Channel**
- **Universal Operational Amplifier EVM**

TLV2460
D PACKAGE
(TOP VIEW)



description

The TLV246x is a family of low-power rail-to-rail input/output operational amplifiers specifically designed for portable applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x ideal for buffering analog-to-digital converters.

The operational amplifier has 6.4 MHz of bandwidth and 1.6 V/μs of slew rate with only 500 μA of supply current, providing good ac performance with low power consumption. Devices are available with an optional shutdown terminal, which places the amplifier in an ultralow supply current mode (I_{DD} = 0.3 μA/ch). While in shutdown, the operational-amplifier output is placed in a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/√Hz and input offset voltage of 100 μV.

ORDERING INFORMATION[†]

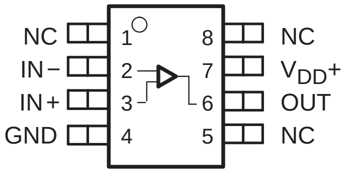
T_A	PACKAGE[‡]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	D	Tape and reel	TLV2462AQDREP	2462AE
	D	Tape and reel	TLV2463AQDREP	V2463AQE
−55°C to 125°C	D	Tape and reel	TLV2462AMDREP	2462AM
	D	Tape and reel	TLV2464AMDREP	V2464AME
	PW	Tape and reel	TLV2464AMPWREP	2464AME

[†] Some of the TLV246x family, along with packaging options, are in the **Product Preview** stage of development. Contact the local Texas Instruments sales office for availability.

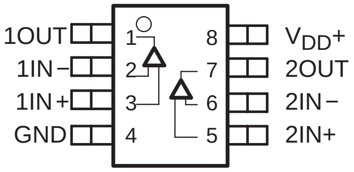
[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TLV246x PACKAGE PINOUTS

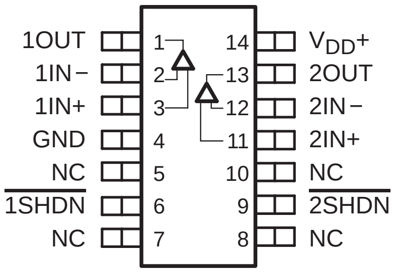
TLV2461
D or PW PACKAGE
(TOP VIEW)



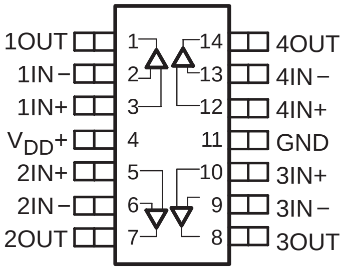
TLV2462
D or PW PACKAGE
(TOP VIEW)



TLV2463
D or PW PACKAGE
(TOP VIEW)



TLV2464
D or PW PACKAGE
(TOP VIEW)



NC − No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . . 6 V
Differential input voltage, V_{ID} . . . . . . − 0.2 V to V_{DD} + 0.2 V
Input current, I_I (any input) . . . . . . ± 200 mA
Output current, I_O . . . . . . ± 175 mA
Total input current, I_I (into V_{DD+}) . . . . . . 175 mA
Total output current, I_O (out of GND) . . . . . . 175 mA
Continuous total power dissipation . . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . . −55°C to 125°C
Maximum junction temperature, T_J . . . . . . 150°C
Storage temperature range, T_{stg} . . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND.

THERMAL RESISTANCE TABLE

PACKAGE	θ_{JC} (°C/W)		θ_{JA} (°C/W, 0 Air Flow)	
	High K	Low K	High K	Low K
D (8)	39.4	42.4	97.1	165.5
D (14)	51.5	53.7	86.2	133.5
PW (8)	65.1	69.4	149.4	230.5
PW (14)	45.8	46.6	111.7	131.4

NOTE: Thermal resistances are not production tested and are for informational purposes only.

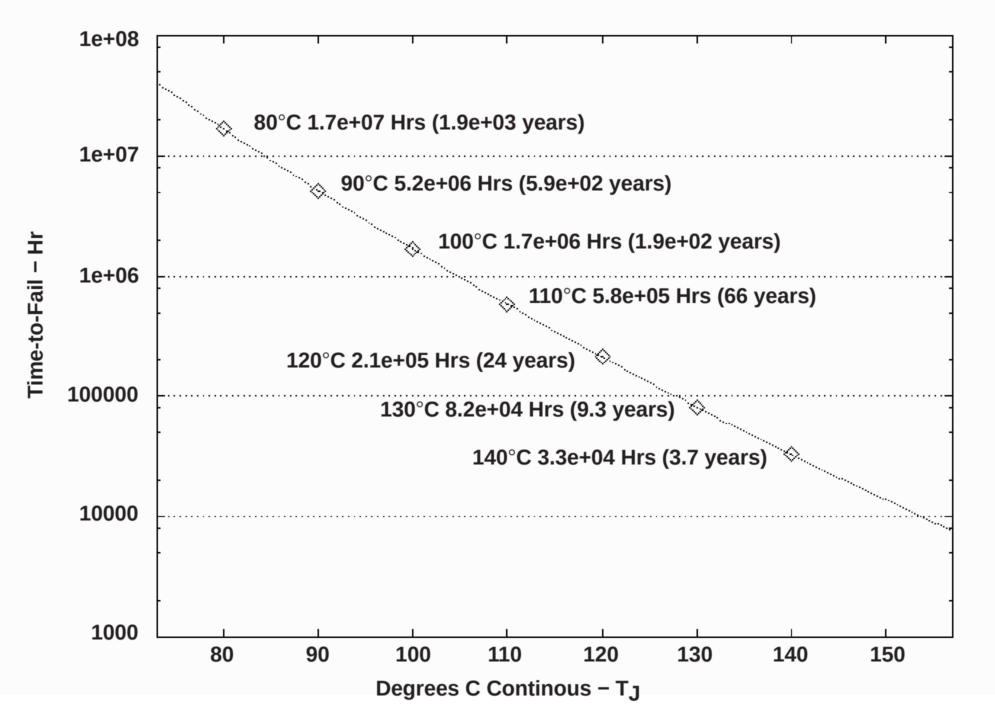


Figure 1. Wirebond Life Estimation Plot

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		−0.2	V_{DD}+0.2	V
Shutdown on/off voltage level‡	V_{IH}	2		V
	V_{IL}		0.7	
Operating free-air temperature, T_A		−40	125	°C

‡ Relative to voltage on the GND terminal of the device.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 3 V, V_O = 1.5 V,	V_{IC} = 1.5 V, R_S = 50 Ω	25°C		150	1500	μV
				Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage					2		μV/°C
I_{IO}	Input offset current	V_{DD} = 3 V, V_O = 1.5 V,	V_{IC} = 1.5 V, R_S = 50 Ω	25°C		2.8	7	nA
				Full range			75	
I_{IB}	Input bias current			25°C		4.4	14	nA
				Full range			75	
V_{OH}	High-level output voltage	I_{OH} = −2.5 mA		25°C		2.9		V
				Full range	2.8			
		I_{OH} = −10 mA		25°C		2.7		
				Full range	2.5			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 2.5 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 1.5 V,	I_{OL} = 10 mA	25°C		0.3		
				Full range			0.5	
I_{OS}	Short-circuit output current	Sourcing		25°C		50		mA
				Full range	20			
		Sinking		25°C		40		
				Full range	20			
I_O	Output current	Measured 1 V from rail		25°C		±40		mA
A_{VD}	Large-signal differential voltage amplification	R_L = 10 kΩ		25°C	90	105		dB
				Full range	89			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		33		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 V to 3 V, R_S = 50 Ω		25°C	66	80		dB
				Full range	60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	85	95		
				Full range	80			
I_{DD}	Supply current (per channels)	V_O = 1.5 V,	No load	25°C		0.5	0.575	mA
				Full range			0.9	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463)	$\overline{SHDN}$ < 0.7 V, Per channel in shutdown		25°C		0.3		μA
				Full range			2.5	

† Full range is −40°C to 125°C for the Q suffix and −55°C to 125°C for the M suffix.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 160 pF,	25°C	1	1.6		V/μs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		16		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.006%		
			A_V = 10			0.02%		
			A_V = 100			0.08%		
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF	R_L = 10 kΩ,	25°C		5.2		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.47		μs
			0.01%			1.78		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.77		
			0.01%			1.98		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 160 pF	25°C		44°		
	Gain margin			25°C		7		dB

† Full range is −40°C to 125°C for the Q suffix and −55°C to 125°C for the M suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5, V_O = 2.5 V, R_S = 50 Ω	25°C		150	1500	μV
			Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage		25°C		2		μV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω	25°C		0.3	7	nA
			Full range			60	
I_{IB}	Input bias current		25°C		1.3	14	nA
			Full range			60	
V_{OH}	High-level output voltage	I_{OH} = −2.5 mA	25°C		4.9		V
			Full range	4.8			
		I_{OH} = −10 mA	25°C		4.8		
			Full range	4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 2.5 mA	25°C		0.1		V
			Full range			0.2	
		V_{IC} = 2.5 V, I_{OL} = 10 mA	25°C		0.2		
			Full range			0.3	
I_{OS}	Short-circuit output current	Sourcing	25°C		145		mA
			Full range	60			
		Sinking	25°C		100		
			Full range	60			
I_O	Output current	Measured at 1 V from rail	25°C		±80		mA
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, R_L = 10 kΩ, V_O = 1 V to 4 V	25°C	92	109		dB
			Full range	90			
$r_{i(d)}$	Differential input resistance		25°C		10^9		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz	25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		29		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = 0 V to 5 V, R_S = 50 Ω	25°C	71	85		dB
			Full range	60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, V_{IC} = V_{DD}/2, No load	25°C	80	85		dB
			Full range	75			
		V_{DD} = 3 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	85	95		dB
			Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load,	25°C		0.55	0.65	mA
			Full range			1	
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463)	$\overline{\text{SHDN}}$ < 0.7 V, Per channels in shutdown	25°C		1		μA
			Full range			3	

† Full range is −40°C to 125°C for the Q suffix and −55°C to 125°C for the M suffix.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 160 pF,	25°C	1	1.6		V/μs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V, R_L = 10 kΩ, f = 10 kHz	A_V = 1	25°C		0.004%		
			A_V = 10			0.01%		
			A_V = 100			0.04%		
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF	R_L = 10 kΩ,	25°C		6.4		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.53		μs
			0.01%			1.83		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			3.13		
			0.01%			3.33		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 160 pF	25°C		45°		
	Gain margin			25°C		7		dB

† Full range is −40°C to 125°C for the Q suffix and −55°C to 125°C for the M suffix.

TYPICAL CHARACTERISTICS

Table of Graphs

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V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IB}	Input bias current	vs Free-air temperature	3, 4
I_{IO}	Input offset current	vs Free-air temperature	3, 4
V_{OH}	High-level output voltage	vs High-level output current	5, 6
V_{OL}	Low-level output voltage	vs Low-level output current	7, 8
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	9, 10
	Open-loop gain	vs Frequency	11, 12
	Phase	vs Frequency	11, 12
A_{VD}	Differential voltage amplification	vs Load resistance	13
	Capacitive load	vs Load resistance	14
Z_o	Output impedance	vs Frequency	15, 16
CMRR	Common-mode rejection ratio	vs Frequency	17
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	18, 19
I_{DD}	Supply current	vs Supply voltage	20
		vs Free-air temperature	21
	Amplifier turnon characteristics		22
	Amplifier turnoff characteristics		23
	Supply current turnon		24
	Supply current turnoff		25
	Shutdown supply current	vs Free-air temperature	26
SR	Slew rate	vs Supply voltage	27
V_n	Equivalent input noise voltage	vs Frequency	28, 29
		vs Common-mode input voltage	30, 31
THD	Total harmonic distortion	vs Frequency	32, 33
THD+N	Total harmonic distortion plus noise	vs Peak-to-peak signal amplitude	34, 35
ϕ_m	Phase margin	vs Frequency	11, 12
		vs Load capacitance	36
		vs Free-air temperature	37
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		vs Free-air temperature	39
	Large signal follower		40, 41
	Small signal follower		42, 43
	Inverting large signal		44, 45
	Inverting small signal		46, 47

TYPICAL CHARACTERISTICS

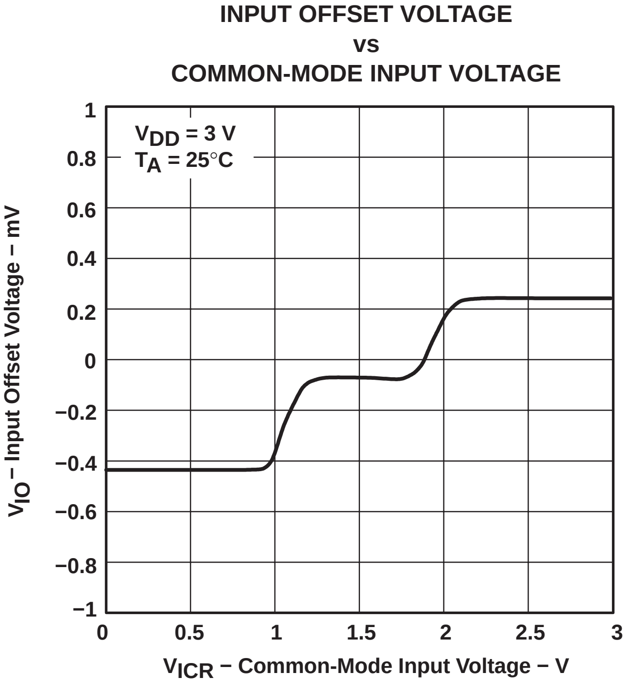


Figure 2

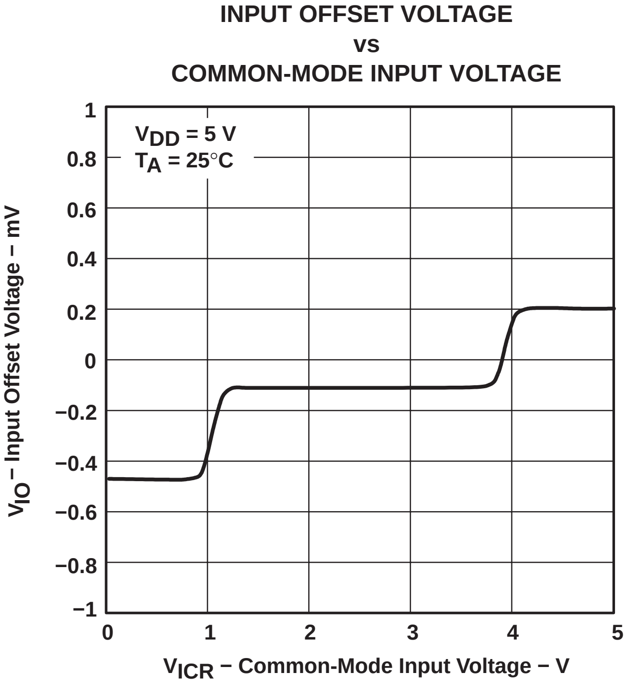


Figure 3

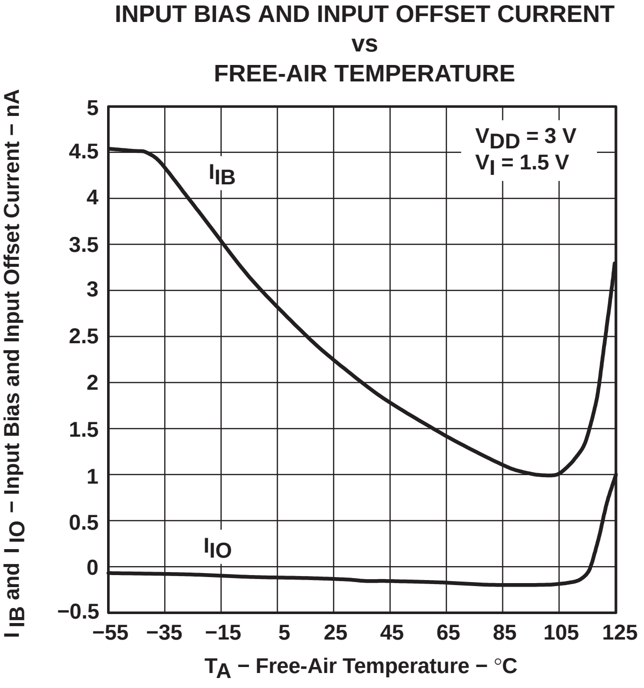


Figure 4

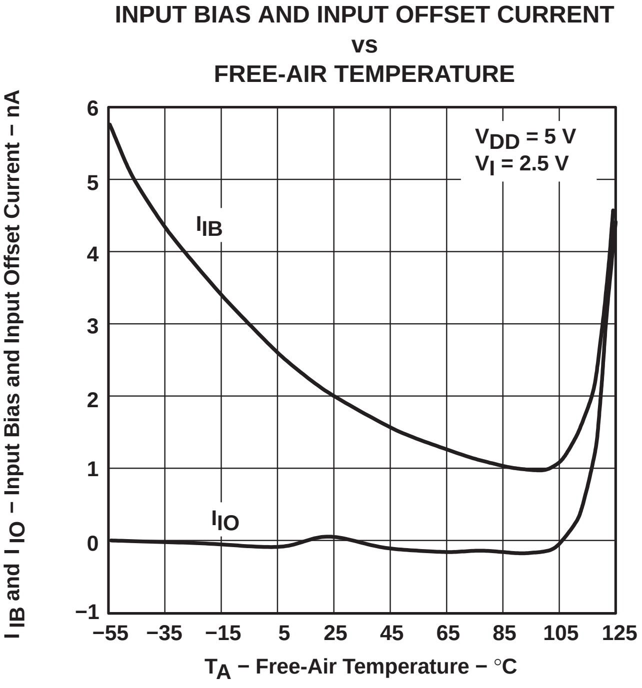


Figure 5

TYPICAL CHARACTERISTICS

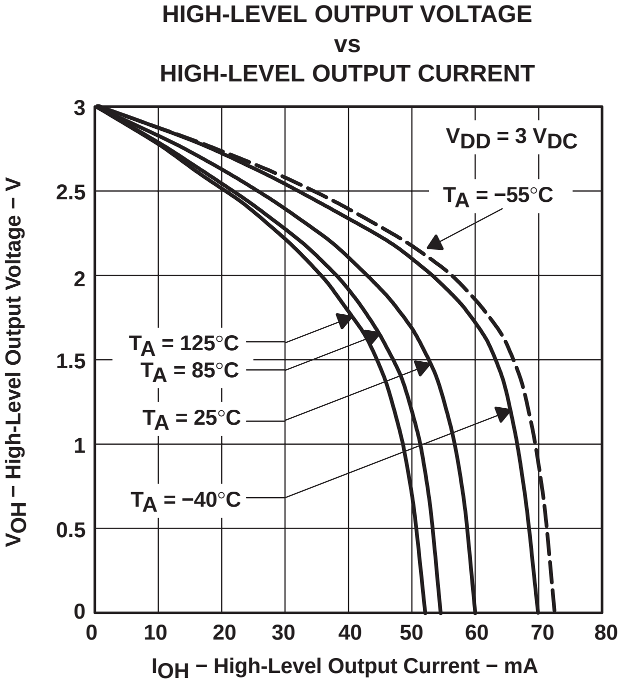


Figure 6

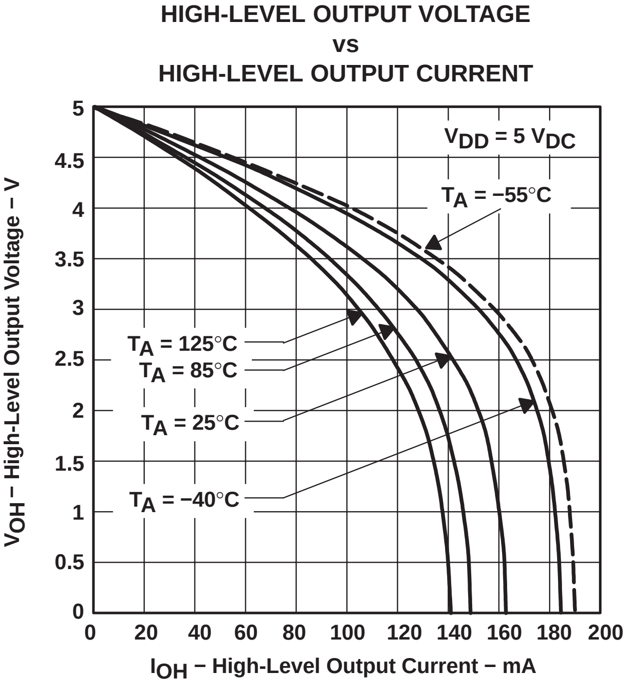


Figure 7

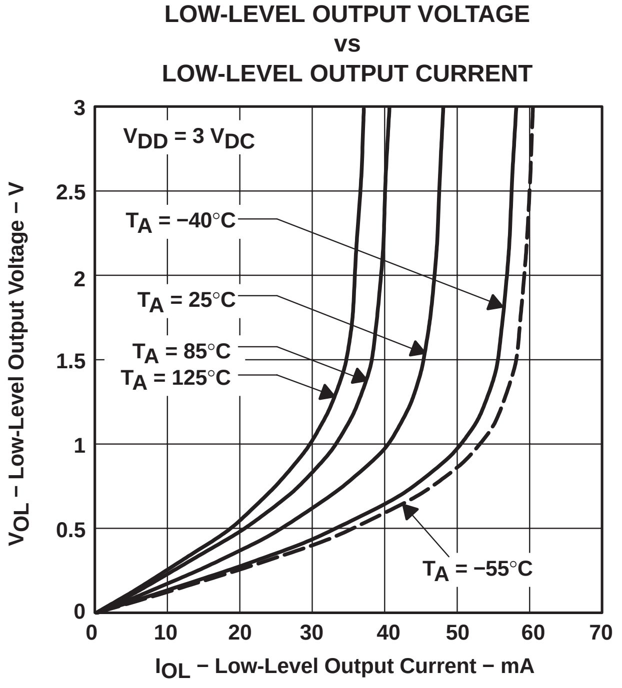


Figure 8

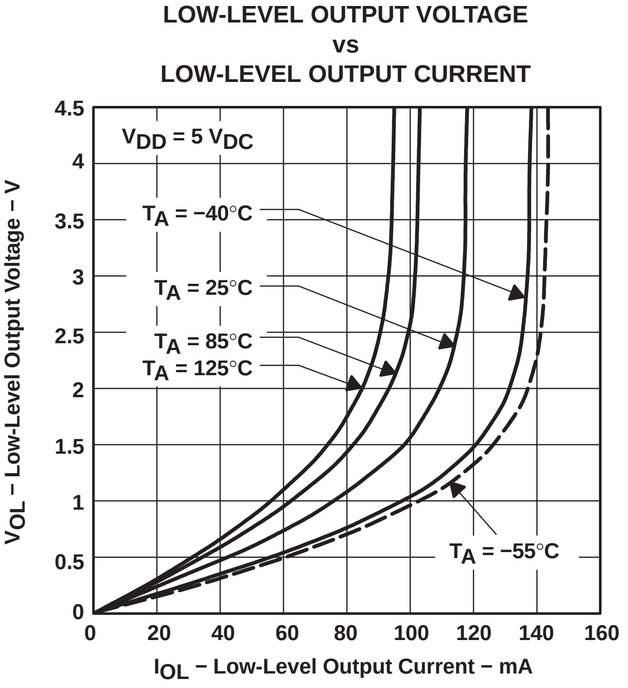


Figure 9

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

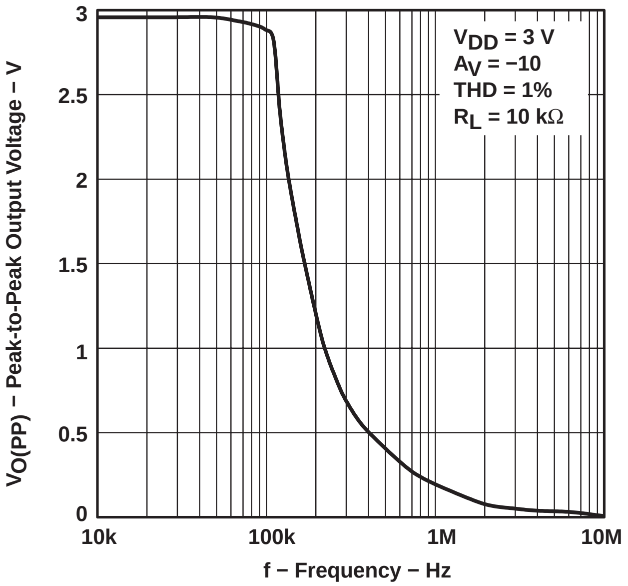


Figure 10

PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

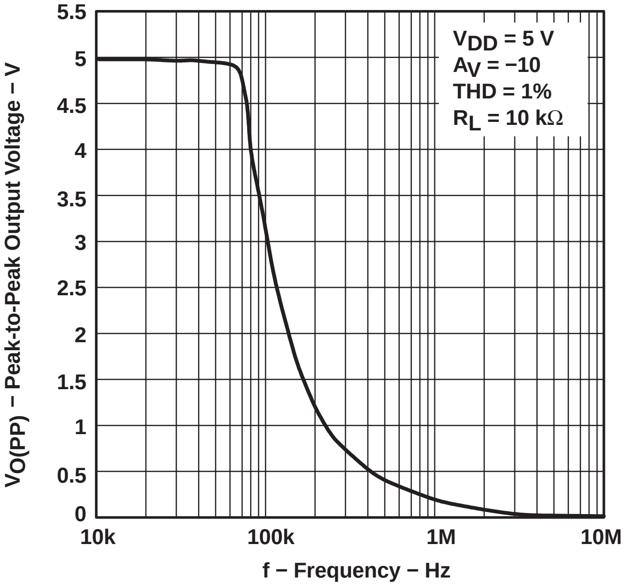


Figure 11

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

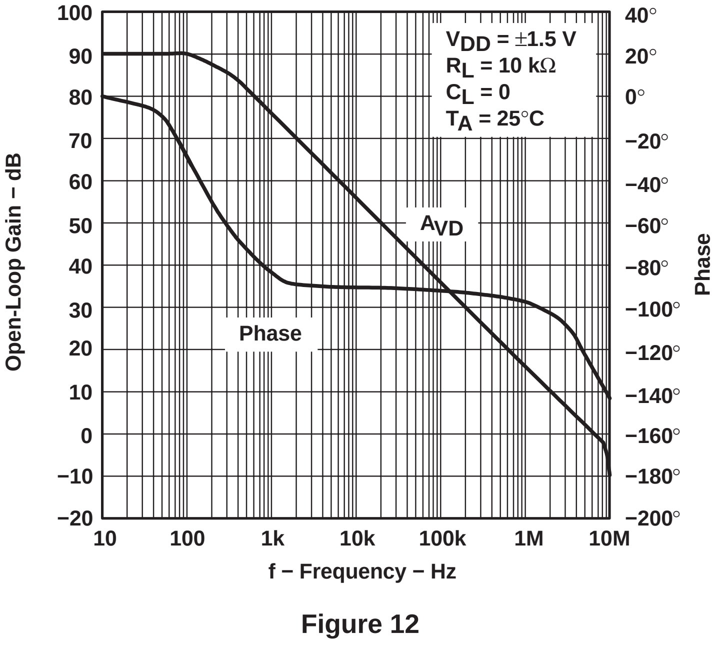


Figure 12

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

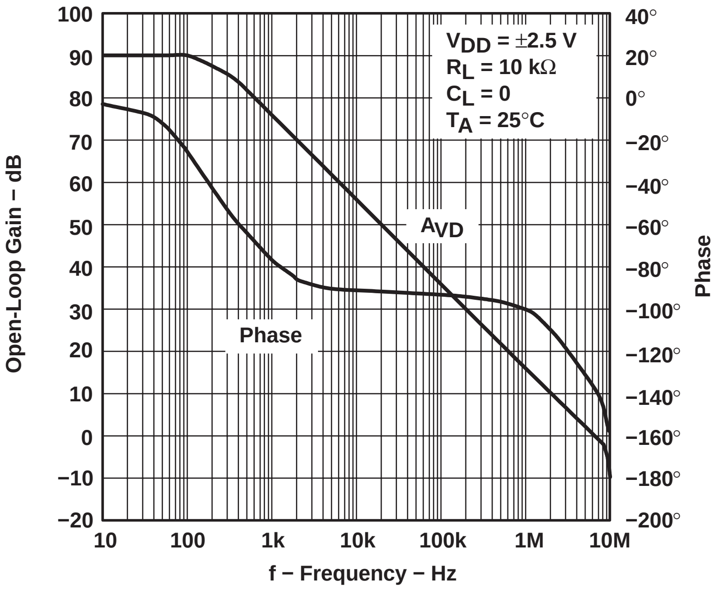


Figure 13

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

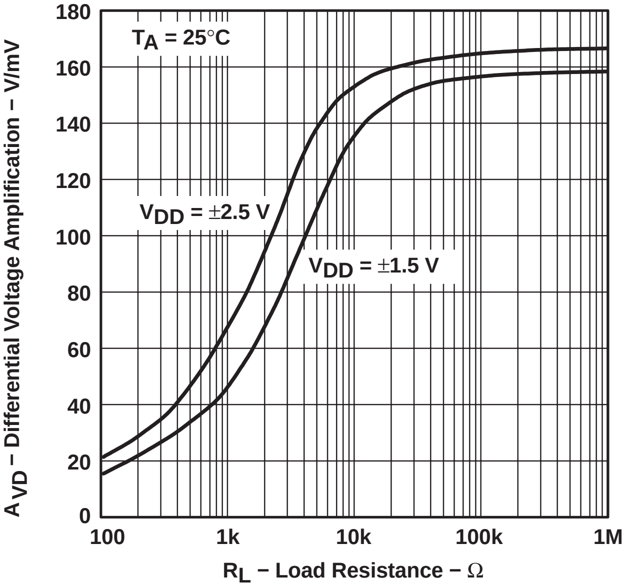


Figure 14

CAPACITIVE LOAD
vs
LOAD RESISTANCE

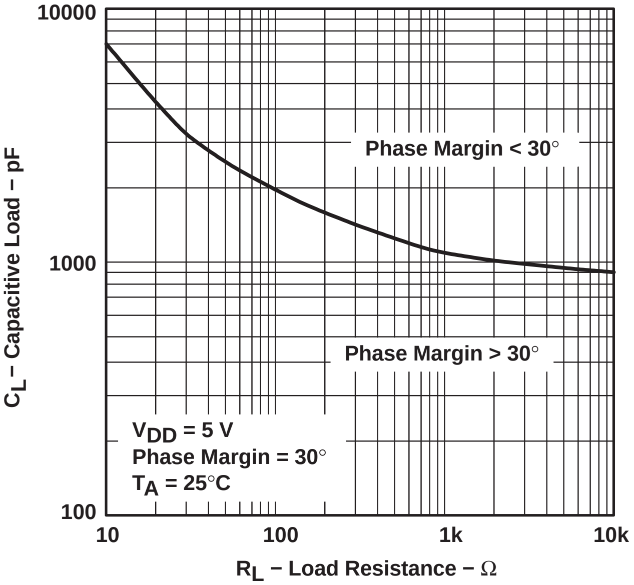


Figure 15

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

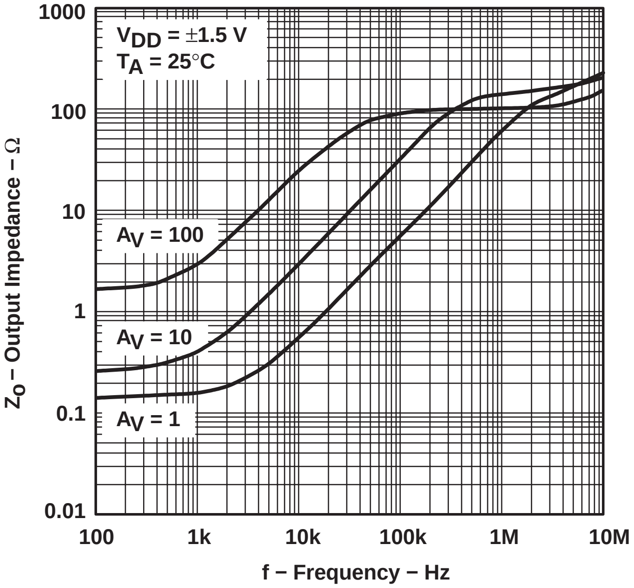


Figure 16

OUTPUT IMPEDANCE vs FREQUENCY

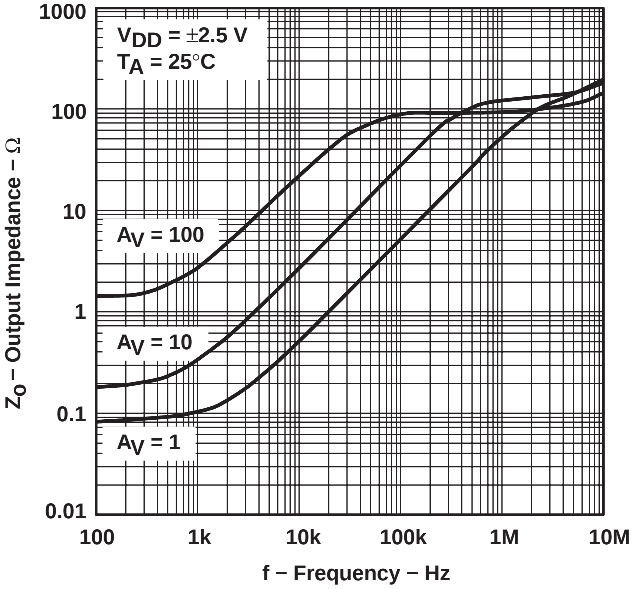


Figure 17

COMMON-MODE REJECTION RATIO vs FREQUENCY

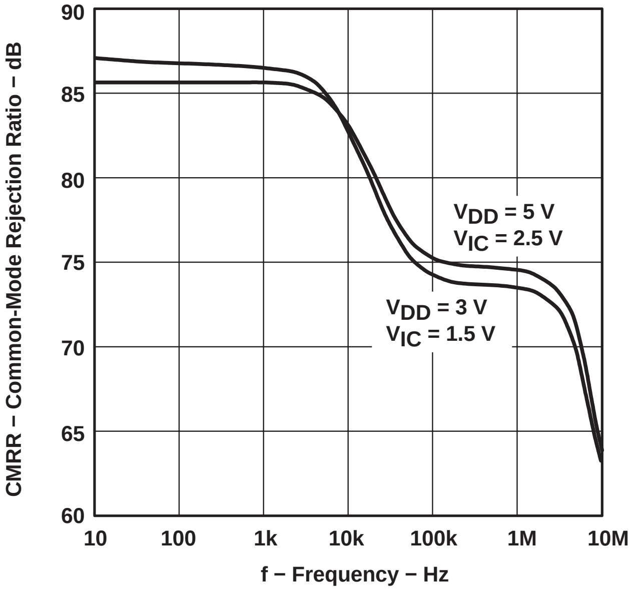


Figure 18

TYPICAL CHARACTERISTICS

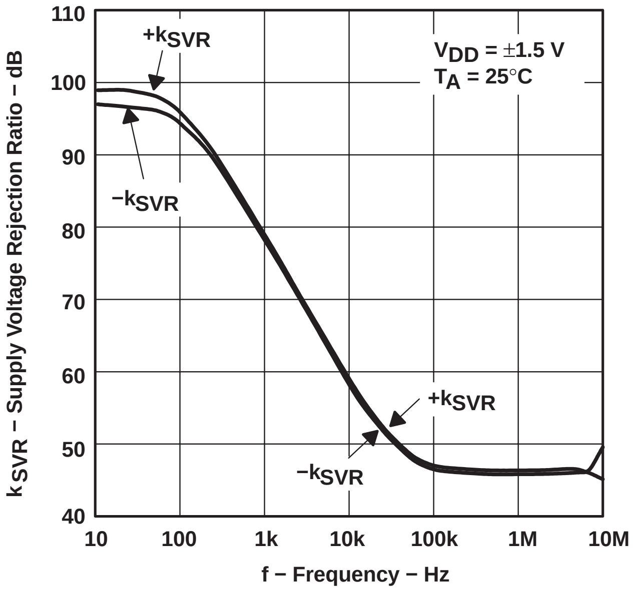

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 19

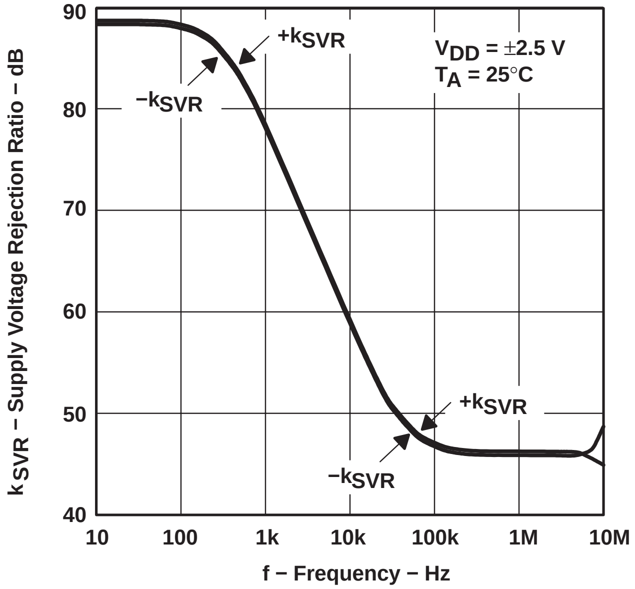

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 20

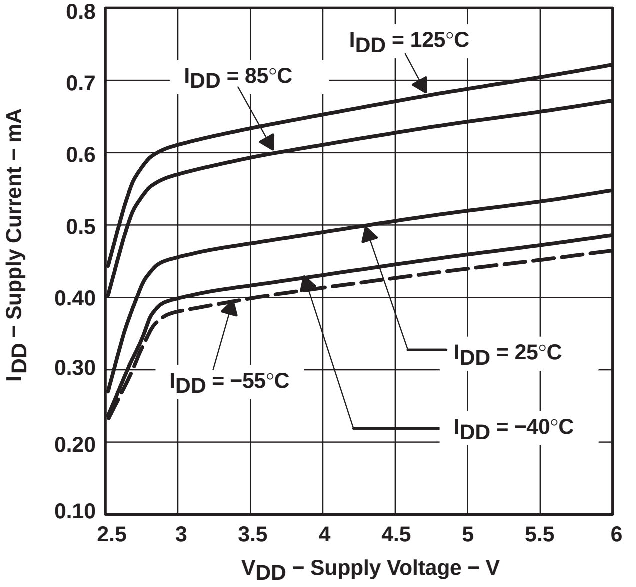

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 21

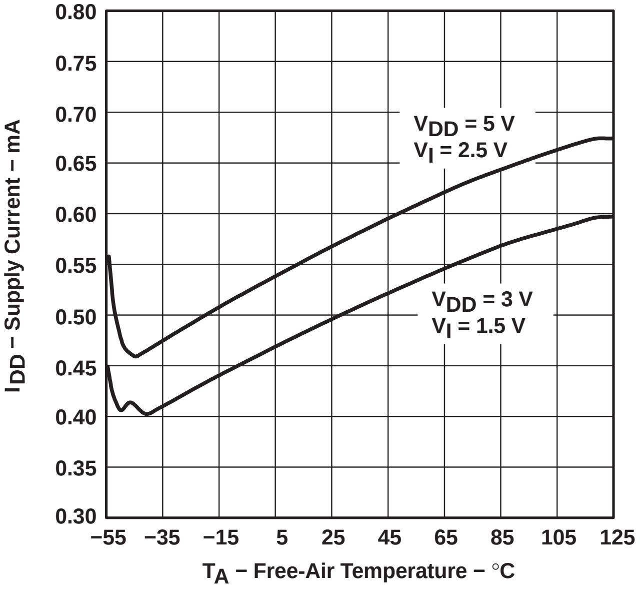

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 22

TYPICAL CHARACTERISTICS

AMPLIFIER WITH A SHUTDOWN PULSE TURNON CHARACTERISTICS

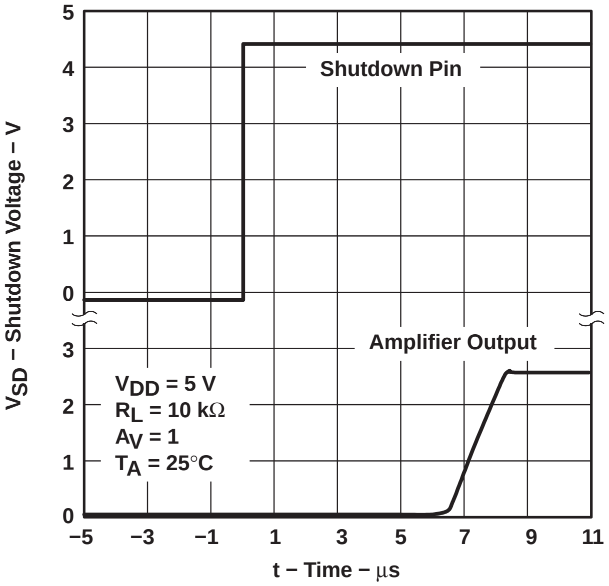


Figure 23

AMPLIFIER WITH A SHUTDOWN PULSE TURNOFF CHARACTERISTICS

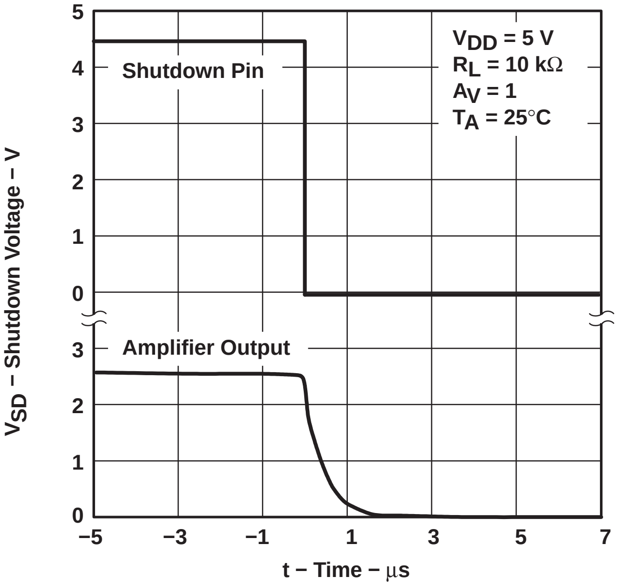


Figure 24

SUPPLY CURRENT WITH A SHUTDOWN PULSE TURNON CHARACTERISTICS

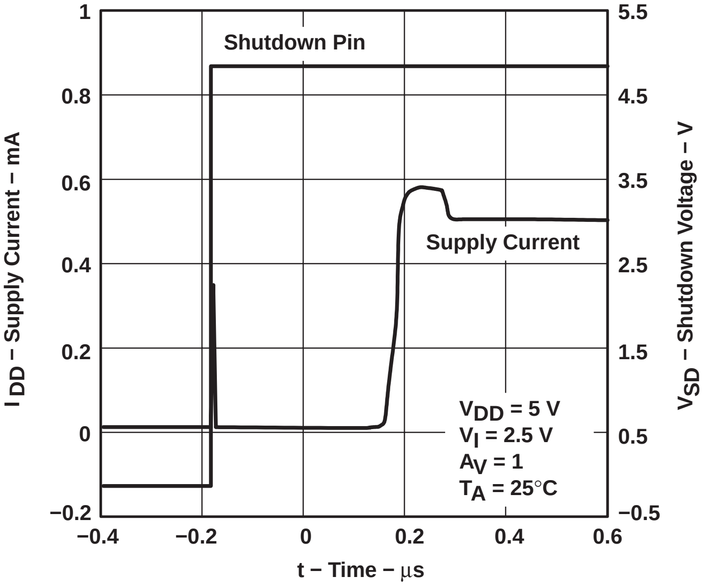


Figure 25

TYPICAL CHARACTERISTICS

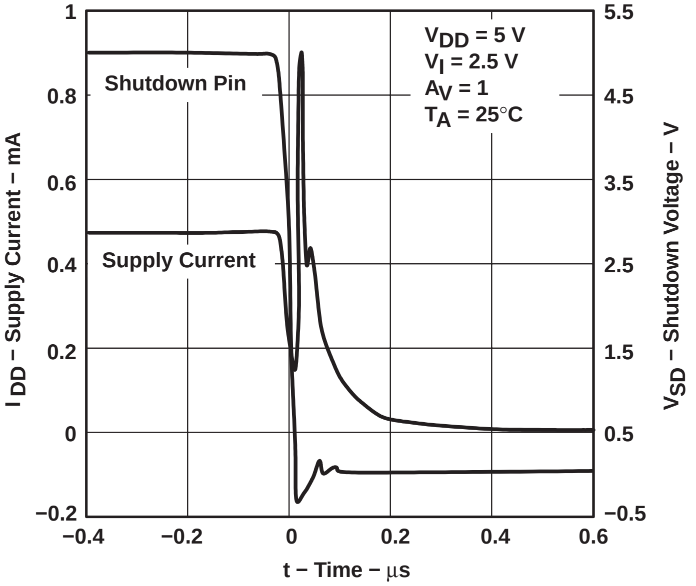

TURNOFF SUPPLY CURRENT
WITH A SHUTDOWN PULSE

Figure 26

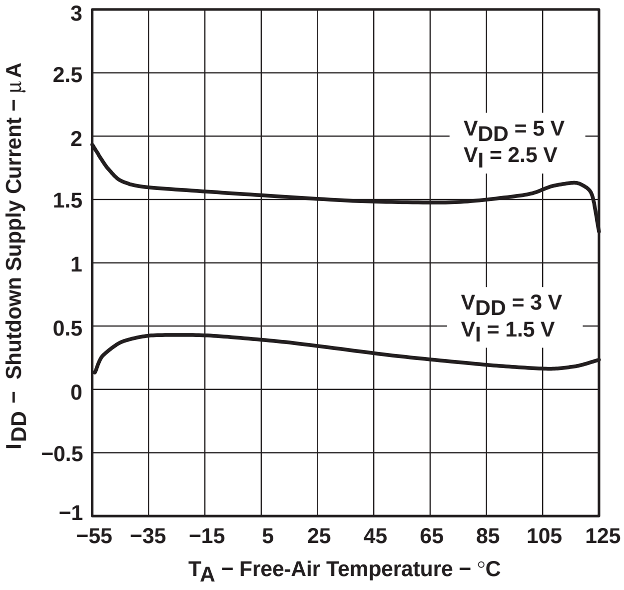

SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 27

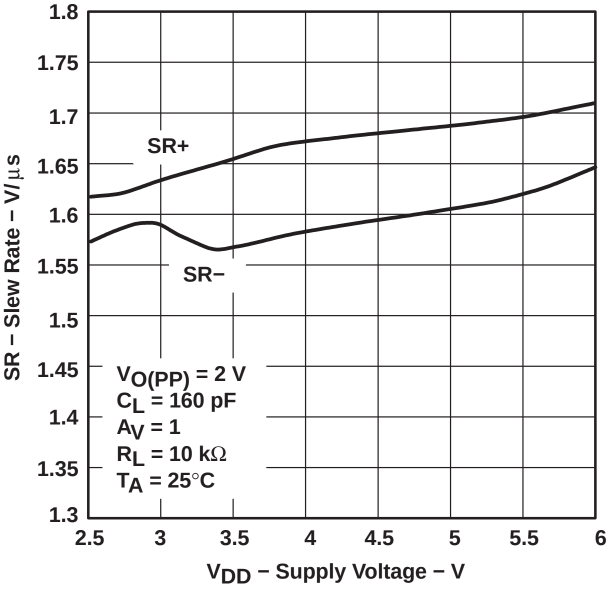

SLEW RATE
vs
SUPPLY VOLTAGE

Figure 28

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

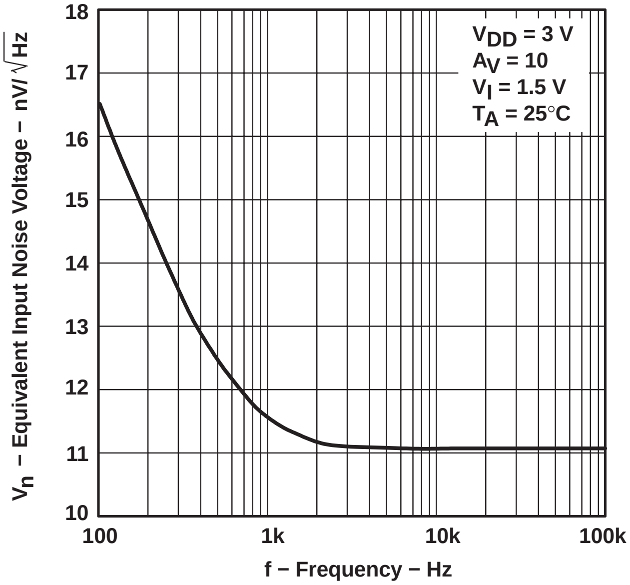


Figure 29

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

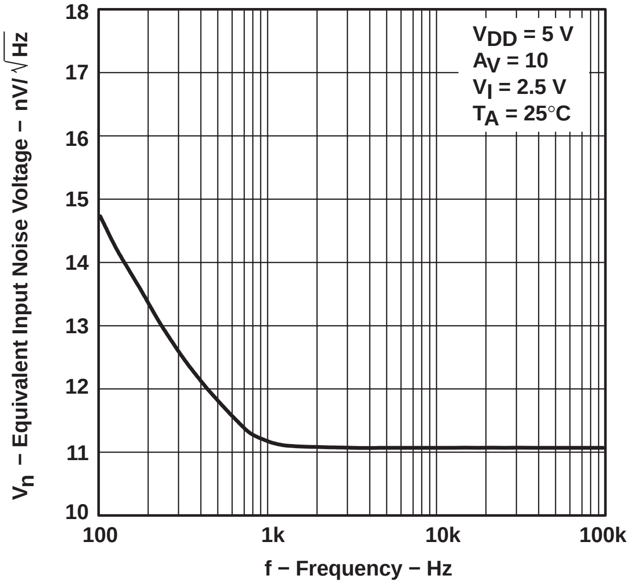


Figure 30

EQUIVALENT INPUT NOISE VOLTAGE vs COMMON-MODE INPUT VOLTAGE

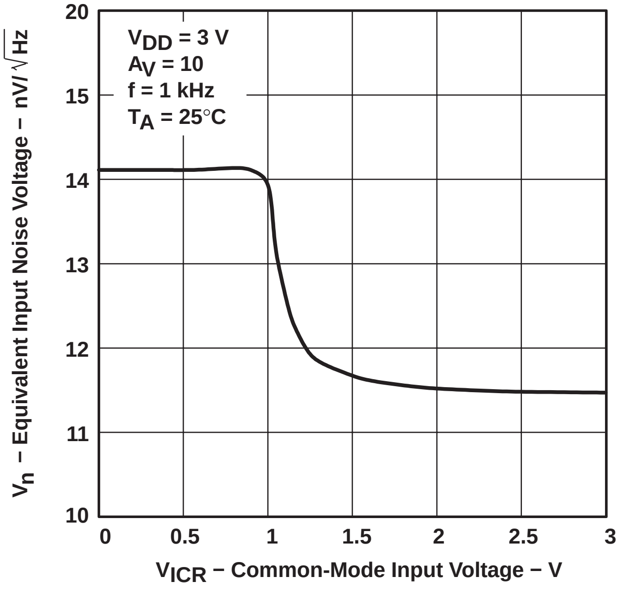


Figure 31

EQUIVALENT INPUT NOISE VOLTAGE vs COMMON-MODE INPUT VOLTAGE

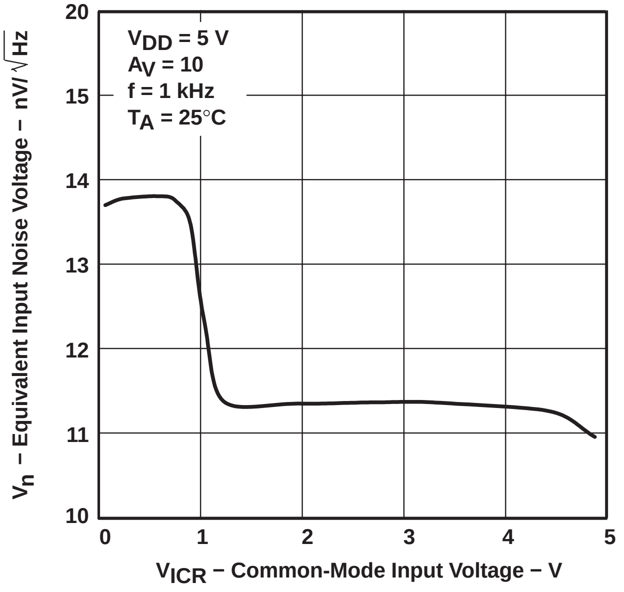


Figure 32

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs FREQUENCY

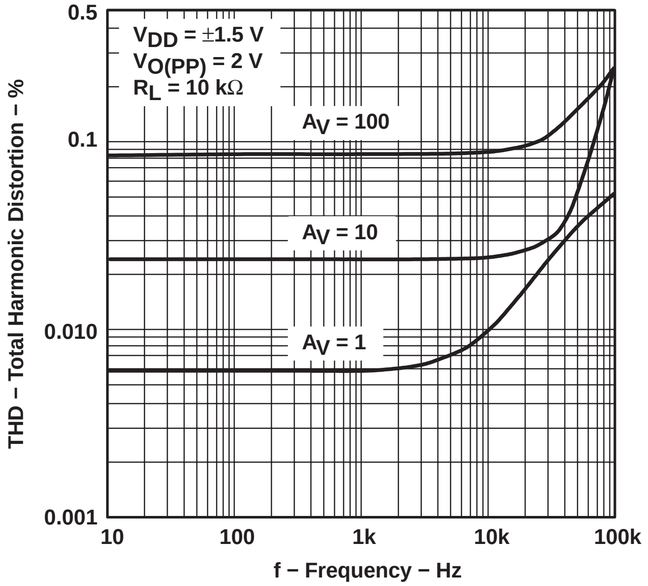


Figure 33

TOTAL HARMONIC DISTORTION vs FREQUENCY

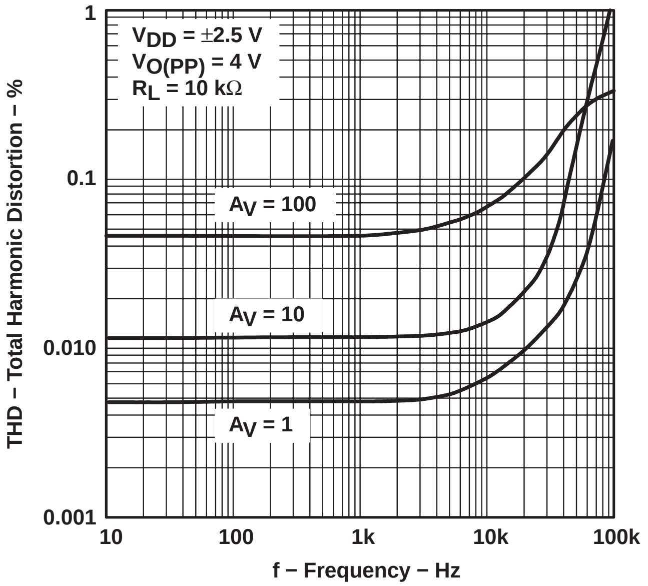


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK SIGNAL AMPLITUDE

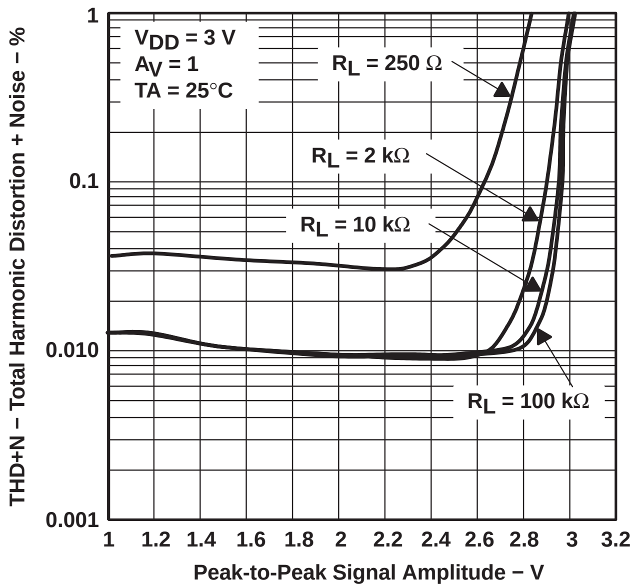


Figure 35

TOTAL HARMONIC DISTORTION PLUS NOISE vs PEAK-TO-PEAK SIGNAL AMPLITUDE

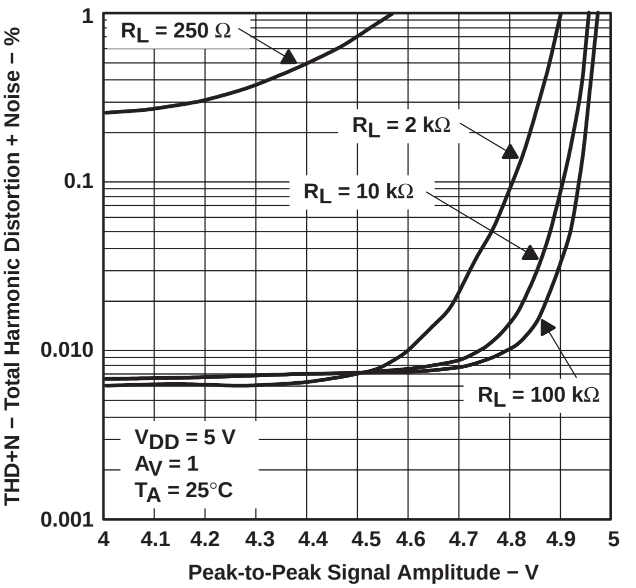


Figure 36

TYPICAL CHARACTERISTICS

PHASE MARGIN vs LOAD CAPACITANCE

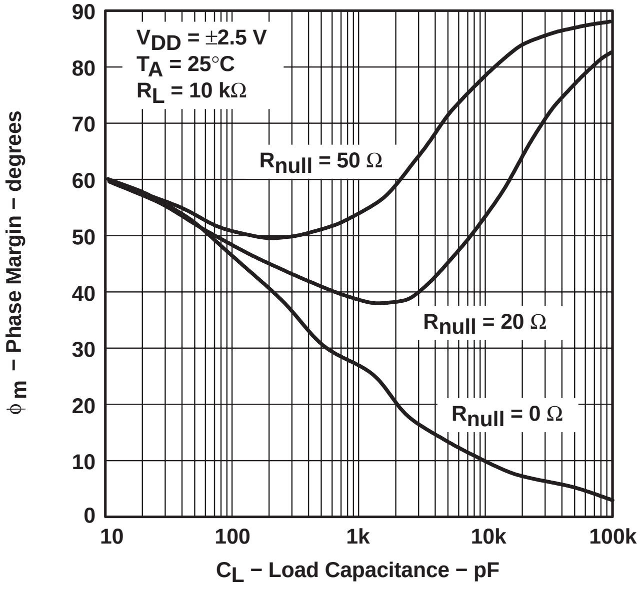


Figure 37

PHASE MARGIN vs FREE-AIR TEMPERATURE

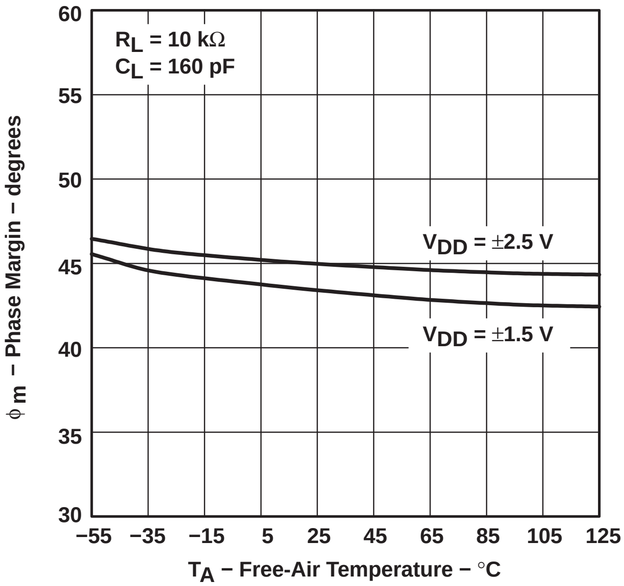


Figure 38

GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

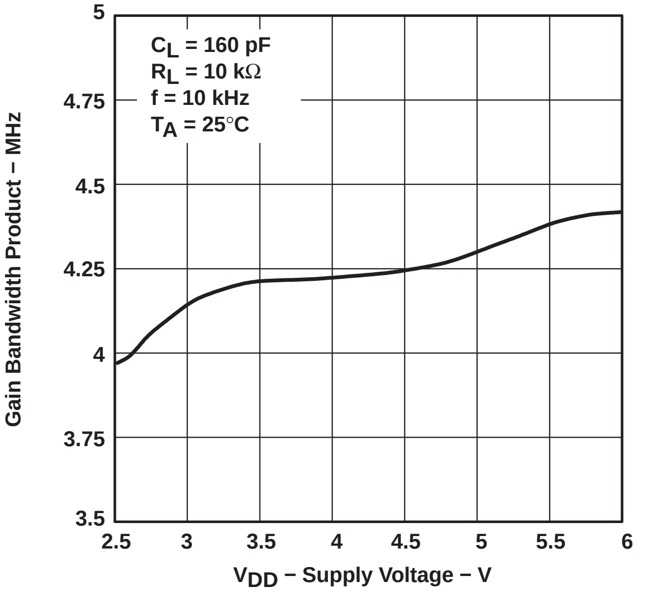


Figure 39

GAIN BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

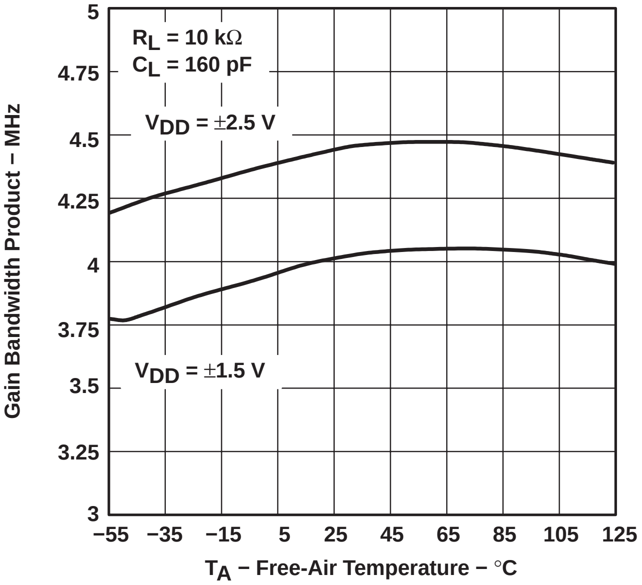


Figure 40

TYPICAL CHARACTERISTICS

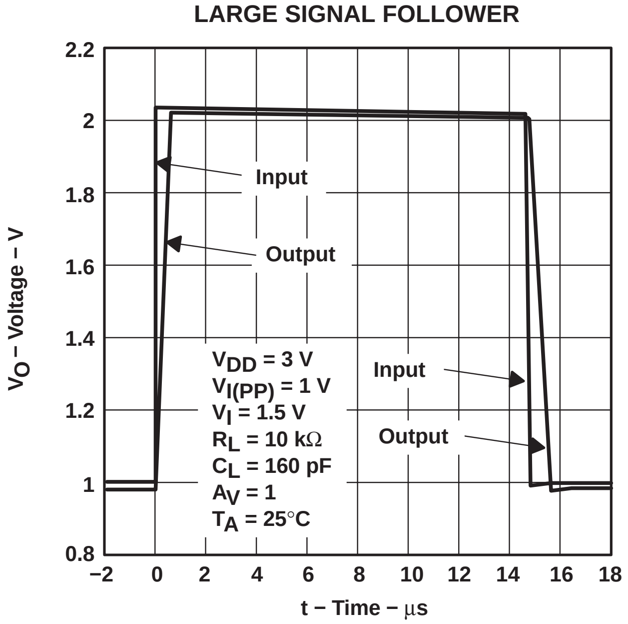


Figure 41

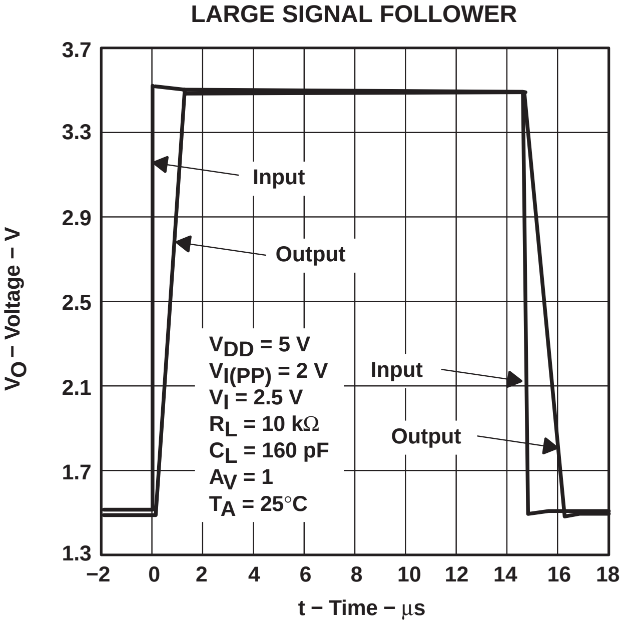


Figure 42

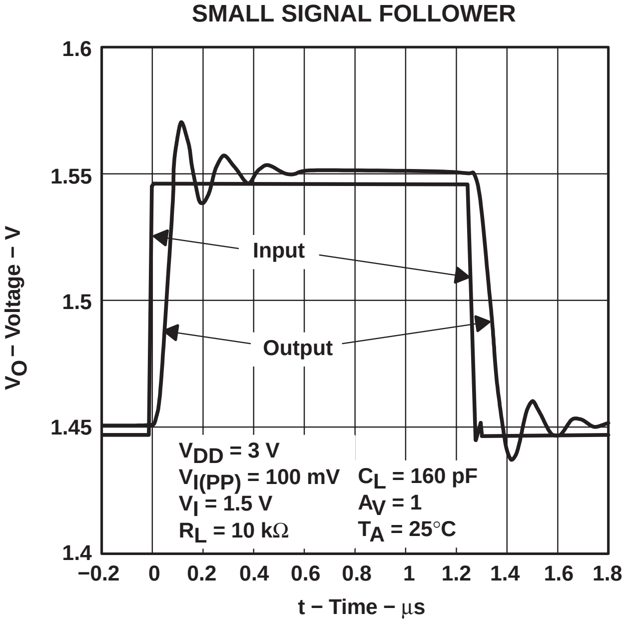


Figure 43

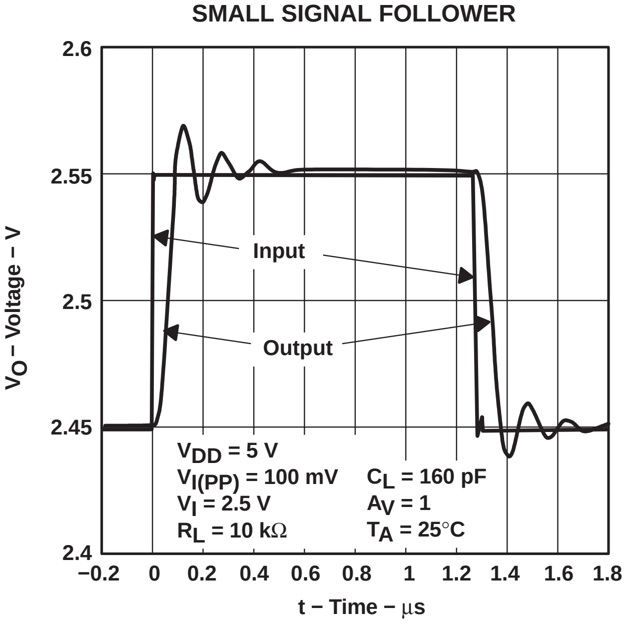


Figure 44

TYPICAL CHARACTERISTICS

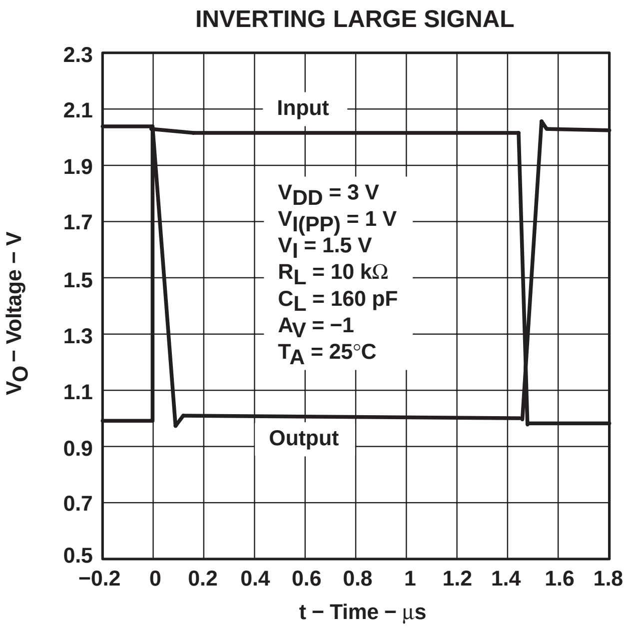


Figure 45

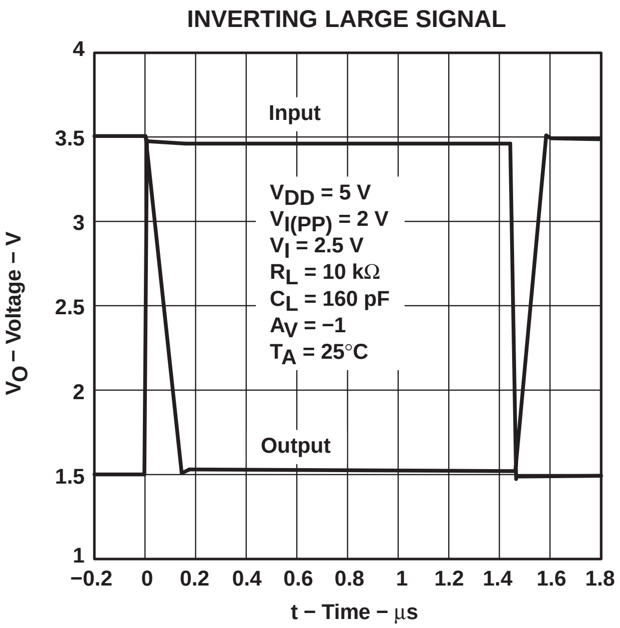


Figure 46

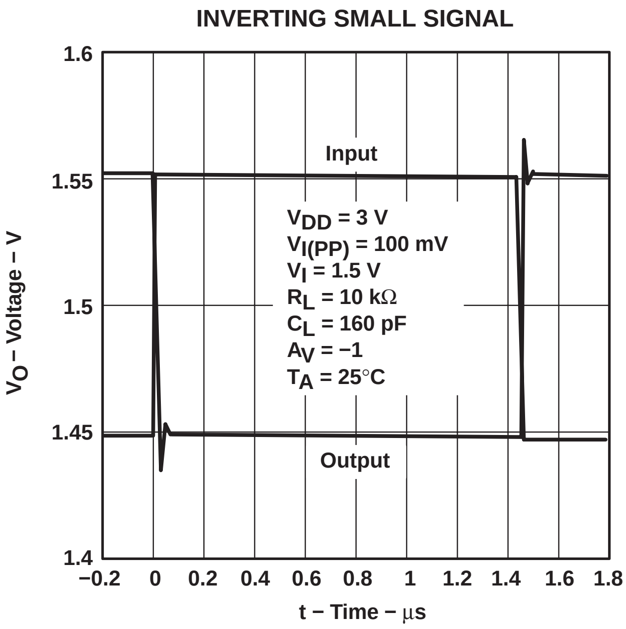


Figure 47

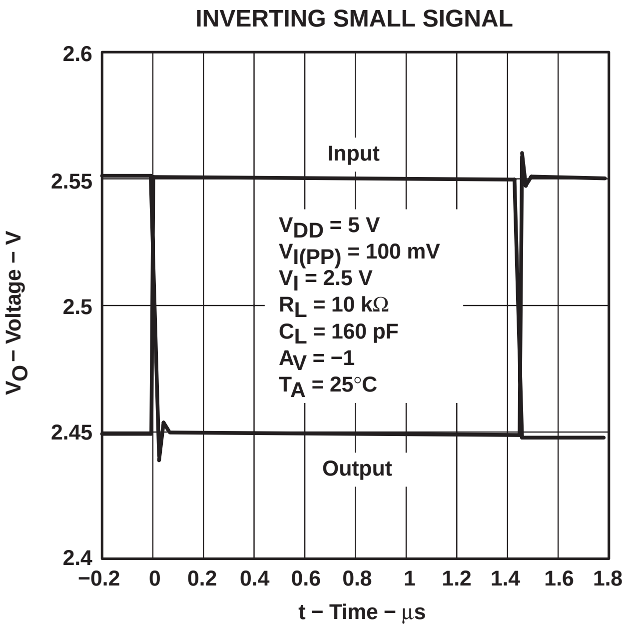


Figure 48

PARAMETER MEASUREMENT INFORMATION

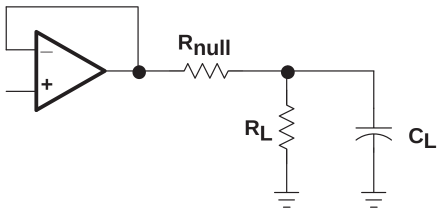


Figure 49

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device’s phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications.

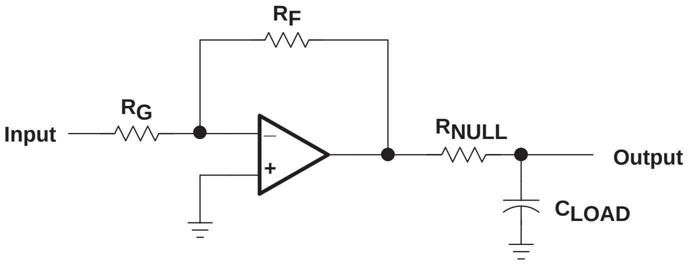
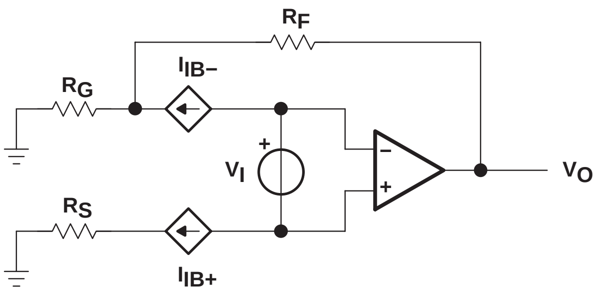


Figure 50. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



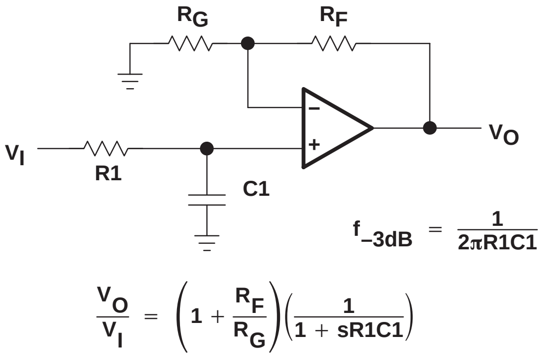
$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\,R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\,R_F$$

Figure 51. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 51).

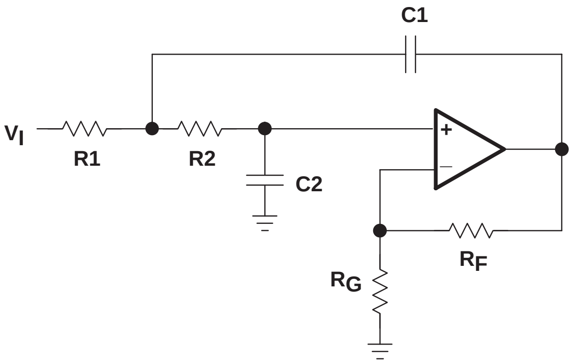


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 52. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 53. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

shutdown function

Two members of the TLV246x family (TLV2460/3) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 μA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier’s output with a shutdown pulse is shown in Figures 22, 23, 24, and 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

circuit layout considerations

To achieve the levels of high performance of the TLV246x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling − Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components − Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

general power dissipation considerations

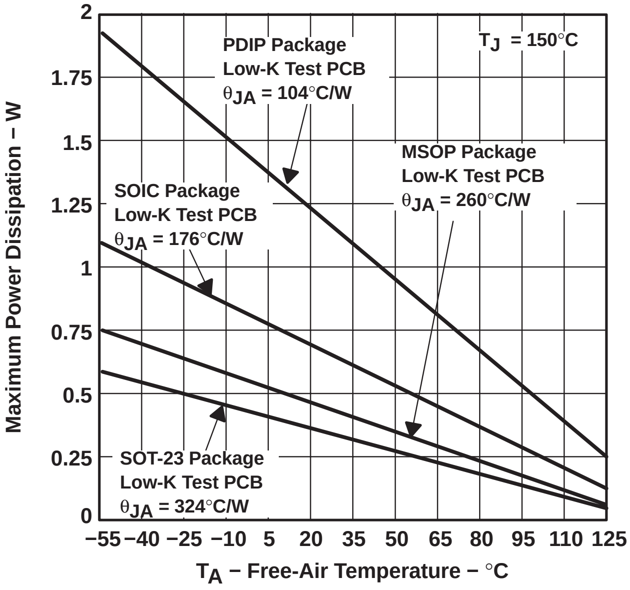
For a given θ_{JA}, the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS246x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 54. Maximum Power Dissipation vs Free-Air Temperature

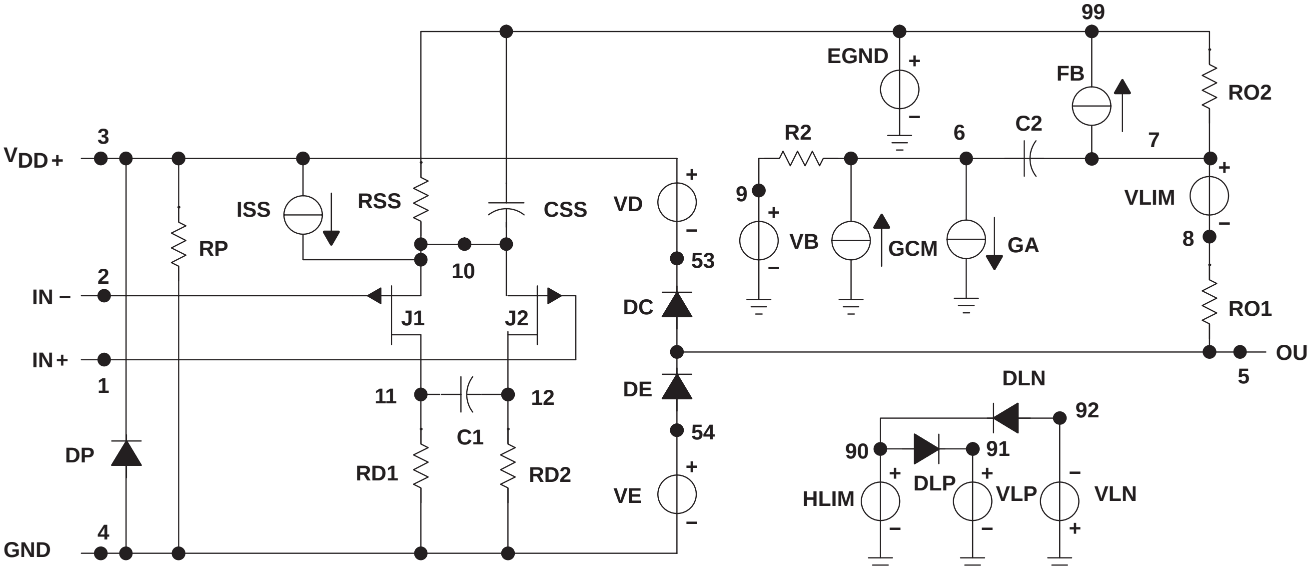
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 54 are generated using the TLV246x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Intergrated Circuit Operational Amplifiers”, *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).



```
.SUBCKT TLV246X   1 2 3 4 5
         C1       11     12     2.46034E−12
         C2       6      7      10.0000E−12
         CSS      10     99     443.21E−15
         DC       5      53     DY
         DE       54     5      DY
         DLP      90     91     DX
         DLN      92     90     DX
         DP       4      3      DX
         EGND     99     0      POLY (2) (3,0) (4,0) 0 .5 .5
         FB       7      99     POLY (5) VB VC VE VLP
         + VLN 0 21.600E6 −1E3 1E3 22E6 −22E6
         GA       6      0      11     12 345.26E−6
         GCM      0      6      10     99 15.4226E−9
         ISS      10     4      DC 18.850E−6
         HLIM     90     0      VLIM 1K
         J1       11     2      10 JX1
         J2       12     1      10 JX2
         R2       6      9      100.00E3
```

```
RD1      3      11     2.8964E3
RD2      3      12     2.8964E3
R01      8      5      5.6000
R02      7      99     6.2000
RP       3      4      8.9127
RSS      10     99     10.610E6
VB       9      0      DC 0
VC       3      53     DC .7836
VE       54     4      DC .7436
VLIM     7      8      DC 0
VLP      91     0      DC 117
VLN      0      92     DC 117
.MODEL DX D (IS=800.00E−18)
.MODEL DY D (IS=800.00E−18 Rs = 1m Cjo=10p)
.MODEL JX1 NJF (IS=1.0000E−12 BETA=6.3239E−3
+ VTO=−1)
.MODEL JX2 NJF (IS=1.0000E−12 BETA=6.3239E−3
+ VTO=−1)
.ENDS
```

Figure 55. Boyle Macromodels and Subcircuit

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macromodel information (continued)

```
.subckt TLV_246Y 1 2 3 4 5 6
        c1      11      12      2.4603E−12
        c2      72      7       10.000E−12
        css     10      99      443.21E−15
        dc      70      53      dy
        de      54      70      dy
        dlp     90      91      dx
        dln     92      90      dx
        dp      4       3       dx
        egnd    99      0       poly(2) (3,0) (4,0) 0 .5 .5
        fb      7       99      poly(5) vb vc ve vlp vln 0
21.600E6 −1E3 1E3 22E6 −22E6
        ga      72      0       11 12 345.26E−6
        gcm     0       72      10 99 15.422E−9
        iss     74      4       dc 18.850E−6
        hlim    90      0       vlim 1K
        j1      11      2       10 jx1
        j2      12      1       10 jx2
        r2      72      9       100.00E3
        rd1     3       11      2.8964E3
        rd2     3       12      2.8964E3
        ro1     8       70      5.6000
        ro2     7       99      6.2000
rp      3       71      8.9127
rss     10      99      10.610E6
rs1     6       4       1G
rs2     6       4       1G
rs3     6       4       1G
rs4     6       4       1G
s1      71      4       6  4  s1x
s2      70      5       6  4  s1x
s3      10      74      6  4  s1x
s4      74      4       6  4  s2x
vb      9       0       dc 0
vc      3       53      dc .7836
ve      54      4       dc .7436
vlim    7       8       dc 0
vlp     91      0       dc 117
vln     0       92      dc 117
.model dx D(Is=800.00E−18)
.model dy D(Is=800.00E−18 Rs=1m Cjo=10p)
.model jx1 NJF(Is=1.0000E−12 Beta=6.3239E−3 Vto=−1)
.model jx2 NJF(Is=1.0000E−12 Beta=6.3239E−3 Vto=−1)
.model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
.model s2x  VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
.ends
```

Figure 54. Boyle Macromodels and Subcircuit (Continued)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2462AMDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2462AM
TLV2462AMDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2462AM
TLV2462AQDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AE
TLV2462AQDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AE
TLV2464AMDREP	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	V2464AME
TLV2464AMDREP.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	V2464AME
TLV2464AMDREPG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	V2464AME
TLV2464AMPWREP	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2464AME
TLV2464AMPWREP.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2464AME
V62/03619-03XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2462AE
V62/03619-06XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2462AM
V62/03619-07YE	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	V2464AME
V62/03619-07ZE	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	2464AME

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV2462A-EP, TLV2462A-EP-Q, TLV2464A-EP :

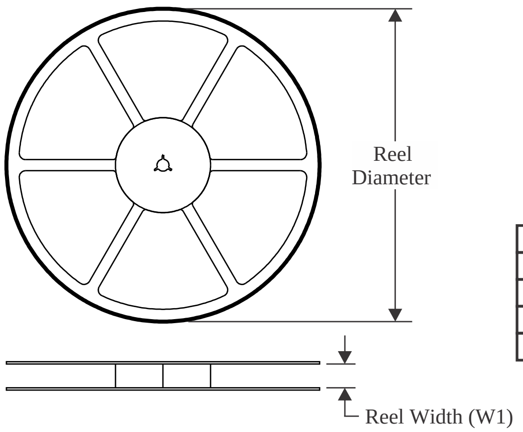
- Catalog : TLV2462A, TLV2464A
- Automotive : TLV2462A-Q1, TLV2462A-Q1, TLV2464A-Q1
- Enhanced Product : TLV2462A-EP
- Military : TLV2462AM

NOTE: Qualified Version Definitions:

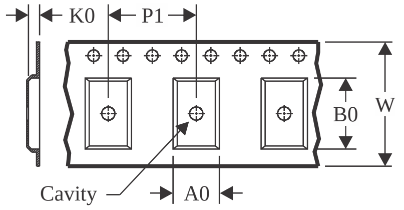
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

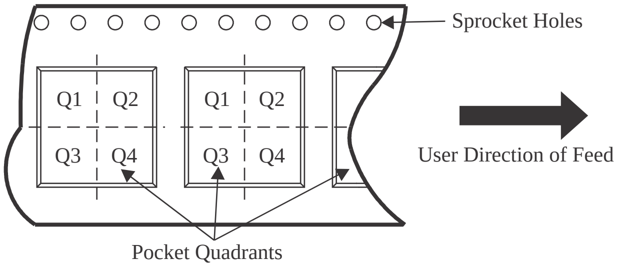


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

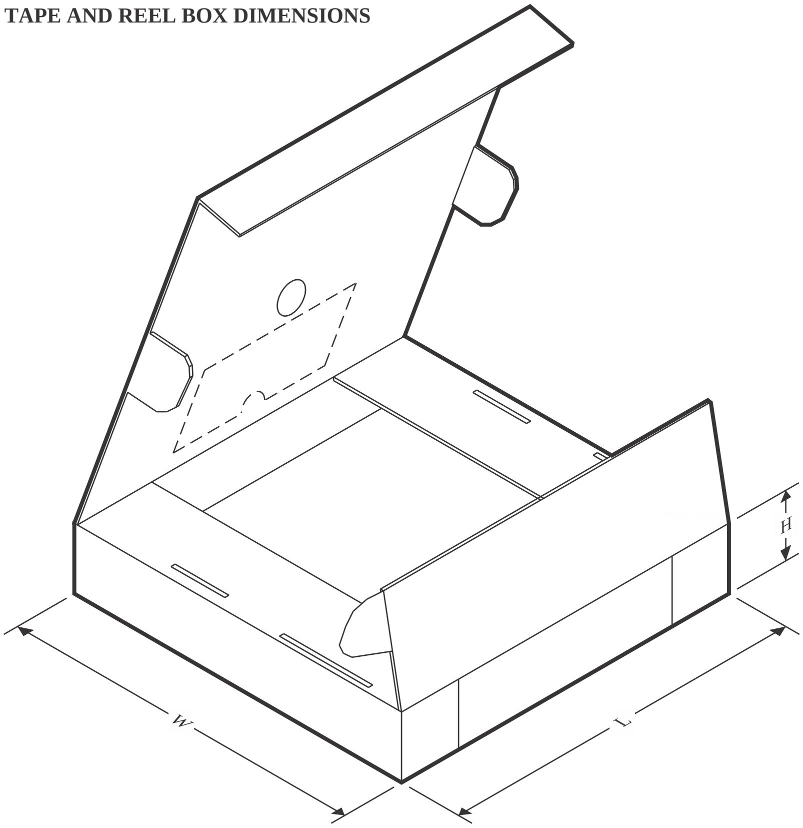
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2462AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2462AQDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2464AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2464AMPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2462AMDREP	SOIC	D	8	2500	353.0	353.0	32.0
TLV2462AQDREP	SOIC	D	8	2500	340.5	338.1	20.6
TLV2464AMDREP	SOIC	D	14	2500	353.0	353.0	32.0
TLV2464AMPWREP	TSSOP	PW	14	2000	353.0	353.0	32.0

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