TLVx365-Q1 Automotive, 50MHz, Zero-Crossover, Low-Distortion, High-CMRR, RRI/O, Single-Supply Operational Amplifiers

1 Features

- AEC-Q100 qualified
  - Temperature grade 1: –40°C to +125°C
- Gain bandwidth: 50MHz
- Zero-crossover distortion topology:
  - CMRR: 115dB (typical)
  - Rail-to-rail input and output
    - Input 100mV beyond supply rail
- Noise: 4.5nV/√Hz
- Slew rate: 27V/µs
- Fast settling: 0.2µs to 0.01%
- Precision:
  - Offset drift: 2.6µV/°C (maximum)
  - Input bias current: 20pA (maximum)
- Operating voltage: 2.2V to 5.5V

2 Applications

- HEV/EV DC/DC converter
- HEV/EV inverter and motor control
- HEV/EV onboard charger (OBC) and wireless charger
- e-Turbo/charger
- Automotive HVAC compressor module
- Gesturing

3 Description

The TLV365-Q1 and TLV2365-Q1 (TLVx365-Q1) devices are a family of zero-crossover, rail-to-rail input and output, CMOS operational amplifiers, optimized for low voltage and cost-sensitive applications. Low-noise (4.5nV/√Hz) and high-speed operation (50MHz gain bandwidth) make these devices an excellent choice for driving sampling analog-to-digital converters (ADCs) in applications such as low-side current sensing, audio, signal conditioning, and sensor amplification.

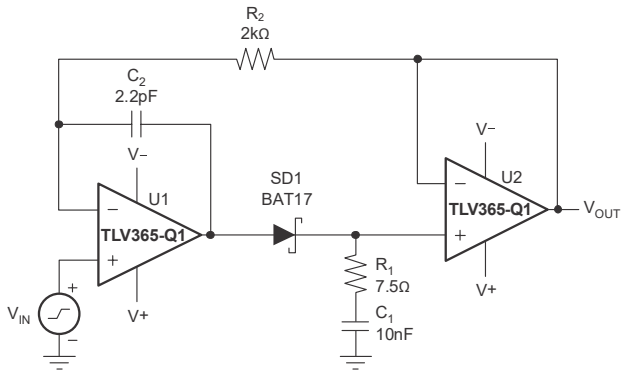
Special features include an excellent common-mode rejection ratio (CMRR), no input stage crossover distortion, high input impedance, and rail-to-rail input and output swing. The input common-mode range includes both the negative and positive supplies. The output voltage swings to within 12mV of the rails.

The TLVx365-Q1 are specified for operation from −40°C to +125°C.

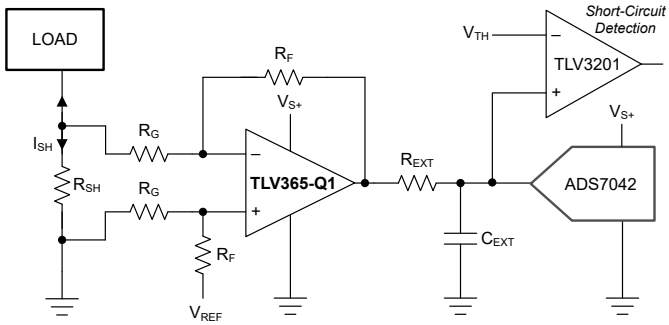
Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
TLV365-Q1	Single	DBV (SOT-23, 5)
TLV2365-Q1	Dual	D (SOIC, 8)
		DGK (VSSOP, 8)

(1) For more information, see Section 11.



Fast-Settling Peak Detector



TLVx365-Q1 for Current Sensing

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4 Device Comparison Table

DEVICE	INPUT TYPE	OFFSET DRIFT TYPICAL (µV/C)	MINIMUM GAIN STABLE (V/V)	I_Q/CHANNEL TYPICAL (mA)	GAIN BANDWIDTH (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)
TLVx365-Q1	CMOS	0.5	1	4.6	50	27	4.5
OPAx607-Q1	CMOS	0.3	6	0.9	50	24	3.8
OPAx365-Q1	CMOS	1	1	4.6	50	25	4.5

5 Pin Configuration and Functions

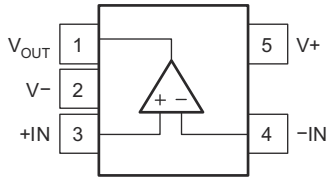


Figure 5-1. TLV365-Q1 DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions: TLV365-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	4	Input	Negative (inverting) input signal
+IN	3	Input	Positive (noninverting) input signal
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply
V_{OUT}	1	Output	Output

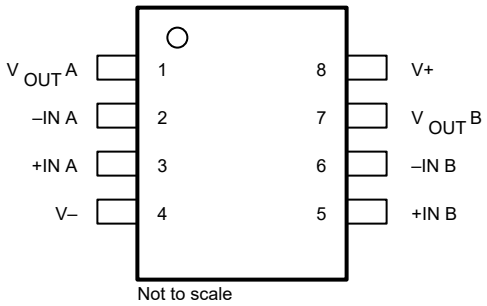


Figure 5-2. TLV2365-Q1 D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP (Top View)

Table 5-2. Pin Functions: TLV2365-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Negative (inverting) input signal, channel A
–IN B	6	Input	Negative (inverting) input signal, channel B
+IN A	3	Input	Positive (noninverting) input signal, channel A
+IN B	5	Input	Positive (noninverting) input signal, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply
V_{OUT}A	1	Output	Output, channel A
V_{OUT}B	7	Output	Output, channel B

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		6	V
V_I	Input voltage	(V–) – 0.5	(V+) + 0.5	V
V_{ID}	Differential input voltage		±5	V
I_I	Continuous input current(2)		±10	mA
I_{SC}	Output short-circuit(3)	Continuous		
T_A	Operating temperature	–40	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Limit the current of input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	2.2		5.5	V
T_A	Specified temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV365-Q1	TLV2365-Q1		UNIT
		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179	140	179	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78	89	71	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46	80	101	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19	28	13	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46	80	100	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at V_S = 2.2 V to 5.5 V, T_A = 25°C, R_L = 10 kΩ, V_{CM} = V_{OUT} = mid-supply, and gain = 1 V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			±0.4	±1.9	mV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C		±0.5	±2.6	µV/°C
PSRR	Power-supply rejection ratio	V_S = 2.2 V to 5.5 V, T_A = –40 to +125°C		100		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±5	±20	pA
		T_A = –40°C to +125°C		See Figure 6-5		
NOISE						
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz		5.4		μV_{PP}
e_N	Input voltage noise density	f = 500 kHz		4.5		nV/√Hz
i_n	Input current noise density	f = 1 kHz		5.8		fA/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 100 mV < V_{CM} < (V+) + 100 mV	100	115		dB
		T_A = –40°C to +125°C		110		
INPUT IMPEDANCE						
C_{IN}	Differential			5		pF
	Common-mode			1		
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	R_L = 10 kΩ, (V–) + 0.1 V < V_{OUT} < (V+) – 0.1 V	100	120		dB
		R_L = 10 kΩ, T_A = –40 to +125°C		113		
		R_L = 600 Ω, (V–) + 0.2 V < V_{OUT} < (V+) – 0.2 V	100	120		
		R_L = 600 Ω, T_A = –40 to +125°C		110		
	Phase margin			56		°
FREQUENCY RESPONSE (V_S = 5 V)						
GBW	Gain-bandwidth product			50		MHz
SR	Slew rate			27		V/µs
t_S	Settling time	0.1%, 4-V step		0.15		µs
		0.01%, 4-V step		0.2		
	Overdrive recovery time	V_{IN+} × gain > V_S		< 0.1		µs
THD + N	Total harmonic distortion + noise(1)	V_{OUT} = 4 V_{PP}, f = 1 kHz, R_L = 600 Ω		0.00025		%
	Channel-to-channel crosstalk (TLV2365-Q1 only)	V_{OUT} = 2 V_{PP}, f = 100 kHz		108		dBc
OUTPUT						
	Output voltage swing from supply rails				12	mV
		TLV365-Q1, T_A = –40°C to +125°C			12	
		TLV2365-Q1, T_A = –40°C to +125°C			15	
I_{SC}	Short-circuit current			±85		mA
	Capacitive load drive			See Figure 6-16		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 mA		40		Ω
POWER SUPPLY						
I_Q	Quiescent current per amplifier	I_O = 0 mA		4.6	5.8	mA
		I_O = 0 mA, T_A = –40°C to +125°C			6.3	

(1) Low-pass-filter bandwidth is 20 kHz for f = 1 kHz.

6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)

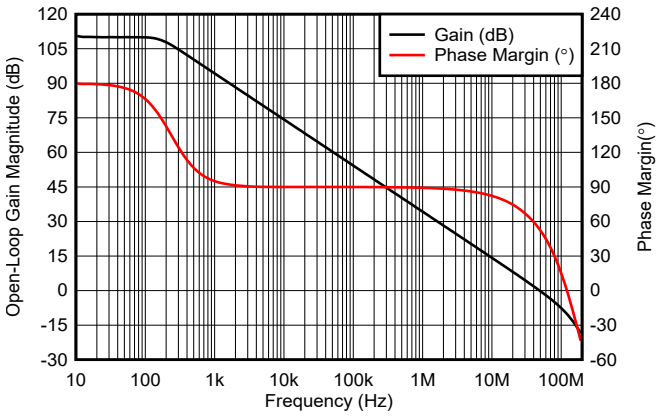


Figure 6-1. Open-Loop Gain and Phase vs Frequency

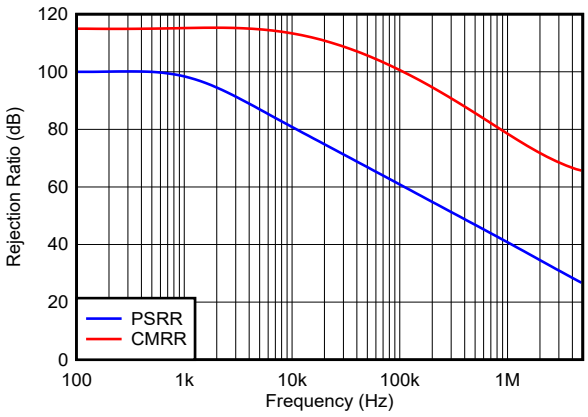
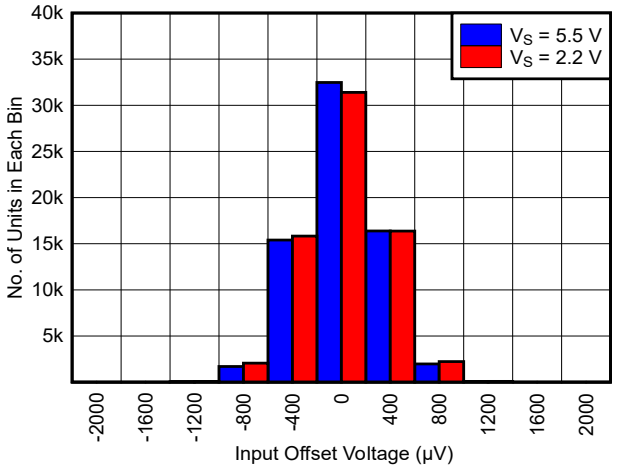
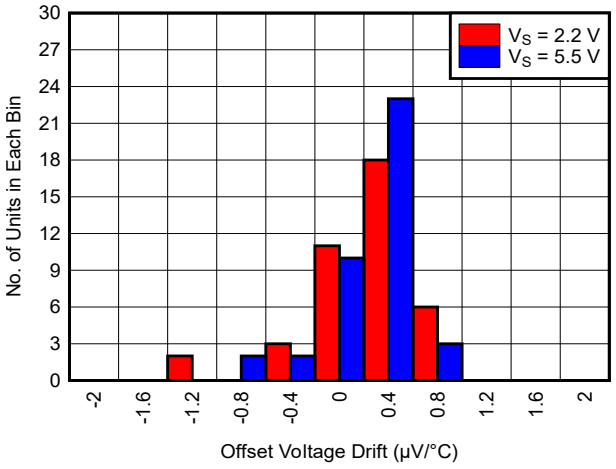


Figure 6-2. Power-Supply and Common-Mode Rejection Ratio



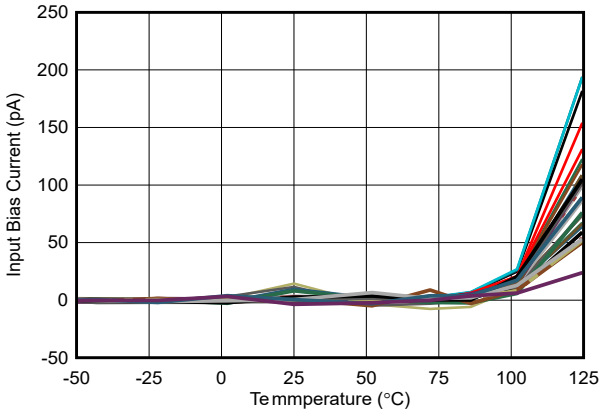
70000 units, µ = 9.3 µV, σ = 320 µV.

Figure 6-3. Offset Voltage Production Distribution



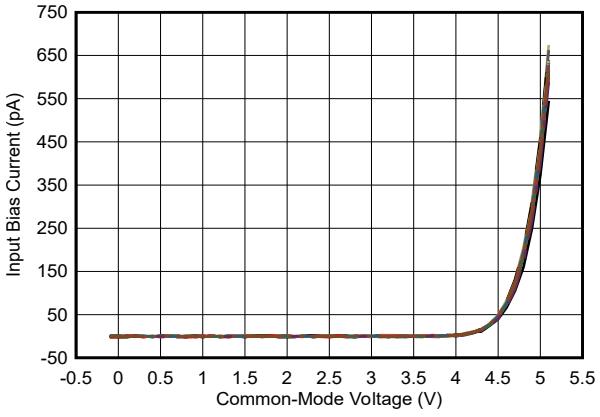
40 units, µ = 0.06 µV/°C, σ = 0.4 µV/°C

Figure 6-4. Offset Voltage Drift Distribution



40 units

Figure 6-5. Input Bias Current vs Temperature

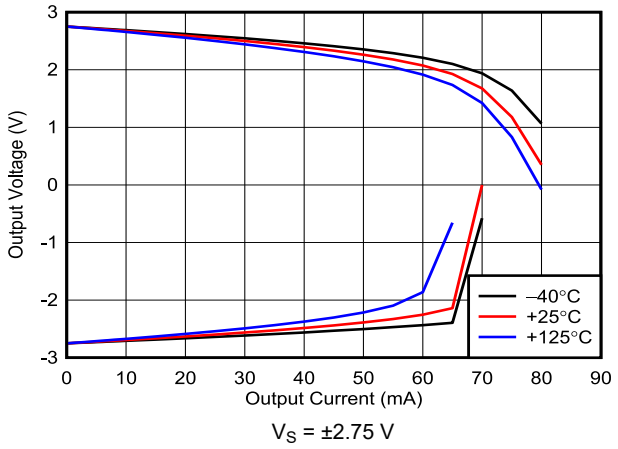


40 units

Figure 6-6. Input Bias Current vs Common-Mode Voltage

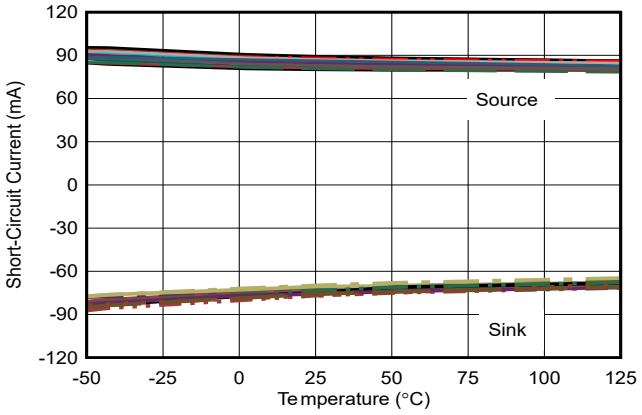
6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)



V_S = ±2.75 V

Figure 6-7. Output Voltage vs Output Current



20 units

Figure 6-8. Short-Circuit Current vs Temperature

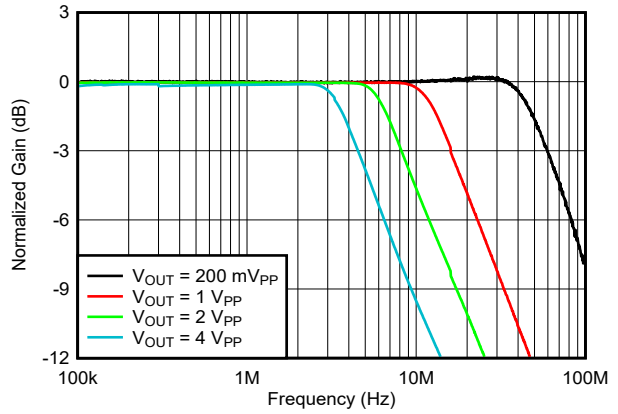


Figure 6-9. Frequency Response vs Output Voltage

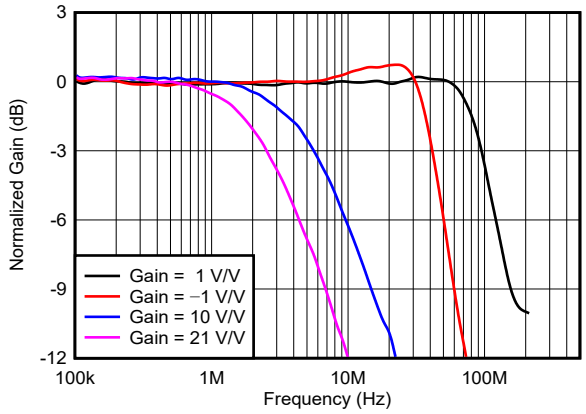


Figure 6-10. Small-Signal Frequency Response vs Gain

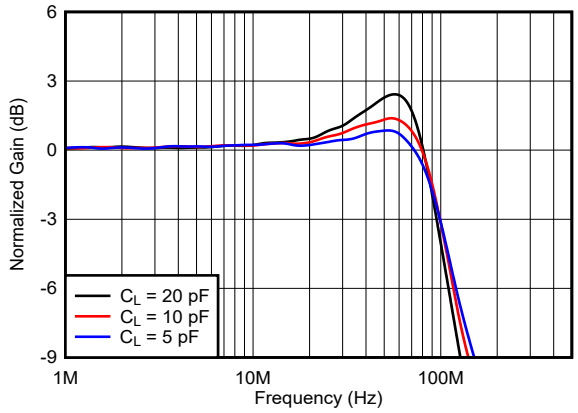
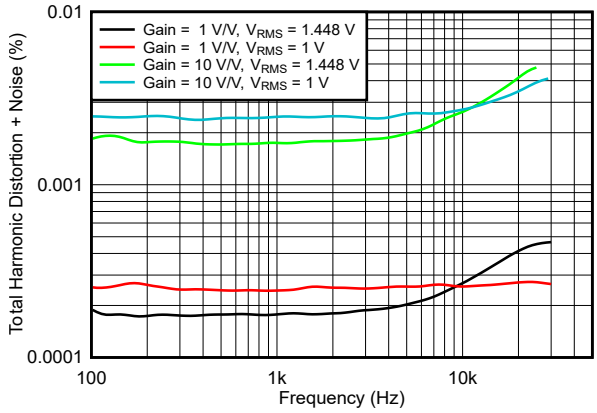


Figure 6-11. Small-Signal Response vs Capacitive Load



R_L = 600 Ω

Figure 6-12. Total Harmonic Distortion + Noise vs Frequency

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)

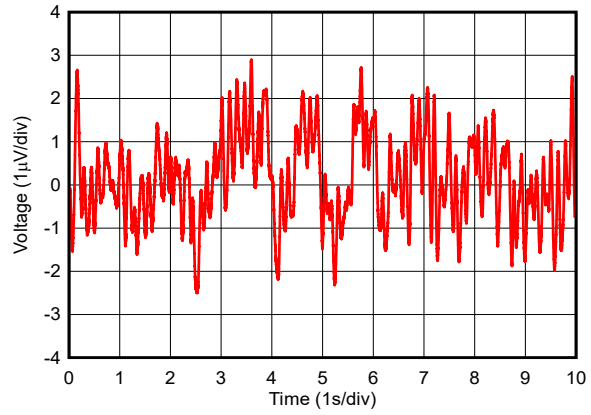


Figure 6-13. 0.1-Hz to 10-Hz Input Voltage Noise

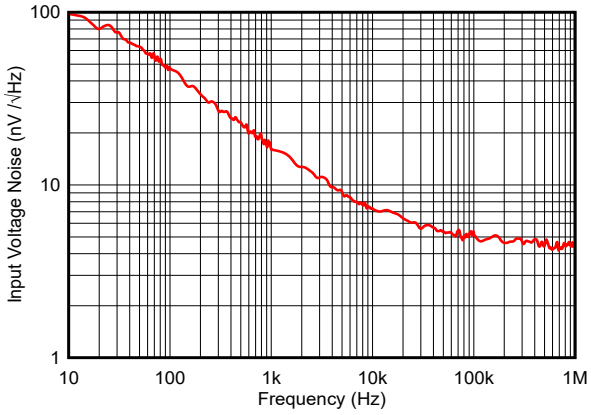


Figure 6-14. Input Voltage Noise Spectral Density

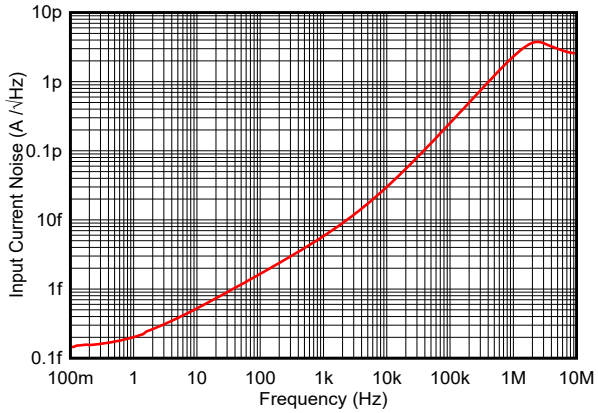
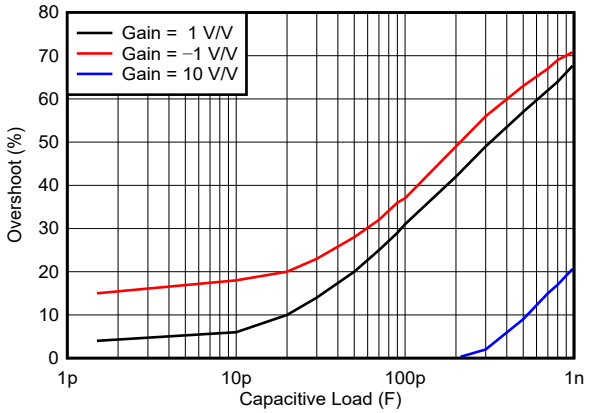


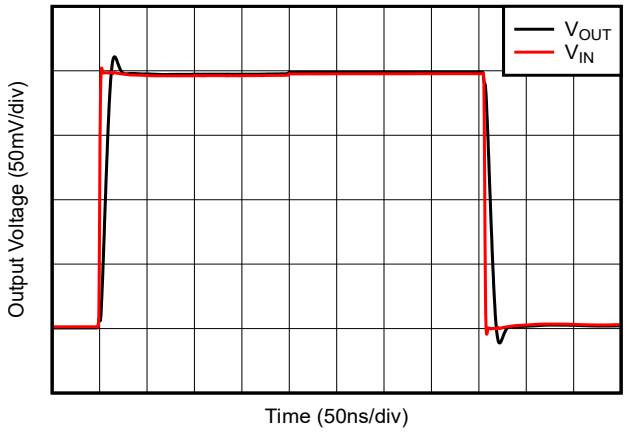
Figure 6-15. Input Current Noise Spectral Density



For gain ≠ 1 V/V, R_F = 1 kΩ

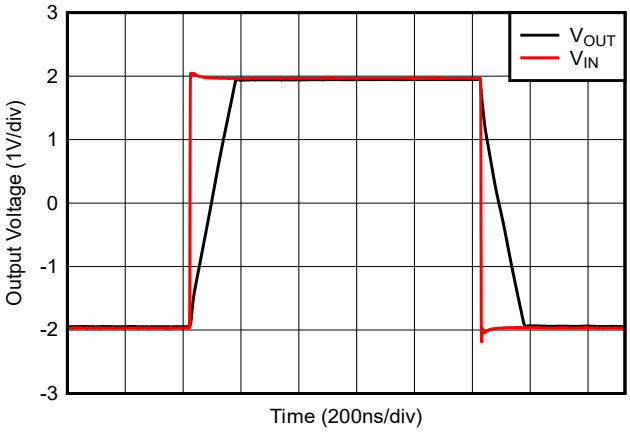
For gain = 1 V/V, R_F = 0 Ω

Figure 6-16. Overshoot vs Capacitive Load



R_L = 600 Ω

Figure 6-17. Small-Signal Step Response



R_L = 600 Ω

Figure 6-18. Large-Signal Step Response

6.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, R_L = 10 kΩ, and gain = 1 V/V (unless otherwise noted)

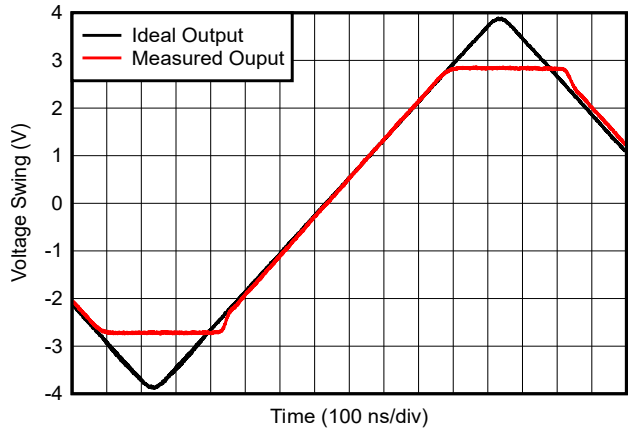


Figure 6-19. Overdrive Recovery

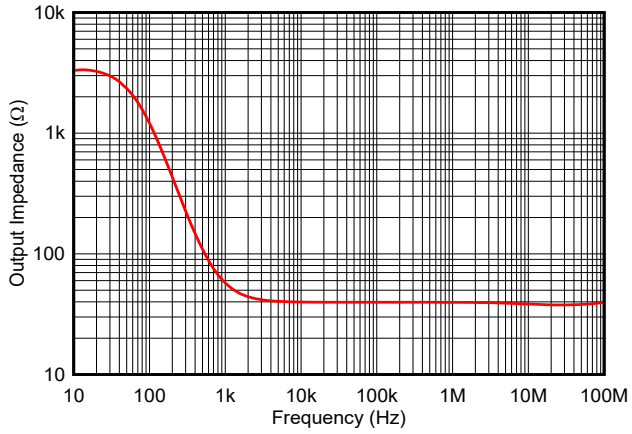


Figure 6-20. Open-Loop Output Impedance

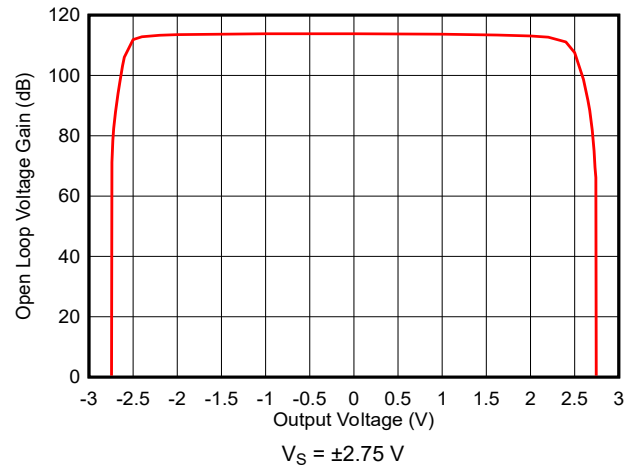


Figure 6-21. Open Loop Voltage Gain vs Output Voltage

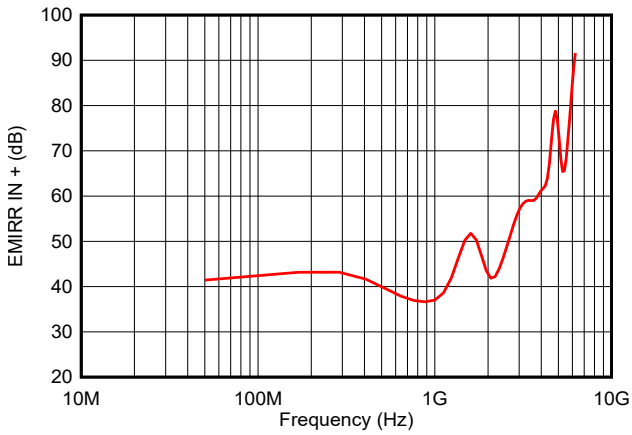


Figure 6-22. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

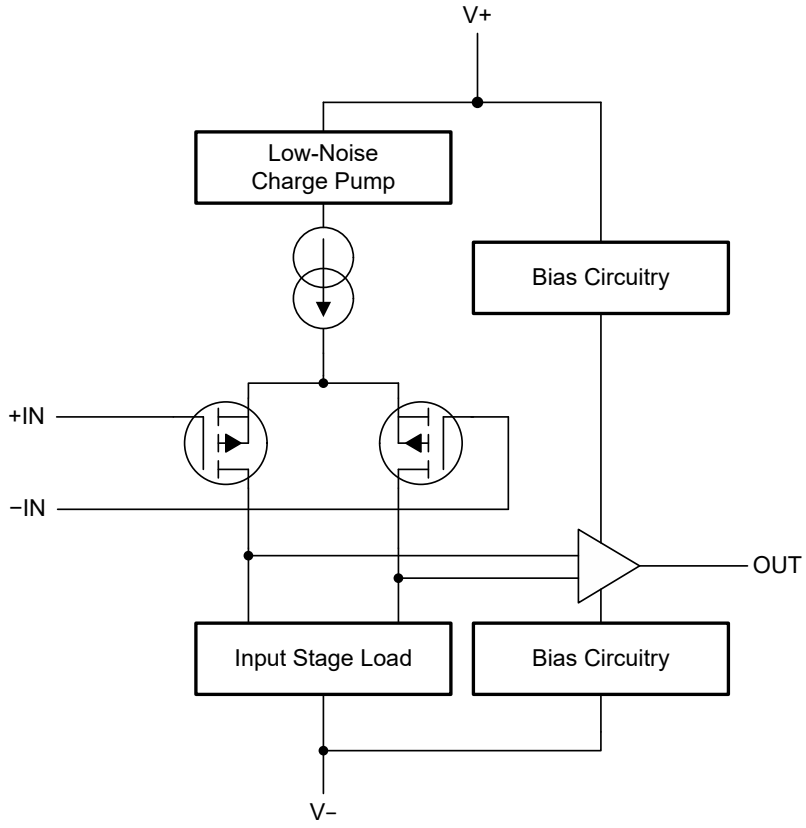
7 Detailed Description

7.1 Overview

The TLVx365-Q1 series of operational amplifiers feature rail-to-rail input and output, wide-bandwidth making these devices an excellent choice for driving ADCs. Other typical applications include signal conditioning, low-side current sensing, signal buffering and sensor amplification. The TLVx365-Q1 operates with either a single supply or dual supplies.

Furthermore, the TLVx365-Q1 amplifier parameters are fully specified from 2.2 V to 5.5 V. Many of the specifications apply from −40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Rail-to-Rail Input

The TLVx365-Q1 product family features true rail-to-rail input operation, with supply voltages as low as ±1.1 V (2.2 V). A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary stage operational amplifiers. As shown in Figure 7-1, this topology also allows the TLVx365-Q1 to provide excellent common-mode performance over the entire input range, which extends 100 mV beyond both power-supply rails. When driving ADCs, the highly linear V_{CM} range of the TLVx365-Q1 makes sure that the system linearity performance is not compromised. For a simplified schematic illustrating the rail-to-rail input circuitry, see Section 7.2.

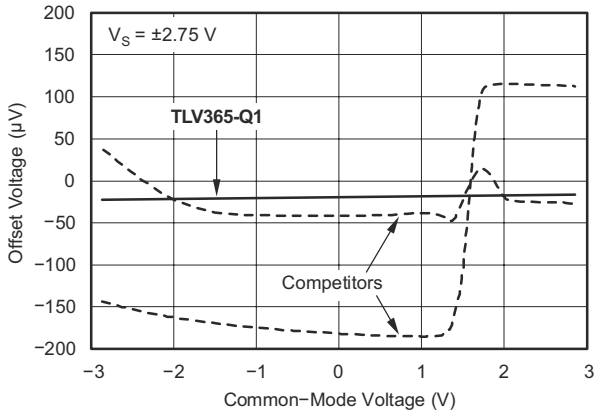


Figure 7-1. TLVx365-Q1 Linear Offset Over the Entire Common-Mode Range

7.3.2 Input and ESD Protection

Figure 7-2 shows that the TLVx365-Q1 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection if the current is limited to 10 mA; see also Section 6.1. Figure 7-3 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input; the resistor must be kept to the minimum value in noise-sensitive applications.

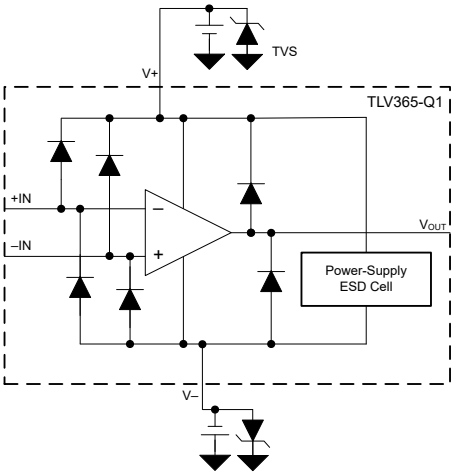


Figure 7-2. ESD Protection Scheme

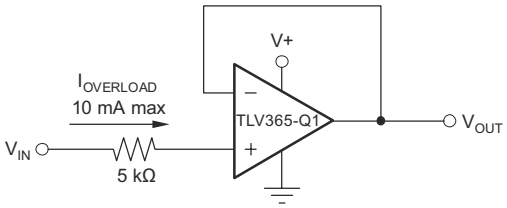


Figure 7-3. Input Current Protection

7.3.3 Driving Capacitive Loads

The TLVx365-Q1 can be used in applications where driving a capacitive load is required. An op amp in a unity-gain, buffer configuration and driving a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher gain. The capacitive load, in conjunction with the op-amp output impedance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. This degradation is observed in the increase in peaking with increased capacitive load in Figure 6-16.

Improving Capacitive Load Drive shows one technique to increase the capacitive-load drive capability of the amplifier operating in unity gain is to insert a small resistor, R_{ISO}, in series with the output. This resistor significantly reduces the overshoot and ringing associated with capacitive loads.

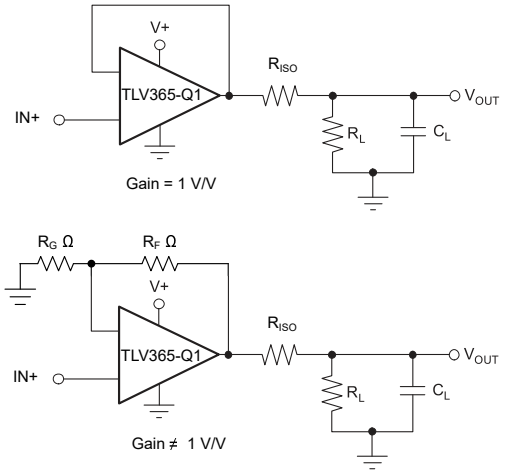
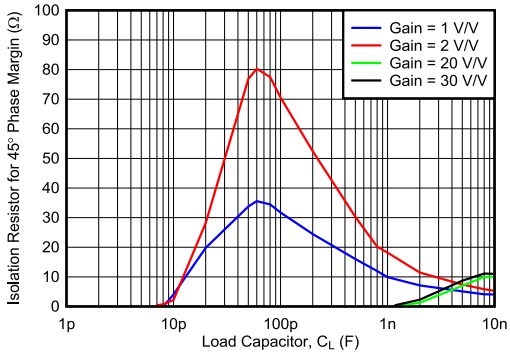


Figure 7-4. Improving Capacitive Load Drive

A possible drawback of this technique is the voltage divider created with the added series resistor (R_{ISO}) and any resistor (R_L) connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that also reduces the output swing. The error contributed by the voltage divider can be insignificant. For instance, with a load resistance of R_L = 10 kΩ and R_{ISO} = 20 Ω, the gain error is only approximately 0.2%.

The following figure shows the recommended isolation resistor (R_{ISO}) to be connected at the output of TLVx365-Q1 for different capacitive loads. The TLVx365-Q1 can drive higher capacitive loads without the need of isolation resistors at higher gains.



For gain > 1 V/V, R_F = 1 kΩ

For gain = 1 V/V, R_F = 0 Ω

Figure 7-5. Recommended Isolation Resistor vs Capacitive Load

7.3.4 Active Filter

The TLVx365-Q1 is an excellent choice for active filter applications requiring a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 7-6 shows a 500-kHz, second-order, low-pass filter using a multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, rolloff is −40 dB/dec. The Butterworth response is designed for applications requiring predictable gain characteristics, such as the antialiasing filter used ahead of an ADC.

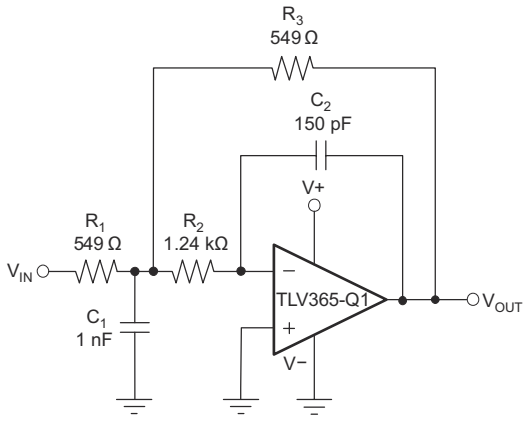


Figure 7-6. Second-Order Butterworth, 500-kHz Low-Pass Filter

When considering the MFB filter, the output is inverted, relative to the input. If this inversion is not desired, then a noninverting output can be achieved through one of these options:

- add an inverting amplifier
- add an additional second-order MFB stage
- use a noninverting filter topology, such as the Sallen-Key

Figure 7-7 shows the Sallen-Key topology.

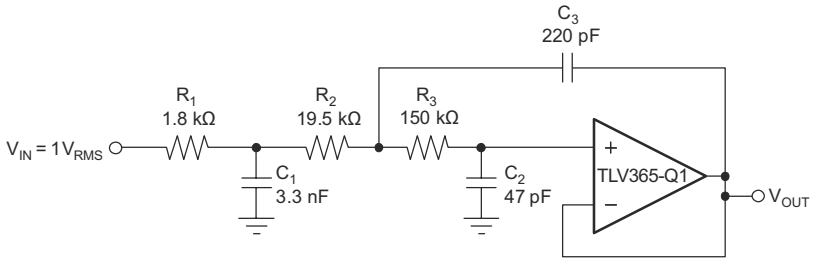


Figure 7-7. Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

7.4 Device Functional Modes

The TLVx365-Q1 have a single-mode of operation. The devices can be configured with unipolar supplies, split and symmetrical bipolar supplies (±2.5 V, for example), or split and asymmetrical supplies (+4 V and –1 V, for example). There are no power-down or low-power modes in the TLVx365-Q1.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLVx365-Q1 offer outstanding dc and ac performance. These devices operate with up to a 5.5-V power supply, offer an ultra-low input bias current and a 50-MHz bandwidth with true rail-to-rail input capability.

8.1.1 Overdrive Recovery Performance

The TLVx365-Q1 family exhibits excellent overdrive recovery when the output is driven well beyond the V+ or V– supplies. When configured in a low-side current-sensing configuration (see Figure 8-1), the output of the op amp (TLVx365-Q1) is often driven to or less than ground as a result of ground bounce at the power ground or the ≤ 0-A current being measured across shunt resistance R_{SH}. The TLVx365-Q1 has the ability to recover from an overdrive event in < 100 ns. Figure 8-2 shows the comparison of the overdrive recovery performance of TLVx365-Q1 and other popular op amps in the same category.

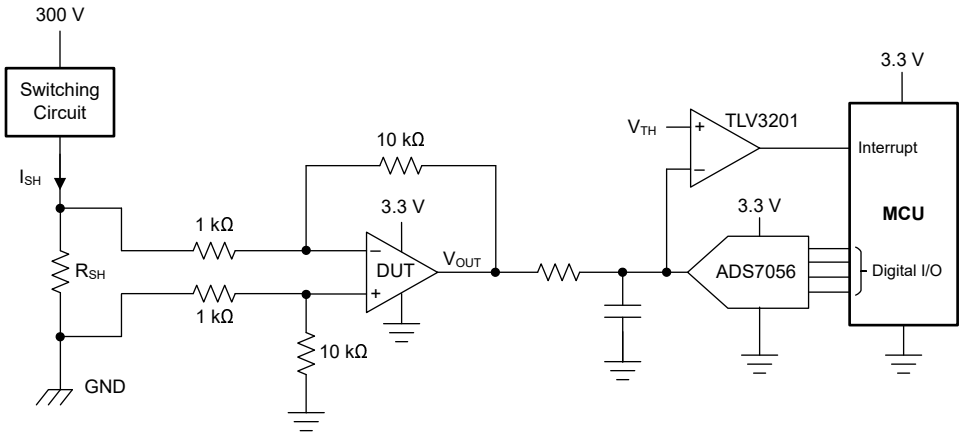
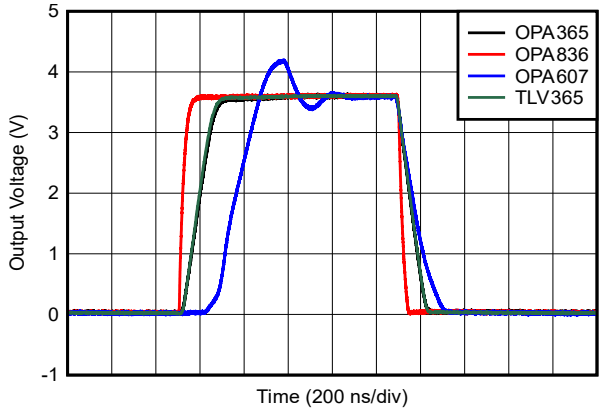


Figure 8-1. Low-Side Current-Sensing Application Circuit



Gain = 10 V/V, V_{OUT} driven to (V–) – 1 V

Figure 8-2. TLVx365-Q1 Overdrive Recovery

8.1.2 Achieving an Output Level of Zero Volts

Certain single-supply applications require the op-amp output to swing from 0 V to a positive full-scale voltage and have high accuracy. An example is an op amp employed to drive a single-supply ADC having an input range from 0 V to 3.3 V. Rail-to-rail output amplifiers with very light output loading can achieve an output level within few millivolts of 0 V (or V+ at the high end), but not true 0 V. Furthermore, the deviation from 0 V only becomes greater as the required load current increases. This increased deviation is a result of limitations of the CMOS output stage.

When a pulldown resistor is connected from the amplifier output to a negative voltage source, the TLVx365-Q1 can achieve an output level of 0 V, and even a few millivolts below 0 V. Figure 8-3 shows a circuit using this technique.

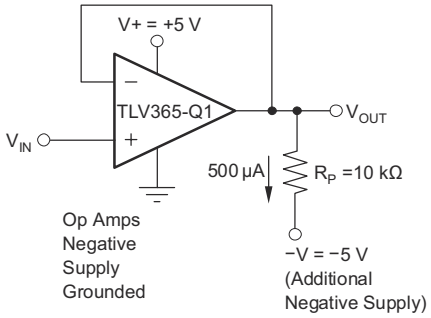


Figure 8-3. Swing-to-Ground

A pulldown current of approximately 500 µA is required when TLVx365-Q1 is connected as a unity-gain buffer. Pulldown resistor R_L is calculated from $R_L = [(V_O - V_{NEG}) / (500\ \mu A)]$.

Figure 8-4 shows the offset voltage vs output swing.

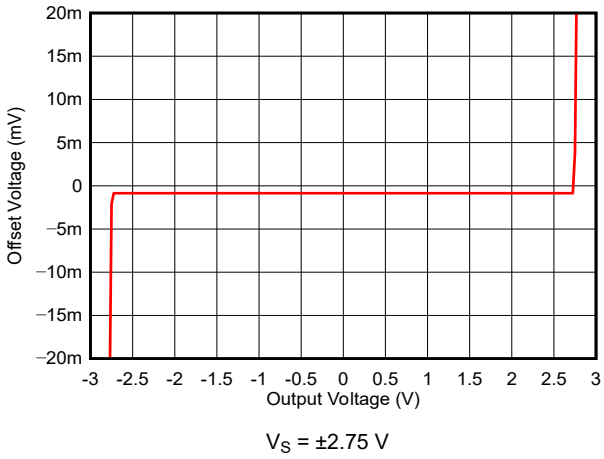


Figure 8-4. Offset Voltage vs Output Swing

8.2 Typical Applications

8.2.1 Second-Order Low-Pass Filter

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The TLVx365-Q1 is designed to construct high-speed, high-precision active filters. Figure 8-5 shows a second-order low-pass filter commonly encountered in signal processing applications.

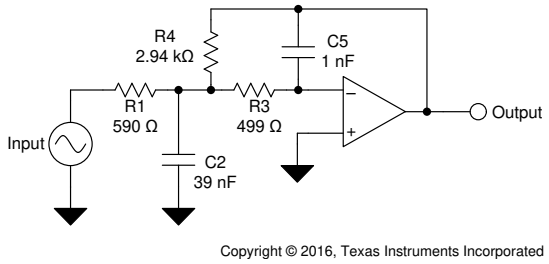


Figure 8-5. Second-Order Low-Pass Filter

8.2.1.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order, Chebyshev filter response with 3-dB gain peaking in the pass band

8.2.1.2 Detailed Design Procedure

Figure 8-5 shows the infinite-gain, multiple-feedback circuit for a low-pass network function. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, use Equation 2 to calculate the gain at dc and the low-pass cutoff frequency.

$$\text{Gain} = \frac{R_4}{R_1}$$
$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

8.2.1.3 Application Curve

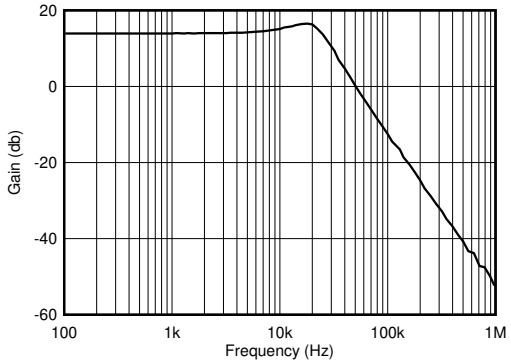


Figure 8-6. TLVx365-Q1 Second-Order 25 kHz, Chebyshev, Low-Pass Filter

8.2.2 ADC Driver and Reference Buffer

Figure 8-7 shows the use of a TLVx365-Q1 op amp as a SAR ADC input and reference pin driver. Sensors, which are used for interfacing with the physical environment, exhibit high output impedance and cannot drive SAR ADC inputs directly. The TLVx365-Q1 devices exhibit a very low-input bias current of 20 pA (maximum), and therefore do not load these high-output impedance sensors. A wide-GBW amplifier connected to the output of these sensors is needed to charge the switching capacitors at the SAR ADC input and to settle fast, to the required accuracy, within the given acquisition time.

The ADC core draws transient current from the reference input during the conversion (digitization) phase, which must be driven with a wide-GBW amplifier to offer fast settling and maintain a stable reference voltage for excellent digitization performance. The TLVx365-Q1 reference buffer is used in a composite loop with the OPA378 precision amplifier because of limitations in precision performance of wide-GBW amplifiers. The precision amplifier maintains low-offset output, whereas the TLVx365-Q1 provide the output drive and fast-settling performance.

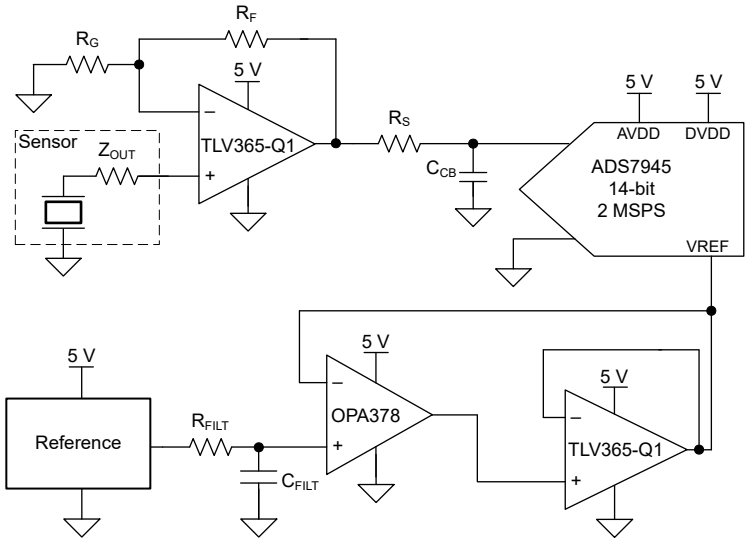


Figure 8-7. TLVx365-Q1 as a SAR ADC Driver

8.3 Power Supply Recommendations

The TLVx365-Q1 family can be configured with unipolar supplies, split and symmetrical bipolar supplies (±2.5 V, for example), or split and asymmetrical supplies (+4 V and –1 V, for example). The maximum permissible voltage, V_S, is 6 V.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including the following guidelines:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole or through the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - The TLVx365-Q1 is capable of peak output current (in excess of 50 mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors, such as 1-µF solid tantalum capacitors, can improve dynamic performance in these applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Figure 8-8 shows that keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

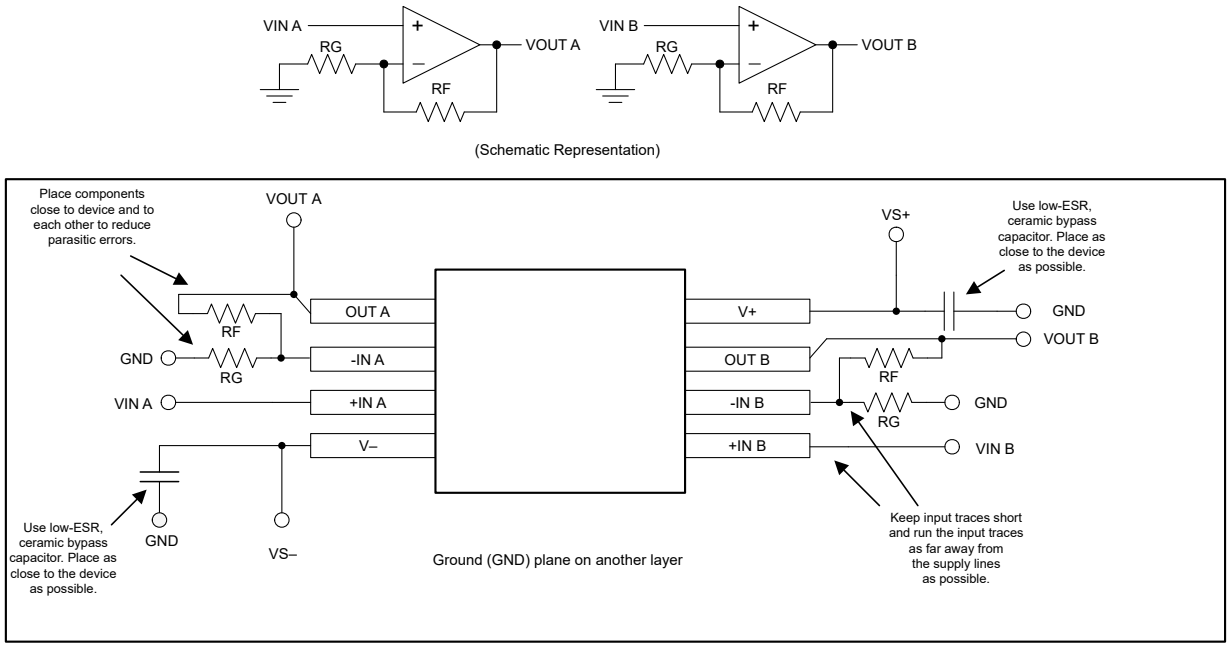


Figure 8-8. Layout Recommendation for TLV2365-Q1 SOIC Package

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.1.1.3 DIP-Adapter-EVM

Speed up your op amp prototyping and testing with the DIP-Adapter-EVM, which provides a fast, easy and inexpensive way to interface with small, surface-mount devices. Connect any supported op amp using the included Samtec terminal strips or wire them directly to existing circuits. The DIP-Adapter-EVM kit supports the following industry-standard packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT-23-6, SOT-23-5 and SOT-23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6).

9.1.1.4 DIYAMP-EVM

The DIYAMP-EVM is a unique evaluation module (EVM) that provides real-world amplifier circuits, enabling the user to quickly evaluate design concepts and verify simulations. This EVM is available in three industry-standard packages (SC70, SOT23, and SOIC) and 12 popular amplifier configurations, including amplifiers, filters, stability compensation, and comparator configurations for both single and dual supplies.

9.1.1.5 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

9.1.1.6 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

9.2 Documentation Support

9.2.1 Related Documentation

The following documents are relevant to using the TLVx365-Q1, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- Texas Instruments, *FilterPro™ software* user's guide
- Texas Instruments, *Low Power Input and Reference Driver Circuit for ADS8318 and ADS8319* application report
- Texas Instruments, *Op Amp Performance Analysis* application bulletin
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application bulletin
- Texas Instruments, *The Best of Baker's Best – Amplifiers eBook* reference book

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2024) to Revision C (March 2025)	Page
• Changed TLV2365-Q1 status from advanced information (preview) to production data (active)	1

Changes from Revision A (December 2023) to Revision B (September 2024)	Page
• Changed TLV2365-Q1 device status from preview to advanced information (preview with samples)	1
• Added TLV2365-Q1 advanced information DGK package	1
• Added *Thermal Information* for DGK package	4

Changes from Revision * (June 2023) to Revision A (December 2023)	Page
• Changed data sheet status from advanced mix to production mix	1
• Changed status of TLV365-Q1 in DBV package from advanced information (preview) to production data (active)	1

11 Mechanical, Packaging, and Orderable Information

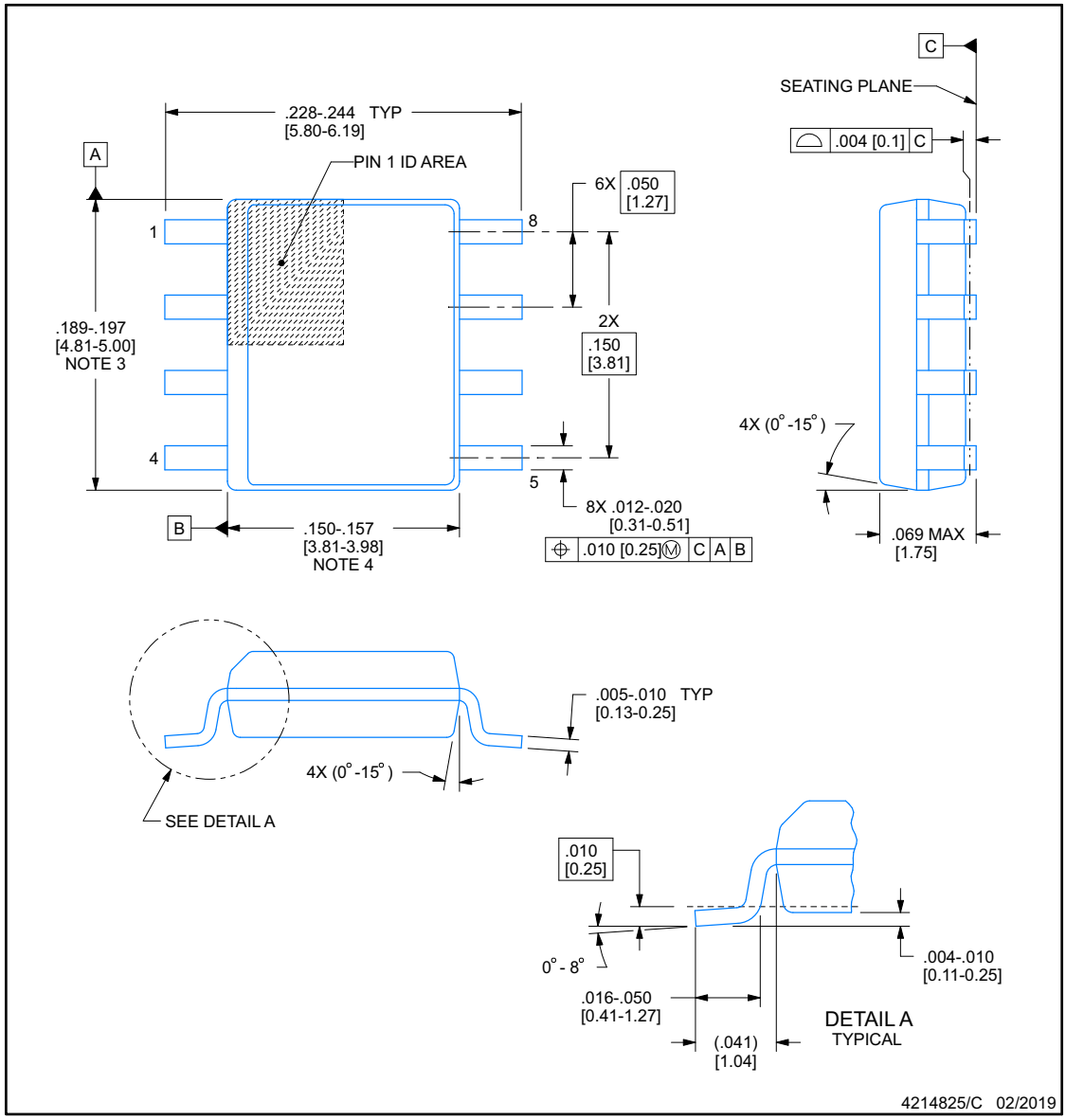
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

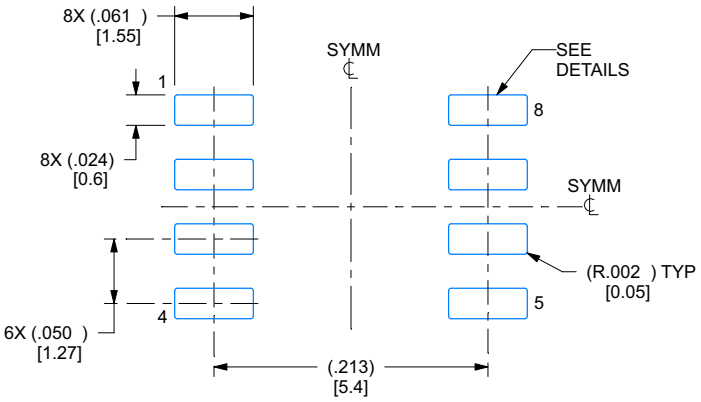
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

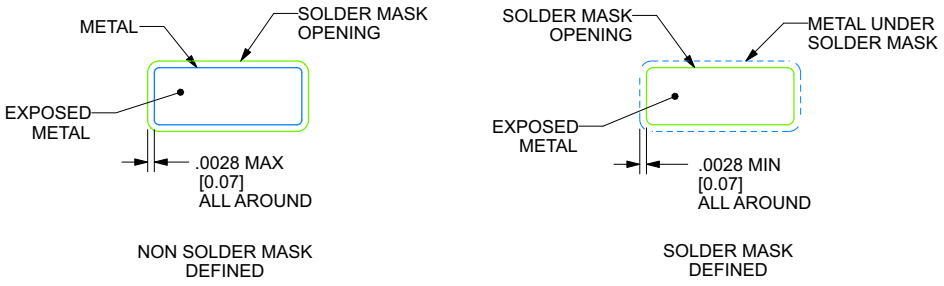
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

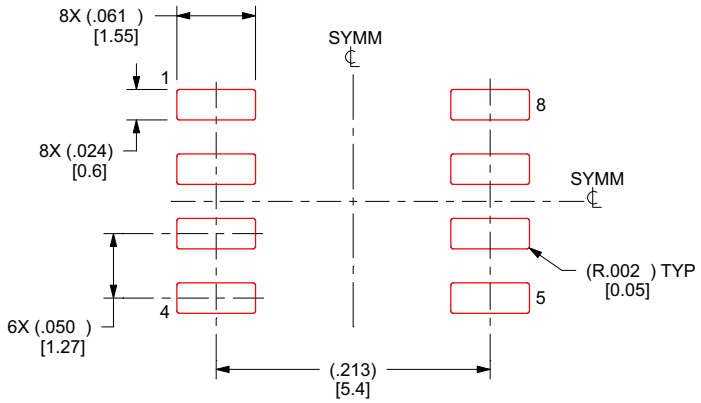
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2365QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q65
TLV2365QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2Q65
TLV2365QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2365Q
TLV2365QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T2365Q
TLV365QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	Q365
TLV365QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	Q365

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV2365-Q1, TLV365-Q1 :

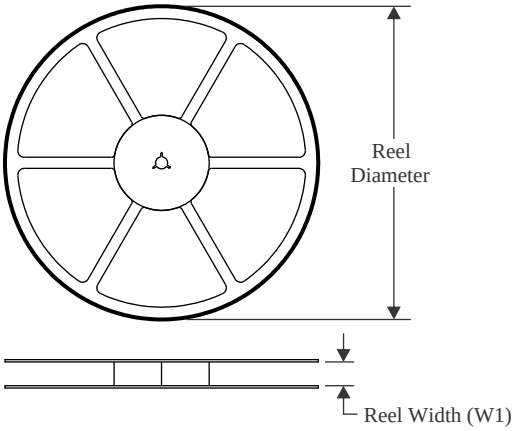
- Catalog : TLV2365, TLV365

NOTE: Qualified Version Definitions:

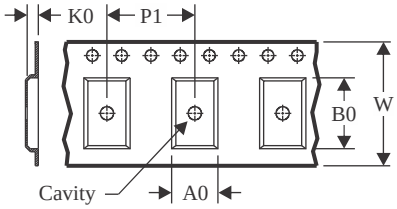
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

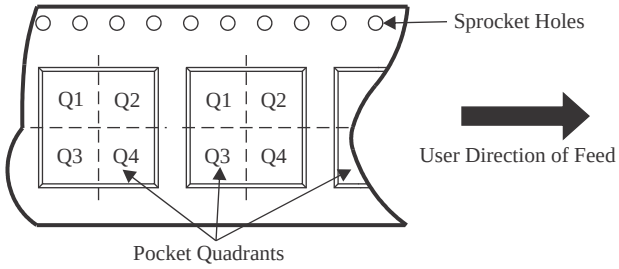


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

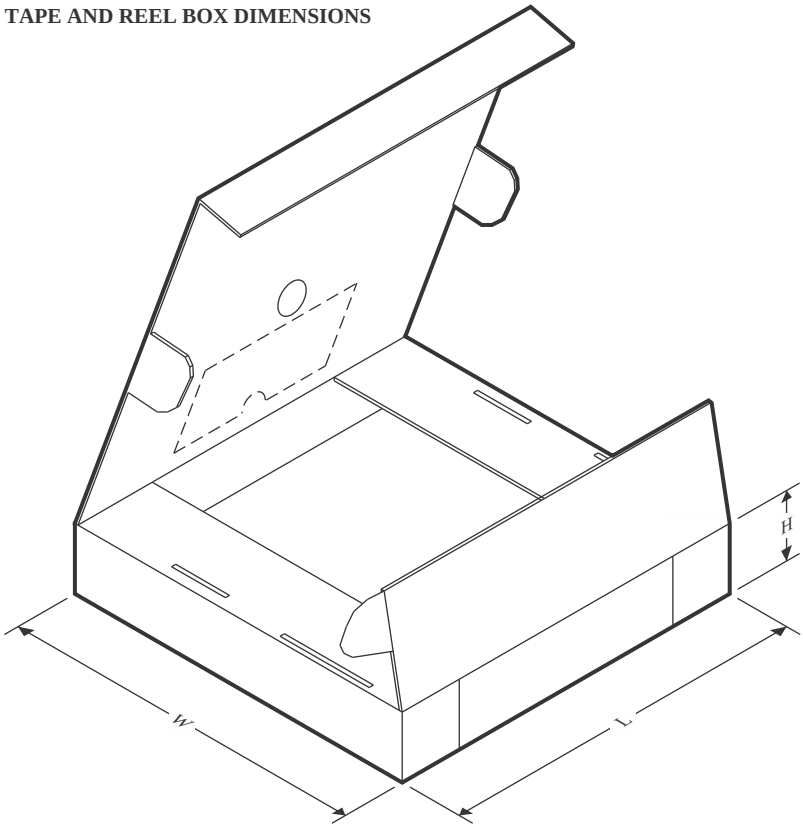
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

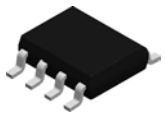
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2365QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2365QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV365QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2365QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV2365QDRQ1	SOIC	D	8	3000	340.5	338.1	20.6
TLV365QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

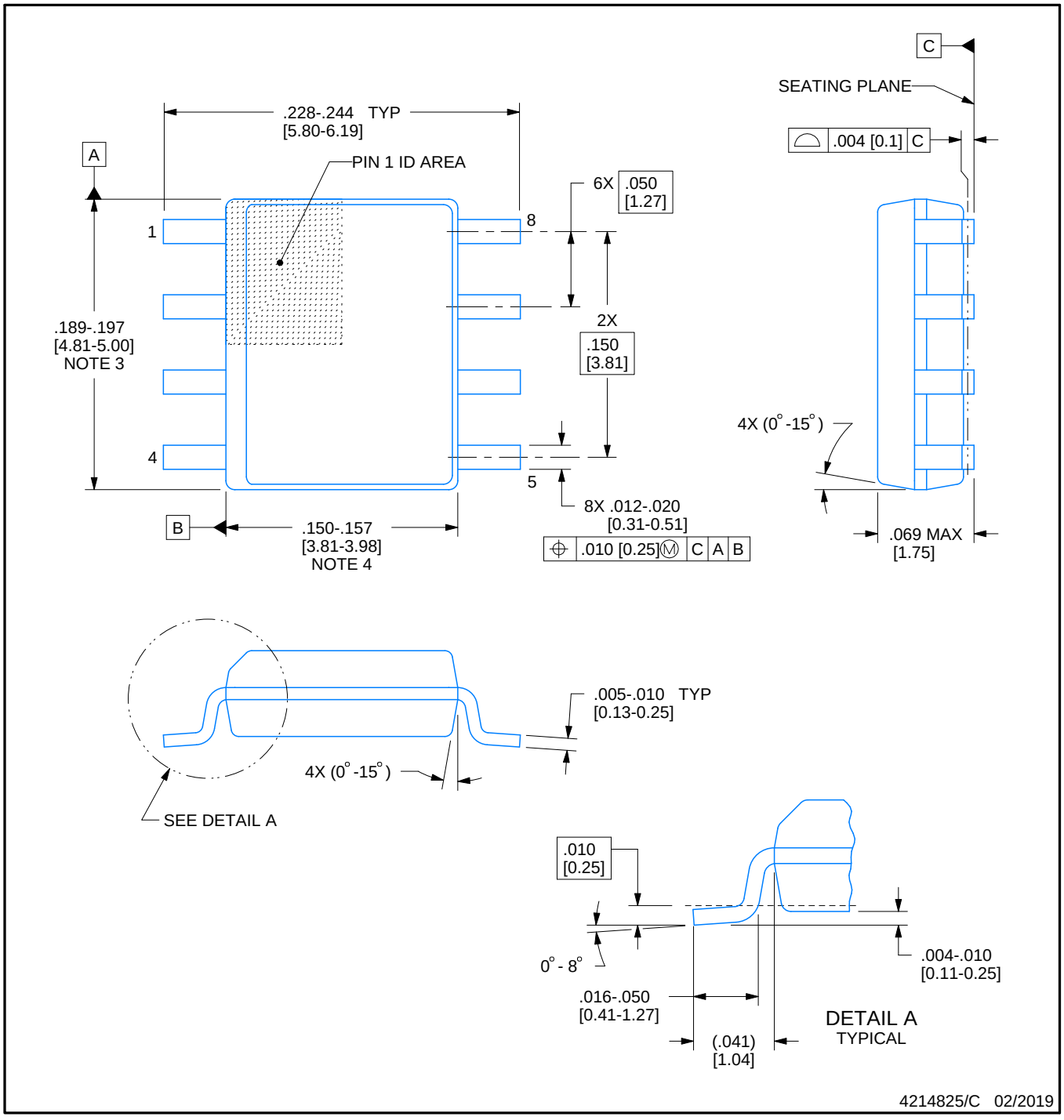


PACKAGE OUTLINE

D0008A

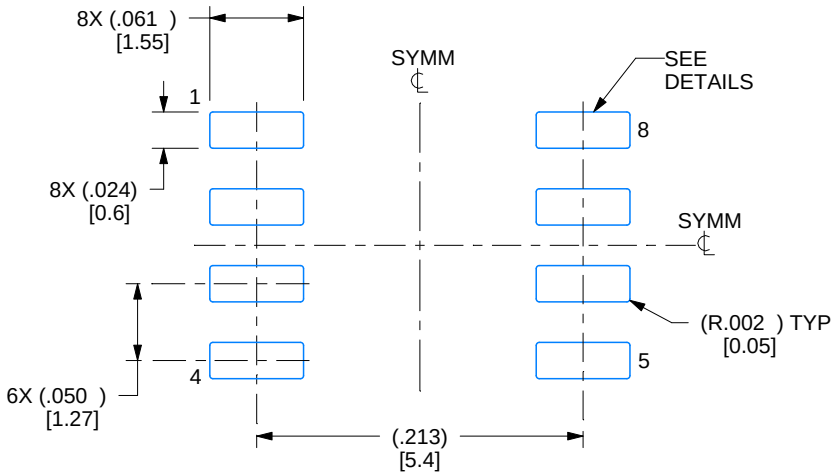
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

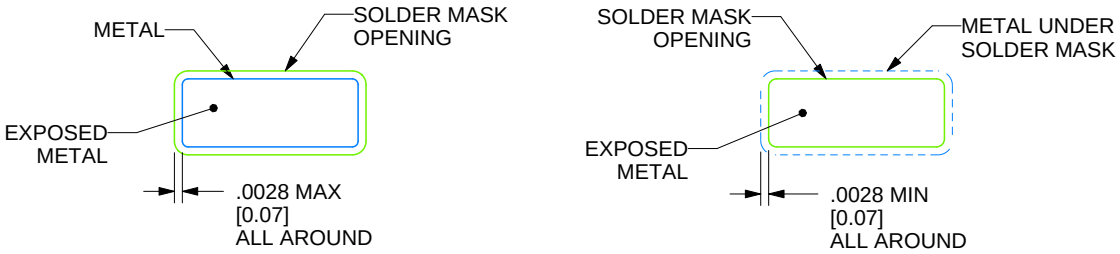


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

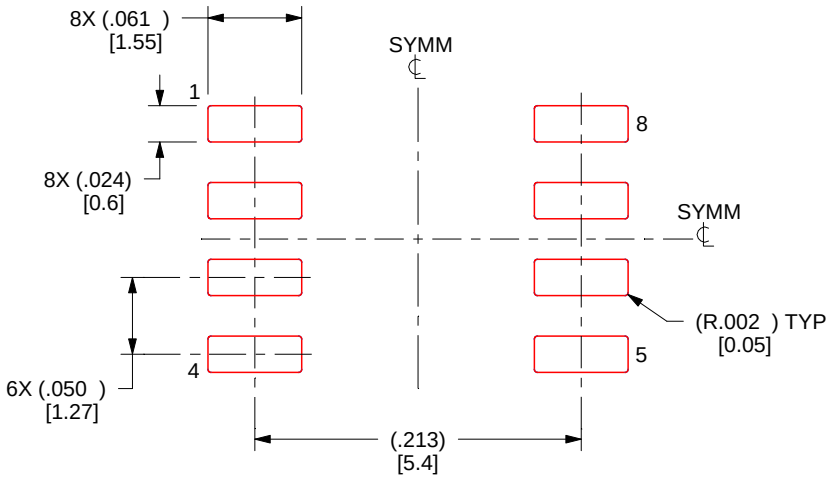
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

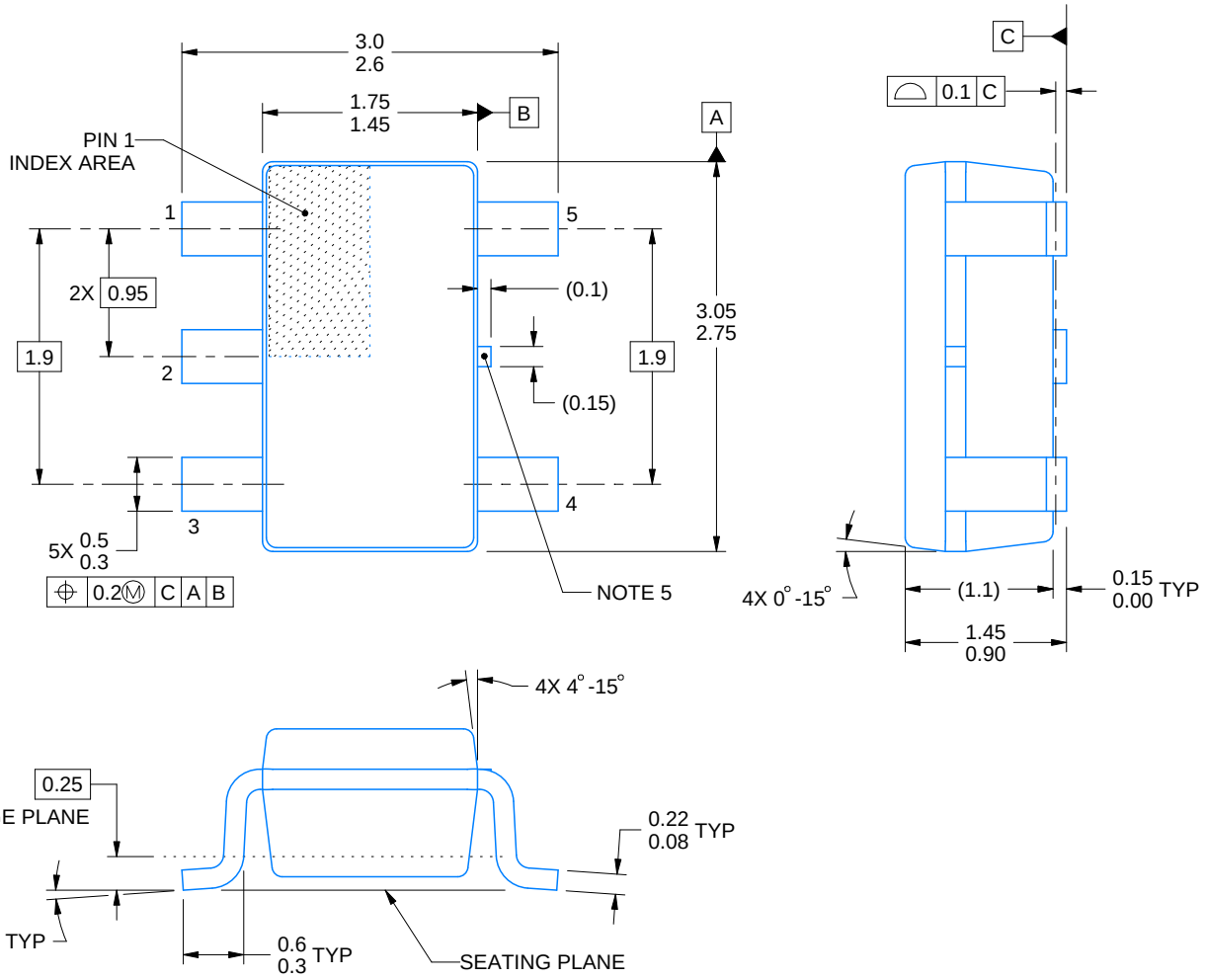
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

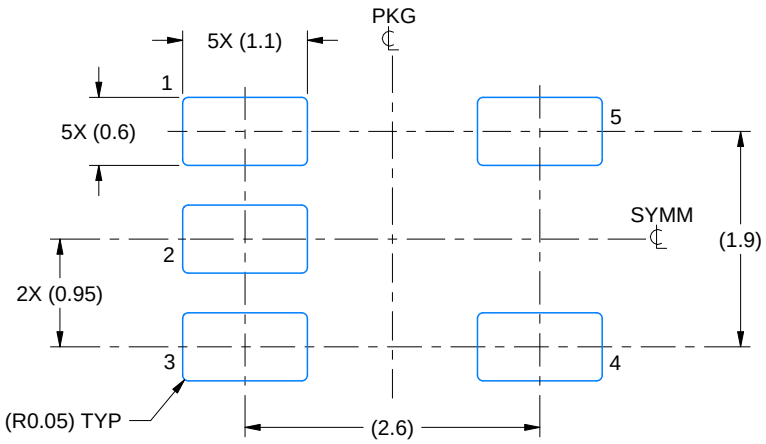
SMALL OUTLINE TRANSISTOR



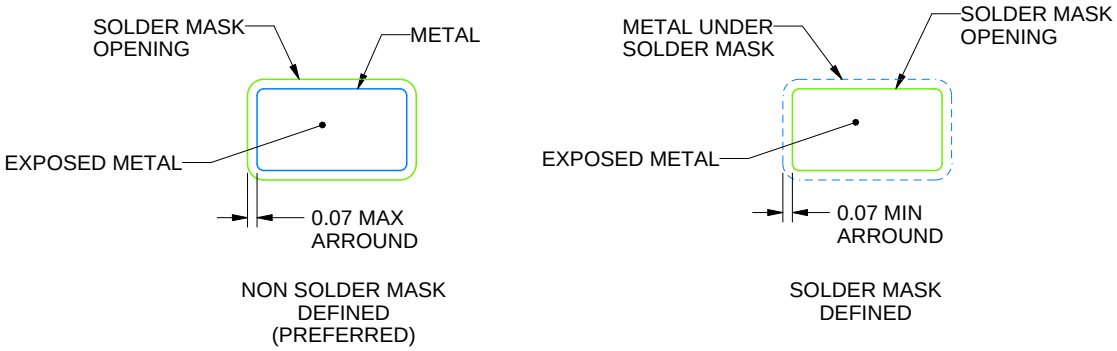
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

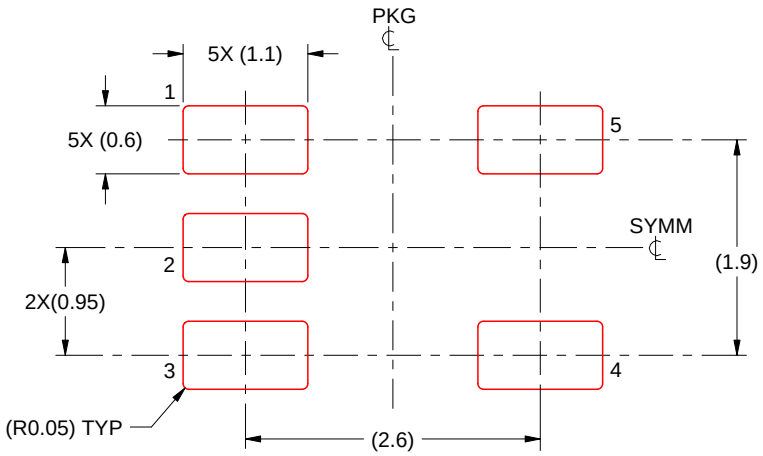


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

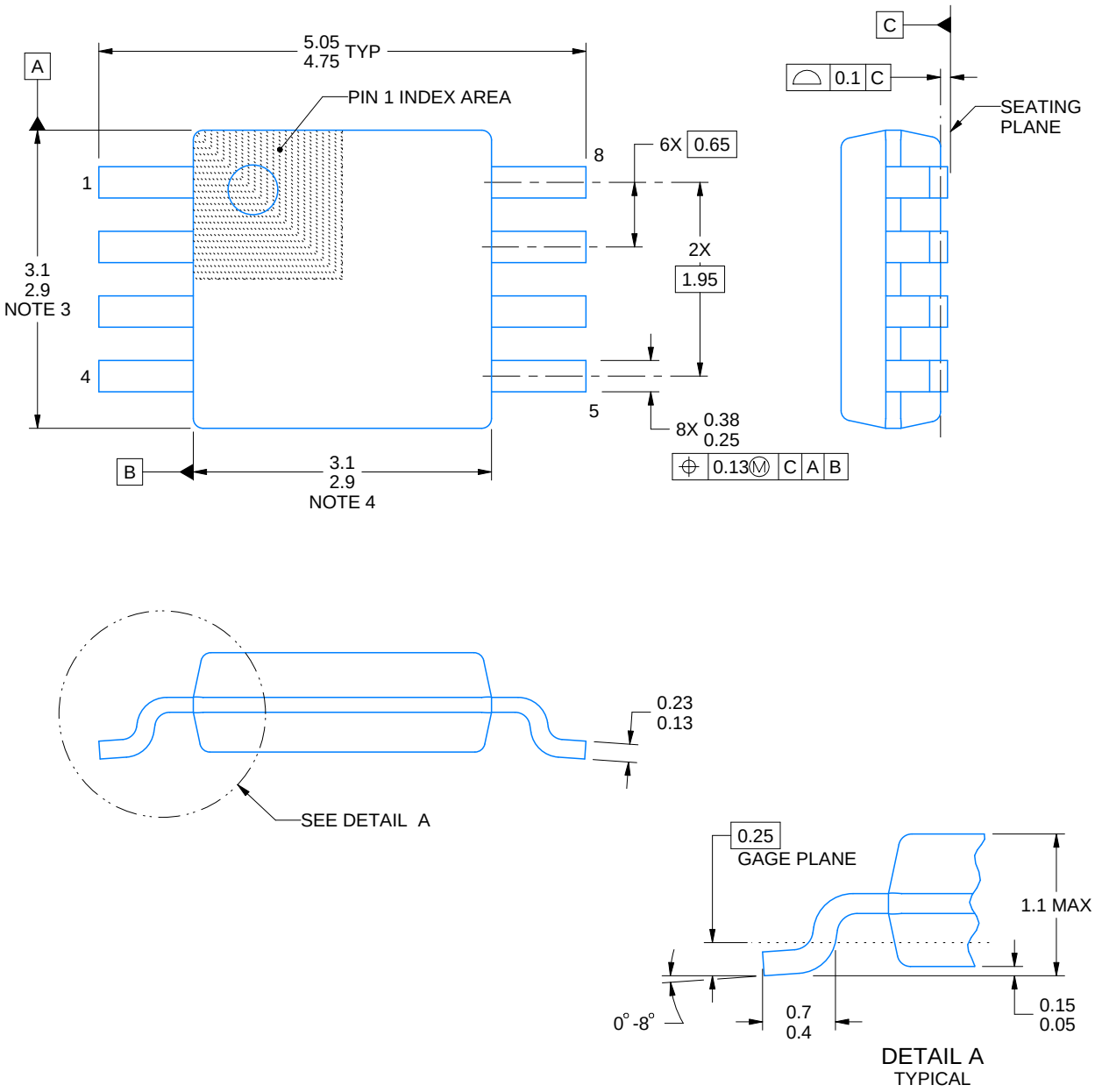
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

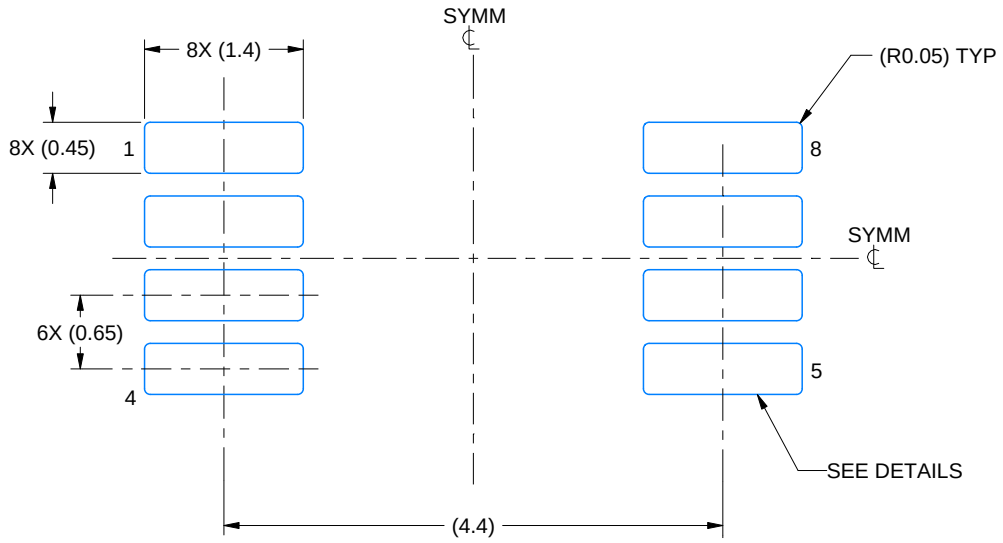
SMALL OUTLINE PACKAGE



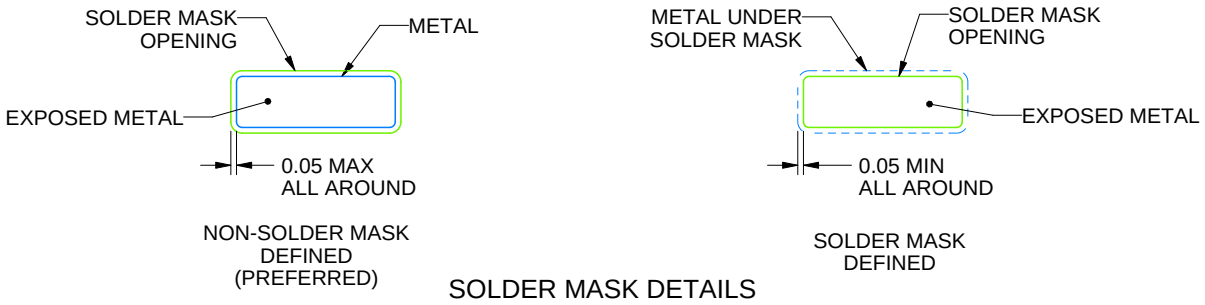
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

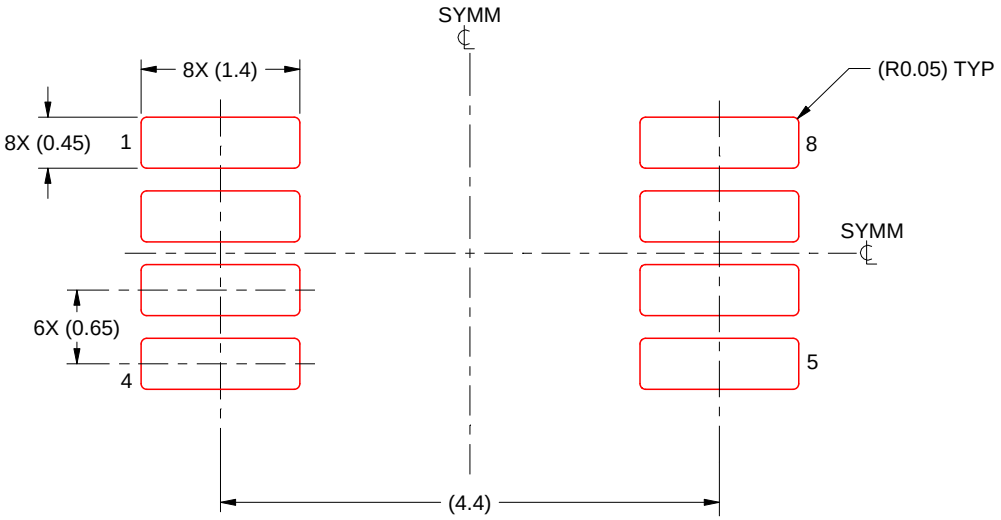


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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