

TLV2352 Dual Low-Voltage Differential Comparators

1 Features

Wide range of supply voltages: 2V to 8V

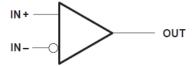
- Wide range of supply voltages: 2.7V to 8V (TLV2352IDR and TLV2352IPWR only)
- Fully characterized at 3V and 5V
- Very-low supply-current drain: 120µA typical at 3V
- Output compatible with TTL, MOS, and CMOS
- Fast response time: 200ns typical for TTL-level input step
- High input impedance: $10^{12}\Omega$ typical
- Extremely low input bias current: 5pA typical
- Common-mode input voltage range includes ground
- **Built-in ESD protection**

2 Description

The TLV2352 consists of two independent, lowpower comparators specifically designed for single power-supply applications and operates with powersupply rails as low as 2V (2.7V TLV2352IDR and TLV2352IPWR only). When powered from a 3V supply, the typical supply current is only 120µA.

The TLV2352 is designed using the Texas Instruments CMOS technology and therefore features an extremely high input impedance (typically greater than $10^{12}\Omega$), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and can be connected to achieve positivelogic wired-AND relationships. The TLV2352I is fully characterized at 3V and 5V for operation from -40°C to 85°C. The TLV2352M is fully characterized at 3V and 5V for operation from -55°C to 125°C.

The TLV2352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 1000V ESD rating using Human Body Model testing. However, care must be exercised in handling this device as exposure to ESD can result in degradation of the device parametric performance.



Symbol (Each Comparator)



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3 Device Comparison Table

Device Information

	V _{IO} max			PACKAGE	D DEVICES		
T _A	at 25°C	SMALL OUTLINE (D) ⁽¹⁾	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)(2)	PLASTIC DIP (U)
–40°C to 85°C	5mV	TLV2352ID	_	_	TLV2352IP	TLV2352IPWLE	_
–55°C to 125°C	5mV	_	TLV2352MFK	TLV2352MJG	_	_	TLV2352MU

- 1) The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).
- (2) The PW packages are only available left-ended taped and reeled (e.g., TLV2352IPWLE).

4 Pin Configuration and Functions

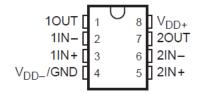
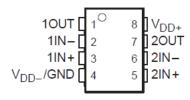


Figure 4-1. TLV2352I D or P Package TLV2352M JG Package (Top View)



NC - No internal connection

Figure 4-3. TLV2352I PW Package (Top View)

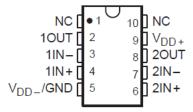


Figure 4-2. TLV2254M U Package (Top View)

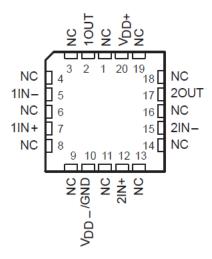


Figure 4-4. TLV2352M FK Package (Top View)



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V _{DD}	Supply voltage ⁽²⁾			8	V
V _{ID}	Differential input voltage ⁽³⁾			±VDD	V
V _I	Input voltage range		-0.3	VDD	V
Vo	Output voltage			8	V
1	Input current			±5	mA
О	Output current Duration of output short-circuit current to GND ⁽⁴⁾			20	mA
	Duration of output short-circuit current to GND ⁽⁴⁾		Unlimited		
ГА	Operating free-air temperature range	TLV2352I	-40	85	°C
¹ A	Operating free-all temperature range	TLV2352M	-55	125	C
T _{stg}	Storage temperature range		-65	150	°C
		D package			
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	P package		260	°C
		PW package			
		FK package			
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	JG package	1	300	°C
		U package	1		

⁽¹⁾ Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage	2	8	V	
V_{DD}	Supply voltage (TLV2352IDR and TLV2	2.7	8	V	
\/	Common-mode input voltage	V _{DD} = 3V	0	1.75	V
V _{IC}	Common-mode input voitage	V _{DD} = 5V	0	3.75	V
_	Out and the second state of the second state o	TLV2352I	-40	85	°C
T _A	Operating free-air temperature	TLV2352M	-55	125	C

Product Folder Links: TLV2352



5.3 Electrical Characteristics TLV2352I

at specified free-air temperature(1)

							TLV2	352I			
	PARAMETER	TEST CO	TEST CONDITIONS		V	_{DD} = 3V		Vı	_{DD} = 5V		UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage $V_{IC} = V_{ICR}$ min			25°C		1	5		1	5	mV
V IO	input onset voltage	AIC - AICKIIIII	/IC - VICRITIIII				7			7	IIIV
I _{IO}	I _{IO} Input offset current					1			1		pА
'IO	input onset current			85°C			1			1	nA
L.	Input bias current					5			5		pА
I _{IB}	input bias current	85°C		2			2	nA			
				25°C	0 to 2			0 to 4			
V _{ICR}	Common-mode input voltage range				0 to			0 to			V
	Tomago rango			Full range	1.75			3.75			
	High-level output current	V _{ID} = 1V		25°C		0.1			0.1		nA
I _{OH}	nigri-level output current	VID - IV		Full range			1			1	μA
V	Low-level output voltage	V _{ID} = -1V	1 - 2mA	25°C		115	300		150	400	mV
V _{OL}	Low-level output voltage	V _{ID} = -1V	I _{OL} = 2mA	Full range			600			700	IIIV
I _{OL}	Low-level output current	V _{ID} = -1V	V _{OL} = 1.5V	25°C	6	16		6	16		mA
1	Supply current	\/ = 1\/	No load	25°C		120	250		140	300	
I _{DD}	Supply current	V _{ID} = 1V	INO IOAU	Full range			350			400	μA

⁽¹⁾ All characteristics are measured with zero common-mode input voltages unless otherwise noted.

5.4 Switching Characteristics TLV2352I 3V

 $V_{dd} = 3V$, $T_a = 25$ °C

PARAMETER	TEG	TI	UNIT			
PARAMETER	TEC	ST CONDITIONS	MIN	TYP	MAX	ONII
Response time	ponse time $R_L = 5.1 \text{k}\Omega$, $C_L = 15 \text{pF}^{(1)}$ (2) 100mV input step with 5mV overdrive			640		ns

5.5 Switching Characteristics TLV2352I 3V (TLV2352IDR and TLV2352IPWR only)

 $V_{dd} = 3V$, $T_a = 25$ °C

PARAMETER	TEG	TI	UNIT			
PARAMETER	TEX	ST CONDITIONS	MIN	TYP	MAX	ONII
Response time	$R_L = 5.1 \text{k}\Omega, C_L = 15 \text{pF}^{(1)}$ (2)	100mV input step with 10mV overdrive		200		ns

⁽¹⁾ C_L includes probe and jig capacitance.

5.6 Switching Characteristics TLV2352I 5V

 V_{DD} = 5V, T_A = 25°C

PARAMETER	TEQ	Т	UNIT			
	IES	T CONDITIONS	MIN	TYP	MAX	UNIT
Response time	$R_L = 5.1k\Omega, C_L = 15pF^{(1)}$ (2)	100mV input step with 5mV overdrive		650		ns
Response une	N_ = 3.1K12, O_ = 13pF(/ (/	TTL-level input step		200		115

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Product Folder Links: TLV2352

⁽²⁾ Full range is -40°C to 85°C.

⁽²⁾ The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1V with V_{DD} = 3V or V_O = 1.4V with V_{DD} = 5V.



5.7 Switching Characteristics TLV2352I 5V (TLV2352IDR and TLV2352IPWR only)

 V_{DD} = 5V, T_A = 25°C

PARAMETER	TEQ	TI	UNIT			
	123	T CONDITIONS	MIN	TYP	MAX	ONII
Response time	$R_L = 5.1k\Omega$, $C_L = 15pF^{(1)}$ (2)	100mV input step with 10mV overdrive		200		nc
Response time	KL = 5.1kt2, CL = 15pr(**/->	100mV overdrive		100		ns

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses $V_O = 1V$ with $V_{DD} = 3V$ or $V_O = 1.4V$ with $V_{DD} = 5V$.

5.8 Electrical Characteristics TLV2352M

at specified free-air temperature(1)

							TLV2	352M			
	PARAMETER	TEST CO	TEST CONDITIONS		Vı	_{DD} = 3V		V	_{DD} = 5V		UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _{IC} = V _{ICR} min		25°C		1	5		1	5	mV
V IO	input onset voltage	VIC - VICRIIII	ı	Full range			10			10	1110
l. a	I _{IO} Input offset current					1			1		pА
I _{IO}	input onset current			125°C			10			10	nA
1	Input bias current			25°C		5			5		pА
I _{IB}	input bias current			125°C			20			20	nA
	Common-mode input voltage range			25°C	0 to 2			0 to 4			
V _{ICR}			Full range	0 to			0 to			V	
	veillage rainge			Full range	1.75			3.75			
	High-level output current	V _{ID} = 1V		25°C		0.1			0.1		nA
I _{OH}	nigri-level output current	VID - IV		Full range			1			1	μA
V _{OL}	Low-level output voltage	V _{ID} = -1V	I _{OL} = 2mA	25°C		115	300		150	400	mV
V OL	Low-level output voltage	VID 1 V	IOL - ZIIIA	Full range			600			700	1110
I _{OL}	Low-level output current	V _{ID} = -1V	V _{OL} = 1.5V	25°C	6	16		6	16		mA
1	Supply current	V = 4V	No load	25°C		120	250		140	300	0
I _{DD}	очрріў сипепі	V _{ID} = 1V	INO IOAU	Full range			350			400	μA

(1) All characteristics are measured with zero common-mode input voltages unless otherwise noted.

(2) Full range is – 55°C to 125°C.

5.9 Switching Characteristics TLV2352M 3V

 V_{DD} = 3V, T_A = 25°C

PARAMETER	TEST	CONDITIONS	TL	V2352M		UNIT
PARAMETER	IEST	CONDITIONS	MIN	TYP	MAX	ONIT
Response time	R_L = 5.1kΩ, C_L = 100pF ^{(1) (2)} 100mV input step with 5mV overdrive				1400	ns

(1) C_L includes probe and jig capacitance.

(2) The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1V with V_{DD} = 3V or V_O = 1.4V with V_{DD} = 5V.

Product Folder Links: TLV2352



5.10 Switching Characteristics TLV2352M 5V

 V_{DD} = 5V, T_A = 25°C

PARAMETER	TEST	CONDITIONS	TL	UNIT		
PARAMETER	IEST	MIN	TYP	MAX	UNIT	
Response time	P = 5.1k0 C = 100pE(1)(2)	100mV input step with 5mV overdrive			1300	no
	KL - 5.1K22, CL - 100pr(**/\-	TTL-level input step			900	ns

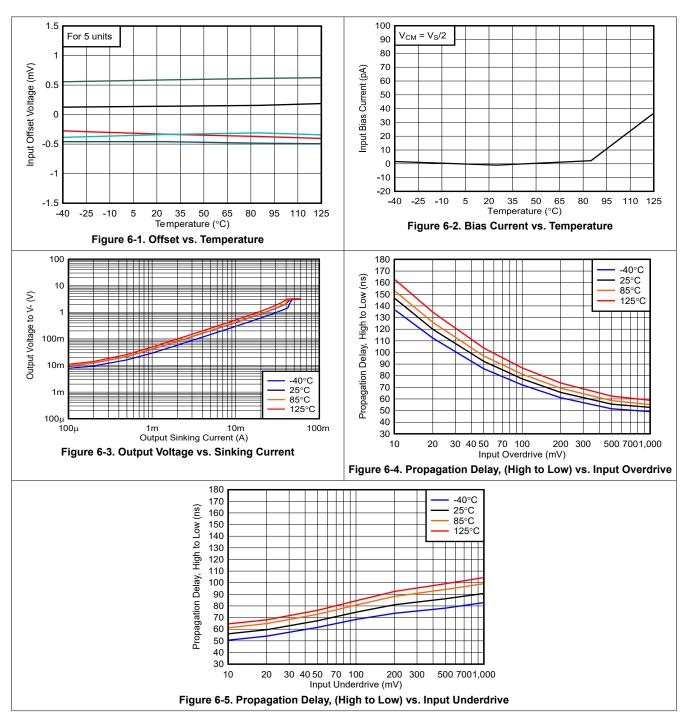
Product Folder Links: TLV2352

 C_L includes probe and jig capacitance. The response time specified is the interval between the input step function and the instant when the output crosses $V_O = 1V$ with $V_{DD} = 1$ (1) (2) $3V \text{ or } V_O = 1.4V \text{ with } V_{DD} = 5V.$



6 Typical Characteristics (TLV2352IDR and TLV2352IPWR only)

At T_A = 25°C, V_S = 3.3V, V_{CM} = $V_S/2V$, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10k Ω , unless otherwise noted.



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7 Device and Documentation Support

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7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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7.3 Trademarks

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7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2025) to Revision D (July 2025)	Page
Removed TLV2352Y throughout data sheet	1
Specified electrical characteristic differences for orderables TLV2352IDR and TLV2352IPWR	
Changes from Revision B (March 1999) to Revision C (June 2025)	Page
Updates throughout data sheet to reflect performance of new die	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
5962-9688101QPA	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9688101QPA TLV2352M
TLV2352ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	23521
TLV2352IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	23521
TLV2352IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	23521
TLV2352IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2352IP
TLV2352IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLV2352IP
TLV2352IPW	Obsolete	Production	TSSOP (PW) 8	-	-	Call TI	Call TI	-40 to 85	TY2352
TLV2352IPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352
TLV2352IPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352
TLV2352MJG	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLV2352MJG
TLV2352MJG.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLV2352MJG
TLV2352MJGB	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9688101QPA TLV2352M
TLV2352MJGB.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9688101QPA TLV2352M

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

PACKAGE OPTION ADDENDUM

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(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV2352, TLV2352M:

Catalog: TLV2352

Military: TLV2352M

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION



TAPE DIMENSIONS KO P1 BO W Cavity A0

A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	U	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

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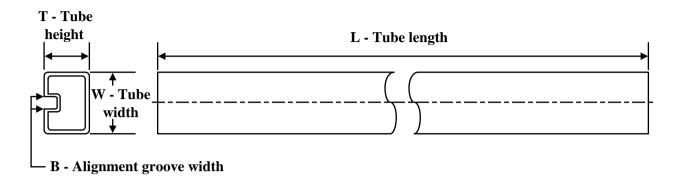
*All dimensions are nominal

Device	Package Type	Package Type Package Drawing		SPQ	Length (mm)	Width (mm)	Height (mm)	
TLV2352IDR	SOIC	D	8	2500	353.0	353.0	32.0	
TLV2352IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0	

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2352IP	Р	PDIP	8	50	506	13.97	11230	4.32
TLV2352IP.A	Р	PDIP	8	50	506	13.97	11230	4.32

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