TLV192x Family of 65V Comparators with Integrated 2.5V Voltage Reference

1 Features

- Wide supply range: 3.3V to 65V
- Fail-safe inputs up to 65V
- Open-drain output up to 65V
- 2.5V, 1.5%, 100ppm maximum voltage reference
- Reference output can drive up to 1mA
- 3mV input offset voltage
- 900ns propagation delay
- Power-on-reset provides a known startup condition
- Low supply current: 8uA per channel
- Pin spacings meet IPC2221A creepage requirements (SOIC).
- Temperature range: -40°C to +125°C

2 Applications

- Motor drives
- Appliances
- Grid infrastructure
- Factory automation and control
- Traction inverter

3 Description

The TLV1921 and TLV1922 are a family of single and dual 65V comparators with an integrated 2.5V reference that is externally accessible. The inputs are fail-safe tolerant up to 65V independent of the supply voltage. This makes the comparators well suited for 12V and 24V industrial systems where operating voltage compliance to 65V is required. Likewise, the fail-safe inputs eliminate power supply sequencing concerns.

The single and dual channel options have an externally available 2.5V reference output and undedicated comparator inputs allowing for inverting and non-inverting configurations. The dual also has an externally available 2.5V refernce output which is internally connected to the non-inverting input of the first comparator. The dual configuration enables window comparator applications or dual channel over-voltage detection.

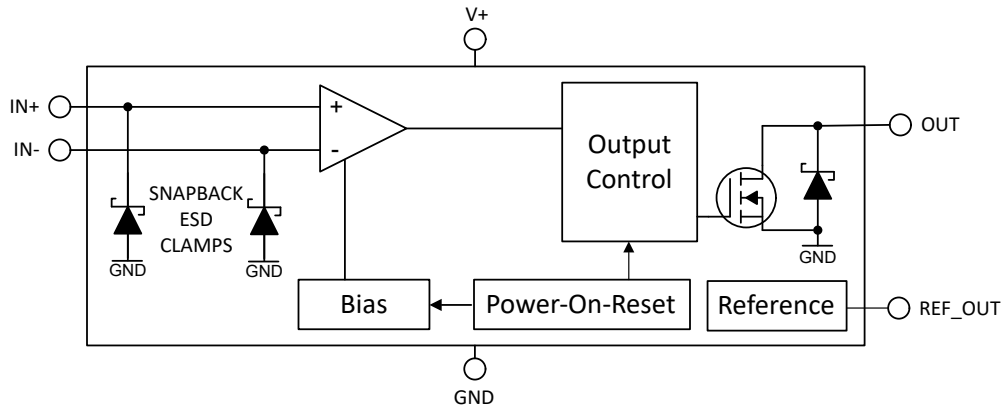
All devices include a Power-On Reset (POR) feature that sets the output to a known state until the minimum supply voltage has been reached and the output responds to the inputs, thus preventing false outputs during system power-up and power-down.

The Family of comparators have an open-drain output stage that is 65V compliant.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM) (2)
TLV1921	SOIC (8) (Preview)	3.91mm × 4.90mm
	SC-70 (6) (Preview)	2.00mm × 1.25mm
TLV1922	SOIC (8) (Preview)	3.91mm × 4.90mm
	WSON (8)	2.00mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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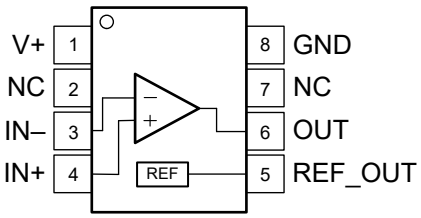
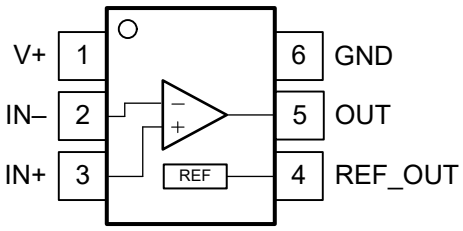
4 Pin Configuration and Functions

Pin Configuration: TLV1921



D Package
8-Pin SOIC
Top View

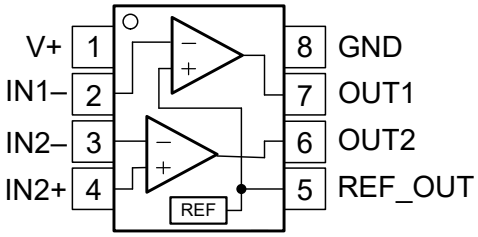


DCK Package
6-Pin SC-70
Top View

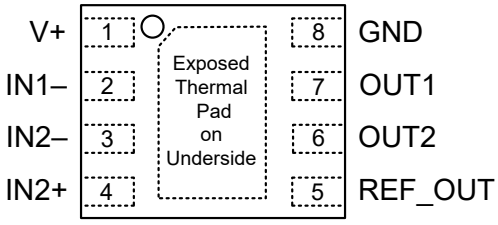
Table 4-1. Pin Functions: TLV1921

NAME	PINS		I/O	DESCRIPTION
	SC-70	SOIC		
V+	1	1	–	Positive Supply Voltage
NC	–	2	–	No Connect
IN–	2	3	I	Inverting (–) input
IN+	3	4	I	Non-Inverting (+) Input
REF_OUT	4	5	O	Reference Output
OUT	5	6	O	Comparator Output
NC	–	7	–	No Connect
GND	6	8	–	Negative Supply Voltage

Pin Configurations: TLV1922



D Package
8-Pin SOIC
Top View



DSG Package
8-Pin WSON
Top View

Table 4-2. Pin Functions: TLV1922

PIN		I/O	DESCRIPTION
NAME	NO.		
V+	1	—	Positive Supply Voltage
IN1–	2	I	Inverting input pin of comparator 1
IN2–	3	I	Inverting input pin of comparator 2
IN2+	4	I	Noninverting input pin of comparator 2
REF_OUT	5	O	Reference Output
OUT2	6	O	Output pin of comparator 2
OUT1	7	O	Output pin of comparator 1
GND	8	—	Negative supply voltage

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – GND	–0.3	70	V
Input pins: (IN+, IN–) from GND(2)	–0.3	65	V
Current into Input pins: (IN+, IN–)(2)	–10	10	mA
Comparator output voltage: (OUT) from GND(3)	–0.3	65	V
Comparator output short circuit current(4)		10	mA
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to GND. Inputs (IN+, IN–) can be greater than (V+) as long as within the –0.3V to 65V range. Inputs below –0.3V must be current-limited to less than –10mA, while inputs beyond +65V must be externally voltage clamped.
(3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN–) as long as it is within the –0.3V to 65V range
(4) Short-circuit to +5V. Continuous output short circuits can result in excessive heating eventually exceeding the maximum allowed junction temperature, leading to eventual device destruction.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information - Single

THERMAL METRIC(1)		TLV1921		UNIT
		D (SOIC-8)	DCK (SC-70)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	–	–	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	–	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	–	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	–	–	°C/W
ψ_{JB}	Junction-to-board characterization parameter	–	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.4 Thermal Information - Dual

THERMAL METRIC[1]		TLV1922		UNIT
		D (SOIC-8)	DSG (WSON-8)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	–	78.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	–	99.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	–	44.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	–	5.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	–	44.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	19.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – GND	3.3	65	V
Input voltage range from GND	–0.2	65	V
Output voltage range from GND	–0.2	65	V
Ambient temperature, T_A	–40	125	°C

5.6 Electrical Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 24V, V_{CM} = 2.5V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage		–3	±0.5	3	mV
V_{OS}	Input offset voltage	T_A = –40°C to +125°C	–4		4	mV
dV_{IO}/dT	Input offset voltage drift	V_{CM} = 2.5V T_A = –40°C to +125°C		±1.2		µV/°C
V_{HYS}	Input hysteresis voltage		1.2	3	5	mV
V_{HYS}	Input hysteresis voltage	T_A = –40°C to +125°C	1		6	mV
INPUT COMMON MODE RANGE						
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 3.3V to 65V	(V–) – 0.2		(V+) – 1.5	V
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 3.3V to 65V T_A = –40°C to +125°C	(V–) – 0.2		(V+) – 2	V
C_{IC}	Input Common Mode Capacitance			2		pF
VOLTAGE REFERENCE						
V_{OUT}	Reference Voltage		2.462	2.5	2.538	V
	Accuracy			±0.2%	±1.5%	
	Accuracy	T_A = –40°C to +125°C			±1.75%	
dV_{OUT}/d_T	Temperature Drift	T_A = –40°C to +125°C		40	100	ppm/°C
dV_{OUT}/dI_{LOAD}	Load Regulation, Sourcing	0mA < I_{SOURCE} ≤ 0.5mA		4		mV/mA
	Load Regulation, Sinking	0mA < I_{SINK} ≤ 0.5mA		4		mV/mA
ILOAD	Output Current			1		mA
dV_{OUT}/dV_S	Line Regulation	3.3V ≤ V_S ≤ 65V		10	100	µV/V
V_{noise}	Noise	f = 0.1Hz to 10Hz		0.2		mV_{PP}
INPUT BIAS CURRENT						
I_B	Input bias current			±2		pA
I_B	Input bias current	T_A = –40°C to +125°C	–1.2		1.2	nA
I_{OS}	Input offset current			±20		pA
INPUT IMPEDANCE						
C_{ID}	Input Differential Mode Capacitance			8		pF
OUTPUT						
V_{OL}	Voltage swing from (V–)	V_{PU} = 5V, R_{PU} = 10k I_{SINK} = 5mA T_A = –40°C to +125°C		150	300	mV
I_{OL}	Short-circuit current	Sinking @5V T_A = –40°C to +125°C		35		mA
POWER SUPPLY						
I_Q	Quiescent current per comparator	Output is logic high, V_{PU} = 5V, R_{PU} = 10k		8	11	µA
I_Q	Quiescent current per comparator	Output is logic high, V_{PU} = 5V, R_{PU} = 10k T_A = –40°C to +125°C			13	µA

5.6 Electrical Characteristics (continued)

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 24V, V_{CM} = 2.5V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{POR}	Power On Reset Voltage			2.45		V
t_{ON}	Power-up time			2		ms

5.7 Switching Characteristics

For V_S (TOTAL SUPPLY VOLTAGE) = (V+) – (V–) = 24V and V_{PU} = 3.3V, V_{CM} = 2.5V at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-LH}	Propagation delay time, low-to-high	V_{OD} = 100mV, V_{UD} = 100mV C_L = 15pF, T_A = 25°C, VCM = V_{REF}		1.2		µs
T_{PD-HL}	Propagation delay time, high-to-low	V_{OD} = 100mV, V_{UD} = 100mV C_L = 15pF, T_A = 25°C, VCM = V_{REF}		0.9		µs
T_{FALL}	Output Fall Time, 80% to 20%	C_L = 15 pF, V_{OD} = 100mV, V_{UD} = 100mV, R_{PU} = 5.1k		10		ns

5.8 Typical Characteristics

At T_A = 25°C, V_S = 24V, VCM = 2.5V, R_P = 5.1kΩ, C_L = 15pF, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

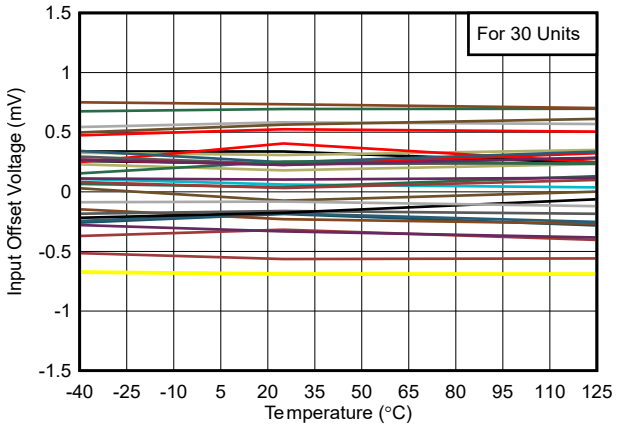


Figure 5-1. Offset vs. Temperature

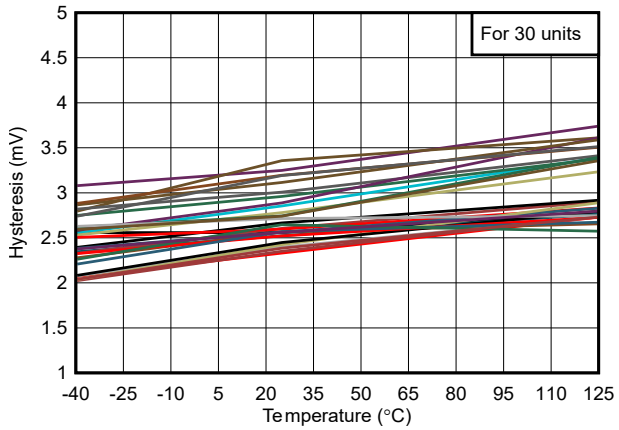


Figure 5-2. Hysteresis vs. Temperature

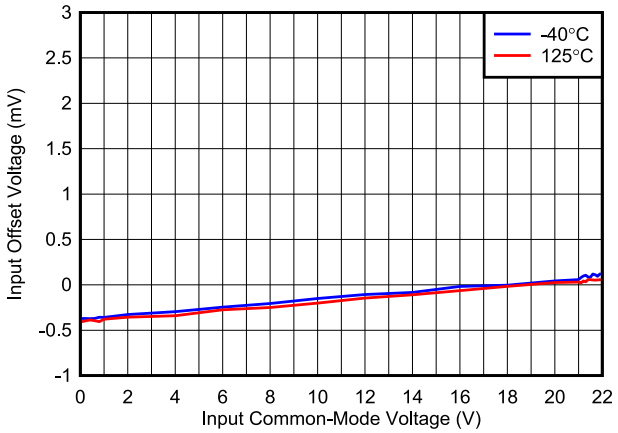


Figure 5-3. Offset vs. Common-Mode, 24V

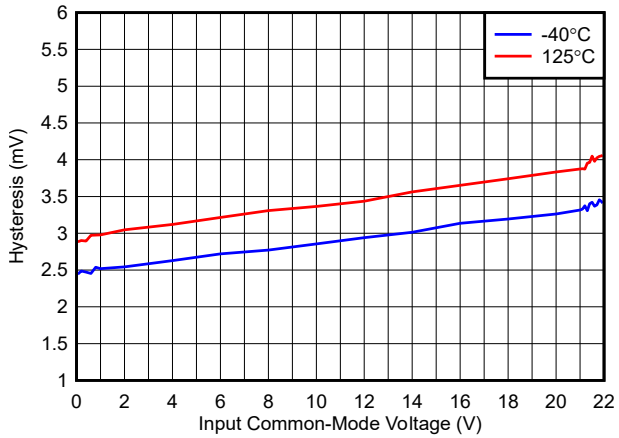


Figure 5-4. Hysteresis vs. Common-Mode, 24V

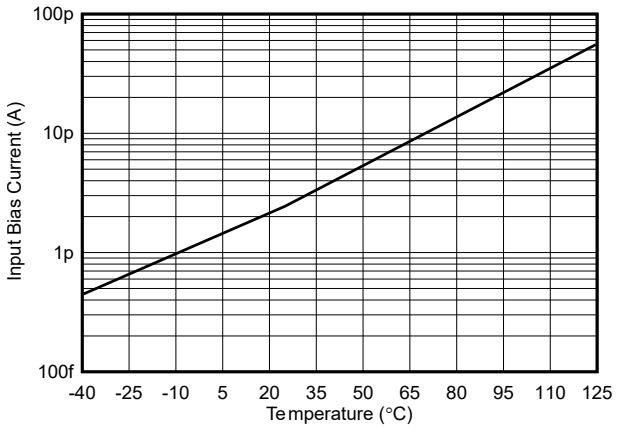


Figure 5-5. Bias Current vs. Temperature, 24V

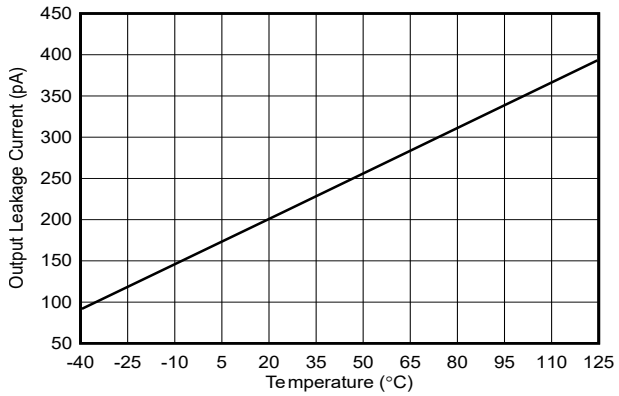


Figure 5-6. Output Leakage Current vs. Temperature

5.8 Typical Characteristics (continued)

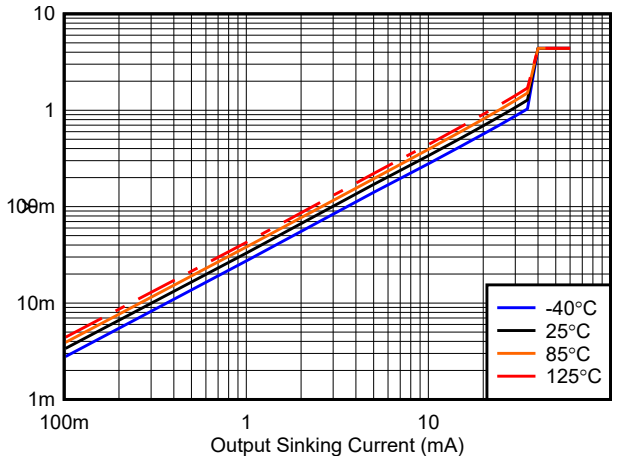


Figure 5-7. Output Voltage vs. Output Sinking Current, 4.5V

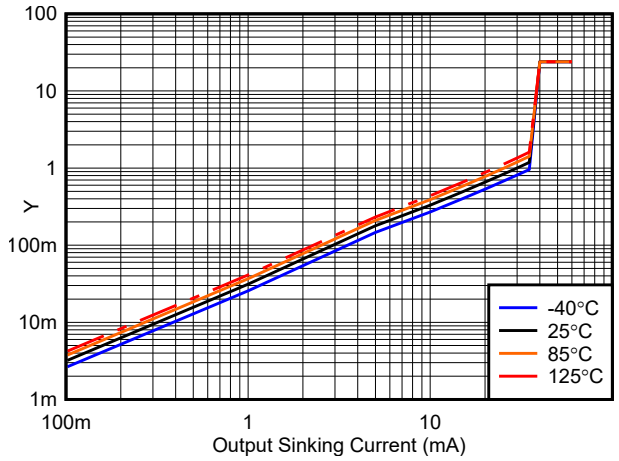


Figure 5-8. Output Voltage vs. Output Sinking Current, 24V

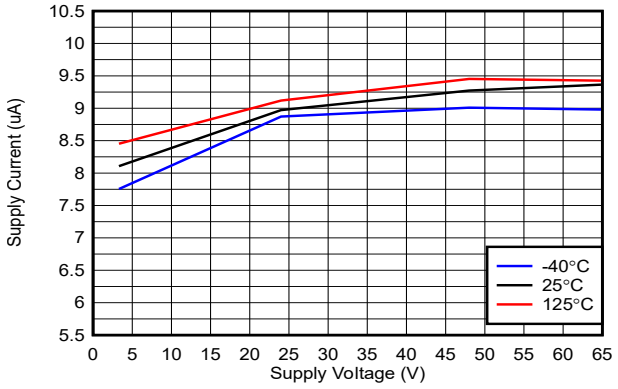


Figure 5-9. Supply Current vs. Supply Voltage (Output Low)

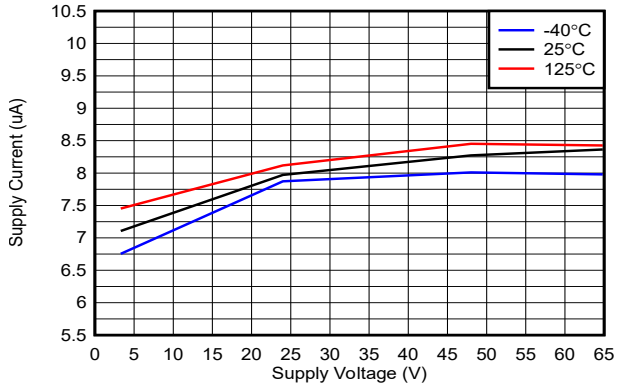


Figure 5-10. Supply Current vs. Supply Voltage (Output High)

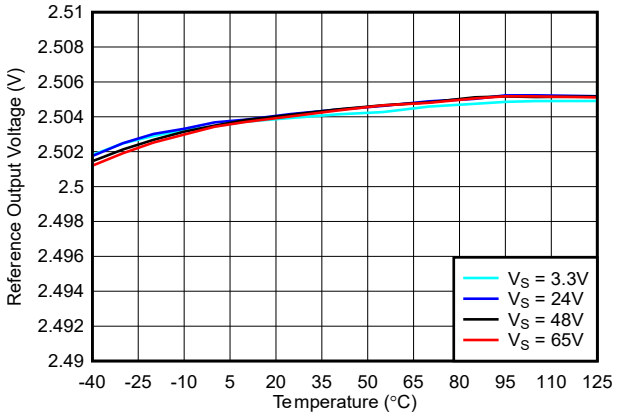


Figure 5-11. Reference Voltage vs. Temperature

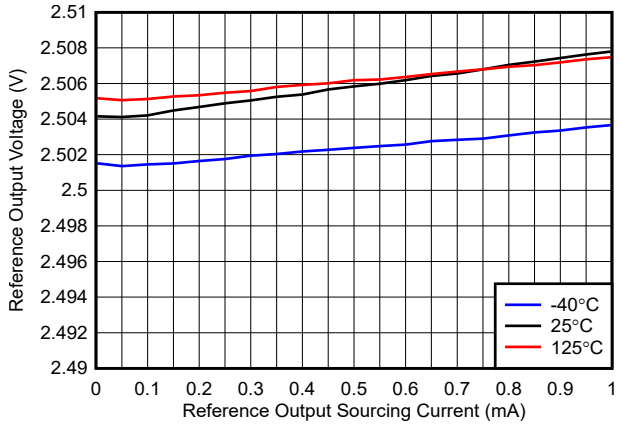


Figure 5-12. Reference Voltage vs. Reference Output Sourcing Current

5.8 Typical Characteristics (continued)

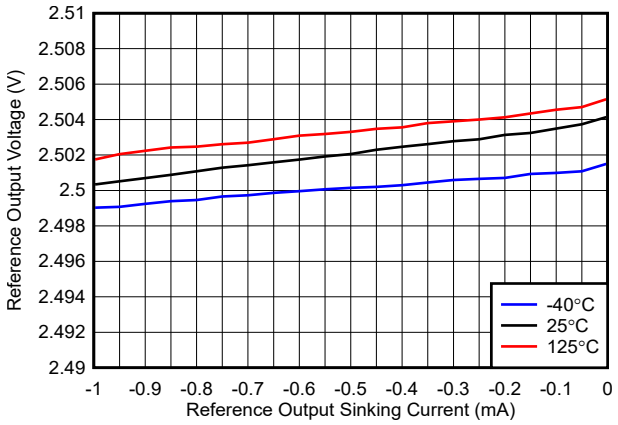


Figure 5-13. Reference Voltage vs. Reference Output Sinking Current

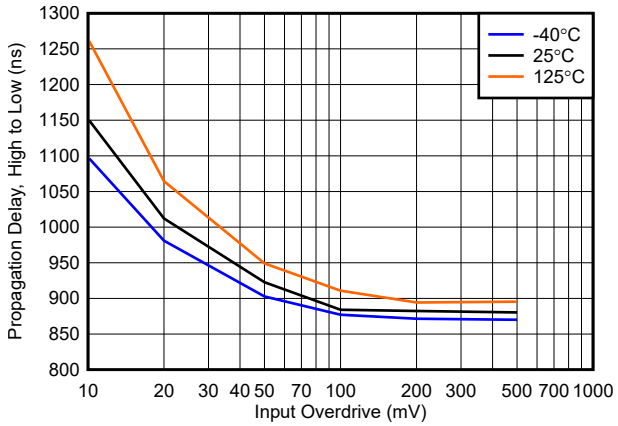


Figure 5-14. Propagation Delay, High to Low, 24V

6 Detailed Description

6.1 Overview

The TLV192x is a family of comparators with a wide supply range of 3.3V to 65V with an intergrated 2.5V that is externally available and capable of sinking and sourcing up to 1mA.

The single has a independant reference output and undedicated comparator inputs.

The dual has a reference output which is also internally connected to the non-inverting input of the first comaprator. The second comaprator has undedicated inputs that can be connected to the reference output or external references, to allow for maximum configuratuion flexibility.

The inputs are fail-safe capable up to 65V. This makes the comparators well suited for high voltage systems without causing damage during faults or transients. The unique pinout seprates the high-voltage input and supply pins from the low voltage output and GND pins to ease layout for creepage requirements.

The family also includes a Power-On Reset (POR) feature that makes sure the output is in a known state until the minimum supply voltage has been reached before the output responds to the inputs, thus preventing false outputs during system power-up and power-down.

The output is an open-drain output capable of being pulled-up to 65V, independant of the comparator supply..

6.2 Functional Block Diagrams

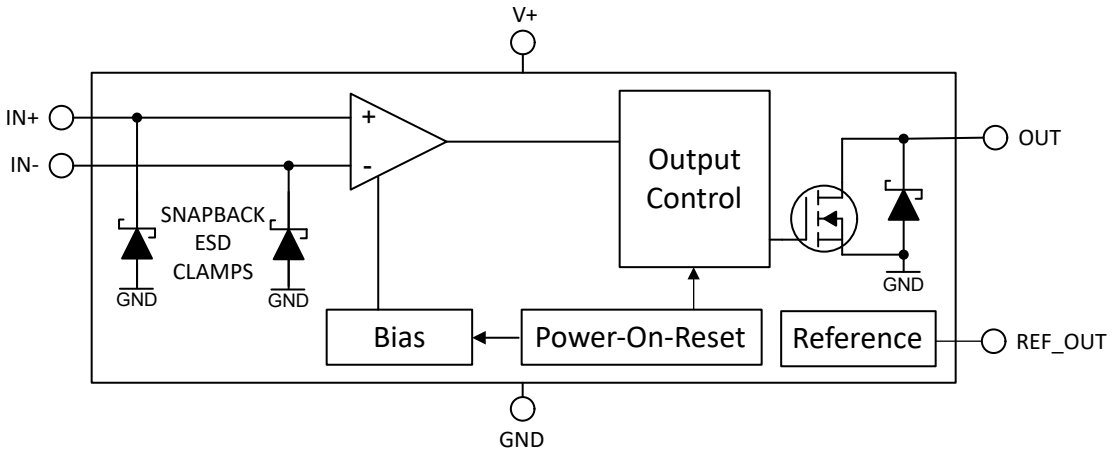


Figure 6-1. Block Diagram

6.3 Feature Description

The TLV192x is a family of 65 Volt comparators with a 3.3V to 65V supply voltage range, a 2.5V reference that is externally available, Power-On Reset (POR), Fail-safe inputs up to 65V, and a open-drain output capable of being pulled-up to 65V, independent of the comparator supply. The features are described in detail in the following sections.

6.4 Device Functional Modes

6.4.1 Inputs

6.4.1.1 Input Voltage and Common Mode Voltage Ranges

The TLV192x has an input voltgae range of -0.2V to 65V and a common mode (switching threshold) range of -0.2V to (V+) - 2V. The common mode voltage (referred to as the switching threshold) is the point where the comparator transistions from one output state to the other.

The TLV192x has a "feature" where if one of the input pins remains within the common mode voltage range (-0.2V to (V+) - 2V), and the supply voltage is valid and not in POR, the output state is correct.

The following is a summary of input voltage range conditions and the outcomes:

1. When both IN- and IN+ are within the common mode voltage range:
   a. If IN- is greater than IN+ and the offset voltage, the output is low.
   b. If IN- is less than IN+ and the offset voltage, the output is high.
   c. If IN- is equal to IN+, the output state is technically indeterminite and output state is determined by the random polarity of the internal offset votlage.
2. When IN- is higher than the common mode voltage range and IN+ is within the common mode voltage range, the output is low.
3. When IN+ is higher than the common mode voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the common mode voltage range, the output is low, regardless of which input is greater.

Operating outside the common mode range causes changes in specifications such as propagation delay and input bias current. Likewise, there is a recovery time when re-entering the common mode voltage range.

6.4.1.2 Fail-Safe Inputs

Fail-safe is defined as maintaining the same high input impedance when V+ is unpowered or within the recommended operating ranges and is not damaged. The TLV192x inputs are fault tolerant up to 65V independent of V+.

The fail-safe input voltage is any value between 0V and 65V from GND, even while V+ is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the specified range.

The fail-safe inputs have snapback ESD protection from each pin to GND which allows these pins to exceed the supply voltage (V+) up to 65V. If input voltages exceed 65V, an external clamp is required. Likewise, negative voltages on the inputs are ESD clamped to GND and need to be limited to less than -0.2V.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any transient currents the clamps conduct. The current needs to be limited to 10mA or less. This series resistance can be part of any resistive input dividers or networks.

6.4.1.3 Unused Inputs

If a channel is not used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together causes high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs are to be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input is grounded and the other input connected to a reference voltage, or even (V+).

6.4.2 Open-Drain Output

The TLV192x features a open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled-up to an external voltage from 0 V up to 65V, independent of the comparator supply voltage (V+). The open-drain output also allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to less than 100 uA to optimize V_{OL} logic levels. Lower pull-up resistor values help increase the risetime, but at the expense of increasing V_{OL} and higher power dissipation. The risetime is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) create an exponential rising edge due to the output RC time constant and increase the risetime.

Directly shorting the output to the pull-up voltage results in thermal runaway and eventual device destruction at high (>65V) pull-up voltages. If output shorts are possible, a series current limitng resistor is recommended to limit the power dissipation. Shorting the output to V+ can eventually destroy the device.

Unused open drain outputs can be left floating, or tied to the GND pin if floating pins are not desired.

The open-drain output ESD protection consists of a snapback ESD clamp between the output and GND.

6.4.3 Reference Output

The integrated 2.5V voltage reference offers low 100ppm/°C (maximum) drift provided on a separate output pin that allows use of external dividers or to provide a reference voltage for other external circuitry. The reference is stable with up to a 10nF capacitive load and can sink or source up to 500µA (typical) of output current.

6.4.4 Power-On Reset (POR)

The TLV192x has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry activates for up to 4ms after the minimum supply voltage threshold (V_{POR}) crossed **and** the reference output is stable. The output goes high-Z immediately when the supply voltage drops below V_{POR}. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

The POR circuit keeps the output high impedance (HI-Z) during the POR period (t_{on}).

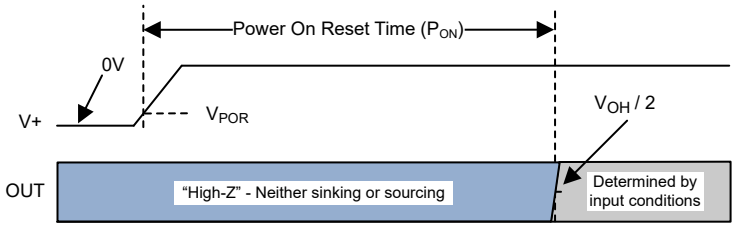


Figure 6-2. Power-On Reset Timing Diagram

6.4.5 Internal Hysteresis

The TLV192x contains up to 5mV of internal hysteresis. Information on hysteresis and how to increase the system hystereis by adding external hysteresis can be found in the Hysteresis section.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

If IN- is equal to IN+, the output state is technically indeterminite and output state is determined by the random polarity of the internal offset votlage. This condition is commonly seen when wiring the inputs directly across a low value shunt resistor at zero shunt load current.

Table 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output.

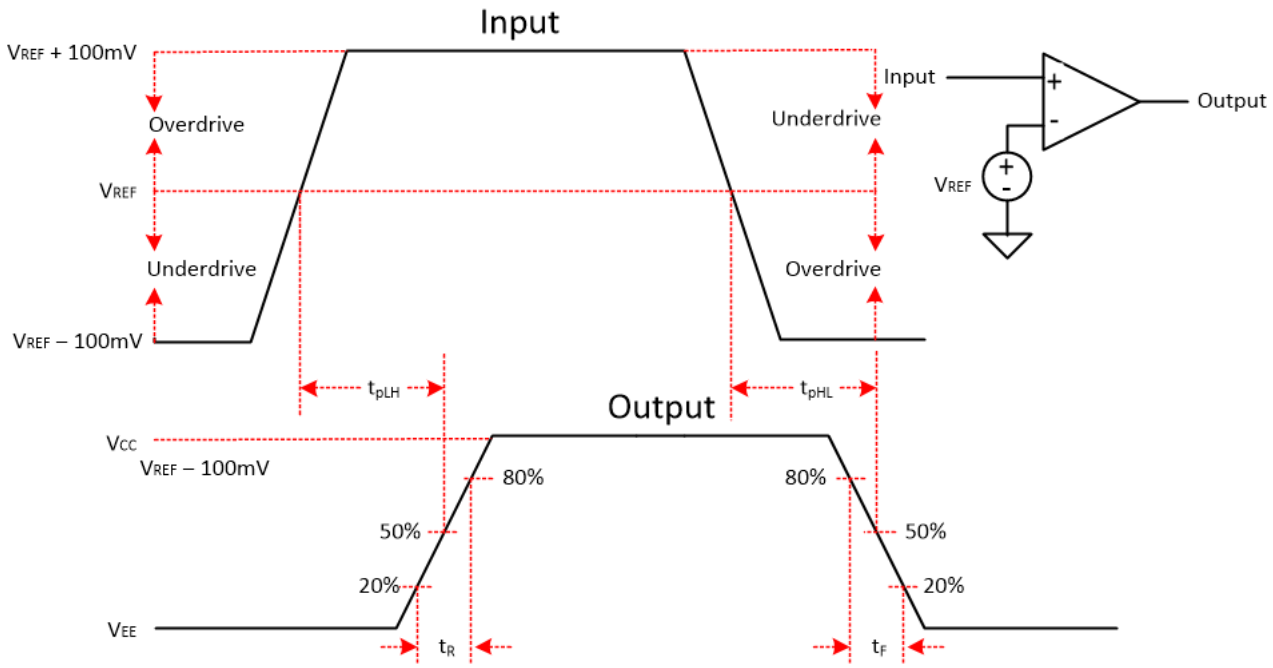


Figure 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired,TI recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration can produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This usually occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV192x devices only have a minimal amount of internal hysteresis of 5mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The Hysteresis Transfer Curve is shown in Figure 7-2 below. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

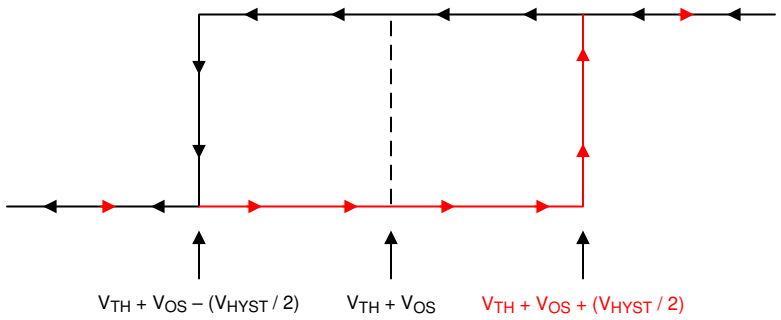


Figure 7-2. Hysteresis Transfer Curve

For more information, please see *Comparator with and without hysteresis circuit* - SBOA219

7.1.2.1 Inverting and Non-Inverting Hysteresis using Open-Drain Output

TLV192x output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

7.2 Typical Applications

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. The figure below shows a simple window comparator circuit monitoring a 24V PLC power supply. Window comparators require open drain outputs if the outputs are directly connected together.

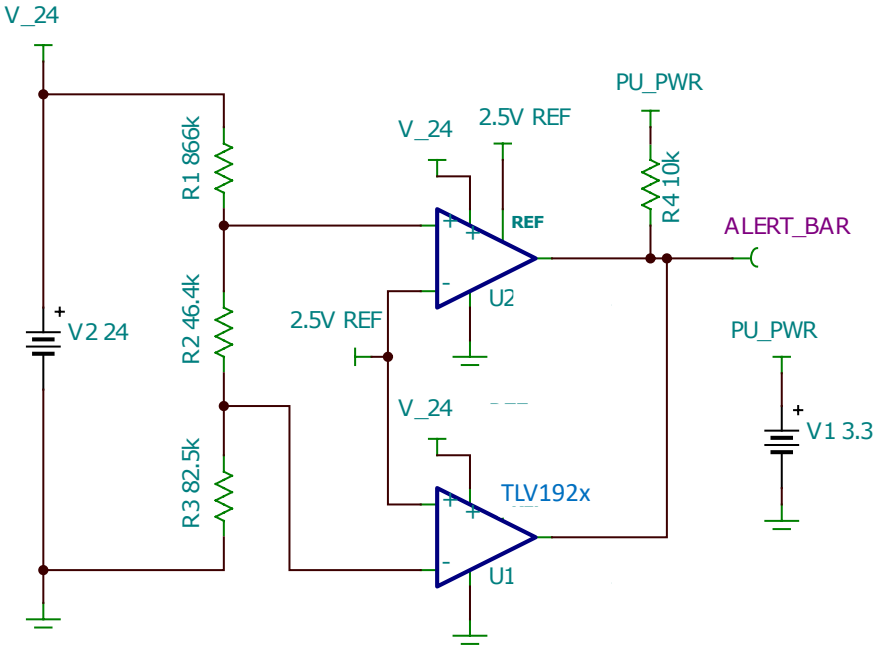


Figure 7-3. Window Comparator

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- ALERT_BAR (logic low output) when the 24V suply is less than 19.2V
- ALERT_BAR (logic low output) when the 24V suply is greater than 30V
- Current dissipated in the resistor string is 30uA
- Comparator operates from the 24V supply that is being monitored

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLV192x is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, ALERT_BAR is pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from 2.5V / 30uA which is approximately 83.3kohms.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from (2.5V /19.2uA) - R3 which is approximately 46.9kohms.

Lastly, the value of R1 is calculated from 1Mohm - (R2 + R3) which is approximately 870kohms. Please note that standard 1% resistor values were selected for the circuit.

The respective comparator outputs (ALERT_BAR) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.

7.2.1.3 Application Curve

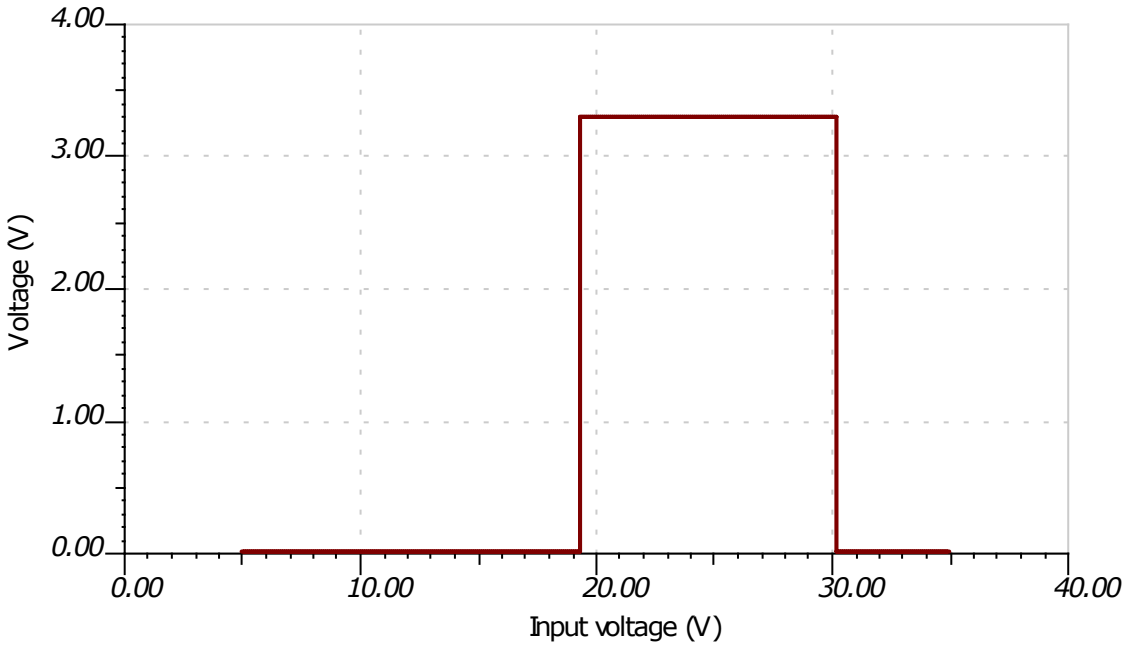


Figure 7-4. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.3 Power Supply Recommendations

For minimum operating voltage of 3.3V, using the internal 2.5V reference directly causes the input common mode voltage range ((V+) - 2V) to be violated. If operation at 3.3V is desired, the 2.5V reference needs to be divided down externally so the voltage is less than (V+) - 2V (or 1.3V in this example). For the dual comparator

where the 2.5V reference is internally connected, the output still operates in a known operating state but does not reflect the differential input condition when both inputs are outside the common mode range.

Furthermore, due to the fast output edge rates, bypass capacitors on the supply pin are critical to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) &(V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output can swing "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications it is important maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and need to be treated as high speed logic devices. The bypass capacitor needs to be as close to the supply pin as possible and connected to a solid ground plane, directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor is added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations are used when routing long distances.

7.4.2 Layout Example

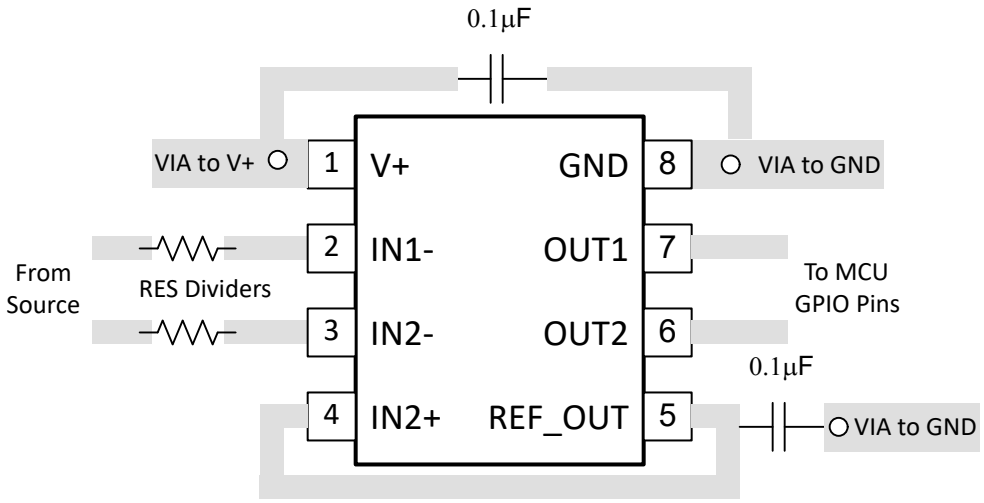


Figure 7-5. Dual Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV1922DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1922
TLV1922DSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1922

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

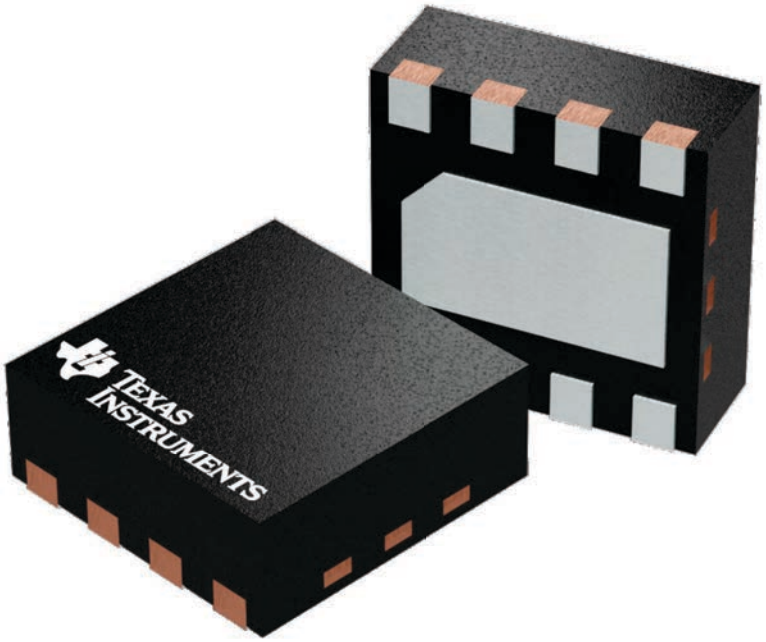
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



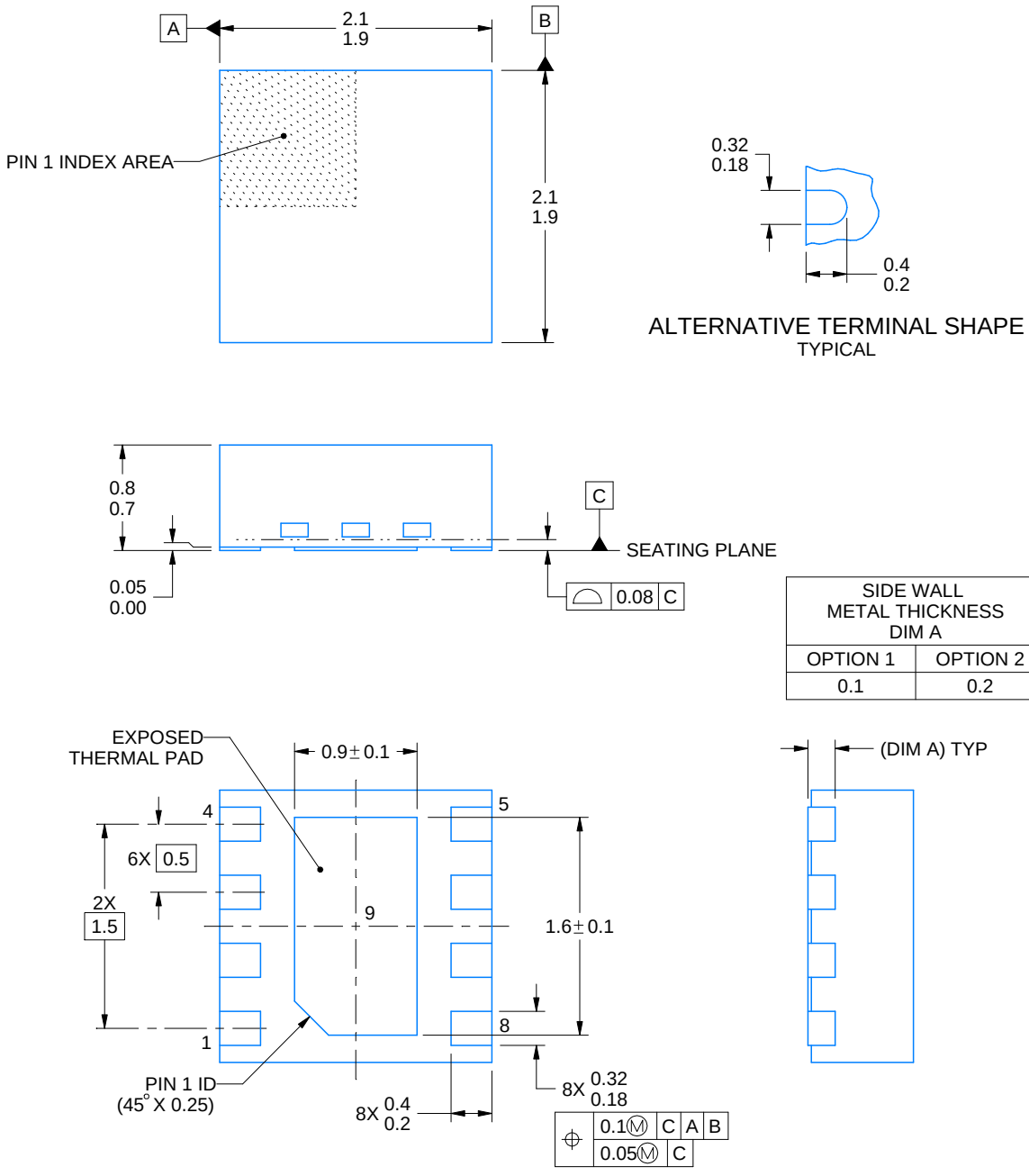
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

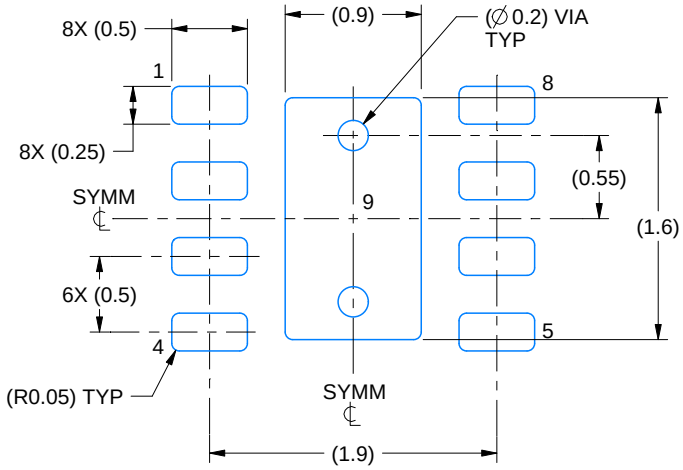
PLASTIC SMALL OUTLINE - NO LEAD



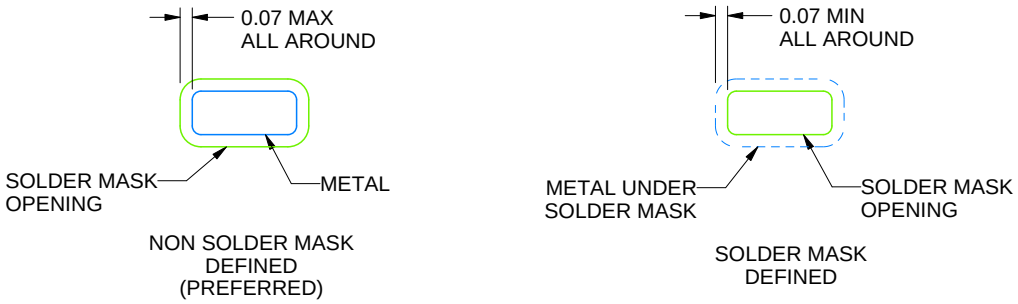
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

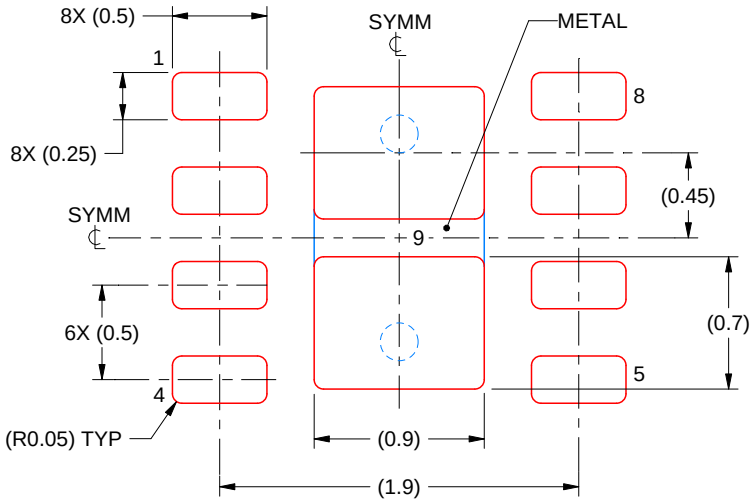


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025