

TLV181x and TLV182x Family of 40V Rail-to-Rail Input Comparators with Push-Pull or **Open-Drain Output Options**

1 Features

- Wide 2.4V to 40V supply range
- Rail-to-rail input
- Power-On Reset (POR) for known start-up
- Low input offset voltage 500µV
- 420ns typical propagation delay
- Low guiescent current 5µA per channel
- Low input bias current 150fA
- Push-pull output option (TLV181x)
- Open-drain output option (TLV182x)
- Full -40°C to +125°C temperature range
- 2 kV ESD protection
- **Functional Safety-Capable**
 - Documentation available to aid functional safety system design

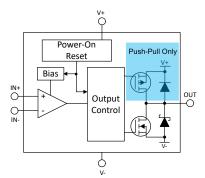
2 Applications

- **Appliances**
- Factory automation and control
- Motor drives
- Infotainment and cluster

3 Description

The TLV181x and TLV182x are a family of 40 volt single, dual and quad channel comparators with multiple output options. The family offers railto-rail inputs with push-pull or open-drain output options. The family has an excellent speed-to-power combination with a propagation delay of 420ns with a full supply voltage range of 2.4V to 40V with a quiescent supply current of only 5µA per channel.

All devices include a Power-On Reset (POR) feature. This makes sure the output is in a known state until



TLV18xx Block Diagram

the minimum supply voltage has been reached before the output responds to the inputs, thus preventing false outputs during system power-up and powerdown.

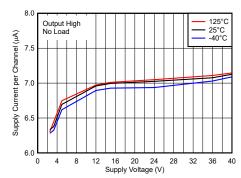
The TLV181x comparators have a push-pull output stage capable of sinking and sourcing milliamps of current when controlling an LED or driving a capacitive load such as a MOSFET gate.

The TLV182x comparators have an open-drain output stage that can be pulled up to 40V independent of comparator supply voltage.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TLV1811,	SC-70 (6)	1.25mm x 2.00mm
TLV1821 (Single)	SOT-23 (5)	1.60mm x 2.90mm
TLV1811L,	SC-70 (5)	1.25mm x 2.00mm
TLV1821L (Single - alt pinout)	SOT-23 (5)	1.60mm x 2.90mm
	SOIC (8)	3.91mm × 4.90mm
TLV1812.	TSSOP (8)	3.00mm × 4.40mm
TLV1822	VSSOP (8)	3.00mm × 3.00mm
(Dual)	WSON (8)	2.00mm × 2.00mm
	SOT-23 (8)	1.60mm × 2.90mm
	SOIC (14)	3.91mm × 8.65mm
TLV1814, TLV1824	TSSOP (14)	4.40mm × 5.00mm
(Quad)	SOT-23 (14)	4.20mm x 2.00mm
	WQFN (16)	3.00mm × 3.00mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



TLV18xx Supply Current vs. Supply Voltage

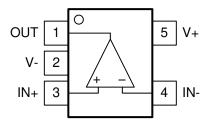


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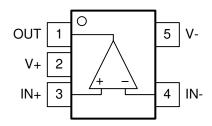
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7.1 Overview			



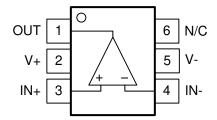
4 Pin Configuration and Functions Pin Functions:TLV18x1 TLV18x1L



TLV18x1 TLV18x1L Standard "North West" pinout DBV, DCK Packages, SOT-23-5, SC-70-5 Top View



TLV1811L and TLV1821L DBV Package,
"LMC72x1/TLV72x1 type" pinout with reversed supplies
SOT-23-5,
Top View



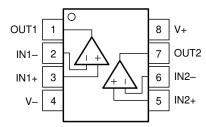
TLV1811L and TLV1821L DCK Package,
"TLV72x1 6-pin type" pinout with reversed supplies and shifted VSC-70-6,
Top View

Table 4-1. Pin Functions: TLV1811, TLV1821, TLV1811L and TLV1821L

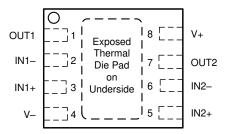
	TLV1811, TLV1821		TLV1811L, TLV1821L PINS		I/O	
NAME	PINS					DESCRIPTION
	SOT-23	SC-70	SOT-23	SC-70		
OUT	1	1	1	1	0	Output
V-	2	2	5	5	-	Negative Supply Voltage
IN+	3	3	3	3	1	Non-Inverting (+) Input
IN-	4	4	4	4	I	Inverting (-) Input
V+	5	5	2	2	-	Positive Supply Voltage
N/C	-	-	-	6	-	No Connection



Pin Functions:TLV1812 and TLV1822



D, DGK, PW, DDF Packages 8-Pin SOIC, VSSOP, TSSOP, SOT-23-8 Top View



NOTE: Connect exposed thermal pad directly to V- pin.

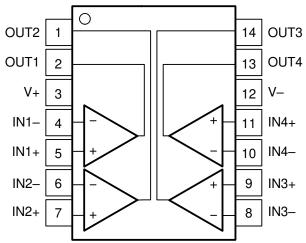
DSG Package, 8-Pad WSON With Exposed Thermal Pad, Top View

Table 4-2. Pin Functions: TLV1812 and TLV1822

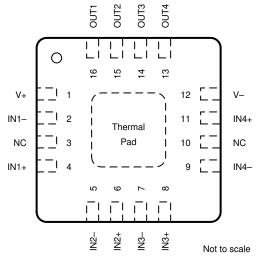
	PIN	I/O	DESCRIPTION			
NAME	NO.	1/0	DESCRIPTION			
OUT1	1	0	Output pin of the comparator 1			
IN1-	2	I	Inverting input pin of comparator 1			
IN1+	3	I	Noninverting input pin of comparator 1			
V-	4	_	Negative (low) supply			
IN2+	5	I	Noninverting input pin of comparator 2			
IN2-	6	- 1	Inverting input pin of comparator 2			
OUT2	7	0	Output pin of the comparator 2			
V+	8	_	Positive supply			
Thermal Pad	_	_	Connect directly to V- pin			



Pin Functions: TLV1814 and TLV1824



D, PW, DYY Package, 14-Pin SOIC, TSSOP, SOT-23, Top View



NOTE: Connect exposed thermal pad directly to V- pin.

RTE Package, 16-Pad WQFN With Exposed Thermal Pad, Top View

Table 4-3. Pin Functions: TLV1814 and TLV1824

PIN		I/O	DESCRIPTION				
NAME	SOIC	WQFN	1/0	DESCRIPTION			
OUT2 ⁽¹⁾	1	15	0	Output pin of the comparator 2			
OUT1 ⁽¹⁾	2	16	0	Output pin of the comparator1			
V+	3	1	_	Positive supply			
IN1-	4	2	I	Negative input pin of the comparator 1			
IN1+	5	4	I	Positive input pin of the comparator 1			
IN2-	6	5	I	Negative input pin of the comparator 2			
IN2+	7	6	I	Positive input pin of the comparator 2			
IN3-	8	7	I	Negative input pin of the comparator 3			
IN3+	9	8	I	Positive input pin of the comparator 3			
IN4-	10	9	I	Negative input pin of the comparator 4			
IN4+	11	11	I	Positive input pin of the comparator 4			
V-	12	12	_	Negative supply			
OUT4	13	13	0	Output pin of the comparator 4			
OUT3	14	14	0	Output pin of the comparator 3			
NC	_	3	_	No Internal Connection - Leave floating or GND			
NC	_	10	_	No Internal Connection - Leave floating or GND			
Thermal Pad	_	PAD	_	Connect directly to V- pin.			

⁽¹⁾ Some manufacturers transpose the names of channels 1 and 2. Electrically the pinouts are identical, just a difference in channel naming convention.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$	-0.3	42	V
Input pins (IN+, IN–) from (V–) (2)	-0.3	(V+) + 0.3	V
Current into Input pins (IN+, IN-)	-10	10	mA
Output (OUT) voltage (Open-Drain) from (V–) ⁽³⁾	-0.3	42	V
Output (OUT) voltage (Push-Pull) from (V–)	-0.3	(V+) + 0.3	V
Output (OUT) current (4) (5) (6)	-10	10	mA
Junction temperature, T _J		150	°C
Storage temperature, T _{stg}	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond the supply rails must be current-limited to 10mA or less.
- (3) Output (OUT) for open drain can be greater than (V+) and inputs (IN+, IN-) as long as within the -0.3V to 42V range
- (4) The output is diode-clamped to (V-) for both output options, and diode clamped to (V+) for the push-pull output option. The open drain version does not have a clamp to V+. Please see the *Outputs* and *ESD Protection* section of the *Application Information* Section for more information.
- (5) Output sinking and sourcing current is internally limited to <35mA when operating within the Absolute Maximum output voltage limits. The Absolute Maximum Output Current limit specified here is the maximum current through the clamp structure when exceeding the supply votlage below (V-) for both output options, or above (V+) for the push-pull option.
- (6) Short-circuit from output to (V–) or (V+). Continuous output short circuits at elevated supply voltages can result in excessive heating and exceeding the maximum allowed junction temperature, leading to eventual device destruction.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V	
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	V	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage: $V_S = (V+) - (V-)$		2.4	40	V
Input voltage range from (V–)		-0.2	(V+) + 0.2	V
Output voltage range from (V–)	Open Drain	-0.2	40	V
Output voltage range from (V–)	Push Pull	-0.2	(V+) + 0.2	V
Ambient temperature, T _A		-40	125	°C



5.4 Thermal Information - Single

THERMAL METRIC(1)		TLV18	TLV18x1 and TLV18x1L			
		DCK (SC-70)	DCK (SC-70)	DBV (SOT-23)	UNIT	
		5 PINS	6 PINS	5 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	226.6	185.6	203.4	°C/W	
R _{0JC(top)}	Junction-to-case (top) thermal resistance	129.5	137.6	105.4	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	76.5	106.6	°C/W	
ΨЈТ	Junction-to-top characterization parameter	51.5	59.8	54.0	°C/W	
ΨЈВ	Junction-to-board characterization parameter	78.3	76.2	106.0	°C/W	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	_	_	_	°C/W	

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.5 Thermal Information - Dual

THERMAL METRIC ⁽¹⁾							
		D (SOIC)	PW (TSSOP)	DDF (SOT-23)	DSG (WSON)	DGK (VSSOP)	UNIT
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	136.1	187.5	170.4	79.9	178.3	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	76.8	76.7	90.3	100.1	66.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79.7	118.1	88.1	46.4	100.0	°C/W
ΨЈТ	Junction-to-top characterization parameter	26.8	14.4	7.5	5.3	9.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.9	116.4	87.6	46.4	98.3	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	_	_	_	21.6	_	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

5.6 Thermal Information - Quad

THERMAL METRIC ⁽¹⁾						
		D (SOIC)	PW (TSSOP)	DYY (SOT-23- THN)	RTE (WQFN)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	104.2	124.1	119.9	53.8	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance	60.3	52.4	60.6	58.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	60.2	67.2	79.0	29.0	°C/W
ΨЈТ	Junction-to-top characterization parameter	20.7	7.5	3.3	2.2	°C/W
ΨЈВ	Junction-to-board characterization parameter	59.8	66.6	41.2	28.9	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	_	_	_	13.1	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.



5.7 Electrical Characteristics

For V_S (Total Supply Votlage) = (V+) - (V-) = 12V, $V_{CM} = V_S / 2$ at $T_A = 25^{\circ}C$ (Unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET V	OLTAGE					
V _{OS}	Input offset voltage		-3	±0.5	3	mV
V _{OS}	Input offset voltage	T _A = -40°C to +125°C	-4		4	mV
dV _{IO} /dT	Input offset voltage drift	T _A = -40°C to +125°C		±1.2		μV/°C
PSRR	Power supply rejection ratio	V _S = 2.4V to 40V, V _{CM} = (V–)		100		dB
POWER SU	JPPLY					
		Output Low, T _A = 25°C TLV1811 Only		6	7.5	
I.	Quiescent current, No	Output Low, T _A = -40°C to +125°C TLV1811 Only			8.5	μA
I _Q	Load	Output High, T _A = 25°C TLV1811 Only		8	10	μΛ
		Output High, T _A = -40°C to +125°C TLV1811 Only			11	
		Output Low, T _A = 25°C		6	7.5	
L	Quiescent current per	Output Low, $T_A = -40^{\circ}C$ to $+125^{\circ}C$			8.5	μΑ
IQ	comparator, No Load	Output High, T _A = 25°C		7	9	μΛ
		Output High, $T_A = -40^{\circ}\text{C}$ to +125°C			10	
V _{POR}	Power On Reset Voltage			1.7		V
INPUT BIA	S CURRENT					
I _B	Input bias current			150		fA
I _B	Input bias current	T _A = -40°C to +125°C	-1.2		1.2	nA
Ios	Input offset current			10		fA
INPUT CAF	PACITANCE					
C _{ID}	Input Capacitance, Differential			2		pF
C _{IC}	Input Capacitance, Common Mode			8		pF
INPUT COI	MMON MODE RANGE					
V _{CM-Range}	Common-mode voltage range	V _S = 2.4V to 40V T _A = -40°C to +125°C	(V-) - 0.2		(V+) + 0.2	V
OUTPUT						
V _{OL}	Voltage swing from (V–)	I _{SINK} = 4mA T _A = -40°C to +125°C			250	mV
V _{OH}	Voltage swing from (V+) (for Push-Pull only)	I _{SOURCE} = 4mA T _A = -40°C to +125°C			250	mV
I _{LKG}	Open-drain output leakage current	V _{ID} = +0.1V, V _{PULLUP} = (V+) T _A = -40°C to +125°C		0.1		nA
I _{OL}	Short-circuit current	Sinking	15	30		mA
I _{OH}	Short-circuit current	Sourcing (for Push-Pull only)	15	30		mA



5.8 Switching Characteristics

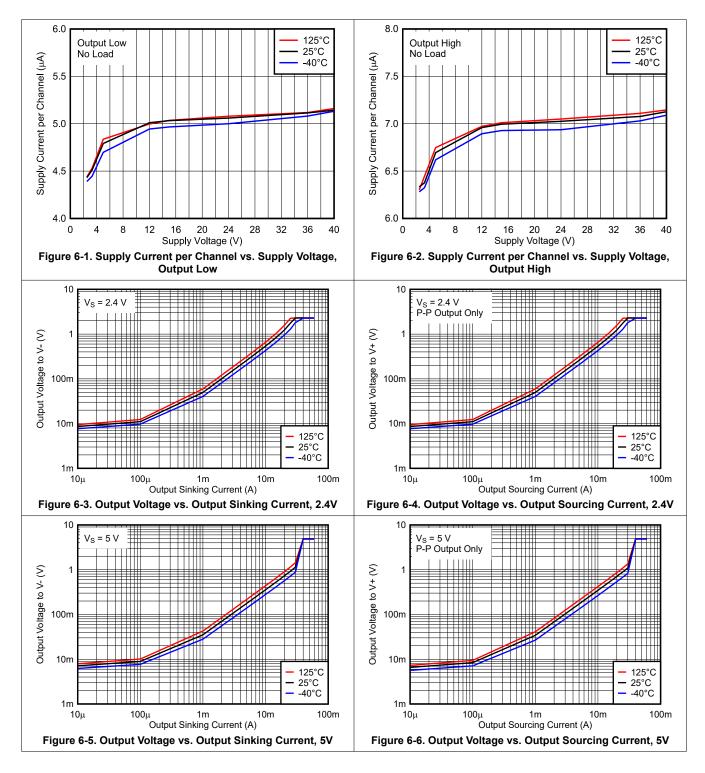
For V_S (Total Supply Voltage) = (V+) - (V-) = 12V, $V_{CM} = V_S / 2$ at $T_A = 25$ °C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
OUTPUT								
T _{PD-HL}	Propagation delay time, high-to-low	V _{OD} = 10mV, C _L = 50pF		900		ns		
T _{PD-HL}	Propagation delay time, high-to-low	V _{OD} = 100mV, C _L = 50pF		450		ns		
T _{PD-LH}	Propagation delay time, low-to- high, push-pull output	V _{OD} = 10mV, C _L = 50pF		900		ns		
T _{PD-LH}	Propagation delay time, low-to- high, push-pull output	V _{OD} = 100mV, C _L = 50pF		420		ns		
T _{RISE}	Output Rise Time, 20% to 80%, push-pull output	C _L = 50pF		15		ns		
T _{FALL}	Output Fall Time, 80% to 20%	C _L = 50pF		15		ns		
F _{TOGGLE}	Toggle Frequency	V _{ID} = 100mV, C _L = 50pF		500		kHz		
POWER C	POWER ON TIME							
P _{ON}	Power on-time			200		μs		



6 Typical Characteristics

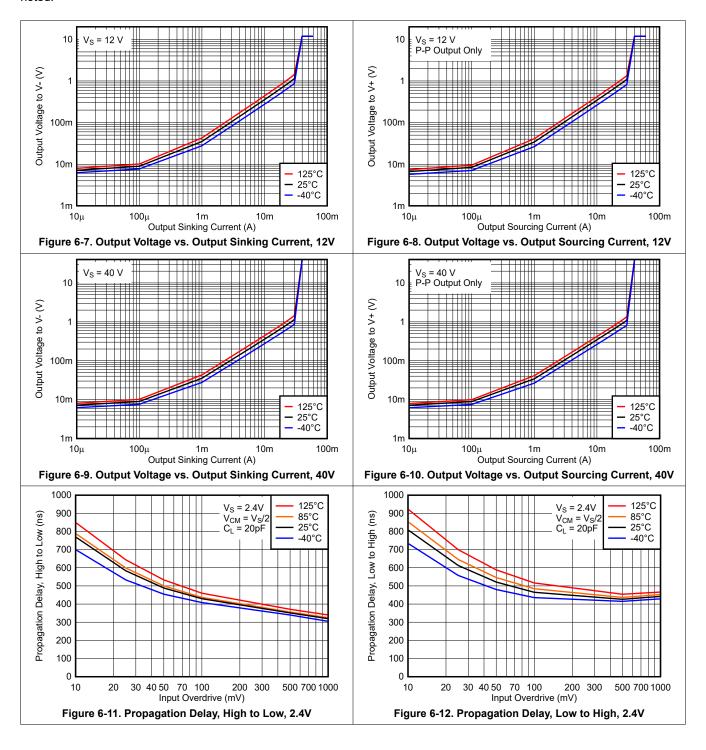
 $T_A = 25$ °C, $V_S = 12$ V, $R_{PULLUP} = 2.5$ k, $C_L = 20$ pF, $V_{CM} = 0$ V, $V_{UNDERDRIVE} = 100$ mV, $V_{OVERDRIVE} = 100$ mV unless otherwise noted.





6 Typical Characteristics (continued)

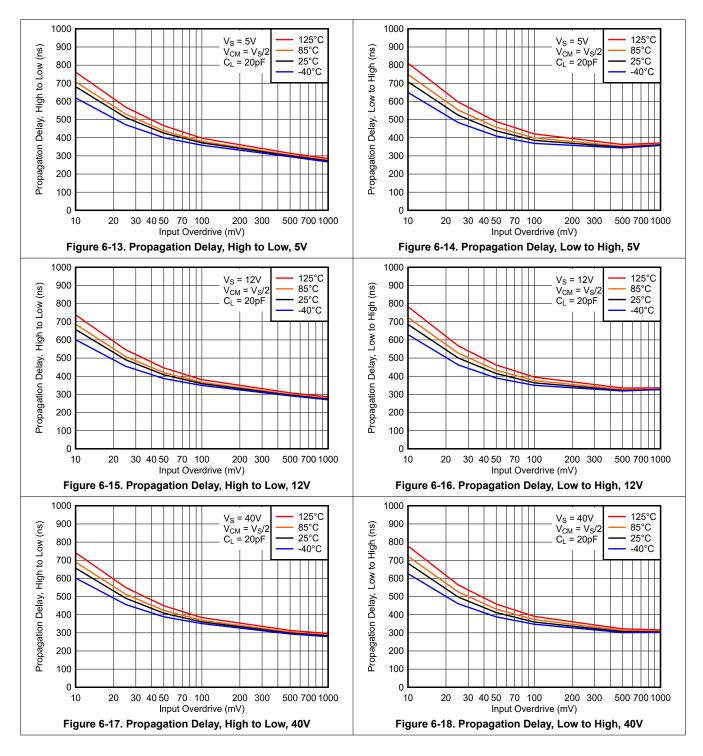
 $T_A = 25$ °C, $V_S = 12$ V, $R_{PULLUP} = 2.5$ k, $C_L = 20$ pF, $V_{CM} = 0$ V, $V_{UNDERDRIVE} = 100$ mV, $V_{OVERDRIVE} = 100$ mV unless otherwise noted.





6 Typical Characteristics (continued)

 $T_A = 25$ °C, $V_S = 12$ V, $R_{PULLUP} = 2.5$ k, $C_L = 20$ pF, $V_{CM} = 0$ V, $V_{UNDERDRIVE} = 100$ mV, $V_{OVERDRIVE} = 100$ mV unless otherwise noted.





7 Detailed Description

7.1 Overview

The TLV181x and TLV182x devices are micro-power comparators with push-pull and open-drain output options. Operating down to 2.4V while only consuming only 5µA per channel, the TLV181x and TLV182x are well suited for portable, automotive and industrial applications. An internal power-on reset circuit is designed so that the output remains in a known state during power-up and power-down.

7.2 Functional Block Diagrams

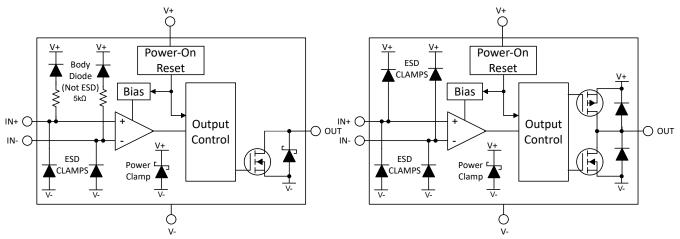


Figure 7-1. TLV182x Open-Drain Block Diagram

Figure 7-2. TLV181x Push-Pull Block Diagram

7.3 Feature Description

TLV18xx Family Options

The TLV18xxy family consists of several output and pinout options, all featuring 40V operation, micro-power 5µA supply currents, 420ns propagation delay, and a Power-On Reset (POR) function.

The TLV18xx family has two output options:

The TLV181x has a push-pull (sink-source) output.

The TLV182x has a **open-drain** (sink only) output, capable of being pulled-up to any voltage up to 40V, independent of comparator supply voltage.

The TLV1811L and TLV1821L are alternate pinouts of the TLV1811 and TLV1821 that allow upgrading older devices such as the TLV7211, TLV7221, LMC7211 and LMC7221 family.

7.4 Device Functional Modes

7.4.1 Inputs

7.4.1.1 TLV18xx Rail-to-Rail Input

The TLV18xx input voltage range extends from 200mV below V- to 200mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

The Rail-to-Rail input does have an ESD clamp to the V+ supply line and therefore the input voltage must not exceed the supply voltages by more than 200mV. TI does not recommend applying signals to the rail to rail inputs with no supply voltage.

7.4.1.2 ESD Protection

The TLV182x open-drain option ESD protection consists of a snapback ESD clamp between the output and V-to allow the output to be pulled above V+ to a maximum of 40V. For the inputs, there is a "lower" ESD clamp between V- and the inputs and there is also a parasitic "upper" ESD soft-clamp diode between the input and V+ with a $5k\Omega$ equivelent resistance (as shown in Figure 7-1). These are not traditional ESD cells and current must be limited to 1mA or less across the this upper diode junction and resistance. External diode clamping is recommended if the input voltage can exceed V+ during operation.

The TLV181x push-pull inputs and output ESD protection contains a conventional diode-type "upper" ESD clamp between the I/O pins and V+, and a "lower" ESD clamp between the I/O pins and V-. The inputs or output must not exceed the supply rails by more than 200mV.

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limiting the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

7.4.1.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even V+ (as long as the input is directly connected to the V+ pin to avoid transients).

7.4.2 Outputs

7.4.2.1 TLV181x Push-Pull Output

The TLV181x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the opposite supply rail (V+ when output "low" or V- when output "High") can result in thermal runaway and eventual device destruction at high (>12 V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs mustbe left floating, and never tied to a supply, ground, or another output.

7.4.2.2 TLV182x Open-Drain Output

The TLV182x features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 40V, independent of the comparator supply voltage (V+). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values can help increase the rising edge rise-time, but at the expense of increasing V_{OL} and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 M Ω) creates an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to V+ can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs can be left floating, or can be tied to the V- pin if floating pins are not desired.



7.4.3 Power-On Reset (POR)

The TLV18xx family has an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 200 μ s after the minimum supply voltage threshold of 2.4V is crossed, or immediately when the supply voltage drops below 2.4V. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV181x push-pull output devices, the output is held low during the POR period (t_{on}).

For the TLV182x open drain output option the POR circuit keeps the output high impedance (Hi-Z) during the POR period (t_{on}).

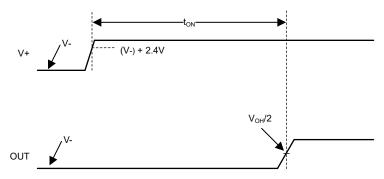


Figure 7-3. Power-On Reset Timing Diagram

Note: The output voltage rises with the pull-up voltage during the POR period.

7.4.4 Hysteresis

The TLV18xx family does not have internal hysteresis. Due to the wide effective bandwidth and low input offset voltage, there is a possibility for the output to "chatter" when the absolute differential voltage is near zero as the comparator triggers on internal wideband noise. This is normal comparator behavior and is expected. TI recommends that the user add external hysteresis if slow moving signals are expected. See Section 8.1.2 in the following section.



8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator Definitions

8.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 8-1 example below, if V_{IN} is less than V_{REF} , the output voltage (V_O) is logic low (V_{OL}) . If V_{IN} is greater than V_{REF} , the output voltage (V_O) is at logic high (V_{OH}) . Table 8-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 8-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V _{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V _{OL})

8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in the Comparator Timing Diagram and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called overdrive (V_{OD}) and underdrive (V_{UD}) voltage levels (see Overdrive and Underdrive Voltage).

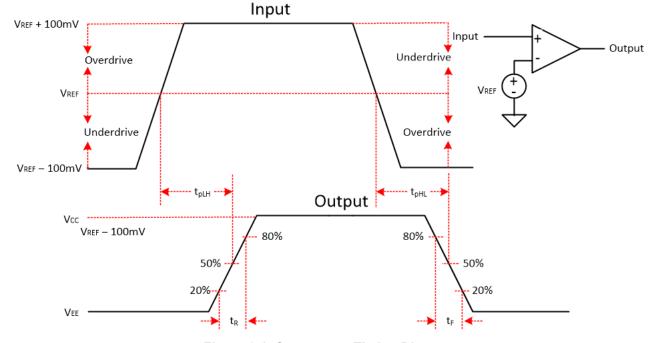


Figure 8-1. Comparator Timing Diagram



8.1.1.3 Overdrive and Underdrive Voltage

The overdrive voltage, V_{OD} , is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 8-1 example. Similarly, underdrive voltage, V_{UD} , is how far below REF the input starts. The overdrive and underdrive voltages influence the propagation delay (t_p). See curves in the Typical Characteristics section for more details. The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes tp to increase. This is particularly important in applications where rail-to-rail input swings are present at the comparator inputs. The result can be skewed propagation delay (difference between t_{PLH} and t_{PHL}). As a low power comparator, TI does not recommend using this comparator family if variation in propagation delay is critical.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

8.1.2 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 8-2. This curve is a function of three components: V_{TH} , V_{OS} , and V_{HYST} :

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip
 point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

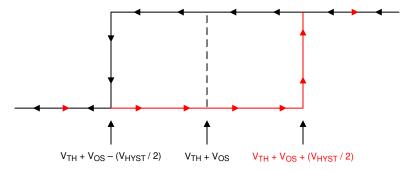


Figure 8-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

8.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 8-3.



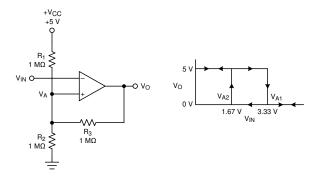


Figure 8-3. TLV181xin an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-3.

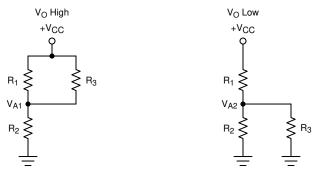


Figure 8-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A , the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 8-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2}$$
 (1)

When V_{IN} is greater than V_A , the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}) .

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)}$$
 (2)

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_{A} = V_{A1} - V_{A2} \tag{3}$$

8.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 8-5,



Figure 8-5. TLV181x in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 8-6.

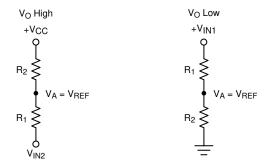


Figure 8-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF} , the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1} .

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF} , the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2} . Use Equation 5 to calculate V_{IN2} .

$$V_{IN2} = \frac{V_{REF} (R1 + R2) - V_{CC} \times R1}{R2}$$
 (5)

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2} , as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2}$$
 (6)

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

8.1.2.3 Inverting and Non-Inverting Hysteresis using Open-Drain Output

An open drain output device, such as the TLV182x, can also be used, but the output pull-up resistor must also be taken into account in the calculations. The pull-up resistor is seen in series with the feedback resistor when the output is high. Thus, the feedback resistor is actually seen as R2 + R_{PULLUP}. TI recommends that the pull-up resistor be at least 10 times less than the feedback resistor value.

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 8-7 shows a simple window comparator circuit. Window comparators require open drain outputs (TLV182x) if the outputs are directly connected together.



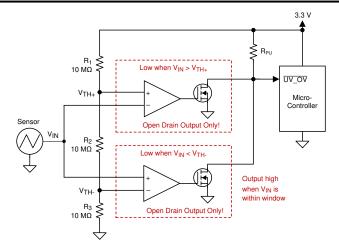


Figure 8-7. Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- UV_Alert (logic low output) when the 24V suply is less than 19.2V
- OV Alert (logic low output) when the 24V suply is greater than 30V
- Current dissipated in the resistor string is 30uA
- Comparator operates from the 5V supply
- 2.5V external reference is utilized

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLC3702-EP is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, OV_Alert and UV_Alert nets are pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from 2.5V / 30uA which is approximately 83.3kohms.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from (2.5V /19.2uA) - R3 which is approximately 46.9kohms.

Lastly, the value of R1 is calculated from 1Mohm - (R2 + R3) which is approximately 870kohms. Please note that standard 1% resistor values are selected for the circuit

The respective comparator outputs (OV_Alert and UV_Alert) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.



8.2.1.3 Application Curve

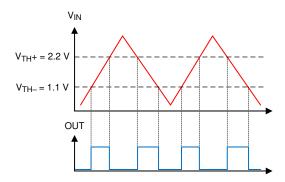


Figure 8-8. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

8.2.2 Square-Wave Oscillator

Square-wave oscillator can be used as low cost timing reference or system supervisory clock source. A push-pull output (TLV181x) is recommended for best symmetry.

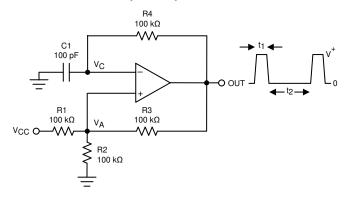


Figure 8-9. Square-Wave Oscillator

8.2.2.1 Design Requirements

The square-wave period is determined by the RC time constant of the capacitor C_1 and resistor R_4 . The maximum frequency is limited by propagation delay of the device and the capacitance load on the output. The low input bias current allows a lower capacitor value and larger resistor value combination for a given oscillator frequency, which helps to reduce BOM cost and board space. TI recommends that R4 be over several kilo-ohms to minimize loading the output.

8.2.2.2 Detailed Design Procedure

The oscillation frequency is determined by the resistor and capacitor values. The following calculation provides details of the steps.



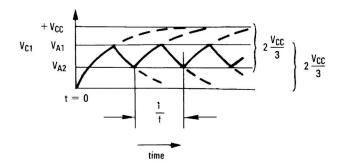


Figure 8-10. Square-Wave Oscillator Timing Thresholds

First consider the output of Figure 8-9 as high, which indicates the inverted input V_C is lower than the noninverting input (V_A) . This causes the C_1 to be charged through R_4 , and the voltage V_C increases until equal to the noninverting input. The value of V_A at the point is calculated by Equation 7.

$$V_{A1} = \frac{V_{CC} \times R_2}{R_2 + R_1 IIR_3} \tag{7}$$

if
$$R_1 = R_2 = R_3$$
, then $V_{A1} = 2V_{CC}/3$

At this time the comparator output trips pulling down the output to the negative rail. The value of V_A at this point is calculated by Equation 8.

$$V_{A2} = \frac{V_{CC}(R_2 IIR_3)}{R_1 + R_2 IIR_3} \tag{8}$$

if
$$R_1 = R_2 = R_3$$
, then $V_{A2} = V_{CC}/3$

The C_1 now discharges though the R_4 , and the voltage V_{CC} decreases until reaching V_{A2} . At this point, the output switches back to the starting state. The oscillation period equals to the time duration from for C_1 from $2V_{CC}/3$ to V_{CC} / 3 then back to $2V_{CC}/3$, which is given by $R_4C_1 \times In 2$ for each trip. Therefore, the total time duration is calculated as $2R_4C_1 \times In 2$.

The oscillation frequency can be obtained by Equation 9:

$$f = 1/(2 R4 \times C1 \times In2)$$
(9)

8.2.2.3 Application Curve

Figure 8-11 shows the simulated results of an oscillator using the following component values:

- $R_1 = R_2 = R_3 = R_4 = 100k\Omega$
- $C_1 = 100pF, C_L = 20pF$
- V+ = 5V, V- = GND
- C_{strav} (not shown) from V_A TO GND = 10pF

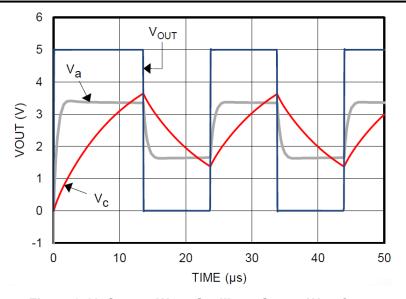


Figure 8-11. Square-Wave Oscillator Output Waveform

8.2.3 Adjustable Pulse Width Generator

Figure 8-12 is a variation on the square wave oscillator that allows adjusting the pulse widths.

R₄ and R₅ provide separate charge and discharge paths for the capacitor C depending on the output state.

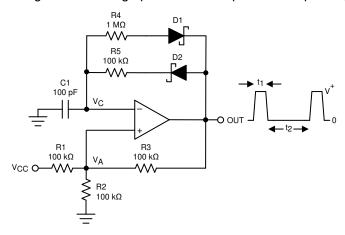


Figure 8-12. Adjustable Pulse Width Generator

The charge path is set through R_5 and D_2 when the output is high. Similarly, the discharge path for the capacitor is set by R_4 and D_1 when the output is low.

The pulse width t_1 is determined by the RC time constant of R_5 and C. Thus, the time t_2 between the pulses can be changed by varying R_4 , and the pulse width can be altered by R_5 . The frequency of the output can be changed by varying both R_4 and R_5 . At low voltages, the effects of the diode forward drop (0.8V, or 0.15V for Shottky) must be taken into account by altering output high and low voltages in the calculations.

8.2.4 Time Delay Generator

The circuit shown in Figure 8-13 provides output signals at a prescribed time interval from a time reference and automatically resets the output low when the input returns to 0V. This is useful for sequencing a "power on" signal to trigger a controlled start-up of power supplies.



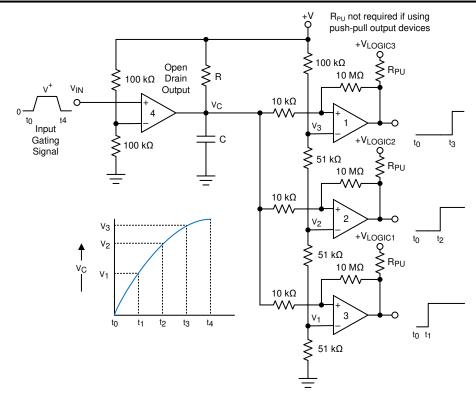


Figure 8-13. Time Delay Generator

Consider the case of V_{IN} = 0. The output of comparator 4 is also at ground, "shorting" the capacitor and holding the node at 0V. This implies that the outputs of comparators 1, 2, and 3 are also at 0V. When an input signal is applied, the output of open drain comparator 4 goes High-Z and C charges exponentially through R. This is indicated in the graph. The output voltages of comparators 1, 2, and 3 switch to the high state in sequence when V_C rises above the reference voltages V_1 , V_2 and V_3 . A small amount of hysteresis has been provided by the $10k\Omega$ and $10M\Omega$ resistors to insure fast switching when the RC time constant is chosen to give long delay times. A good starting point is $R = 100k\Omega$ and $C = 0.01\mu F$ to $1\mu F$.

All outputs immediately go low when V_{IN} falls to 0V, due to the comparator output going low and immediately discharging the capacitor.

Comparator 4 must be a open-drain type output (TLV182x), whereas comparators 1 though 3 can be either open drain or push-pull output, depending on system requirements. R_{PU} is not required for push-pull output devices.

8.2.5 Logic Level Shifter

The output of the TLV182x is the uncommitted drain of the output transistor. Many open-drain outputs can be tied together to provide an output OR'ing function if desired.

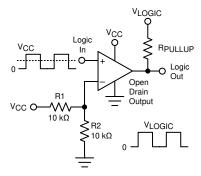


Figure 8-14. Universal Logic Level Shifter



The two $10k\Omega$ resistors bias the input to half of the input logic supply level to set the threshold in the mid-point of the input logic levels. Only one shared output pull-up resistor is needed and can be connected to any pull-up voltage between 0V and 5.5V. The pullup voltage (V_{LOGIC}) must match the driven logic input "high" level.

8.2.6 One-Shot Multivibrator

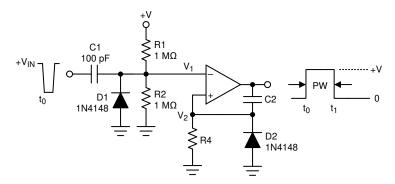


Figure 8-15. One-Shot Multivibrator

A monostable multivibrator has one stable state in which the circuit can remain indefinitely. The circuit can be triggered externally to another quasi-stable state. A monostable multivibrator can thus be used to generate a pulse of desired width.

The desired pulse width is set by adjusting the values of C_2 and R_4 . The resistor divider of R_1 and R_2 can be used to determine the magnitude of the input trigger pulse. The output changes state when $V_1 < V_2$. Diode D_2 provides a rapid discharge path for capacitor C_2 to reset at the end of the pulse. The diode also prevents the non-inverting input from being driven below ground.

8.2.7 Bi-Stable Multivibrator

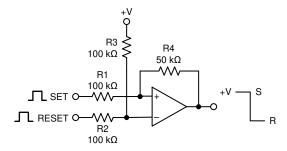


Figure 8-16. Bi-Stable Multivibrator

A bi-stable multivibrator has two stable states. The reference voltage is set up by the voltage divider of R_2 and R_3 . A pulse applied to the SET terminal switches the output of the comparator high. The resistor divider of R_1 and R_2 now sets the non-inverting input to a voltage greater than the reference voltage. A pulse applied to RESET toggles the output low.

8.2.8 Zero Crossing Detector

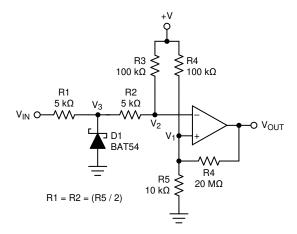


Figure 8-17. Zero Crossing Detector

A voltage divider of R_4 and R_5 establishes a reference voltage V_1 at the non-inverting input. By making the series resistance of R_1 and R_2 equal to R_5 , the comparator output switches when V_{IN} = 0V. Diode D_1 clamps V_3 near ground. The voltage divider of R_2 and R_3 then prevents V_2 from going below ground. A small amount of hysteresis is setup to maintain rapid output voltage transitions.

8.2.9 Pulse Slicer

A Pulse Slicer is a variation of the Zero Crossing Detector and is used to detect the zero crossings on an input signal with a varying baseline level. This circuit works best with symmetrical waveforms. The RC network of R_1 and C_1 establishes an mean reference voltage V_{REF} , which tracks the mean amplitude of the V_{IN} signal. The non-inverting input is directly connected to V_{REF} through R2. R2 and R3 are used to produce hysteresis to keep transitions free of spurious toggles. The time constant is a tradeoff between long-term symmetry and response time to changes in amplitude.

If the waveform is data, the data can be encoded in the recommended NRZ (Non-Return to Zero) format to maintain proper average baseline. Asymmetrical inputs can suffer from timing distortions caused by the changing V_{REF} average voltage.

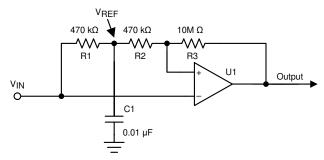


Figure 8-18. Pulse Slicer

For this design, follow these design requirements:

- The RC constant value (R₂ and C₁) must support the targeted data rate to maintain a valid tripping threshold.
- The hysteresis introduced with R₂ and R₄₃ helps to avoid spurious output toggles.

The TLV182x can also be used, but with the addition of a pull-up resistor on the output (not shown for clarity).

Figure 8-19 shows the results of a 9600 baud data signal riding on a varying baseline.

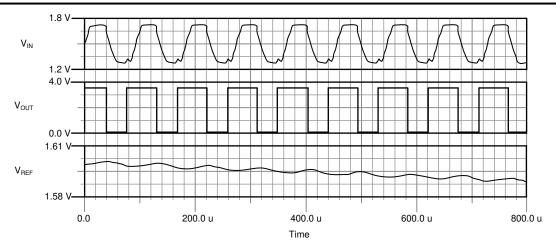


Figure 8-19. Pulse Slicer Waveforms

8.3 Power Supply Recommendations

Due to the fast output edge rates, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR $0.1\mu F$ ceramic bypass capacitor directly between V_{CC} pin and ground pins. Narrow, peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies (V+ and V-), or "single" supplies (V+ and GND), with GND applied to the V- pin. Input signals must stay within the specified input range (between V+ and V-) for either type. Note that with a "split" supply the output swings "low" (V_{OI}) to V- potential and not GND.

8.4 Layout

8.4.1 Layout Guidelines

For accurate comparator applications, a clean, stable power supply is important to minimize output glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the $V_{\rm CC}$ and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V_{CC} or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (\leq 100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations can be used when routing long distances.



8.4.2 Layout Example

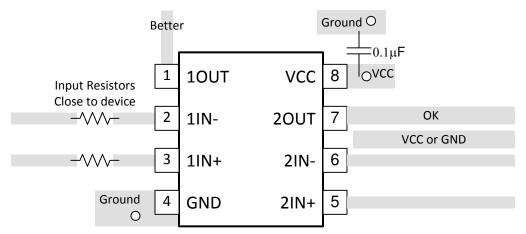


Figure 8-20. Dual Layout Example



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design. Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

Zero crossing detection using comparator circuit - SNOA999

PWM generator circuit - SBOA212

How to Implement Comparators for Improving Performance of Rotary Encoder in Industrial Drive Applications - SNOAA41

A Quad of Independently Func Comparators - SNOA654

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.



10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2024) to Revision E (July 2025)	Page
Restored missing rows and tables	6
Changes from Revision C (September 2023) to Revision D (December 2024)	Page
 Replaced block digram and added graph XX Replaced block diagram and added graph 	
Updated ESD text	14
Changes from Revision B (December 2022) to Revision C (September 2023)	Page
Removed preview for several Duals and Quad SOIC releases	1
Changes from Revision A (November 2022) to Revision B (December 2022)	Page
Removed previews for TLV1811/21 Single releases	1
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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TLV1811DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XJT
TLV1811DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XJT
TLV1811DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XST
TLV1811DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XST
TLV1811LDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XNT
TLV1811LDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XNT
TLV1811LDCKR	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XTT
TLV1811LDCKR.A	Active	Production	SC70 (DCK) 6	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XTT
TLV1812DDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32EF
TLV1812DDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32EF
TLV1812DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31US
TLV1812DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31US
TLV1812DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1812
TLV1812DR.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1812
TLV1812DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	10D
TLV1812DSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	10D
TLV1812PWR	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1812
TLV1812PWR.A	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1812
TLV1814DR	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814D
TLV1814DR.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814D
TLV1814DYYR	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814B1
TLV1814DYYR.A	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1814B1
TLV1814PWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1814B1
TLV1814PWR.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1814B1
TLV1814RTER	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1814B
TLV1814RTER.A	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1814B
TLV1821DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XLT
TLV1821DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XLT





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Orderable part number	Status (1)	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TLV1821DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XUT
TLV1821DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2XUT
TLV1821LDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XMT
TLV1821LDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2XMT
TLV1822DDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32DF
TLV1822DDFR.A	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	32DF
TLV1822DGKR	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31VS
TLV1822DGKR.A	Active	Production	VSSOP (DGK) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	31VS
TLV1822DR	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1822
TLV1822DR.A	Active	Production	SOIC (D) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1822
TLV1822DSGR	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	10E
TLV1822DSGR.A	Active	Production	WSON (DSG) 8	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	10E
TLV1822PWR	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1822
TLV1822PWR.A	Active	Production	TSSOP (PW) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1822
TLV1824DR	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1824D
TLV1824DR.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1824D
TLV1824DYYR	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1824DYY
TLV1824DYYR.A	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV1824DYY
TLV1824PWR	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1824B1
TLV1824PWR.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1824B1
TLV1824RTER	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1824B
TLV1824RTER.A	Active	Production	WQFN (RTE) 16	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T1824B

⁽¹⁾ Status: For more details on status, see our product life cycle.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

PACKAGE OPTION ADDENDUM

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- (4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV1811, TLV1812, TLV1814, TLV1821, TLV1822, TLV1824:

- Automotive: TLV1811-Q1, TLV1812-Q1, TLV1814-Q1, TLV1821-Q1, TLV1822-Q1, TLV1824-Q1
- Enhanced Product: TLV1812-EP, TLV1822-EP

NOTE: Qualified Version Definitions:

- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1811DBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1811DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1811LDBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1811LDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1812DDFR	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1812DGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1812DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1812DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV1812PWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV1814DR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV1814DYYR	SOT-23- THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV1814PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV1814RTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV1821DBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1821DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV1821LDBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV1822DDFR	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV1822DGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1822DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV1822DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV1822PWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV1824DR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV1824DYYR	SOT-23- THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV1824PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV1824RTER	WQFN	RTE	16	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1811DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1811DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV1811LDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1811LDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV1812DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV1812DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV1812DR	SOIC	D	8	3000	353.0	353.0	32.0
TLV1812DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV1812PWR	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV1814DR	SOIC	D	14	3000	353.0	353.0	32.0
TLV1814DYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV1814PWR	TSSOP	PW	14	3000	353.0	353.0	32.0
TLV1814RTER	WQFN	RTE	16	5000	367.0	367.0	35.0
TLV1821DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1821DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV1821LDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV1822DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV1822DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0



PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV1822DR	SOIC	D	8	3000	353.0	353.0	32.0
TLV1822DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV1822PWR	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV1824DR	SOIC	D	14	3000	353.0	353.0	32.0
TLV1824DYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV1824PWR	TSSOP	PW	14	3000	353.0	353.0	32.0
TLV1824RTER	WQFN	RTE	16	5000	367.0	367.0	35.0





- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-178.

- 4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
- 5. Support pin may differ or may not be present.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.





- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.





- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

 4. Falls within JEDEC MO-203 variation AB.





NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC QUAD FLATPACK - NO LEAD



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- 5. Reference JEDEC Registration MO-345, Variation AB





- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
 3. Reference JEDEC MO-203.

- 4. Support pin may differ or may not be present.5. Lead width does not comply with JEDEC.
- 6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side





NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 10. Board assembly site may have different recommendations for stencil design.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.





- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.







- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC SMALL OUTLINE - NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

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- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.





NOTES: (continued)

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NOTES: (continued)

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