10Gbps 1-8 CHANNEL MULTI-RATE SERIAL LINK AGGREGATOR

Check for Samples: TLK10081

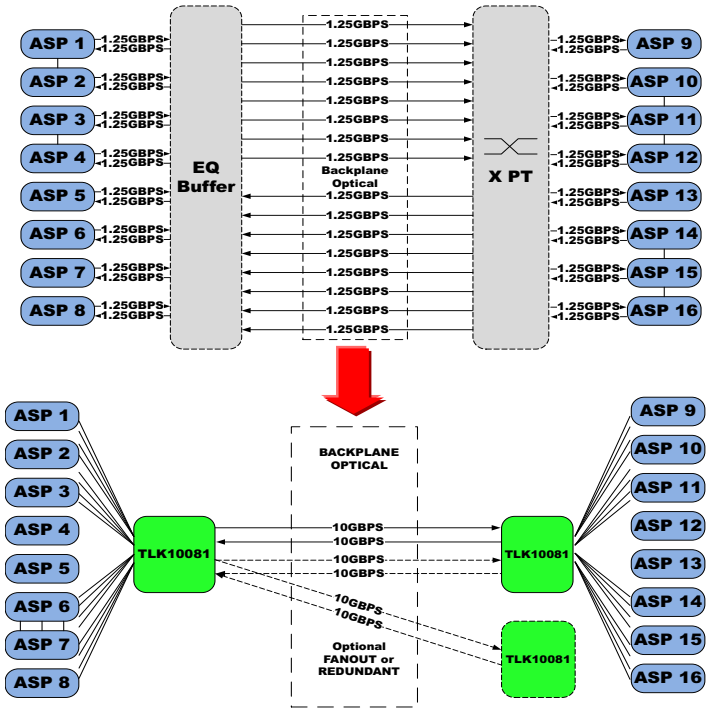
1 INTRODUCTION

1.1 Features

- Automatic Digital Multiplexing/De-Multiplexing of 1 to 8 Independent Lower Speed Gigabit Serial Lines into a Single Higher Speed Gigabit Serial Line with Extensive Media Transmission Capabilities.
- 1~8 x (0.25 to 1.25 Gbps) to 1 x (2 to 10 Gbps) Multiplexing
- 1 x (0.5 to 2.5 Gbps) to 1 x (0.5 to 2.5 Gbps)
- Dynamic Port Aggregation Supported
- Programmable High Speed Redundant Switching
- Wide Data Rate Range for Multiple Application Support
- Transmit De-Emphasis and Adaptive Receiver Equalization on Both Low Speed and High Speed Sides
- MDIO Clause 22 control interface
- 8B/10B ENDEC Coding Support
- Raw (Unencoded) Data Support
- Core Supply 1V; I/O: 1.5V/1.8V
- Superior Signal Integrity Performance
- Low Power Operation: < 800 mW per channel (typ)
- Rate Matching Support (For compatible data protocols like GE PCS)
- Full Non-Blocking Receiver Crosspoint Mapping Capability
- Flexible Clocking
- Multi Drive Capability (SFP+, backplane, cable)
- Support for Programmable High Speed Lane Alignment Characters
- Support for Programmable HS/LS 10-Bit Alignment Characters
- Wide Range of Built-in Test Patterns
- 144-pin, 13mmx13mm FCBGA Package

1.2 Applications

- Gigabit Serial Link Aggregation
- Communications System Backplanes
- Machine Vision
- Video/Image Data Processing



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1.3 Description

The TLK10081 is a multi-rate link aggregator intended for use in high-speed bi-directional point-to-point data transmission systems. The device allows for a reduction in the number of physical links required for a certain data throughput by multiplexing multiple lower-rate serial links into higher-rate serial links.

The TLK10081 has a low-speed interface which can accommodate one to eight bidirectional serial links running at rates from 250 Mbps to 1.25 Gbps (maximum of 10 Gbps total throughput). The device's high speed interfaces can operate at rates from 1 Gbps to 10 Gbps. The high speed interface is designed to run at 8 x the low speed serial rate regardless of the number of lanes connected. Filler data will be placed on any unused lanes in order to keep the interleaved lane ordering constant. This allows for low speed lanes to be hot swapped during normal operation without requiring a change in configuration.

A 1:1 mode is also supported for data rates ranging from 0.5 Gbps to 2.5 Gbps, whereby both low speed and high speed are rate matched. The TX and RX datapaths are also independent, so TX may operate in 8:1 mode while RX operates in 1:1 mode. This independence is restricted to using the same low speed line rate. For example, the TX can operate at 8 x 1.25 Gbps while RX operates at 1 x 1.25 Gbps.

The individual Low Speed lanes may also operate at independent rates in byte interleave mode, provided they are operating at integer multiples. The High Speed line rate must be configured based on the fastest Low Speed line rate.

The device has multiple interleaving/de-interleaving schemes that may be used depending on the data type. These schemes allow for the low speed lane ordering to be recovered after the lanes are transmitted over a single high-speed link. There is also a programmable scrambling/de-scrambling function available to help ensure that the high-speed data has suitable properties for transmission (i.e., sufficient transition density for clock recovery and DC balance over time) even for non-ideal input data.

The TLK10081 has the ability to perform lane alignment on 2, 3, or 4 lanes with up to four bytes of lane de-skew.

Both the low speed and high speed side interfaces (transmitters and receivers) use CML signaling with integrated termination resistors and feature programmable transmitter de-emphasis levels and adaptive receive equalization to help compensate for media impairments at higher frequencies. The device's serial transceivers used are capable of interfacing to optical modules as well as higher-loss connections such as PCB backplanes and controlled-impedance copper cabling.

To aid in system synchronization, the TLK10081 is capable of extracting clocking information from the serial input data streams and outputting a recovered clock signal. This recovered clock can be input to a jitter cleaner in order to provide a synchronized system clock. The device also has two reference clock input ports and a flexible internal PLL, allowing for various serial rates to be supported with a single reference clock input frequency.

The device has various built-in self-test features to aid with system validation and debugging. Among these are pattern generation and verification on all serial lanes as well as internal data loopback paths.

2 PHYSICAL CHARACTERISTICS

2.1 Block Diagram

A simplified block diagram of the TLK10081 device for 8:1 mode is shown in Figure 2-1 and Figure 2-2. This low-power transceiver consists of two serializer/deserializer (SERDES) blocks, one on the low speed side and the other on the high speed side. The core logic block that lies between the two SERDES blocks carries out all the logic functions including test pattern generation and verification.

The TLK10081 provides a management data input/output (MDIO) control interface as well as a JTAG interface for device configuration, control, and monitoring. Detailed descriptions of the TLK10081 pin functions are provided in Figure 2-1.

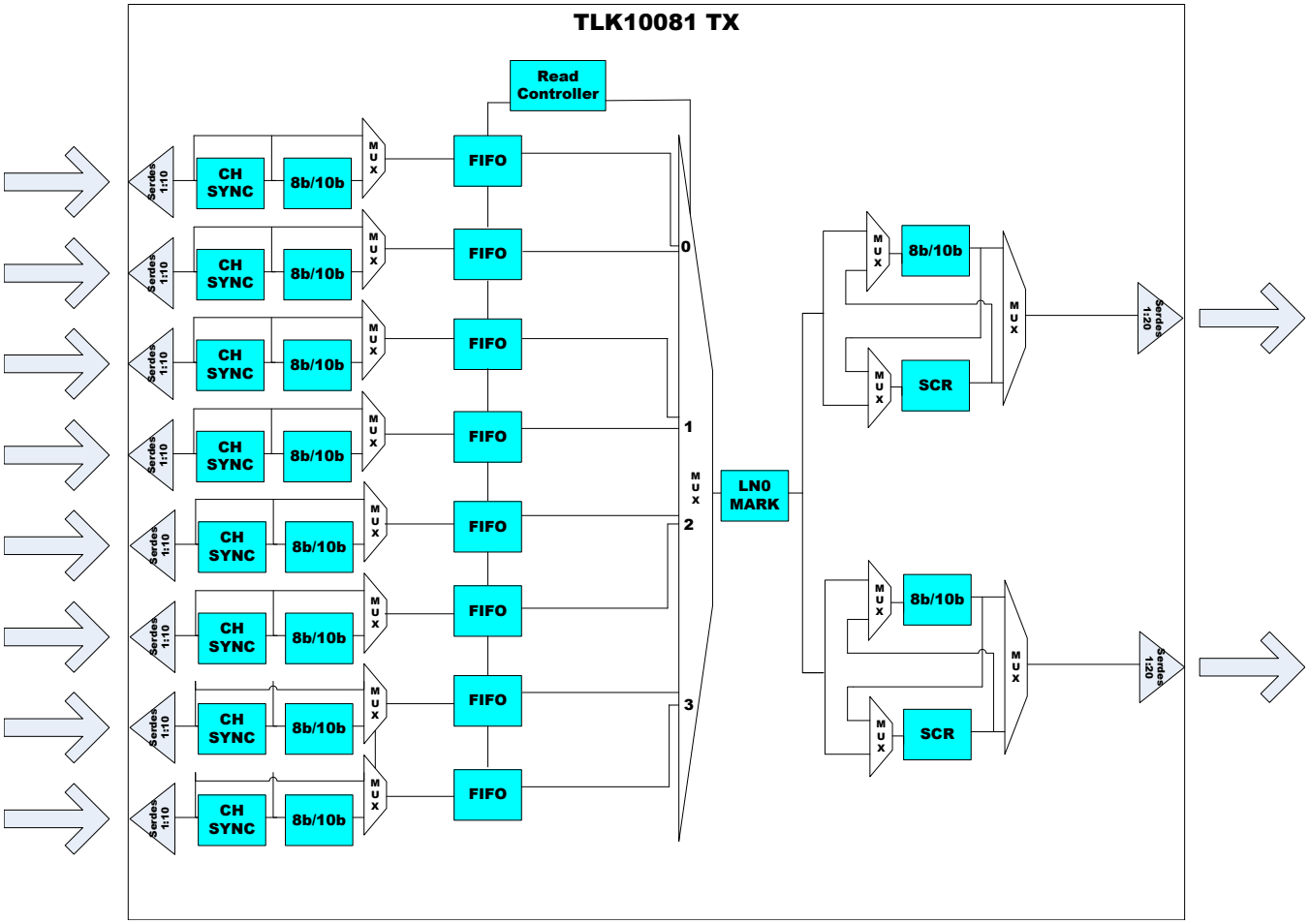


Figure 2-1. A Simplified Block Diagram of the TLK10081 (TX)

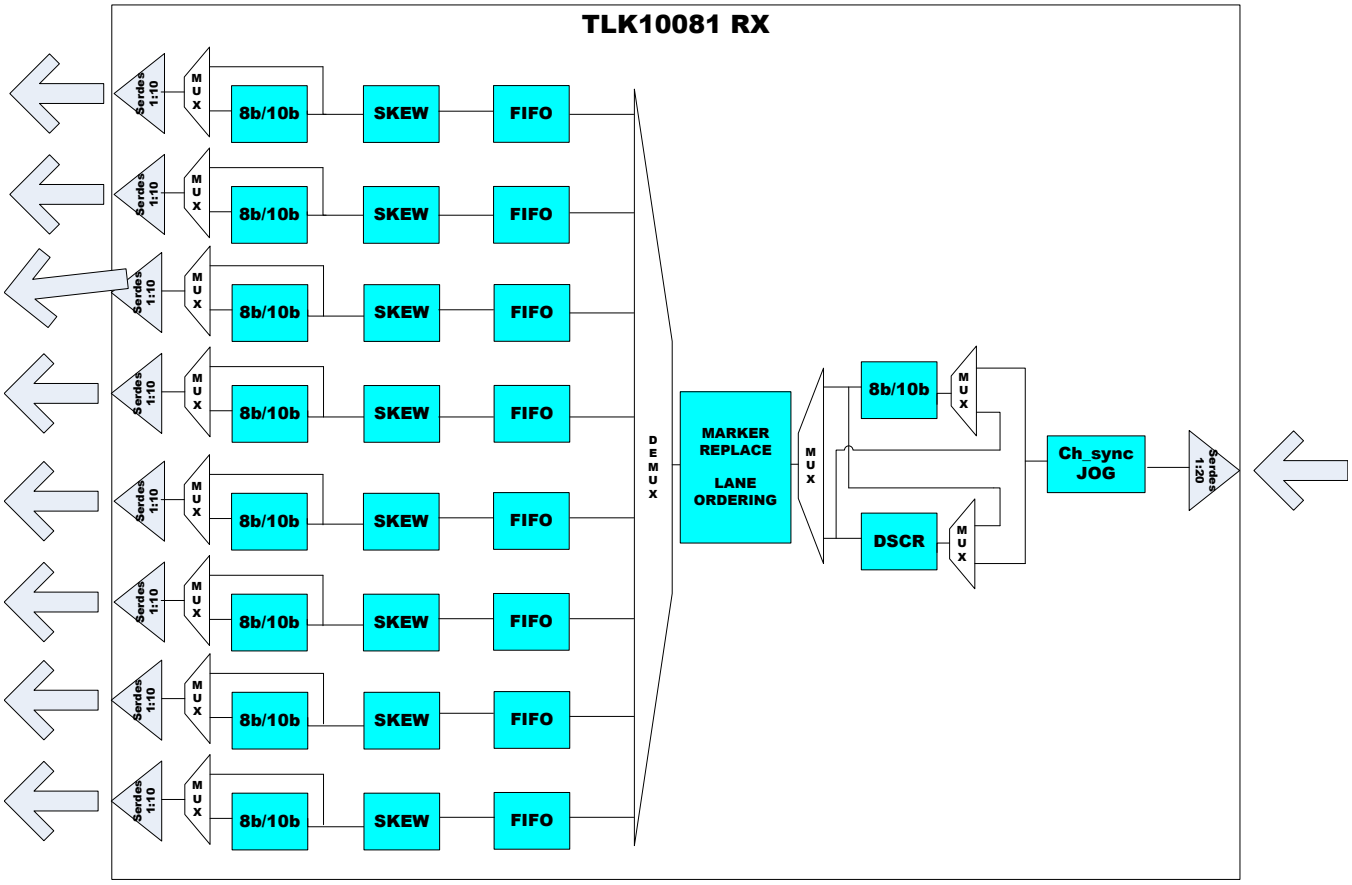


Figure 2-2. A Simplified Block Diagram of the TLK10081 (RX)

2.2 Package

A 13-mm x 13-mm, 144-pin PBGA package with a ball pitch of 1 mm is used. The device pin-out is as shown in Figure 2-3 and is described in detail in Table 2-1 and Table 2-2.

	1	2	3	4	5	6	7	8	9	10	11	12
A	INA1P	VSS	INA0N	INA0P	VSS	OUTA0P	OUTA0N	PDTRXA_N	CLKOUTBP	CLKOUTBN	VSS	HSRXAN
B	INA1N	INA2P	VSS	VSS	OUTA1P	OUTA1N	VSS	TMS	PRBSEN	RXCTRL_0	VSS	HSRXAP
C	VSS	INA2N	VDDRA_LS	OUTA2P	OUTA2N	VSS	VDDO0	TDI	CLKOUTAP	CLKOUTAN	AMUXA	VSS
D	INA3P	VDDA_LS	VSS	AMUXB	VSS	TDO	VPP	TCK	GPO0	VSS	VSS	HSTXAP
E	INA3N	VSS	OUTA3N	VSS	TRST_N	VDDD	DVDD	VDDD	LOSA	PRTAD0	VDDRA_HS	HSTXAN
F	VSS	VDDA_LS	OUTA3P	VDDT_LS	VSS	VDDD	DVDD	VSS	VDDT_HS	VSS	VDDA_HS	VSS
G	VSS	VDDA_LS	VSS	VDDT_LS	VSS	DVDD	VSS	DVDD	PRTAD1	VDDA_HS	VSS	HSRXBN
H	INA4P	VSS	OUTA4N	VSS	RESET_N	VDDD	DVDD	VDDD	GPO1	REFCLK_SEL	VSS	HSRXBP
J	INA4N	VDDA_LS	OUTA4P	PDTRXB_N	VSS	PRTAD3	MDIO	MDC	PRBS_PASS	GPI0	VDDRB_HS	VSS
K	VSS	INA5P	VDDRB_LS	OUTA5N	OUTA5P	VSS	VDDO1	LOSB	REFCLK1P	REFCLK1N	VSS	HSTXBP
L	INA6P	INA5N	VSS	VSS	OUTA6N	OUTA6P	VSS	RXCTRL_1	PRTAD2	TESTEN	VSS	HSTXBN
M	INA6N	VSS	INA7P	INA7N	VSS	OUTA7N	OUTA7P	PRTAD4	GPI1	REFCLK0P	REFCLK0N	VSS

Figure 2-3. The Pin-Out of the TLK10081

2.3 Terminal Functions

The details of the terminal functions of the TLK10081 device are provided in Table 2-1 and Table 2-2.

Table 2-1. Pin Description - Signal Pins

TERMINAL		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
CHANNEL A			
HSTXAP HSTXAN	D12 E12	Output CML VDDA_HS	**High Speed Transmit Channel A Output.** HSTXAP and HSTXAN comprise the high speed side transmit direction Channel A differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXAP HSRXAN	B12 A12	Input CML VDDA_HS	**High Speed Receive Channel A Input.** HSRXAP and HSRXAN comprise the high speed side receive direction Channel A differential serial input signal. These CML input signals must be AC coupled.
INA[7:0]P/N	M3/M4 L1/M1 K2/L2 H1/J1 D1/E1 B2/C2 A1/B1 A4/A3	Input CML VDDA_LS	**Low Speed Channel A Inputs.** INAP and INAN comprise the low speed side transmit direction differential input signals. These signals must be AC coupled.
OUTA[7:0]P/N	M7/M6 L6/L5 K5/K4 J3/H3 F3/E3 C4/C5 B5/B6 A6/A7	Output CML VDDA_LS	**Low Speed Channel A Outputs.** OUTAP and OUTAN comprise the low speed side receive direction differential output signals. During device reset (RESET_N asserted low) these pins are driven differential zero. These signals must be AC coupled.
LOSA	E9	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	C**hannel A Receive Loss Of Signal (LOS) Indicator.** LOSA=0: Signal detected. LOSA=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXAP/N has a differential input signal swing of ≤75 mV_{pp}, LOSA will be asserted (if enabled). If the input signal is greater than 150 mV_{p-p}, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSA real-time, configured via MDIO During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXA_N asserted low), this pin is floating. During register based power down, this pin is floating. It is highly recommended that LOSA be brought to an easily accessible point on the application board (header) in the event that debug is required.
RXCTRL_0	B10	Input LVCMOS 1.5V/1.8V VDDO0	**Channel A Bit Interleave Lane Rotation Jog.** A toggle of this pin, either from high to low or from low to high, causes a lane rotation of the HSRXAP/N source data.
GPO0	D9	Output LVCMOS 1.5V/1.8V VDDO0 40Ω Driver	**Channel A Multi-purpose Status Indicator.** This pin should be left unconnected in the device application.
PDTRXA_N	A8	Input LVCMOS 1.5V/1.8V VDDO0	**Transceiver Power Down.** When this pin is held low (asserted), the device is placed in power down mode. When deasserted, the device operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
CHANNEL B (High Speed Interface Only)			
HSTXBP HSTXBN	K12 L12	Output CML VDDA_HS	**Serial Transmit Channel B Output.** HSTXBP and HSTXBN comprise the high speed side transmit direction Channel B differential serial output signal. During device reset (RESET_N asserted low) these pins are driven differential zero. These CML outputs must be AC coupled.
HSRXBP HSRXBN	H12 G12	Input CML VDDA_HS	**Serial Receive Channel B Input.** HSRXBP and HSRXBN comprise the high speed side receive direction Channel B differential serial input signal. These CML input signals must be AC coupled.

Table 2-1. Pin Description - Signal Pins (continued)

TERMINAL		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
LOSB	K8	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Channel B Receive Loss of Signal (LOS) Indicator.** LOSB=0: Signal detected. LOSB=1: Loss of signal. Loss of signal detection is based on the input signal level. When HSRXBP/N has a differential input signal swing of ≤75 mVpp, LOSB will be asserted (if enabled). If the input signal is greater than 150 mVp-p, LOS will be deasserted. Outside of these ranges, the LOS indication is undefined. Other functions can be observed on LOSB real-time, configured via MDIO. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXB_N asserted low), this pin is floating. During register based power down, this pin is floating. It is highly recommended that LOSB be brought to an easily accessible point on the application board (header) in the event that debug is required.
RXCTRL_1	L8	Input LVCMOS 1.5V/1.8V VDDO1	**Channel B Bit Interleave Lane Rotation Jog.** A toggle of this pin, either from high to low or from low to high, causes a lane rotation of the HSRXBP/N source data.
GPO1	H9	Output LVCMOS 1.5V/1.8V VDDO1 40Ω Driver	**Channel B General Purpose Output.** This pin should be left unconnected in the device application.
PDTRXB_N	J4	Input LVCMOS 1.5V/1.8V VDDO1	**Transceiver Power Down.** When this pin is held low (asserted), Channel B is placed in power down mode. When deasserted, Channel B operates normally. After deassertion, a software data path reset should be issued through the MDIO interface.
REFERENCE CLOCKS AND CONTROL AND MONITORING SIGNALS			
REFCLK0P/N	M10 / M11	Input LVDS/LVPECL DVDD	**Reference Clock Input Zero.** This differential input is a clock signal used as a reference to one or both channels.The reference clock selection is done through MDIO or REFCLKA_SEL and REFCLKB_SEL pins. This input signal **must** be AC coupled. If unused, REFCLK0P/N should be pulled down to GND through a shared 100 ohm resistor.
REFCLK1P/N	K9 / K10	Input LVDS/LVPECL DVDD	**Reference Clock Input One.** This differential input is a clock signal used as a reference to one or both channels. The reference clock selection is done through MDIO. This input signal **must** be AC coupled. If unused, REFCLK1P/N should be pulled down to GND through a shared 100 ohm resistor.
REFCLK_SEL	H10	Input LVCMOS 1.5V/1.8V VDDO0	**Reference Clock Select.** This input, when low, selects REFCLK0P/N as the clock reference to Channel A/B SERDES. When high, REFCLK1P/N is selected as the clock reference to Channel A/B SERDES. If software control is desired, this input signal should be tied low. Default reference clock for Channel A/B is REFCLK0P/N.
CLKOUTAP/N CLKOUTBP/N	C9/C10 A9/A10	Output CML DVDD	**Channel A/B Output Clock.** By default, this output is enabled and outputs the high speed side Channel A recovered byte clock (high speed line rate divided by 20). Optionally it can be configured to output the VCO clock divided by 2. Additional MDIO-selectable divide ratios of 1, 2, 4, 5, 8, 10, 16, 20, and 25 are available. See Figure 5-1. These CML outputs must be AC coupled. During device reset (RESET_N asserted low) these pins are driven differential zero. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), these pins are floating. During register based power down, these pins are floating.
PRBSEN	B9	Input LVCMOS 1.5V/1.8V VDDO0	**Enable PRBS:** When this pin is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of both channels. This signal is logically OR'd with MDIO register bits A.13:12, and B.13:12. PRBS 2^{31}-1 is selected by default, and can be changed through MDIO.
PRBS_PASS	J9	Output LVCMOS /1.8V VDDO1 40Ω Driver	**Receive PRBS Error Free (Pass) Indicator.** When PRBS test is enabled (PRBSEN=1): PRBS_PASS=1 indicates that PRBS pattern reception is error free. PRBS_PASS=0 indicates that a PRBS error is detected. The channel, high speed or low speed side, and lane (for low speed side) that this signal refers to is chosen through MDIO register bits 0.3:0. During device reset (RESET_N asserted low) this pin is driven low. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register based power down, this pin is floating. It is highly recommended that PRBS_PASS be brought to easily accessible point on the application board (header), in the event that debug is required.

Table 2-1. Pin Description - Signal Pins (continued)

TERMINAL		DIRECTION TYPE SUPPLY	DESCRIPTION
SIGNAL	BGA		
PRTAD[4:0]	M8 J6 L9 G9 E10	Input LVCMOS 1.5V/1.8V VDDO[1:0]	**MDIO Port Address.** Used to select the MDIO port address. The TLK10081 will respond if the port address field on MDIO protocol (PA[4:0]) matches PRTAD[4:0].)
RESET_N	H5	Input LVCMOS 1.5V/1.8V VDDO01	**Low True Device Reset.** RESET_N must be held asserted (low logic level) for at least 10µs after device power stabilization.
MDC	J8	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO1	**MDIO Clock Input.** Clock input for the Clause 22 MDIO interface. Note that an external pullup is generally not required on MDC.
MDIO	J7	Input/Output LVCMOS 1.5V/1.8V VDDO1 25Ω Driver	**MDIO Data I/O.** MDIO interface data input/output signal for the Clause 22 MDIO interface. This signal must be externally pulled up to VDDO using a 2kΩ resistor. During device reset (RESET_N asserted low) this pin is floating. During software initiated power down the management interface remains active for control register writes and reads. Certain status bits are not deterministic as their generating clock source may be disabled as a result of asserting either power down input signal. During pin based power down (PDTRXA_N and PDTRXB_N asserted low), this pin is floating. During register based power down (1.15 asserted high both channels), this pin is driven normally.
TDI	C8	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pullup)	**JTAG Input Data.** TDI is used to serially shift test data and test instructions into the device during the operation of the test port. In system applications where JTAG is not implemented, this input signal may be left floating. During pin based power down (PDTRXA_N **and** PDTRXB_N asserted low), this pin is not pulled up. During register based power down, (1.15 asserted high both channels), this pin is pulled up normally.
TDO	D6	Output LVCMOS 1.5V/1.8V VDDO0 50Ω Driver	**JTAG Output Data.** TDO is used to serially shift test data and test instructions out of the device during the operation of the test port. When the test port is not in use, TDO is in a high impedance state. During device reset (RESET_N asserted low) this pin is floating. During pin based power down (PDTRXA_N **and** PDTRXB_N asserted low), this pin is not pulled up. During register based power down, (1.15 asserted high both channels), this pin is pulled up normally.
TMS	B8	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pullup)	**JTAG Mode Select.** TMS is used to control the state of the internal test-port controller. In system applications where JTAG is not implemented, this input signal can be left unconnected. During pin based power down (PDTRXA_N **and** PDTRXB_N asserted low), this pin is not pulled up. During register based power down, (1.15 aserted high both channels), this pin is pulled up normally.
TCK	D8	Input LVCMOS with Hysteresis 1.5V/1.8V VDDO0	**JTAG Clock.** TCK is used to clock state information and test data into and out of the device during boundary scan operation. In system applications where JTAG is not implemented, this input signal should be grounded.
TRST_N	E5	Input LVCMOS 1.5V/1.8V VDDO0 (Internal Pulldown)	**JTAG Test Reset.** TRST_N is used to reset the JTAG logic into system operational mode. This input can be left unconnected in the application and is pulled down internally, disabling the JTAG circuitry. If JTAG is implemented on the application board, this signal should be deasserted (high) during JTAG system testing, and otherwise asserted (low) during normal operation mode. During pin based power down (PDTRXA_N **and** PDTRXB_N asserted low), this pin is not pulled down. During register based power down (1.15 asserted high both channels), this pin is pulled down normally.
TESTEN	L10	Input LVCMOS 1.5V/1.8V VDDO1	**Test Enable.** This signal is used during the device manufacturing process. It should be grounded through a resistor in the device application board.
GPI0	J10	Input LVCMOS 1.5V/1.8V VDDO1	**General Purpose Input Zero.** This signal is used during the device manufacturing process. It should be grounded through a resistor on the device application board.
GPI1	M9	Input LVCMOS 1.5V/1.8V VDDO1	**General Purpose Input One.** This signal is used during the device manufacturing process. It should be grounded through a resistor on the device application board.
AMUXA	C11	Analog I/O	**SERDES Channel A Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.
AMUXB	D4	Analog I/O	**SERDES Channel B Analog Testability I/O.** This signal is used during the device manufacturing process. It should be left unconnected in the device application.

Table 2-2. Pin Description - Power Pins

TERMINAL		TYPE	DESCRIPTION
SIGNAL	BGA		
VDDA_LS/HS	D2, F2, G2, J2, F11, G10	Power	**SERDES Analog Power.** VDDA_LS and VDDA_HS provide supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board.
VDDT_LS/HS	F4, G4, F9	Power	**SERDES Analog Power.** VDDT_LS and VDDT_HS provide termination and supply voltage for the analog circuits on the low-speed and high-speed sides respectively. 1.0V nominal. Can be tied together on the application board.
VDDD	E6, E8, F6, H6, H8	Power	**SERDES Digital Power.** VDDD provides supply voltage for the digital circuits internal to the SERDES. 1.0V nominal.
DVDD	E7, F7, G6, G8, H7	Power	**Digital Core Power.** DVDD provides supply voltage to the digital core. 1.0V nominal.
VDDRA_LS, VDDRB_LS	C3, K3	Power	**SERDES Analog Regulator Power.** VDDRA_LS and VDDRB_LS provide supply voltage for the internal PLL regulator for the low speed side. 1.5V or 1.8V nominal.
VDDRA_HS	E11	Power	**SERDES Analog Regulator Power.** VDDRA_HS provides supply voltage for the internal PLL regulator for high speed Channel A. 1.5V or 1.8V nominal.
VDDRB_HS	J11	Power	**SERDES Analog Regulator Power** VDDRB_HS provides supply voltage for the internal PLL regulator for high speed Channel B. 1.5V or 1.8V nominal.
VDDO[1:0]	K7, C7	Power	**LVCMOS I/O Power.** VDDO0 and VDDO1 provide supply voltage for the LVCMOS inputs and outputs. 1.5V or 1.8V nominal. Can be tied together on the application board.
VPP	D7	Power	**Factory Program Voltage.** Used during device manufacturing. The application must connect this power supply directly to DVDD.
VSS	A2, A5, A11, B3, B4, B7, B11, C1, C6, C12, D3, D5, D10, D11, E2, E4, F1, F5, F8, F10, F12, G1, G3, G5, G7, G11, H2, H4, H11, J5, J12, K1, K6, K11, L3, L4, L7, L11, M2, M5, M12	Ground	**Ground.** Common analog and digital ground.

3 FUNCTIONAL DESCRIPTION

The TLK10081 allows for high-speed interleaving/de-interleaving of 1 to 8 serial data streams to aggregate them into a single physical link. The data processing required to support this functionality is detailed in the following subsections.

3.1 Transmit (Interleaving) Direction

Two configurations for TLK10081 transmit data path with the device configured to operate in the normal transceiver (mission) mode are shown in Figure 3-1 and Figure 3-2.

In the transmit direction, the lower-rate serial lanes to be interleaved are first received by a deserializer (one per lane) capable of resolving data at up to 5 Gbps. This deserialized data can be optionally aligned to 10-bit word boundaries (based on a user-defined 10-bit alignment character) and optionally 8b/10b decoded. If these functions are not relevant to the data being received, they can be bypassed. The received data on each is input to a FIFO in order to compensate for phase differences between the low speed serial links and the high speed side of the chip. This FIFO is also capable of clock tolerance compensation if needed.

The high speed side can then aggregate the data in one of two ways – (1) word interleaving or (2) bit interleaving. If word interleaving is chosen, the low speed data streams are interleaved in a round-robin fashion 10 bits at a time. If bit interleaving is chosen, the interleaving is performed on a bit-by-bit basis. In either case, provisions need to be taken so that the far-end receiver is able to correctly identify the lane assignments. This is handled by the device's lane ordering logic, described in Section 3.3.

The high-speed aggregate data stream can then be optionally 8b/10b encoded and optionally scrambled by a polynomial scrambling function. These functions provide different ways of ensuring the high speed serial output can be received properly by a device at the other end of the link (by increasing the transition density and by giving a more even distribution of high and low levels). Note that if both the encoding and scrambling functions are used, the user can determine whether to first encode the data and then scramble or to first scramble the data and then encode. If the latter option is chosen, scrambling is not performed on control codes (Kx.x). The resulting data is then output by a serializer capable of data rates up to 10 Gbps.

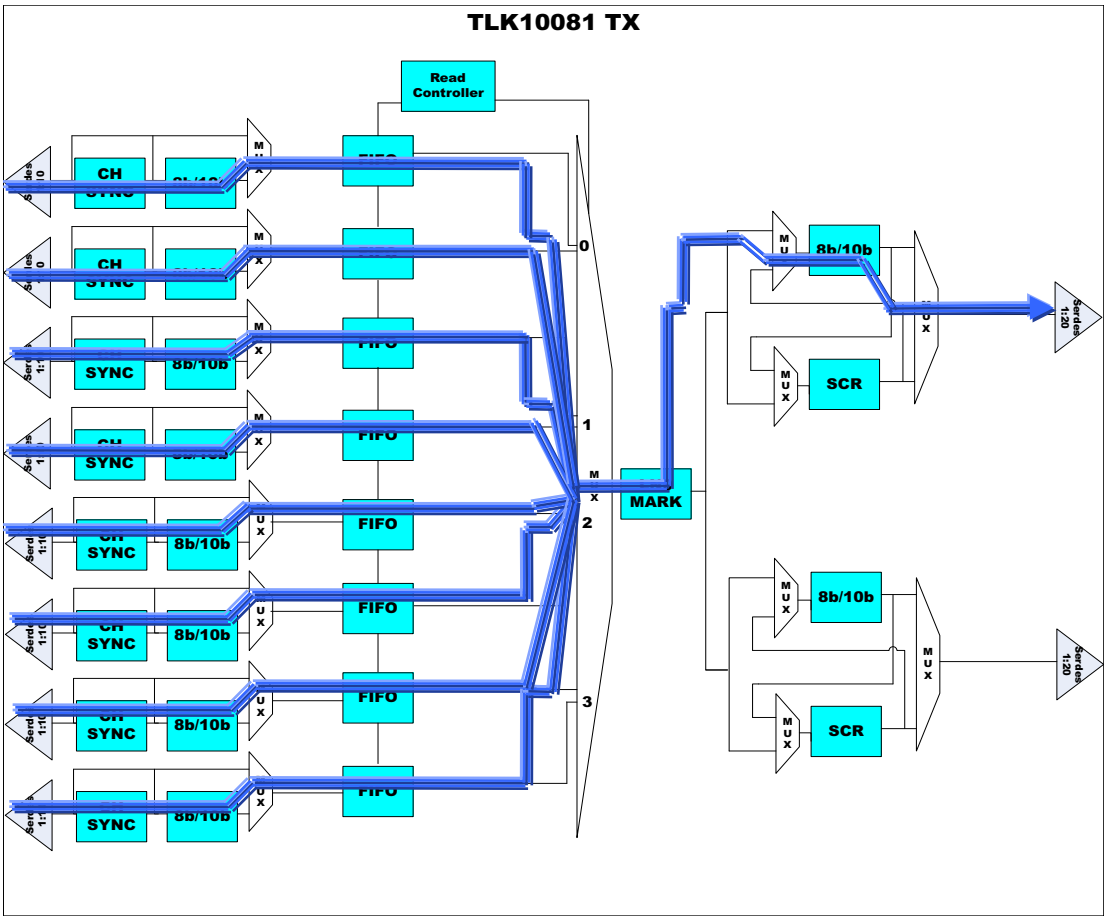


Figure 3-1. Transmit Datapath, 10-Bit Mode

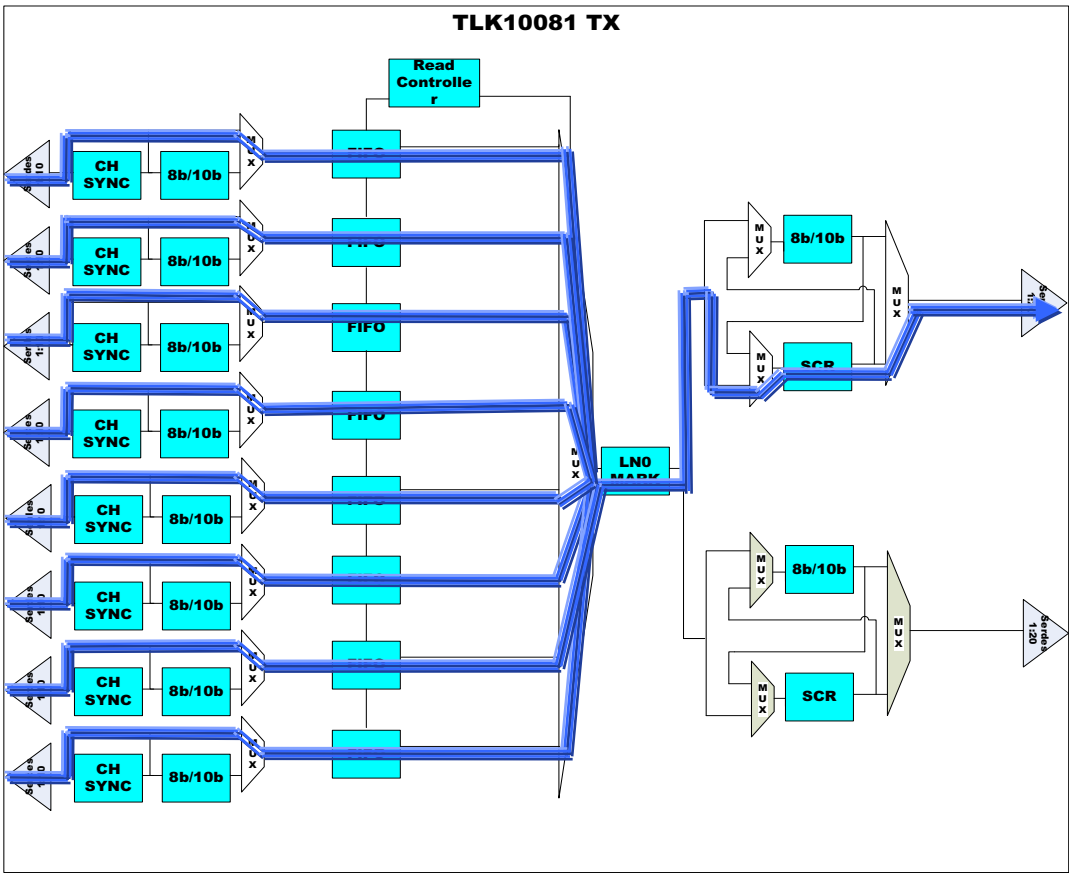


Figure 3-2. Transmit Datapath, Raw Serial Data (Bit Interleave)

3.2 Receive (De-Interleaving) Direction

With the device configured to operate in the normal transceiver (mission) mode, the receive data paths are as shown in Figure 3-2, Receive data path (10-bit mode), and Figure 3-3, Receive data path (raw serial mode).

In the receive direction, the high speed aggregate stream is received by a deserializer capable of data rates up to 10 Gbps. The deserialized data is then aligned to 20-bit boundaries by the device's channel synchronization logic. This alignment can be based on a user-defined 10-bit alignment code (in the case of 8b/10b or otherwise 10-bit delineated data) or can be done arbitrarily (for cases where 10-bit delineation is not meaningful). In either case, the chosen word boundaries can be adjusted manually if necessary to adjust the bit assignments.

Once the data is aligned, it can be optionally 8b/10b decoded or descrambled as needed before being input to the device's receive lane ordering logic (discussed in detail in Section 3.3). After lane assignments are determined, the de-aggregated serial data streams are input to independent FIFOs in order to absorb phase variations between the high-speed and low-speed clock domains and to compensate for clock rate differences if desired.

Each low speed data stream will pass through a programmable skew buffer (in case delays need to be added to certain lanes in order to meet system-level skew requirements) and optionally 8b/10b encoded before being output by a serializer capable of rates up to 1.25 Gbps.

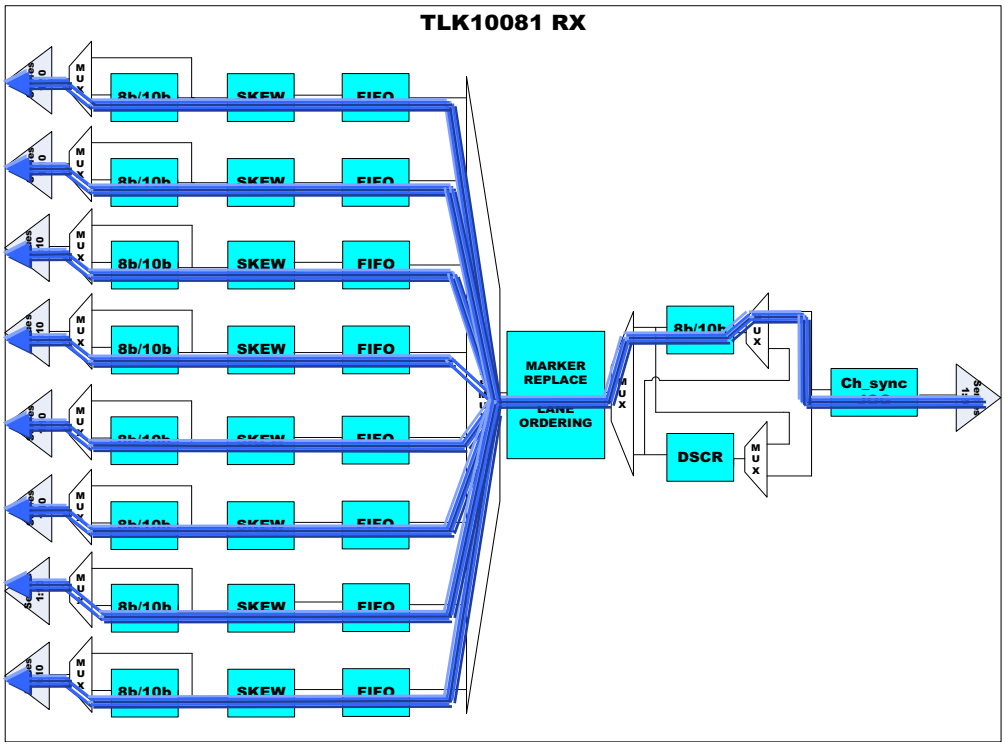


Figure 3-3. Receive Datapath, 10-Bit Mode

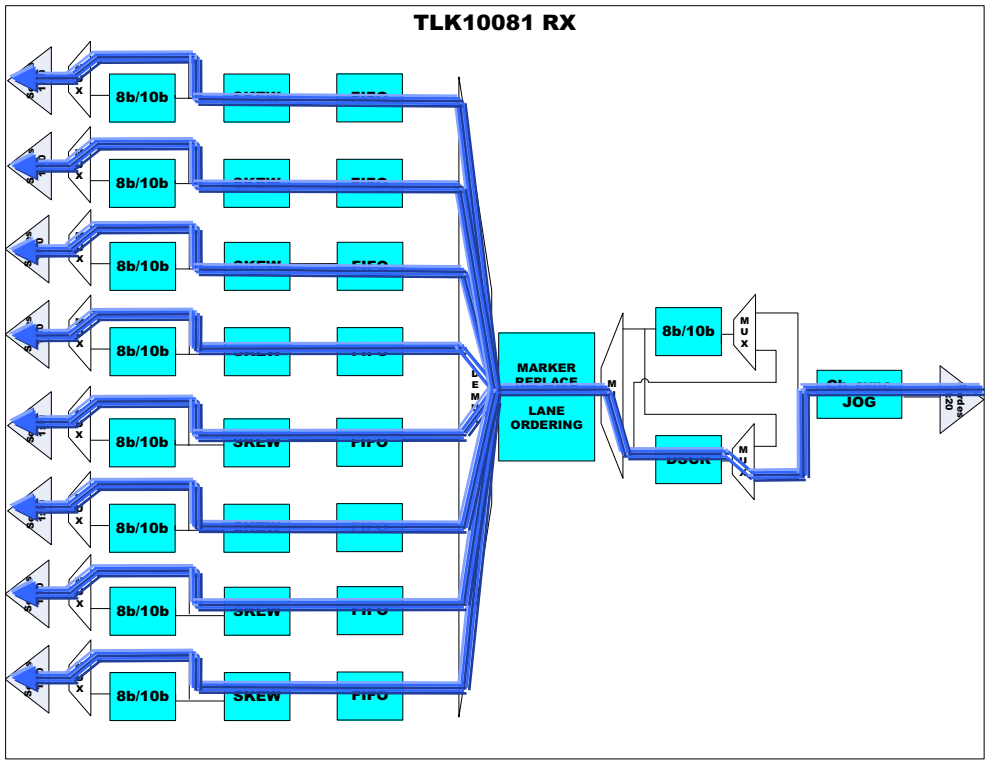


Figure 3-4. Receive Datapath, Raw Serial Data

In 1:1 mode, the receive datapath is similar to 8:1 mode, but does not have a skew buffer or a programmable descrambler. Lanes 1-7 are not used.

3.3 Lane Ordering

When multiple serial data links are multiplexed into a single physical link, special provisions need to be taken in order for the original lane assignments to be recovered at the far end of the link. The TLK10081 provides several methods to accomplish this.

3.3.1 Reserved Lane Marker Characters

If the data to be aggregated can be deserialized into 10-bit words, then it is possible to identify certain reserved codes that can be used to keep track of lane assignments. In the TX direction, the TLK10081 can be configured to identify a programmable “search” character (one that is expected to occur in the data stream) and replace it with another programmable “replace” character (one that is not expected to occur in the data stream). In the RX direction, the device can search for this reserved code in the high speed data it is receiving and use the position of the code in the aggregated data stream to determine the correct lane assignments. This code can then be replaced with another programmable character before being output on the low speed side. This allows for the lane marking process to be transparent to systems interfacing to the TLK10081’s low speed side.

3.3.2 Training Sequence

If it not possible to define reserved lane marking codes (for example, if the low-speed serial data does not have 10-bit delineation or unused codes), then it is possible to configure the TLK10081 so that lane ordering is determined at link start-up (prior to normal data transmission). This is accomplished via a training sequence sent over the high speed link from the transmitting device to the receiving device. Once the receiver has detected the training sequence and has determined lane ordering (as indicated through MDIO registers), then the transmitter can transition into normal operation.

3.3.3 Manual Lane Rotation

If the application allows for lane ordering to be determined at a system level instead, the TLK10081 provides a manual method for cycling through the possible lane order rotations. If manual rotation is used, then the device will iterate through different rotations as controlled by either MDIO registers or the RXCTRL pins.

3.3.4 Reserved Lane

If fewer than eight low speed lanes are required by the application, one lane can be used to continuously send lane ordering information. This allows for continual monitoring of lane ordering so that the assignments can be quickly re-established in the event of a link disruption.

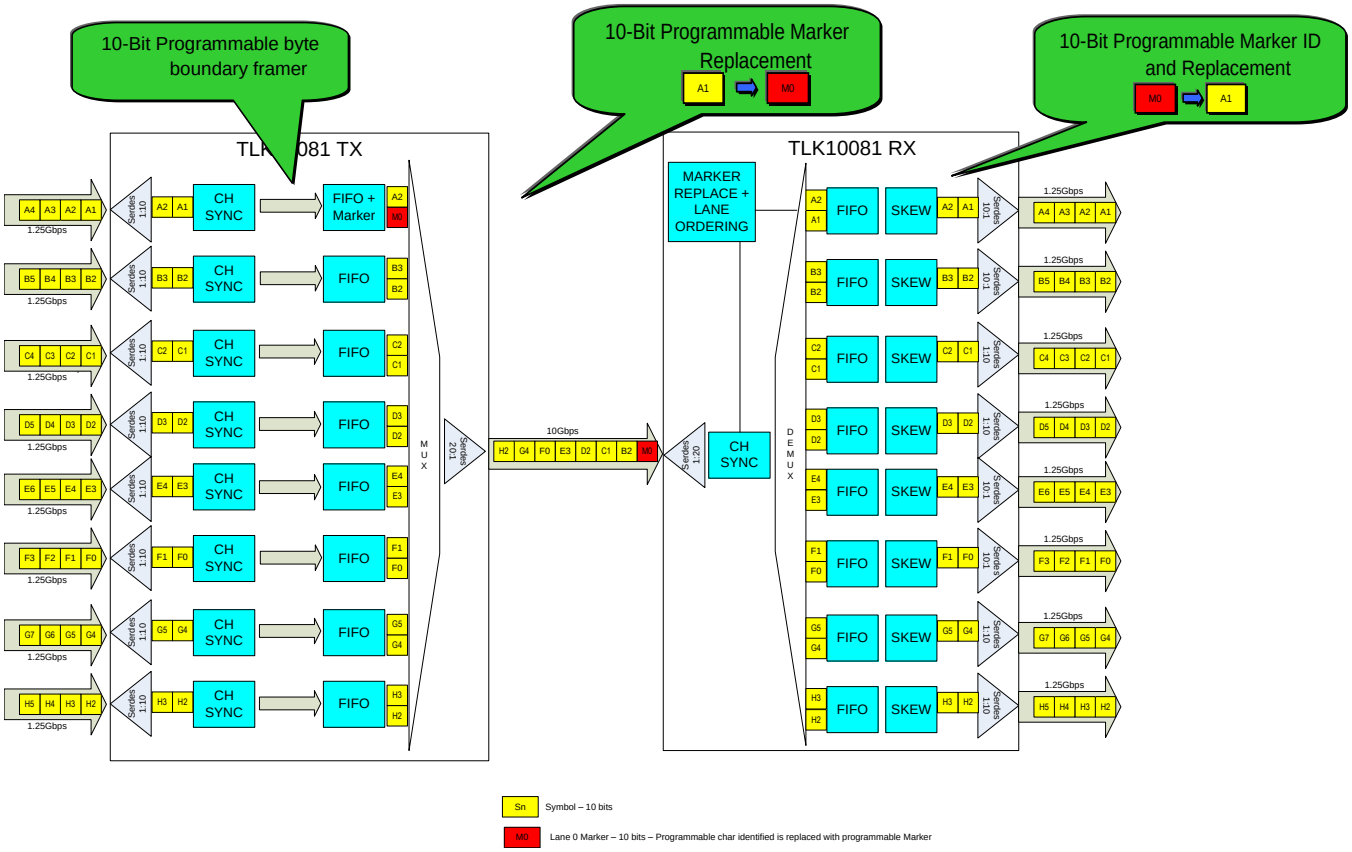


Figure 3-5. Block Diagram of the Interleave/De-interleave Scheme

3.4 Additional Functionality

3.4.1 1:1 Mode

The TLK10081 also supports a 1:1 mode for data retiming. The data path for this mode is shown below. In the transmit direction, data is received by the low-speed deserializer on Lane 0 of the selected channel, aligned to word boundaries (if applicable), 8b/10b decoded (if applicable), input to a phase-correction FIFO capable of clock tolerance compensation, optionally 8b/10b encoded, and transmitted out the high speed serial ports. The receive direction operates similarly, but in the opposite direction (eventually outputting the serial data on low speed Lane 0).

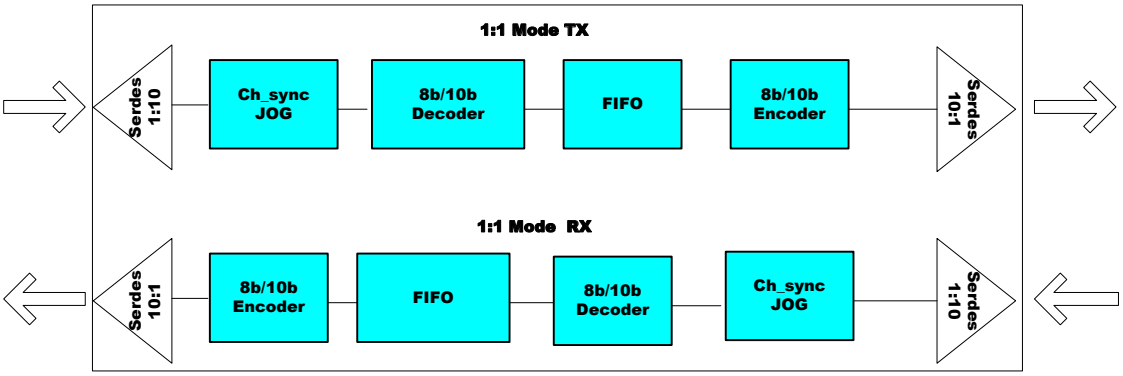


Figure 3-6. 1:1 Mode Datapath

Note that it is possible to operate one direction (transmit or receive) of a particular channel in 1:1 mode while the other direction operates in 8:1 mode.

3.4.2 Clock Tolerance Compensation

The phase-correction FIFOs used to interface between the low speed and high speed clock domains within the device are also capable of clock tolerance compensation (CTC). If enabled, the CTC function will correct for clock rate mismatches by periodically inserting or deleting a user-defined reserved “idle” character. Note that character insertion only occurs immediately following detection of an existing “idle” character, so these should occur regularly in the data stream to ensure that compensation can be performed frequently enough to avoid FIFO collisions.

3.4.3 Crosspoint Switch

The TLK10081’s default lane ordering passes through low speed input lanes (0 through 7) into fixed positions in the outputted high speed aggregate link. The high speed receiver will then identify which positions correspond to which lanes and output them accordingly on its low speed outputs. However, it is possible to reconfigure the data sources that are associated with each output lane/position through MDIO. For each HS transmit output, the source can be selected from the low speed input of the same channel or from either channel's high speed input. For the LS transmit output, data can be sourced from the low speed input or either channel's high speed input.Since the data source (input) assigned to each output is configured independently, a broadcast/fan-out function can be supported.

3.4.4 Unused Lanes

Some lanes may not be used all the time. When they are disconnected, data stuffing must occur to fill in the void left by the missing input data. In TLK10081, the data pattern sent to represent lane down should not alias with actual data; therefore, a repeated fill data sequence is used. The active/not active status of all lanes can be monitored through MDIO.

To implement the lane down function on the RX side, eight separate state machines will monitor the high speed data for the fill sequence and indicate the status of each lane through the low speed status register 0x13.

3.4.5 Test Pattern Generationa and Verification

The TLK10081 has an extensive suite of built in test functions to support system diagnostic requirements. Each channel has sets of internal test pattern generators and verifiers.

Several patterns can be selected via the MDIO interface that offer extensive test coverage. The low speed side supports generation and verification of pseudo-random bit sequence (PRBS) 2^7-1, 2^{23}-1, and 2^{31}-1 patterns. In addition to those PRBS patterns, the high speed side supports High-frequency (HF), Low-frequency (LF), Mixed-frequency (MF), and continuous random test pattern (CRPAT) long/short pattern generation and verification as defined in IEEE Standard 802.3.

The TLK10081 provides two pins: PRBSEN and PRBS_PASS, for additional and easy control and monitoring of PRBS pattern generation and verification. When the PRBSEN is asserted high, the internal PRBS generator and verifier circuits are enabled on both transmit and receive data paths on high speed and low speed sides of both channels. This signal is logically OR’d with an MDIO register bits A.13:12 and B.13:12.

PRBS 2^{31}-1 is selected by default, and can be changed through MDIO.

When PRBS test is enabled (PRBSEN=1):

PRBS_PASS=1 indicates that PRBS pattern reception is error free.

PRBS_PASS=0 indicates that a PRBS error is detected. The channel, the side (high speed or low speed), and the lane (for low speed side) that this signal refers to is chosen through MDIO register bit 0.3:0.

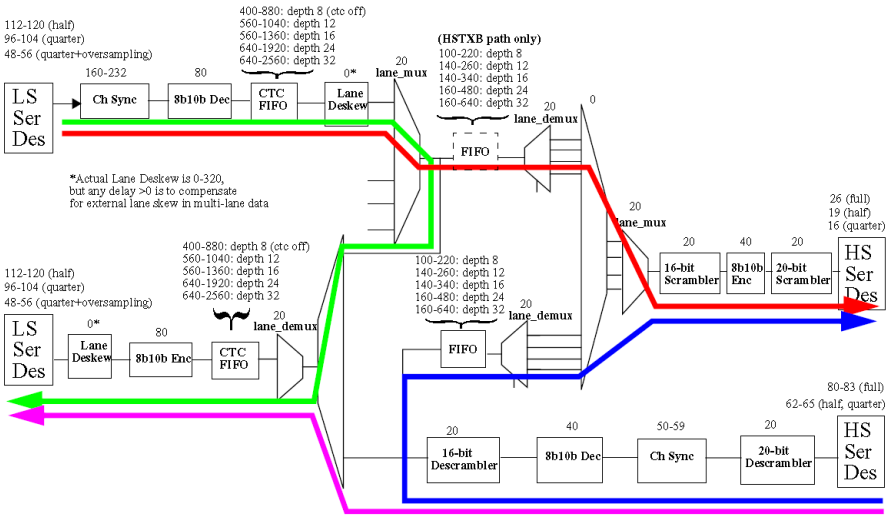
3.4.6 Power Down Mode

The TLK10081 can be put in power down either through device inputs pins or through MDIO control register (1.15). PDTRXA_N: Active low, powers down the channel.

The MDIO management serial interface remains operational when in register based power down mode (1.15 asserted for both channels), but status bits may not be valid since the clocks are disabled. The low speed side and high speed side SERDES outputs are high impedance when in power down mode. Please see the detailed per pin description for the behavior of each device I/O signal during pin based and register based power down.

3.4.7 Transmit / Receive Latency

The latency through the TLK10081 is shown in Figure 3-7. Note that the latency ranges shown indicate static rather than dynamic latency variance, i.e., the range of possible latencies when the serial link is initially established. During normal operation, the latency through the device is fixed.



Latency: HS Full Rate, LS Half Rate, 8-Lanes, 8-deep FIFO
LS In -> HS Out: 918-1478 (Typical 1198) UI (add 100-220 for HSTXB path)
LS In -> LS Out: 1384-2432 (Typical 1908) UI
HS In -> LS Out: 822-1322 (Typical 1072) UI
HS In -> HS Out: 436-568 (Typical 502) UI

Figure 3-7. TLK10081 Transmit / Receive Latency

4 SERDES INTERFACES

4.1 High Speed CML Output

The high speed data output driver is implemented using Current Mode Logic (CML) with integrated pull up resistors, requiring no external components. The transmit outputs must be AC coupled.

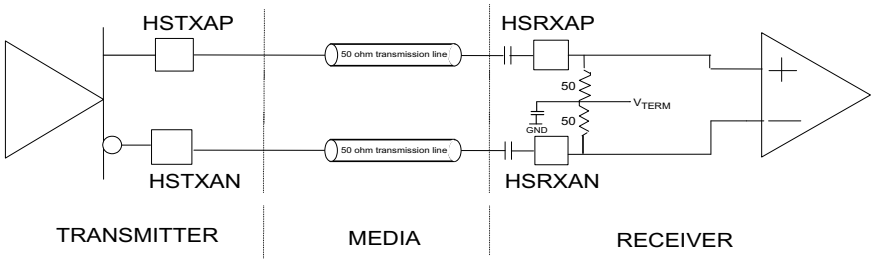


Figure 4-1. Example of High Speed I/O AC Coupled Mode (Channel A HS side is shown)

Current Mode Logic (CML) drivers often require external components. The disadvantage of the external component is a limited edge rate due to package and line parasitic. The CML driver on TLK10081 has on-chip 50Ω termination resistors terminated to VDDT, providing optimum performance for increased speed requirements. The transmitter output driver is highly configurable allowing output amplitude and de-emphasis to be tuned to a channel's individual requirements. Software programmability allows for very flexible output amplitude control. Only AC coupled output mode is supported.

When transmitting data across long lengths of PCB trace or cable, the high frequency content of the signal is attenuated due to the skin effect of the media. This causes a “smearing” of the data eye when viewed on an oscilloscope. The net result is reduced timing margins for the receiver and clock recovery circuits. In order to provide equalization for the high frequency loss, 4-tap finite impulse response (FIR) transmit de-emphasis is implemented. A highly configurable output driver maximizes flexibility in the end system by allowing de-emphasis and output amplitude to be tuned to a channel’s individual requirements. Output swing control is via MDIO.

See Figure 7-2 for output waveform flexibility. The level of de-emphasis is programmable via the MDIO interface through control registers (5.7:4 and 5.12:8) through pre-cursor and post-cursor settings. Users can control the strength of the de-emphasis to optimize for a specific system requirement.

4.2 High Speed Receiver

The high speed receiver is differential CML with internal termination resistors. The receiver requires AC coupling. The termination impedances of the receivers are configured as 100 Ohms with the center tap weakly tied to 0.8*VDDT with a capacitor to create an AC ground.

TLK10081 serial receivers incorporate adaptive equalizers. This circuit compensates for channel insertion loss by amplifying the high frequency components of the signal, reducing inter-symbol interference. Equalization can be enabled or disabled per register settings. Both the gain and bandwidth of the equalizer are controlled by the receiver equalization logic.

4.3 Loss of Signal Output Generation (LOS)

Loss of input signal detection is based on the voltage level of each serial input signal INA*P/N, HSRXAP/N, and HSRXBP/N. Anytime the serial receive input differential signal peak to peak voltage level is ≤75 mV_{pp} for High Speed side or ≤ 65mV_{pp} for Low Speed side, LOSA or LOSB are asserted (high true) respectively for Channel A and Channel B (if enabled, disabled by default). Note that an input signal ≥ 150 mV_{pp} for High Speed side and ≥ 175 mV_{pp} for Low Speed side is required for reliable operation of the loss of signal detection circuits. If the input signal is between these two ranges, the SERDES will operate properly, but the LOS indication will not be valid (or robust). The LOS indications are also directly readable through the MDIO interface in respective registers.

The following additional critical status conditions can be combined with the loss of signal condition enabling additional real-time status signal visibility on the LOSA and LOSB outputs per channel:

1. Loss of Channel Synchronization Status – Logically OR'd with LOS condition(s) when enabled. Loss of channel synchronization can be optionally logically OR'd (disabled by default) with the internally generated LOS condition (per channel).
2. Loss of PLL Lock Status on LS and HS sides – Logically OR'd with LOS condition(s) when enabled. The internal PLL loss of lock status bit is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
3. Receive 8B/10B Decode Error (Invalid Code Word or Running Disparity Error) – Logically OR'd with LOS condition(s) when enabled. The occurrence of an 8B/10B decode error (invalid code word or disparity error) is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
4. AGCLOCK (Active Gain Control Currently Locked) – Inverted and Logically OR'd with LOS condition(s) when enabled. HS RX SERDES adaptive gain control unlocked indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).
5. AZDONE (Auto Zero Calibration Done) - Inverted and Logically OR'd with LOS conditions(s) when enabled. HS RX SERDES auto-zero not done indication is optionally OR'd (disabled by default) with the other internally generated loss of signal conditions (per channel).

5 CLOCKING

5.1 Configuring PLL and Line Rates

The TLK10081 includes internal low-jitter high quality oscillators that are used as frequency multipliers for the low speed and high speed SERDES and other internal circuits of the device. Specific MDIO registers are available for SERDES rate and PLL multiplier selection to match line rates and reference clock (REFCLK0/1) frequencies for various applications. Some examples are detailed below on how to select and configure.

The external differential reference clock has a large operating frequency range allowing support for many different applications. The reference clock frequency must be within ± 200 PPM of the incoming serial data rate (± 100 PPM of nominal data rate).

Table 5-1. Line Rate and Reference Clock Selection for the 1:1 Mode

LOW SPEED SIDE					HIGH SPEED SIDE			
LINE RATE (Mbps)	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)		LINE RATE (Mbps(1))	SERDES PLL MULTIPLIER	RATE	REFCLKP/N (MHz)
1000-1250	10	Half	100-125		1000-1250	20	Quarter	100-125
1000-1250	8	Half	125-156.25		1000-1250	16	Quarter	125-156.25
1000-1250	8	Quarter	250-312.5		1000-1250	8	Quarter	250-312.5

(1) High Speed Side SERDES runs at 2x effective data rate.

For other line rates in 8:1 mode, valid reference clock frequencies can be selected with the help of the information provided in Table 5-2 and Table 5-3 for the low speed side and high speed side SERDES. The reference clock frequency has to be the same for the two SERDES and must be within the specified valid ranges for different PLL multipliers.

Table 5-2. Line Rate and Reference Clock Frequency Ranges for the Low Speed Side SERDES

SERDES PLL MULTIPLIER (MPY)	REFERENCE CLOCK (MHz)		HALF RATE (Gbps)		QUARTER RATE (Gbps)	
	MIN	MAX	MIN	MAX(1)	MIN	MAX
4	250	425	1	1.25	0.5	0.85
5	200	425	1	1.25	0.5	1.0625
6	166.667	416.667	1	1.25	0.5	1.25
8	125	312.5	1	1.25	0.5	1.25
10	122.88	250	1.2288	1.25	0.6144	1.25

(1) Reference Clock is lower than Max Reference Clock RateScale: Half Rate = 1, Quarter Rate = 2

Table 5-3. Line Rate and Reference Clock Frequency Ranges for the High Speed Side SERDES

SERDES PLL MULTIPLIER (MPY)	REFERENCE CLOCK (MHz)		FULL RATE (Gbps)		HALF RATE (Gbps)		QUARTER RATE (Gbps)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
4	375	425	6	6.8				
5	300	425	6	8.5	4(1)	4.25	2(1)	2.125
6	250	416.667	6	10	4(1)	5	2(1)	2.5
8	187.5	312.5	6	10	4(1)	5	2(1)	2.5
10	150	250	6	10	4(1)	5	2(1)	2.5
12	125	208.333	6	10	4(1)	5	2(1)	2.5
15	122.88	166.667	7.3728	10	4(1)	5	2(1)	2.5
16	122.88	156.25	7.864	10	4(1)	5	2(1)	2.5
20	122.88	125	9.8304	10	4.9152	5	2.4576	2.5

(1) Reference Clock is higher than Min Reference Clock
RateScale: Full Rate = 0.25, Half Rate = 0.5, Quarter Rate = 1

5.1.1 Refclk Frequency Selection Example

If the low speed side line rate is 0.6Gbps, the high-speed side line rate will be 4.8Gbps. The following steps can be taken to make a reference clock frequency selection:

1. Determine the appropriate SERDES rate modes that support the required line rates. Table 5-2 shows that the 0.6Gbps line rate on the low speed side is only supported in the quarter rate mode (RateScale = 2). Table 5-3 shows that the 4.8Gbps line rate on the high speed side is only supported in the half rate mode (RateScale = 0.5).
2. For each SERDES side, and for all available PLL multipliers (MPY), compute the corresponding reference clock frequencies using the formula:

   Reference Clock Frequency = (LineRate x RateScale)/MPY

   The computed reference clock frequencies are shown in Table 5-4 along with the valid minimum and maximum frequency values.
3. Mark all the common frequencies that appear on both SERDES sides. Note and discard all those that fall outside the allowed range. In this example, the common frequencies are highlighted in Table 5-4 .
4. Select any of the remaining marked common reference clock frequencies. The higher the reference clock frequency usually the better. In this example, any of the following reference clock frequencies can be selected: 150MHz, 200MHz, 240MHz, and 300MHz.

Note that for Low Speed side rates of at least 500Mbps, a general rule to follow is that half rate on the Low Speed side will correspond to full rate on the High Speed side, and quarter rate on the Low Speed side will correspond to half rate on the High Speed side. And, the high speed PLL multiplier will be 2x of low speed.

Table 5-4. Reference Clock Frequency Selection Example

LOW SPEED SIDE SERDES					HIGH SPEED SIDE SERDES			
SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)				SERDES PLL MULTIPLIER	REFERENCE CLOCK FREQUENCY (MHz)		
	COMPUTED	MIN	MAX			COMPUTED	MIN	MAX
4	300	250	425		4	600	375	425
5	240	200	425		5	480	300	425
6	200	166.667	416.667		6	400	250	425
8	150	125	312.5		8	300	187.5	390.625
10	120	122.88	250		10	240	150	312.5
					12	200	125	260.417
					15	160	122.88	208.333
					16	150	122.88	195.3125
					20	120	122.88	156.25

5.1.2 Low Speed Side Rates Below 500Mbps

For serial links below 500Mbps, the Low Speed Side SERDES must be configured using twice the desired data rate. For instance, 270Mbps data must be configured for 540Mbps. In addition, the device must be configured through MDIO to run at half speed (register TBD). This enables over-sampling of data to support data rates lower than the Low Speed side SERDES IP allows. Note that the High Speed SERDES should be configured for the actual data rate, and not 2x. Using the same 270Mbps example, the high speed side should be configured for 0.27x8 = 2.16Gbps.

Also note the Low Speed side and High Speed side will have the same rate, and the High Speed PLL multiplier will be 2x of Low Speed. For 270Mbps/2.16Gbps and a REFCLK of 135Mhz, the Low Speed side will be set to 8x, Quarter Rate (540Mhz) and the High Speed side will be set to 16x, Quarter Rate (2.16Gbps).

5.2 Clocking Architecture

A simplified clocking architecture for the TLK10081 is captured in Figure 5-1. Each channel (Channel A or Channel B) has an option of operating with a differential reference clock provided either on pins REFCLK0P/N or REFCLK1P/N. The choice is made either through MDIO or through REFCLK_SEL pins. The reference clock frequencies for those two clock inputs can be different as long as they fall under the valid ranges shown in Table 5-3. For each channel, the low speed side SERDES, high speed side SERDES and the associated part of the digital core operate from the same reference clock.

The clock and data recovery (CDR) function of the high speed side receiver recovers the clock from the incoming serial data. The high speed side SERDES makes available two versions of clocks for further processing:

1. HS_RXBCLK_A/B: recovered byte clock synchronous with incoming serial data and with a frequency matching the incoming line rate divided by 20.
2. VCO_CLOCK_A/B_DIV2: VCO frequency divided by 2. (VCO frequency = REFCLK x PLL Multiplier).

The above-mentioned clocks can be output through the differential pins, CLKOUTAP/N and CLKOUTBP/N, with optional frequency division ratios of 1, 2, 4, 5, 8, 10, 16, 20, or 25. The clock output options are software controlled through the MDIO interface register 0x15. The maximum CLKOUT frequency is 500MHz.

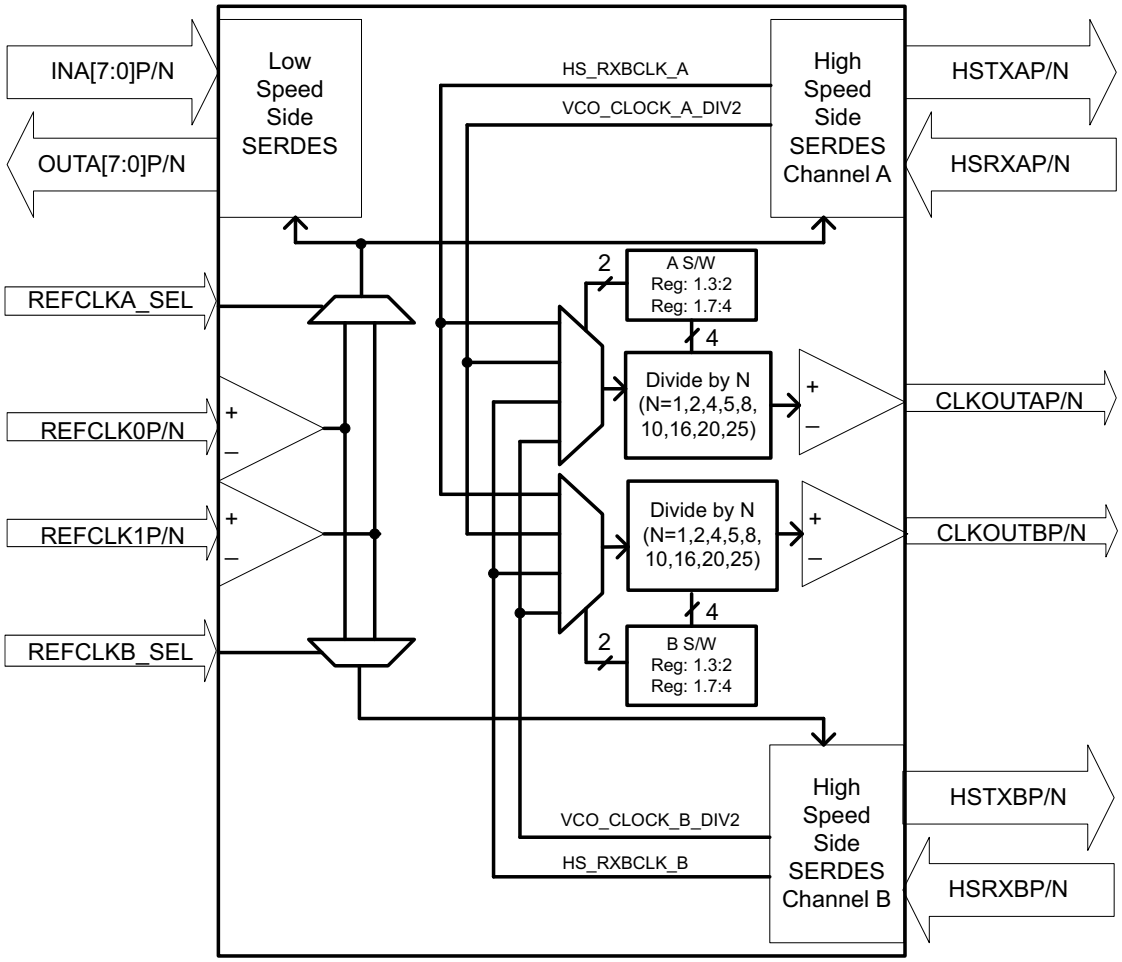


Figure 5-1. Clocking Architecture

6 PROGRAMMERS REFERENCE

PRTAD[4:0] determine the device port address. In this mode, TLK10081 will respond if the PHY address field on the MDIO protocol (PA[4:0]) matches PRTAD[4:0] pin value).

6.1 MDIO Management Interface

The TLK10081 supports the Management Data Input/Output (MDIO) Interface as defined in Clause 22 of the IEEE 802.3 Ethernet specification. The MDIO allows register-based management and control of the serial links. Normal operation of the TLK10081 is possible without use of this interface. However, some features are accessible only through the MDIO.

The MDIO Management Interface consists of a bi-directional data path (MDIO) and a clock reference (MDC). The port address is determined by control pins PRTAD[4:0] as described in Table 2-1).

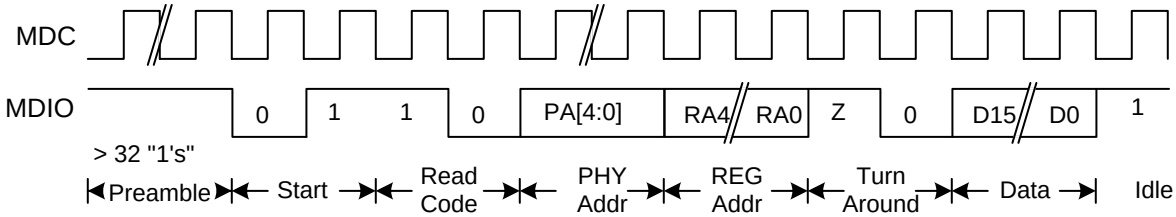
In Clause 22, the control pins PRTAD[4:0] determine the device port address.

TLK10081 will respond if the 5 bits of PHY address field on MDIO protocol (PA[4:0] match PRTAD[4:0]).

The MACRO_ACCESS bit in Register 0x00 determines which high speed channel/port within the TLK10081 is controlled by the high speed registers. A value of 0 selects High Speed Channel A and 1 selects High Speed Channel B. The GLOBAL_WRITE bit can be set to 1 to apply the same settings to both high speed channels.

Write transactions which address an invalid register or device or a read only register will be ignored. Read transactions which address an invalid register will return a 0.

MDIO Protocol Timing: The Clause 22 timing required to read from the internal registers is shown in Figure 6-1. The Clause 22 timing required to write to the internal registers is shown in Figure 6-2.



Note that the 1 in the Turn Around section is externally pulled up, and driven to Z by TLK10081.

Figure 6-1. CL22 - Management Interface Read Timing

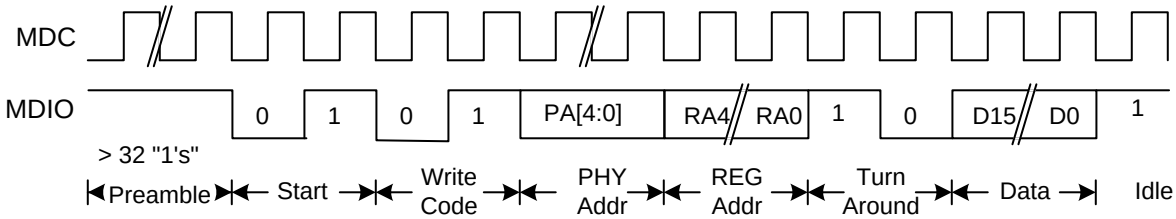


Figure 6-2. CL22 - Management Interface Write Timing

Clause 22 Indirect Addressing: The TLK10081 Register space is divided into two register groups. One register group can be addressed directly through Clause 22, and one register group can be addressed indirectly through Clause 22. The register group which can be addressed through Clause 22 indirectly is implemented in vendor specific register space (16'h8000 onwards). Due to clause 22 register space limitations, an indirect addressing method is implemented so that this extended register space can be accessed through clause 22. To access this register space (16'h8000 onwards), an address control register (Reg 30, 5'h1E) should be written with the register address followed by a read/write transaction to address data register (Reg 31, 5'h1F) to access the contents of the address specified in address control register.

The following timing diagrams illustrate an example write transaction to Register 16'h8000 using indirect addressing in Clause 22.

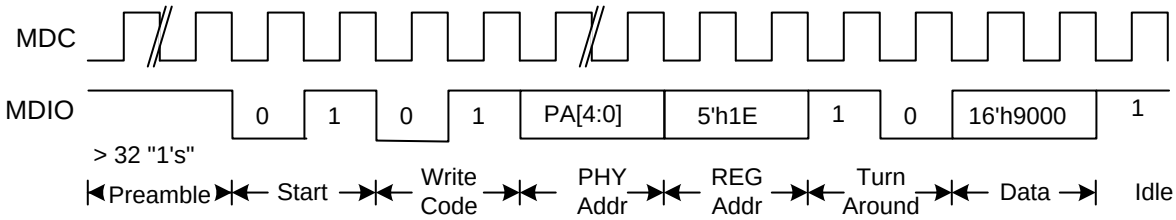


Figure 6-3. CL22 – Indirect Address Method – Address Write

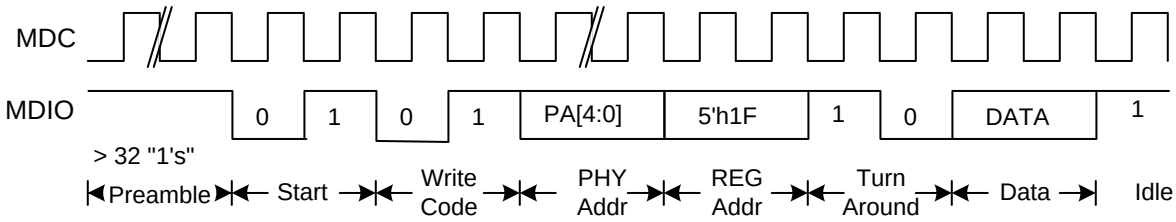


Figure 6-4. CL22 - Indirect Address Method – Data Write

The following timing diagrams illustrate an example read transaction to read contents of Register 16'h8000 using indirect addressing in Clause 22.

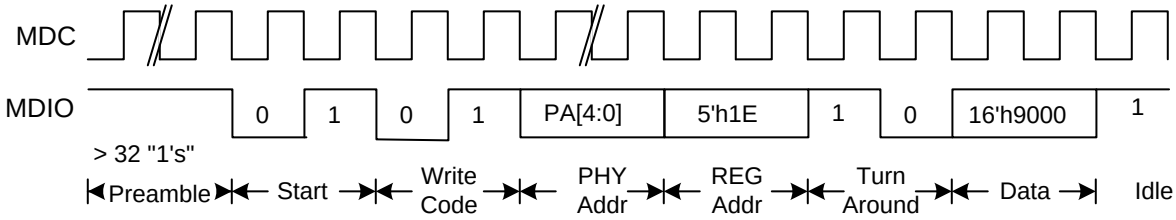
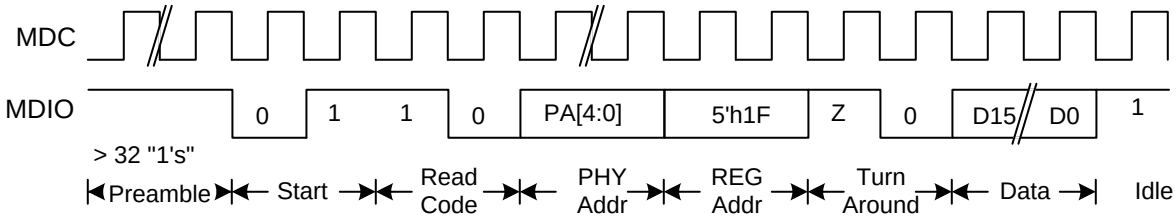


Figure 6-5. CL22 - Indirect Address Method – Address Write



Note that the 1 in the Turn Around section is externally pulled up, and driven to Zero by TLK10081.

Figure 6-6. CL22 - Indirect Address Method – Data Read

6.2 Register Bit Definitions

RW: Read-Write
User can write 0 or 1 to this register bit. Reading this register bit returns the same value that has been written.

RW/SC: Read-Write Self-Clearing
User can write 0 or 1 to this register bit. Writing a "1" to this register creates a high pulse. Reading this register bit always returns 0.

RO: Read-Only
This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value.

RO/LH: Read-Only Latched High
This register can only be read. Writing to this register bit has no effect. Reading a "1" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "0" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched high register, when read high, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read low. If it is still occurring, the second read will read high. Reading this register bit automatically resets its value to 0.

RO/LL: Read-Only Latched Low
This register can only be read. Writing to this register bit has no effect. Reading a "0" from this register bit indicates that either the condition is occurring or it has occurred since the last time it was read. Reading a "1" from this register bit indicates that the condition is not occurring presently, and it has not occurred since the last time the register was read. A latched low register, when read low, should be read again to distinguish if a condition occurred previously or is still occurring. If it occurred previously, the second read will read high. If it is still occurring, the second read will read low. Reading this register bit automatically sets its value to 1.

COR: Clear-On-Read counter
This register can only be read. Writing to this register bit has no effect. Reading from this register bit returns its current value, then resets its value to 0. Counter value freezes at Max.

Table 6-1. GLOBAL_CONTROL_1 (1)

Register Address:0x00		Default: 0x0610	
Bit(s)	**Name**	**Description**	**Access**
15	GLOBAL_RESET	Global reset. 0 = Normal operation (Default 1'b0) 1 = Resets TX and RX data path including MDIO registers. Equivalent to asserting RESET_N.	RW SC (2)
14:13	RESERVED	For TI use only. Always reads 0.	RW
12	MACRO_ACCESS	0 = Access HS/LT Control/status specific to HS macro A (Default 1'b0) 1 = Access HS /LT Control/status specific to alternate HS macro	RW
11	GLOBAL_WRITE	0 = HS/LT Control settings are applied to HS macro specified in MACRO_ACCESS (Default 1'b0) 1 = HS/LT Control settings are applied to both HS 0/1 macros	RW
10:7	RESERVED	For TI use only (Default 4'b1100)	RW
6:5	RESERVED	For TI use only. Always reads 0.	RW
4:0	PRBS_PASS_OVERLAY[4:0]	PRBS_PASS pin status selection. Applicable only when PRBS test pattern verification is enabled on HS side or LS side. PRBS_PASS pin reflects PRBS verification status on selected HS macro/ LS lane 1xx00 = PRBS_PASS reflects combined status of Macro A/B HS serdes PRBS verification. If PRBS verification fails on any channel HS serdes, PRBS_PASS will be asserted low. (Default 5'b10000) 00000 = Status from macro A HS Serdes side 00001 = Reserved status from macro A HS core side 0001x = Reserved 00100 = Status from LS Serdes side Lane 0 00101 = Status from LS Serdes side Lane 1 00110 = Status from LS Serdes side Lane 2 00111 = Status from LS Serdes side Lane 3 01000 = Status from macro B HS Serdes side 01001 = Reserved 0101x = Reserved 01100 = Status from LS Serdes side Lane 4 01101 = Status from LS Serdes side Lane 5 01110 = Status from LS Serdes side Lane 6 01111 = Status from LS Serdes side Lane 7	RW

(1) This global register is channel independent.
(2) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 6-2. CHANNEL_CONTROL_1

Register Address:0x01		Default: 0x4000	
Bit(s)	**Name**	**Description**	**Access**
15	POWERDOWN	Setting this bit high powers down entire data path with exception that MDIO interface stays active. 0 = Normal operation (Default 1'b0) 1 = Power Down mode is enabled.	RW
14	LT_ENABLE	1 = Enable link training (Default 1'b1) 0 = Disable link training This bit should be set to HIGH for auto train mode to function correctly	RW
13:10	RESERVED	For TI use only (Default 4'b0000)	RW
9	RX_BIT_INTERLEAVE	0 = Normal operation. (Default 1'b0) 1 = Enable bit interleave on receive path	RW
8	TX_BIT_INTERLEAVE	0 = Normal operation. (Default 1'b0) 1 = Enable bit interleave on transmit path	RW
7:4	RESERVED	For TI use only (Default 4'b0000)	RW
3	RX_1LN_MODE_SEL	0 = Enable 8ln mode on receive path(Default 1'b0) 1 = Enable 1ln mode on receive datapath	RW
2	TX_1LN_MODE_SEL	1 = Enable 8ln mode on transmit datapath(Default 1'b0) 1 = Enable 1ln mode on transmit datapath	RW
1	REFCLK_SW_SEL	Channel HS Reference clock selection. Applicable only when REFCLK_SEL pin is LOW. 0 = Selects REFCLK_0_P/N as clock reference to HS side serdes macro x (Default 1'b0) 1 = Selects REFCLK_1_P/N as clock reference to HS side serdes macro x	RW
0	LS_REFCLK_SEL	Channel LS Reference clock selection. 0 = LS side serdes reference clock is same as HS side serdes reference clock (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_0_P/N is selected as LS side serdes reference clock and vice versa) (Default 1'b0) 1 = Alternate reference clock is selected as clock reference to LS side serdes (E.g. If REFCLK_0_P/N is selected as HS side serdes macro reference clock, REFCLK_1_P/N is selected as LS side serdes reference clock and vice versa)	RW

Table 6-3. HS_SERDES_CONTROL_1

Register Address:0x02		Default: 0x831D	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only (Default 6'b100000)	RW
9:8	HS_LOOP_BANDWIDTH[1:0]	HS Serdes PLL Loop Bandwidth settings 00 = Medium Bandwidth 01 = Low Bandwidth 10 = High Bandwidth 11 = Ultra High Bandwidth. (Default 2'b11)	RW
7	RESERVED	For TI use only (Default 1'b0)	RW
6	HS_VRANGE	HS Serdes PLL VCO range selection. 0 = VCO runs at higher end of frequency range (Default 1'b0) 1 = VCO runs at lower end of frequency range This bit needs to be set HIGH if VCO frequency (REFCLK *HS_PLL_MULT) is below 2.5 GHz.	RW
5	RESERVED	For TI use only (Default 1'b0)	RW
4	HS_ENPLL	HS Serdes PLL enable control. HS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables PLL in HS serdes 1 = Enables PLL in HS serdes (Default 1'b1)	RW
3:0	HS_PLL_MULT[3:0]	HS Serdes PLL multiplier setting (Default 4'b1101). Refer to Table 6-4	RW

Table 6-4. HS PLL Multiplier Control

2.3:0		2.3:0	
VALUE	**PLL MULTIPLIER FACTOR**	**VALUE**	**PLL MULTIPLIER FACTOR**
0000	Reserved	1000	12x
0001	Reserved	1001	12.5x
0010	4x	1010	15x
0011	5x	1011	16x
0100	6x	1100	16.5x
0101	8x	1101	20x
0110	8.25x	1110	25x
0111	10x	1111	Reserved

Table 6-5. HS_SERDES_CONTROL_2

Register Address:0x03		**Default:0xA848**	
Bit(s)	**Name**	**Description**	**Access**
15:12	HS_SWING[3:0]	Transmitter Output swing control for HS Serdes. (Default 4'b1010) Refer Table 6-6.	RW
11	HS_ENTX	HS Serdes transmitter enable control. HS Serdes transmitter is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables HS serdes transmitter 1 = Enables HS serdes transmitter (Default 1'b1)	RW
10	HS_EQHLD	HSRX Equalizer hold control. 0 = Normal operation (Default 1'b0) 1 = Holds equalizer and long tail correction in its current state	RW
9:8	HS_RATE_TX [1:0]	HS Serdes TX rate settings. 00 = Full rate (Default 2'b00) 01 = Half rate 10 = Quarter rate 11 = Eighth rate	RW
7:6	HS_AGCCTRL[1:0]	Adaptive gain control loop. 00 = Attenuator will not change after lock has been achieved, even if AGC becomes unlocked 01 = Attenuator will not change when in lock state, but could change when AGC becomes unlocked (Default 2'b01) 10 = Force the attenuator off 11 = Force the attenuator on	RW
5:4	HS_AZCAL[1:0]	Auto zero calibration. 00 = Auto zero calibration initiated when receiver is enabled (Default 2'b00) 01 = Auto zero calibration disabled 10 = Forced with automatic update. 11 = Forced without automatic update	RW
3	HS_ENRX	HS Serdes receiver enable control. HS Serdes receiver is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables HS serdes receiver 1 = Enables HS serdes receiver (Default 1'b1)	RW
2:0	HS_RATE_RX [2:0]	HS Serdes RX rate settings. 000 = Full rate (Default 3'b000) 101 = Half rate 110 = Quarter rate 111 = Eighth rate 001 = Reserved 01x = Reserved 100 = Reserved	RW

Table 6-6. HSTX AC Mode Output Swing Control

VALUE 3.15:12	AC MODE
	TYPICAL AMPLITUDE (mVdfpp)
0000	130
0001	220
0010	300
0011	390
0100	480
0101	570
0110	660
0111	750
1000	830
1001	930
1010	1020
1011	1110
1100	1180
1101	1270
1110	1340
1111	1400

Table 6-7. HS_SERDES_CONTROL_3

Register Address:0x04		Default:0x1500	
Bit(s)	**Name**	**Description**	**Access**
15	HS_ENTRACK	HSRX ADC Track mode. 0 = Normal operation (Default 1'b0) 1 = Forces ADC into track mode	RW
14:12	HS_EQPRE[2:0]	Serdes Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude (Default 3'b001) 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude 100 = 9/9 cursor amplitude 101 =11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
11:10	HS_CDRFMULT[:10]	Clock data recovery algorithm frequency multiplication selection (Default 2'b01) 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode 11 = Reserved	RW
9:8	HS_CDRTHR[1:0]	Clock data recovery algorithm threshold selection (Default 2'b01) 00 = Four vote threshold 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	RW
7	RESERVED	For TI use only (Default 1'b0)	RW
6	HS_PEAK_DISABLE	HS Serdes PEAK_DISABLE control 0 = Normal operation (Default 1'b0) 1 = Disables high frequency peaking. Suitable for <6 Gbps operation	RW
5	HS_H1CDRMODE	HS_Serdes H1CDRMODE control 0 = Normal operation (Default 1'b0) 1 = Enables CDR mode suitable for short channel operation.	RW
4:0	HS_TWCRF[4:0]	Cursor Reduction Factor (Default 5'b00000). Refer to Table 6-8.	RW

Table 6-8. HSTX Cursor Reduction Factor Weights

4.4:0		4.4:0	
VALUE	**CURSOR REDUCTION (%)**	**VALUE**	**CURSOR REDUCTION (%)**
00000	0	10000	17
00001	2.5	10001	20
00010	5.0	10010	22
00011	7.5	10011	25
00100	10.0	10100	27
00101	12	10101	30
00110	15	10110	32
00111	Reserved	10111	35
01000		11000	37
01001		11001	40
01010		11010	42
01011		11011	45
01100		11100	47
01101		11101	50
01110		11110	52
01111		11111	55

Table 6-9. HS_SERDES_CONTROL_4

Register Address:0x05		Default:0x2000	
Bit(s)	**Name**	**Description**	**Access**
15	HS_RX_INVPAIR	Receiver polarity. 0 = Normal polarity. HSRXxP considered positive data. HSRXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSRXxP considered negative data. HSRXxN considered positive data	RW
14	HS_TX_INVPAIR	Transmitter polarity. 0 = Normal polarity. HSTXxP considered positive data and HSTXxN considered negative data (Default 1'b0) 1 = Inverted polarity. HSTXxP considered negative data and HSTXxN considered positive data	RW
13	RESERVED	For TI use only (Default 1'b1)	RW
12:8	HS_TWPOST1[4:0]	Adjacent post cursor1 Tap weight. Selects TAP settings for TX waveform. (Default 5'b00000) Refer Table 6-10.	RW
7:4	HS_TWPRE[3:0]	Precursor Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer Table 6-12.	RW
3:0	HS_TWPOST2[3:0]	Adjacent post cursor2 Tap weight. Selects TAP settings for TX waveform. (Default 4'b0000) Refer Table 6-11.	RW

Table 6-10. HSTX Post-Cursor1 Transmit Tap Weights

5.12:8		5.12:8	
VALUE	**TAP WEIGHT (%)**	**VALUE**	**TAP WEIGHT (%)**
00000	0	10000	0
00001	+2.5	10001	–2.5
00010	+5.0	10010	–5.0
00011	+7.5	10011	–7.5
00100	+10.0	10100	–10.0
00101	+12.5	10101	–12.5
00110	+15.0	10110	–15.0
00111	+17.5	10111	–17.5
01000	+20.0	11000	–20.0
01001	+22.5	11001	–22.5
01010	+25.0	11010	–25.0
01011	+27.5	11011	–27.5
01100	+0	11100	–0
01101	+32.5	11101	–32.5
01110	+35.0	11110	–35.0
01111	+37.5	11111	-37.5

Table 6-11. HSTX Post-Cursor2 Transmit Tap Weights

5.3:0		5.3:0	
VALUE	**TAP WEIGHT (%)**	**VALUE**	**TAP WEIGHT (%)**
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 6-12. HSTX Pre-Cursor Transmit Tap Weights

5.7:4		5.7:4	
VALUE	**TAP WEIGHT (%)**	**VALUE**	**TAP WEIGHT (%)**
0000	0	1000	0
0001	+2.5	1001	–2.5
0010	+5.0	1010	–5.0
0011	+7.5	1011	–7.5
0100	+10.0	1100	–10.0
0101	+12.5	1101	–12.5
0110	+15.0	1110	–15.0
0111	+17.5	1111	–17.5

Table 6-13. LS_SERDES_CONTROL_1

Register Address:0x06		**Default:0x8115**	
Bit(s)	**Name**	**Description**	**Access**
15	GLOBAL_LN_WRITE	Global lane write enable. 0 = Control settings are specific to lane addressed. Lane can be specified through LS_LN_CFG_EN 1 = Control settings written to lane specific registers are applied to all lanes (Default 1'b1) Lane specific registers are **LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 & LS_TP_OVERLAY_CONTROL & LS_ALIGN_CODE_CONTROL & LS_LOS_TXFIFO_CONTROL & LN_DATA_SRC_CONTROL & LS_CH_CONTROL_1**	RW
14:12	LS_LN_CFG_EN[2:0]	LS lane cfg control. Writes to lane specific control registers **LS_SERDES_CONTROL_2 & LS_SERDES_CONTROL_3 & LS_TP_OVERLAY_CONTROL & LS_ALIGN_CODE_CONTROL & LS_LOS_TXFIFO_CONTROL & LN_DATA_SRC_CONTROL & LS_CH_CONTROL_1** are applicable to lane selected (Applicable when GLOBAL_LN_WRITE is LOW). Selects selected lane status to be reflected in **LS_LN_ERROR_COUNTER & LS_RXLOS_DET_ERR_COUNT & LS_STATUS_1** 000 = Lane 0 access (Default 3'b000) 001 = Lane 1 access 010 = Lane 2 access 011 = Lane 3 access 100 = Lane 4 access 101 = Lane 5 access 110 = Lane 6 access 111 = Lane 7 access	RW
11:10	RESERVED	For TI use only (Default 2'b00)	RW
9:8	LS_LOOP_ BANDWIDTH[1:0]	LS Serdes PLL Loop Bandwidth settings 00 = Reserved 01 = Applicable when external JC_PLL is NOT used (Default 2'b01) 10 = Applicable when external JC_PLL is used 11 = Reserved	RW
7:5	RESERVED	For TI use only (Default 3'b000)	RW
4	LS_ENPLL	LS Serdes PLL enable control. LS Serdes PLL is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables PLL in LS serdes 1 = Enables PLL in LS serdes (Default 1'b1)	RW
3:0	LS_MPY[3:0]	LS Serdes PLL multiplier setting (Default 4'b0101). Refer to Table 6-14.	RW

Table 6-14. LS PLL Multiplier Control

6.3:0		6.3:0	
VALUE	**PLL MULTIPLIER FACTOR**	**VALUE**	**PLL MULTIPLIER FACTOR**
0000	4x	1000	15x
0001	5x	1001	20x
0010	6x	1010	25x

Table 6-14. LS PLL Multiplier Control (continued)

6.3:0		6.3:0	
VALUE	**PLL MULTIPLIER FACTOR**	**VALUE**	**PLL MULTIPLIER FACTOR**
0011	Reserved	1011	Reserved
0100	8x	1100	Reserved
0101	10x	1101	50x
0110	12x	1110	65x
0111	12.5x	1111	Reserved

Table 6-15. LS_SERDES_CONTROL_2

Register Address:0x07		**Default:0xDD05**	
Bit(s)	**Name**	**Description**	**Access**
15	RESERVED	For TI use only.	RW
14:12	LS_SWING[2:0]	Output swing control on LS Serdes side. (Default 3'b101) Refer to Table 6-16.	RW
11	LS_LOS	LS Serdes LOS detector control 0 = Disable Loss of signal detection on LS serdes lane inputs 1 = Enable Loss of signal detection on LS serdes lane inputs (Default 1'b1)	RW
10	LS_TX_ENRX	LS Serdes enable control on the transmit channel. LS Serdes per lane on transmitter channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
9:8	LS_TX_RATE [1:0]	LS Serdes lane rate settings on transmit channel. 00 = Full rate 01 = Half rate (Default 2'b01) 10 = Quarter rate 11 = Reserved	RW
7:4	LS_DE[3:0]	LS Serdes De-emphasis settings. (Default 4'b0000)	RW
3	RESERVED	For TI use only .	RW
2	LS_RX_ENTX	LS Serdes lane enable control on receive channel. LS Serdes per lane on receiver channel is automatically disabled when PD_TRXx_N is asserted LOW or when register bit 1.15 is set HIGH. 0 = Disables LS serdes lane 1 = Enables LS serdes lane (Default 1'b1)	RW
1:0	LS_RX_RATE [1:0]	LS Serdes lane rate settings on receive channel. 00 = Full rate 01 = Half rate (Default 2'b01) 10 = Quarter rate 11 = Reserved	RW

Table 6-16. LSRX Output AC Mode Output Swing Control

VALUE 7.14:12	**AC MODE**
	TYPICAL AMPLITUDE (mVdfpp)
000	190
001	380
010	560
011	710
100	850
101	950
110	1010
111	1050

Table 6-17. LSRX Output De-emphasis

7.7:4			7.7:4		
VALUE	AMPLITUDE REDUCTION		VALUE	AMPLITUDE REDUCTION	
	(%)	dB		(%)	dB
0000	0	0	1000	38.08	–4.16
0001	4.76	–0.42	1001	42.85	–4.86
0010	9.52	–0.87	1010	47.61	–5.61
0011	14.28	–1.34	1011	52.38	–6.44
0100	19.04	–1.83	1100	57.14	–7.35
0101	23.8	–2.36	1101	61.9	–8.38
0110	28.56	–2.92	1110	66.66	–9.54
0111	33.32	–3.52	1111	71.42	–10.87

Table 6-18. LS_SERDES_CONTROL_3

Register Address:0x08		Default:0x000D	
Bit(s)	Name	Description	Access
15	LS_RX_INVPAIR	LS Serdes lane outputs polarity on the receive channel. 0 = Normal polarity. OUTxyP considered positive data. OUTxyN considered negative data (Default 1'b0) 1 = Inverted polarity. OUTxyP considered negative data. OUTxyN considered positive data	RW
14	LS_TX_INVPAIR	LS Serdes lane inputs polarity on the transmit channel. 0 = Normal polarity. INxyP considered positive data and INxyN considered negative data (Default 1'b0) 1 = Inverted polarity. INxyP considered negative data and INxyP considered positive data	RW
13:12	RESERVED	For TI use only (Default 2'b00)	RW
11:8	LS_EQ[3:0]	LS Serdes Equalization control (Default 4'b0000). Table 6-19	RW
7:0	RESERVED	For TI use only (Default 8'b00001101)	RW

Table 6-19. LS_EQ Serdes Equalization

8.11:8			8.11:8		
VALUE	LOW FREQ GAIN	ZERO FREQ	VALUE	LOW FREQ GAIN	ZERO FREQ
0000	Maximum		1000	Adaptive	365 MHz
0001	Adaptive		1001		275 MHz
0010	Reserved		1010		195 MHz
0011			1011		140 MHz
0100			1100		105 MHz
0101			1101		75 MHz
0110			1110		55 MHz
0111			1111		50 MHz

Table 6-20. HS_OVERLAY_CONTROL

Register Address:0x09		Default:0x0380	
Bit(s)	Name	Description	Access
15:8	RESERVED	For TI use only (Default 8'b00000011)	RW
7	HS_LOS_MASK	0 = HS Serdes LOS status is used to generate HS channel synchronization status. If HS Serdes indicates LOS, channel synchronization indicates synchronization is not achieved 1 = HS Serdes LOS status is not used to generate HS channel synchronization status (Default 1'b1)	RW

Table 6-20. HS_OVERLAY_CONTROL (continued)

Register Address:0x09 Default:0x0380			
Bit(s)	**Name**	**Description**	**Access**
6	LS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of LS SERDES PLL lock status (Default 1'b0) 1 = Allows LS SERDES loss of PLL lock status to be reflected on LOSx pin	RW
5	HS_CH_SYNC_OVERLAY	0 = LOSx pin does not reflect receive channel loss of channel synchronization status or loss of block lock (Default 1'b0) 1 = Allows channel loss of synchronization or loss of block lock to be reflected on LOSx pin	RW
4	HS_INVALID_CODE_ OVERLAY	0 = LOSx pin does not reflect receive channel invalid code word error (Default 1'b0) 1 = Allows invalid code word error to be reflected on LOSx pin	RW
3	HS_AGCLOCK_OVERLAY	0 = LOSx pin does not reflect HS Serdes AGC unlock status (Default 1'b0) 1 = Allows HS Serdes AGC unlock status to be reflected on LOSx pin	RW
2	HS_AZDONE_OVERLAY	0 = LOSx pin does not reflect HS Serdes auto zero calibration not done status (Default 1'b0) 1 = Allows auto zero calibration not done status to be reflected on LOSx pin	RW
1	HS_PLL_LOCK_OVERLAY	0 = LOSx pin does not reflect loss of HS Serdes PLL lock status (Default 1'b0) 1 = Allows HS Serdes loss of PLL lock status to be reflected on LOSx pin	RW
0	HS_LOS_OVERLAY	0 = LOSx pin does not reflect HS Serdes Loss of signal condition (Default 1'b0) 1 = Allows HS Serdes Loss of signal condition to be reflected on LOSx pin	RW

Table 6-21. LS_TP_OVERLAY_CONTROL

Register Address:0x0A Default:0x0500			
Bit(s)	**Name**	**Description**	**Access**
15	LS_RX_OVERSAMPLING	0 = Disable LS lane oversampling on receive path (Default 1'b0) 1 = Enable LS lane oversampling on receive path	RW
14	LS_TX_OVERSAMPLING	0 = Disable LS lane oversampling on transmit path (Default 1'b0) 1 = Enable LS lane oversampling on transmit path	RW
13	LS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by LS_TEST_PATT_SEL on the LS side	RW
12	LS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates PRBS/CRPAT test pattern verification selected by LS_TEST_PATT_SEL on the LS side	RW
10:8	LS_TEST_PATT_SEL[2:0]	LS Test Pattern Selection LS_TEST_PATT_SEL[2:0]. Refer Test pattern procedures section for more information. 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long 100 = CRPAT Short 101, 11x = PRBS pattern selected by LS_PRBS_SEL (Default 3'b101) Errors can be checked by reading LS_LN_ERROR_COUNT register	RW
7	RESERVED	For TI use only (Default 1'b0)	RW
6:4	LS_TX_LANE_DELAY	Manual delay (skew) for selected LS lane on transmit path (Default 3'b000). Applicable only when LS_TX_LANE_DELAY_EN is set. 1 = Enable lane skew delay as specified in LS_TX_LANE_DELAY 000 = 10 bits of lane skew 001 = 20 bits of lane skew 010 = 30 bits of lane skew 011 = 40 bits of lane skew 1xx = Reserved	RW
3	LS_TX_LANE_DELAY_EN	0 = Disable lane skew delay(Default 1'b0) 1 = Overrides any settings from TX0_SKEW_CONFIG (0x16.2:0). Enables skew control through LS_TX_LANE_DELAY.	RW
2	LS_CH_SYNC_OVERLAY	0 = LOSx pin does not reflect LS Serdes lane loss of synchronization condition (Default 1'b0) 1 = Allows LS serdes lane loss of synchronization condition to be reflected on LOSx pin	RW
1	LS_INVALID_CODE_OVERLAY	0 = LOSx pin does not reflect LS Serdes lane invalid code condition (Default 1'b0) 1 = Allows LS serdes lane invalid code condition to be reflected on LOSx pin	RW

Table 6-21. LS_TP_OVERLAY_CONTROL (continued)

Register Address:0x0A		Default:0x0500	
Bit(s)	**Name**	**Description**	**Access**
0	LS_LOS_OVERLAY	0 = LOSx pin does not reflect LS Serdes lane Loss of signal condition (Default 1'b0) 1 = Allows LS serdes lane Loss of signal condition to be reflected on LOSx pin	RW

Table 6-22. HS_TP_CONTROL

Register Address:0x0B		Default:0x0520	
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only.	RW
13	HS_TP_GEN_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern generation selected by bits 11.10:8	RW
12	HS_TP_VERIFY_EN	0 = Normal operation (Default 1'b0) 1 = Activates test pattern verification selected by bits 11.10:8	RW
10:8	HS_TEST_PATT_SEL[2:0]	Test Pattern Selection. Refer Test pattern procedures section for more information. 000 = High Frequency Test Pattern 001 = Low Frequency Test Pattern 010 = Mixed Frequency Test Pattern 011 = CRPAT Long 100 = CRPAT Short 101 = 2^7 - 1 PRBS pattern (Default 3'b101) 110 = 2^{23} - 1 PRBS pattern 111 = 2^{31} - 1 PRBS pattern Errors can be checked by reading HS_ERROR_COUNT register.	RW
7:6	RESERVED	For TI use only (Default 2'b00)	RW
5:4	LS_PRBS_SEL[2:0]	Test Pattern Selection. Refer Test pattern procedures section for more information. 00 = 2^{31} - 1 PRBS pattern 01 = Reserved. 10 = 2^7 - 1 PRBS pattern (Default 2'b10) 11 = 2^{23} - 1 PRBS pattern	RW
3	DEEP_REMOTE_LPBK	0 = Normal functional mode (Default 1'b0) 1 = Enable deep remote loopback mode	RW
2:0	RESERVED	For TI use only (Default 3'b000)	RW

Table 6-23. CLK_SEL_CONTROL

Register Address:0x0D		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:12	LS_TX_FIFO_RESET[7:4]	Reset control for LS lanes 7/6/5/4 FIFO on transmit path (Default 4'b0000) [7] for Lane 7, [6] for Lane 6, [5] for Lane 5, [4] for Lane 4.	RW/SC
11:8	LS_TX_FIFO_RESET[3:0]	Reset control for LS lanes 3/2/1/0 FIFO on transmit path (Default 4'b0000) [3] for Lane 3, [2] for Lane 2, [1] for Lane 1, [0] for Lane 0.	RW/SC
7:6	LANE7_CLK_SEL	00 = Selects LS lane 4 Tx Byteclk as clock for lane 7 (Default 2'b00) 01 = Selects LS lane 6 Tx Byteclk as clock for lane 7 1x = Selects LS lane 7 Tx Byteclk as clock for lane 7	RW
5	LANE6_CLK_SEL	0 = Selects LS lane 4 Tx Byteclk as clock for lane 6 (Default 1'b0) 1 = Selects LS lane 6 Tx Byteclk as clock for lane 6	RW
4	LANE5_CLK_SEL	0 = Selects LS lane 4 Tx Byteclk as clock for lane 5 (Default 1'b0) 1 = Selects LS lane 5 Tx Byteclk as clock for lane 5	RW
3:2	LANE3_CLK_SEL	00 = Selects LS lane 0 Tx Byteclk as clock for lane 3 (Default 2'b00) 01 = Selects LS lane 2 Tx Byteclk as clock for lane 3 1x = Selects LS lane 3 Tx Byteclk as clock for lane 3	RW
1	LANE2_CLK_SEL	0 = Selects LS lane 0 Tx Byteclk as clock for lane 2 (Default 1'b0) 1 = Selects LS lane 2 Tx Byteclk as clock for lane 2	RW
0	LANE1_CLK_SEL	0 = Selects LS lane 0 Tx Byteclk as clock for lane 1 (Default 1'b0) 1 = Selects LS lane 1 Tx Byteclk as clock for lane 1	RW

Table 6-24. RESET_CONTROL

Register Address:0x0E	Default:0x0000		
Bit(s)	**Name**	**Description**	**Access**
15:12	LS_RX_FIFO_RESET[7:4]	Reset control for LS lanes 4-7 FIFO on receive path (Default 4'b0000) [7] for Lane 7, [6] for Lane 6, [5] for Lane 5, [4] for Lane 4.	RW SC(1)
11:8	LS_RX_FIFO_RESET[3:0]	Reset control for LS lanes 0-3 FIFO on receive path (Default 4'b0000) [3] for Lane 3, [2] for Lane 2, [1] for Lane 1, [0] for Lane 0.	
7	HS_TX_FIFO_RESET	Reset control for HS FIFO on transmit path (Default 1'b0)	
6	HS_RX1_FIFO_RESET	Reset control for HS RX1 FIFO (Default 1'b0)	
5	HS_RX0_FIFO_RESET	Reset control for HS RX0 FIFO (Default 1'b0)	
4	LT_RESTART_TRAINING	1 = Restart link/auto train 0 = Normal operation (Default 1'b0)	
3	DATAPATH_RESET	Channel datapath reset control. Required once the desired functional mode is configured. 0 = Normal operation. (Default 1'b0) 1 = Resets channel logic excluding MDIO registers. (Resets both Tx and Rx datapath)	
2:0	RESERVED	For TI use only (Default 3'b000)	

(1) After reset bit is set to one, it automatically sets itself back to zero on the next MDC clock cycle.

Table 6-25. CHANNEL_STATUS_1

Register Address:0x0F	Default:0x0000		
Bit(s)	**Name**	**Description**	**Access**
15	HS_TP_STATUS	Test Pattern status for HS High/Low/Mixed/CRPAT test patterns. 1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in HS_ERROR_COUNTER register (0x10) 0 = Alignment has not been determined	RO
14	LS_TRAINING_FAIL	1 = Training failure has been detected 0 = Training failure has not been detected	RO/LH
13	HS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on HS serial receive inputs	RO/LH
12	HS_AZ_DONE	Auto zero complete indicator. When high, indicates auto zero calibration is complete	RO/LL
11	HS_AGC_LOCKED	Adaptive gain control loop lock indicator. When high, indicates AGC loop is in locked state	RO/LL
10	HS_CHANNEL_SYNC	Channel synchronization status indicator. When high, indicates channel synchronization has achieved	RO/LL
9	RESERVED	For TI use only	RO/LH
8	HS_DECODE_INVALID	Valid when decoder is enabled and during CRPAT test pattern verification. When high, indicates decoder received an invalid code word, or a 8b/10b disparity error. In functional mode, number of DECODE_INVALID errors are reflected in HS_ERROR_COUNTER register (0x10)	RO/LH
7	HS_TX0_FIFO_UNDERFLOW	When high, indicates overflow has occurred in the transmit datapath lane (CTC) FIFO.	RO/LH
6	HS_TX0_FIFO_OVERFLOW	When high, indicates overflow has occurred in the transmit datapath lane (CTC) FIFO.	RO/LH
5	RESERVED	For TI use only	RO/LH
4	BIT_LM_DONE	Applicable only when HS_RX_BIT_INTERLEAVE is set to 1. When high, indicates lane marker detection state machine searched all possible LS lanes, and found valid marker pattern	RO/LH
3	LT_FRAME_LOCK	1 = Training frame delineation detected 0 = Training frame delineation not detected	RO
2	LT_RX_STATUS	1 = Receiver trained and ready to receive data 0 = Receiver training in progress	RO
1	LS_PLL_LOCK	LS Serdes PLL lock indicator When high, indicates LS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO/LL

Table 6-25. CHANNEL_STATUS_1 (continued)

Register Address:0x0F		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
0	HS_PLL_LOCK	HS Serdes PLL lock indicator When high, indicates HS Serdes PLL achieved lock to the selected incoming REFCLK0/1_P/N	RO/LL

Table 6-26. HS_ERROR_COUNTER

Register Address:0x10		Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	HS_ERR_COUNT[15:0]	In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder. In HS test pattern verification mode , this counter reflects error count for the test pattern selected through 11.10:8 When PRBS_EN pin is set, this counter reflects error count for selected PRBS pattern. Counter value cleared to 16'h0000 when read.	COR

Table 6-27. LS_LN_ERROR_COUNTER

Register Address:0x11		Default:0xFFFD	
Bit(s)	**Name**	**Description**	**Access**
15:0	LS_LN_ERR_COUNT[15:0]	LS Lane Error counter. Lane can be selected through LS_LN_CFG_EN[2:0] (6.14:12) In functional mode, this counter reflects number of invalid code words (includes disparity errors) received by decoder. In LS test pattern verification mode , this counter reflects error count for the test pattern selected through 12.10:8 Counter value cleared to 16'h0000 when read.	COR

Table 6-28. LS_STATUS_1 (1)

Register Address:0x13		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	LS_TP_STATUS	Test Pattern status for LS High/Low/Mixed/CRPAT test patterns. 1 = Alignment has achieved and correct pattern has been received. Any bit errors are reflected in LS_LN_ERROR_COUNTER register 0 = Alignment has not been determined	RO
14	LS_RXLOS_DETECT	When high, indicates LOS state machine successfully detected valid LOS pattern for the selected lane. This bit is raw status of LS_ RXLOS_DETECT_LH	RO
13:12	RESERVED	For TI use only.	RO
11	LS_INVALID_DECODE	LS Invalid decode error for selected lane. Error count for each lane can also be monitored through respective LS_LN_ERROR_COUNTER registers	RO/LH
10	LS_LOS	Loss of Signal Indicator. When high, indicates that a loss of signal condition is detected on LS serial receive inputs for selected lane.	RO/LH
9	LS_RXLOS_DETECT_LH	When high, indicates LOS state machine successfully detected valid LOS pattern for the selected lane.	RO/LH
8	LS_CH_SYNC_STATUS	LS Channel sync status for selected lane.	RO/LL
7:4	RESERVED	For TI use only.	RO
3	LS_TX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the transmit datapath lane (CTC) FIFO.	RO/LH
2	LS_TX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the transmit datapath lane (CTC) FIFO.	RO/LH
1	LS_RX_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the receive datapath lane (CTC) FIFO.	RO/LH
0	LS_RX_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath lane (CTC) FIFO.	RO/LH

(1) This is per lane status register. Lane can be selected through LS_LN_CFG[14:12] (Register 0x06)

Table 6-29. HS_STATUS_1

Register Address:0x14		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	RX3_LANE_ALIGN	RX3 lane align status on receive path	RO/LH
14	RX2_LANE_ALIGN	RX2 lane align status on receive path	RO/LH
13	TX3_LANE_ALIGN	TX3 lane align status on transmit path	RO/LH
12	TX2_LANE_ALIGN	TX2 lane align status on transmit path	RO/LH
11	RX1_LANE_ALIGN	RX1 lane align status on receive path	RO/LH
10	RX0_LANE_ALIGN	RX0 lane align status on receive path	RO/LH
9	TX1_LANE_ALIGN	TX1 lane align status on transmit path	RO/LH
8	TX0_LANE_ALIGN	TX0 lane align status on transmit path	RO/LH
7:4	RESERVED	For TI use only.	RO
3	HS_RX1_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the receive datapath lane FIFO when alternate macro HS Rx data is selected.	RO/LH
2	HS_RX1_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath lane FIFO when alternate macro HS Rx data is selected.	RO/LH
1	HS_RX0_FIFO_UNDERFLOW	When high, indicates underflow has occurred in the receive datapath lane FIFO.	RO/LH
0	HS_RX0_FIFO_OVERFLOW	When high, indicates overflow has occurred in the receive datapath lane FIFO.	RO/LH

Table 6-30. CLK_CONTROL

Register Address:0x15		Default:0x0280	
Bit(s)	**Name**	**Description**	**Access**
15:10	RESERVED	For TI use only. Always reads 0.	RW
9	CLKOUT_EN	Output clock enable. 0 = Holds CLKOUTx_P/N output to a fixed value. 1 = Allows CLKOUTx_P/N output to toggle normally (Default 1'b1)	RW
8	CLKOUT_POWERDOWN	0 = Normal operation (Default 1'b0) 1 = Enable CLKOUTx_P/N Power Down.	RW
7:4	CLKOUT_DIV[3:0]	Output clock divide setting. This value is used to divide selected clock (Selected using CLKOUT_SEL) before giving it out onto respective channel CLKOUTx_P/N. 0000 = Divide by 1 0001 = RESERVED 0010 = RESERVED 0011 = RESERVED 0100 = Divide by 2 0101 = RESERVED 0110 = RESERVED 0111 = RESERVED 1000 = Divide by 4 (Default 4'b1000) 1001 = Divide by 8 1010 = Divide by 16 1011 = RESERVED 1100 = Divide by 5 1101 = Divide by 10 1110 = Divide by 20 1111 = Divide by 25	RW
3:0	CLKOUT_SEL[3:0]	Output clock select. Selected Recovered clock sent out on CLKOUTxP/N pins (Default 4'b0000) 00x0 = Selects Macro A HS recovered byte clock as output clock 00x1 = Selects Macro A HS transmit byte clock as output clock 010x = Selects Macro A HSRX VCO divide by 4 clock as output clock 0110 = Selects Lane 0-3 LS recovered byte clock as output clock 0111 = Selects Lane 0-3 LS transmit byte clock as output clock 10x0 = Selects Macro B HS recovered byte clock as output clock 10x1 = Selects Macro B HS transmit byte clock as output clock 110x = Selects Macro B HSRX VCO divide by 4 clock as output clock 1110 = Selects Lane 4-7 LS recovered byte clock as output clock 1111 = Selects Lane 4-7 LS transmit byte clock as output clock	RW

Table 6-31. SKEW_CONFIG_CONTROL

Register Address:0x16		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
14:12	RX1_SKEW_CONFIG[2:0]	Skew config for lanes 4-7 on receive path (Default 3'b000) 000 - No Skew 001 - Align lanes 4,5 010 - Align lanes 4,5,6 X11- Align lanes 4,5,6,7 100 - Align lanes 6,7 101 - Align lanes 4,5 and 6,7 110 - Reserved	RW
10:8	TX1_SKEW_CONFIG[2:0]	Skew config for lanes 4-7 on transmit path (Default 3'b000) 000 - No Skew 001 - Align lanes 4,5 010 - Align lanes 4,5,6 X11- Align lanes 4,5,6,7 100 - Align lanes 6,7 101 - Align lanes 4,5 and 6,7 110 - Reserved	RW

Table 6-31. SKEW_CONFIG_CONTROL (continued)

Register Address:0x16		Default:0x0000	
Bit(s)	**Name**	**Description**	**Access**
6:4	RX0_SKEW_CONFIG[2:0]	Skew config for lanes 0-3 on receive path (Default 3'b000) 000 - No Skew 001 - Align lanes 0,1 010 - Align lanes 0,1,2 X11- Align lanes 0,1,2,3 100 - Align lanes 2,3 101 - Align lanes 0,1 and 2,3 110 - Reserved	RW
2:0	TX0_SKEW_CONFIG[2:0]	Skew config for lanes 0-3 on transmit path (Default 3'b000) 000 - No Skew 001 - Align lanes 0,1 010 - Align lanes 0,1,2 X11- Align lanes 0,1,2,3 100 - Align lanes 2,3 101 - Align lanes 0,1 and 2,3 110 - Reserved	RW

Table 6-32. HS_ALIGN_CODE_CONTROL

Register Address:0x17		Default:0x02BC	
Bit(s)	**Name**	**Description**	**Access**
15	RESERVED	For TI use only (Default 1'b0)	RW
14:12	TX_LANE_MARKER[2:0]	Marker selection on transmit side (Default 3'b000)	RW
11	BIT_LM_EN	0 = Normal operation (Default 1'b0) 1 = Enable lane marker generation in selected LS TX lane through TX_LANE_MARKER When set to 1, lane marker message is generated (CRC field set to 32'hFE00_00FE). When LS_LM_EN and LS_LOS_EN are set to 1, lane marker message is generated.	RW
10:0	RESERVED	For TI use only (Default 11'h2BC)	RW

Table 6-33. BIT_LM_CONTROL

Register Address:0x18		Default:0x0CC8	
Bit(s)	**Name**	**Description**	**Access**
15	RESERVED	For TI use only (Default 1'b0)	RW
14:12	RX_LANE_MARKER[2:0]	Marker selection on receive side (Default 3'b000)	RW
11	BIT_LM_PATT_DETECT_EN	Applicable only when RX_BIT_INTERLEAVE is set to 1. 0 = Normal operation 1 = Enable marker detection (Default 1'b1)	RW
10:0	RESERVED	For TI use only (Default 11'h4C8)	RW

Table 6-34. LS_TXFIFO_CONTROL

Register Address:0x19		Default:0x02BC	
Bit(s)	**Name**	**Description**	**Access**
15:13	LS_TXFIFO_DEPTH_SEL[2:0]	TX FIFO depth select (Default 3'b000)	RW
12:11	LS_TXFFIO_WMK_SEL[1:0]	TX FIFO Water mark select (Default 2'b00)	
10	LS_CHSYNC_ALIGN_CODE_ EN	Lane can be selected in LS_SERDES_CONTROL_1. 0 = Normal operation (Default 1'b0) 1 = Use align code specified in LS_CH_SYNC_ALIGN_CODE in LS ch sync SM	
9:0	LS_CHSYNC_ALIGN_CODE[9:0]	Lane can be selected in LS_SERDES_CONTROL_1. 10 bit align code to use when LS_CHSYNC_ALIGN_CODE_EN is set (Default 10'h2BC)	

Table 6-35. LN_DATA_SRC_CONTROL

Register Address:0x1B	Default: 0x3020[1]		
Bit(s)	**Name**	**Description**	**Access**
15:14	LN_RX_DIV_RATE[1:0]	Divided rate control on the receive side (Default 2'b00) LS divided rate selection on receive path. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14)	RW
13	LN_RX_CTC_EN	LS CTC control on receive path. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14) 0 = CTC disabled for the selected lane on receive path 1 = CTC enabled for the selected lane on receive path (Default 1'b1)	RW
12:11	LN_RX_DATA_SRC_SEL[1:0]	Lane data source selection. Selects the data for selected lane that will be sent out on LS receive out. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14) 0x = LS input 10 = HS input of primary macro(Default 2'b10) 11 = HS input of alternate macro	RW
10:8	LN_RX_DATA_LANE_SEL[2:0]	Lane selection for the data source selected through LN_RX_DATA_SRC_SEL. Selects the data for selected lane that will be sent out on LS receive out. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14) 000 = LS Lane 0 input 001 = LS Lane 1 input 010 = LS Lane 2 input 011 = LS Lane 3 input 100 = LS Lane 4 input 101 = LS Lane 5 input 110 = LS Lane 6 input 111 = LS Lane 7 input	RW
7:6	LN_TX_DIV_RATE[1:0]	Divided rate control on the receive side (Default 2'b00) LS divided rate selection on transmit path. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14) and MACRO_ACCESS(0.13)	RW
5	LN_TX_CTC_EN	LS CTC control on transmit path. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14) 0 = CTC disabled for the selected lane on transmit path 1 = CTC enabled for the selected lane on transmit path (Default 1'b0)	RW
4:3	LN_TX_DATA_SRC_SEL[4:3]	LS lane data source selection. Selects the data for selected lane that will be sent out on HS transmit out. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14) 0x = LS input 10 = HS input (Default 2'b10) 11 = HS input of alternate macro	RW
2:0	LN_TX_DATA_SRC_SEL[2:0]	Lane selection for the data source selected through LN_TX_DATA_SRC_SEL[4:3]. Selects the data for selected lane that will be sent out on HS transmit out. Settings are applicable for the lanes selected through LS_LN_CFG_EN[3:0] (6.15:14) 000 = LS Lane 0 input 001 = LS Lane 1 input 010 = LS Lane 2 input 011 = LS Lane 3 input 100 = LS Lane 4 input 101 = LS Lane 5 input 110 = LS Lane 6 input 111 = LS Lane 7 input	RW

(1) Default for ln0 is 0x3020, ln1 is 0x3121, ln2 is 0x3222, ln 3 is 0x3323. Default for ln4 is 0x3424, ln5 is 0x3525, ln6 is 0x3626, ln7 is 0x3727.

Table 6-36. LS_CH_CONTROL_1

Register Address:0x1C Default: 0x0000			
Bit(s)	**Name**	**Description**	**Access**
15	RESERVED	For TI use only (Default 1'b0)	RW/SC
14:12	LS_RXFIFO_DEPTH_SEL[2:0]	RX FIFO depth select (Default 3'b000)	RW
11:10	LS_RXFIFO_WMK_SEL[1:0]	RX FIFO Water mark select (Default 2'b00)	RW
9	RX_GIGE_EN	0 = Disable GIGE mode on receive path (Default 1'b0) 1 = Enable GIGE mode on receive path	RW
8	TX_GIGE_EN	0 = Disable GIGE mode on transmit path (Default 1'b0) 1 = Enable GIGE mode on transmit path	RW
7:6	RESERVED	For TI use only (Default 2'b00)	RW
5	LS_CHSYNC_FORCE_SYNC	Lane can be selected in LS_SERDES_CONTROL_1. 0 = Keep byte alignment determined by ch sync state machine (Default 1'b0) 1 = Force byte alignment to 9 unless LS_CHSYNC_JOG_EN is 1	RW
4	RESERVED	For TI use only (Default 1'b0)	RW
3	LS_ENC_BYPASS	1 = Disables Encoder on LS side on selected lane. 0 = Normal operation (1'b0)	RW
2	LS_DEC_BYPASS	1 = Disables Decoder on LS side on selected lane. 0 = Normal operation (1'b0)	RW
1:0	LS_CH_SYNC_HYS_SEL[1:0]	LS Channel synchronization hysteresis selection for selected lane. Lane can be selected in LS_SERDES_CONTROL_1. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the LOS state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to LOS 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to LOS	RW

Table 6-37. HS_CH_CONTROL_1

Register Address:0x1D Default: 0x0880			
Bit(s)	**Name**	**Description**	**Access**
15	RESERVED	For TI use only (Default 1'b0)	RW/SC
14:12	HS_RXFIFO_DEPTH_SEL[2:0]	FIFO depth select for both HS RX0/RX1 FIFO's (Default 3'b000)	RW
11	RX_LANE_MARKER_EN	Marker enable control on receive side (Default 1'b1) 0 = Normal operation 1 = Enable marker search/replacement. Marker search/replacement character RW can be selected in VS_RX_MARKER_SEARCH_CHARACTER (0x8002.9:0), VS_RX_MARKER_REPLACE_CHARACTER (0x8003.9:0)	RW
10:8	HS_TXFIFO_DEPTH_SEL[2:0]	HS TX FIFO depth select	RW
7	TX_LANE_MARKER_EN	Marker enable control on transmit side (Default 1'b1) 0 = Normal operation 1 = Enable marker search/replacement. Marker search/replacement character RW can be selected in VS_TX_MARKER_SEARCH_CHARACTER (0x8000.9:0), VS_TX_MARKER_REPLACE_CHARACTER (0x8001.9:0)	RW
6	RESERVED	For TI use only (Default 1'b0)	RW
5	HS_CHSYNC_FORCE_SYNC	0 = Keep byte alignment determined by ch sync state machine (Default 1'b0) 1 = Force byte alignment to 9 unless HS_CHSYNC_JOG_EN is 1	RW
4	HS_CHSYNC_JOG_EN	0 = Disable manual jog function (Default 1'b0) 1 = Enable manual jog function	RW
3	HS_ENC_BYPASS	0 = Normal operation. (Default 1'b0) 1 = Disables 8B/10B encoder on HS side.	RW
2	HS_DEC_BYPASS	0 = Normal operation. (Default 1'b0) 1 = Disables 8B/10B decoder on HS side.	RW

Table 6-37. HS_CH_CONTROL_1 (continued)

Register Address:0x1D		Default: 0x0880	
Bit(s)	**Name**	**Description**	**Access**
1:0	HS_CH_SYNC_HYSTERESIS[1:0]	Channel synchronization hysteresis control on the HS receive channel. 00 = The channel synchronization, when in the synchronization state, performs the Ethernet standard specified hysteresis to return to the unsynchronized state (Default 2'b00) 01 = A single 8b/10b invalid decode error or disparity error causes the channel synchronization state machine to immediately transition from sync to unsync 10 = Two adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync 11 = Three adjacent 8b/10b invalid decode errors or disparity errors cause the channel synchronization state machine to immediately transition from sync to unsync	RW

Table 6-38. EXT_ADDRESS_CONTROL

Register Address:0x1E		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	EXT_ADDR_CONTROL[15:0]	Applicable in Clause 22 mode only. This register should be written with the extended register address to be written/read. Contents of address written in this register can be accessed from Reg 31 (0x1F). (Default 16'h0000)	RW

Table 6-39. EXT_ADDRESS_DATA

Register Address:0x1F		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	EXT_ADDR_DATA[15:0]	Applicable in Clause 22 mode only. This register contains the data associated with the register address written in Register 30 (0x1E)	RW

Table 6-40. VS_TX_MARKER_SEARCH_CHAR

Register Address:0x8000		Default: 0x02BC	
Bit(s)	**Name**	**Description**	**Access**
9:0	TX_SEARCH_MARKER[9:0]	TX Search marker character (Default 10'h2BC)	RW

Table 6-41. VS_TX_MARKER_REPLACE_CHAR

Register Address:0x8001		Default: 0x027C	
Bit(s)	**Name**	**Description**	**Access**
9:0	TX_REPLACE_MARKER[9:0]	TX Replace marker character (Default 10'h27C)	RW

Table 6-42. VS_RX_MARKER_SEARCH_CHAR

Register Address:0x8002		Default: 0x027C	
Bit(s)	**Name**	**Description**	**Access**
9:0	RX_SEARCH_MARKER[9:0]	RX Search marker character (Default 10'h27C)	RW

Table 6-43. VS_RX_MARKER_REPLACE_CHAR

Register Address:0x8003		Default: 0x02BC	
Bit(s)	**Name**	**Description**	**Access**
9:0	RX_REPLACE_MARKER[9:0]	RX Replace marker character (Default 10'h2BC)	RW

Table 6-44. VS_TX_IDLE_P_CHAR

Register Address:0x8004		Default: 0x02BC	
Bit(s)	**Name**	**Description**	**Access**
9:0	TX_IDLE_P[9:0]	TX Idle P character (Default 10'h2BC)	RW

Table 6-45. VS_TX_IDLE_N_CHAR

Register Address:0x8005		Default: 0x02BC	
Bit(s)	**Name**	**Description**	**Access**
9:0	TX_IDLE_N[9:0]	TX Idle N character (Default 10'h2BC)	RW

Table 6-46. VS_RX_IDLE_P_CHAR

Register Address:0x8006		Default: 0x02BC	
Bit(s)	**Name**	**Description**	**Access**
9:0	RX_IDLE_P[9:0]	RX Idle P character (Default 10'h2BC)	RW

Table 6-47. VS_RX_IDLE_N_CHAR

Register Address:0x8007		Default: 0x02BC	
Bit(s)	**Name**	**Description**	**Access**
9:0	RX_IDLE_N[9:0]	RX Idle N character (Default 10'h2BC)	RW

Table 6-48. VS_TX_SCR_CONTROL

Register Address:0x8009		Default: 0xFC00	
Bit(s)	**Name**	**Description**	**Access**
15:2	RESERVED	For TI use only (Default 14'b11111100000000)	RW
1	TX_SCR_20_EN	1 = Enable 20 bit scrambler (post-encoder) on transmit side(Default 1'b0) 0 = Disable 20 bit scrambler (post-encoder) on transmit side	RW
0	TX_SCR_16_EN	1 = Enable 16 bit scrambler (pre-encoder) on transmit side. Seed can be set through 0x800C and 0x800D (Default 1'b0) 0 = Disable 16 bit scrambler (pre-encoder) on transmit side	RW

Table 6-49. VS_TX_SEED_CONTROL_1

Register Address:0x800C		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_SCR_SEED[31:16]	[31:16] bits of 32 bit Tx scrambler seed. TX_SCR_SEED[31:0] must be set to a non-zero value for scrambler to work properly (Default 16'h0000).	RW

Table 6-50. VS_TX_SEED_CONTROL_0

Register Address:0x800D		Default: 0x01FC	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_SCR_SEED[31:16]	[15:0] bits of 32 bit Tx scrambler seed. Bit 0 always set to 1'b0. TX_SCR_SEED[31:0] must be set to a non-zero value for scrambler to work properly (Default 16'h01FC).	RW

Table 6-51. VS_TX_POLY_CONTROL_1

Register Address:0x800E		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_SCR_SEED[31:16]	[31:16] bits of 32 bit Tx scrambler polynomial (Default 16'h0000).	RW

Table 6-52. VS_TX_POLY_CONTROL_0

Register Address:0x800F		Default: 0x00C0	
Bit(s)	**Name**	**Description**	**Access**
15:0	TX_SCR_SEED[31:16]	[15:0] bits of 32 bit Tx scrambler polynomial. Bit 0 always set to 1'b0. (Default 16'h00C0).	RW

Table 6-53. VS_RX_DESCR_CONTROL

Register Address:0x8019		Default: 0xFC00	
Bit(s)	**Name**	**Description**	**Access**
15:2	RESERVED	For TI use only (Default 14'b11111100000000)	RW
1	RX_DESCR_20_EN	1 = Enable 20 bit descrambler (pre-decoder) on transmit side(Default 1'b0) 0 = Disable 20 bit descrambler (pre-decoder) on transmit side	RW
0	RX_DESCR_16_EN	1 = Enable 16 bit descrambler (post-decoder) on transmit side. Seed can be set through 0x801C and 0x801D (Default 1'b0) 0 = Disable 16 bit descrambler (post-decoder) on transmit side	RW

Table 6-54. VS_RX_DESCR_SEED_CONTROL_1

Register Address:0x801C		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	RX_DESCR_SEED[31:16]	[31:16] bits of 32 bit Rx descrambler seed. RX_DESCR_SEED[31:0] must be set to a non-zero value for descrambler to work properly (Default 16'h0000).	RW

Table 6-55. VS_RX_DESCR_SEED_CONTROL_0

Register Address:0x801D		Default: 0x01FC	
Bit(s)	**Name**	**Description**	**Access**
15:0	RX_DESCR_SEED[15:0]	[15:0] bits of 32 bit Rx descrambler seed. Bit 0 always set to 1'b0. RX_DESCR_SEED[31:0] must be set to a non-zero value for descrambler to work properly (Default 16'h01FC).	RW

Table 6-56. VS_RX_DESCR_POLY_CONTROL_1

Register Address:0x801E		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:0	RX_DESCR_POLY[31:16]	[31:16] bits of 32 bit Rx descrambler polynomial (Default 16'h0000).	RW

Table 6-57. VS_RX_DESCR_POLY_CONTROL_0

Register Address:0x801F		Default: 0x00C0	
Bit(s)	**Name**	**Description**	**Access**
15:0	RX_DESCR_POLY[15:0]	[15:0] bits of 32 bit Rx descrambler polynomial. Bit 0 always set to 1'b0. (Default 16'h00C0).	RW

Table 6-58. TI_RESERVED_CONTROL

Register Address:0x8021		Default: 0x000A	
Bit(s)	**Name**	**Description**	**Access**
15:7	RESERVED	For TI use only (Default 9'b000000000)	RW
6	HS_PLL_LOCK_CHECK_ DISABLE	1 = Disable auto HS pll lock status check. 0 = Enable auto HS pll lock status check (Default 1’b0)	RW
5	HS_LOS_CHECK_DISABLE	1 = Disable auto HS los status check 0 = Enable auto HS los sync status check (Default 1’b0)	RW
4	RESERVED	For TI use only (Default 1’b0)	RW
3	CLKOUT_EN_AUTO_DISABLE	This bit controls the signal which flat lines CLKOUT and applicable only when CLKOUT is selected to have HS Recovered byte clock 1 = CLKOUT clock flat lined if HS LOS is detected (Default 1’b1) 0 = CLKOUT clock not flat lined if HS LOS is detected	RW
2:0	RESERVED	For TI use only (Default 3’b010)	RW

Table 6-59. VS_LS_TX_ERROR_CODE

Register Address:0x8026		Default: 0x02FE	
Bit(s)	**Name**	**Description**	**Access**
9:0	LS_TX_ERROR_CODE[9:0]	Error code to be transmitted if LS TX FIFO has error (Default 10’h2FE)	RW

Table 6-60. VS_LS_RX_ERROR_CODE

Register Address:0x8027		Default: 0x02FE	
Bit(s)	**Name**	**Description**	**Access**
9:0	LS_RX_ERROR_CODE[9:0]	Error code to be transmitted if LS RX FIFO has error (Default 10’h2FE)	RW

Table 6-61. VS_HS_RX_ERROR_CODE

Register Address:0x8028		Default: 0x02FE	
Bit(s)	**Name**	**Description**	**Access**
9:0	HS_RX_ERROR_CODE[9:0]	Error code to be transmitted if HS RX FIFO has error (Default 10’h2FE)	RW

Table 6-62. VS_HS_TX_ERROR_CODE

Register Address:0x8029		Default: 0x02FE	
Bit(s)	**Name**	**Description**	**Access**
9:0	HS_TX_ERROR_CODE[9:0]	Error code to be transmitted if HS TX FIFO has error (Default 10’h2FE)	RW

Table 6-63. TI_RESERVED_STATUS

Register Address:0x9020		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15:1	RESERVED	For TI use only.	RO
0	LT_START_PROTOCOL	1 = Start up protocol in progress 0 = Start up protocol complete	RO

Table 6-64. LT_LINK_PARTNER_CONTROL

Register Address:0x9098		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
13	LT_LP_PRESET	1 = KR preset coefficients 0 = Normal operation	RO
12	LT_LP_INITIALIZE	1 = Initialize KR coefficients 0 = Normal operation	RO

Table 6-64. LT_LINK_PARTNER_CONTROL (continued)

Register Address:0x9098		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
9:8	LT_LP_COEFF_SWG	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
7:6	LT_LP_COEFF_PS2	Post2 tap control update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
5:4	LT_LP_COEFF_P1	Coefficient K(+1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
3:2	LT_LP_COEFF_0	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold	RO
1:0	LT_LP_COEFF_M1	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO

Table 6-65. LT_LINK_PARTNER_STATUS

Register Address:0x9099		Default: 0x0000	
Bit(s)	**Name**	**Description**	**Access**
15	LT_LP_RX_READY	1 = LP receiver has determined that training is complete and prepared to receive data 0 = LP receiver is requesting that training continue	RO
9:8	LT_LP_COEFF_SWG_STAT	Swing update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
7:6	LT_LP_COEFF_PS2_STAT	Post2 tap control update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not udated	RO
5:4	LT_LP_COEFF_P1_STAT	Plus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
3:2	LT_LP_COEFF_0_STAT	0 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
1:0	LT_LP_COEFF_M1_STAT	Minus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO

Table 6-66. LT_LOCAL_DEVICE_CONTROL

Register Address:0x909A Default: 0x0000			
Bit(s)	**Name**	**Description**	**Access**
15:14	RESERVED	For TI use only	RO
13	LT_LD_PRESET	1 = KR preset coefficients 0 = Normal operation (Default 1'b0)	RO
12	LT_ LD_INITIALIZE	1 = Initialize KR coefficients 0 = Normal operation (Default 1'b0)	RO
9:8	LT_LD_COEFF_SWG	Swing update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
7:6	LT_LD_COEFF_PS2	Post2 tap control update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
5:4	LT_ LD_COEFF_P1	Coefficient K(+1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
3:2	LT_ LD_COEFF_0	Coefficient K(0) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO
1:0	LT_ LD_COEFF_M1	Coefficient K(-1) update 11 = Reserved 01 = Increment 10 = Decrement 00 = Hold (Default 2'b00)	RO

Table 6-67. LT_LOCAL_DEVICE_STATUS

Register Address: 0x909B Default: 0x0000			
Bit(s)	**Name**	**Description**	**Access**
15	LT_ LD_RX_READY	1 = LD receiver has determined that training is complete and prepared to receive data 0 = LD receiver is requesting that training continue	RO
5:4	LT_ LD_COEFF_P1_STAT	Plus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
3:2	LT_ LD_COEFF_0_STAT	0 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO
1:0	LT_ LD_COEFF_M1_STAT	Minus 1 update 11 = Maximum 01 = Updated 10 = Minimum 00 = Not updated	RO

Table 6-68. TI_Reserved Control and Status Registers

Register Name	Register Address	Default Value	Access		Register Name	Register Address	Default Value	Access
TI_RESERVED_CONTROL	0x0C	0xFFFF	RW		TI_RESERVED_CONTROL	0x9003	0xAF14	RW
TI_RESERVED_STATUS	0x12	0x0000	COR		TI_RESERVED_CONTROL	0x9004	0x007F	RW
TI_RESERVED_CONTROL	0x1A	0x03C8	RW		TI_RESERVED_CONTROL	0x9005	0x1C00	RW
TI_RESERVED_CONTROL	0x8008	0x0115	RW		TI_RESERVED_CONTROL	0x9006	0x0000	RW
TI_RESERVED_CONTROL	0x800A	0xBC3C	RW		TI_RESERVED_CONTROL	0x9007	0x4890	RW
TI_RESERVED_CONTROL	0x800B	0x0000	RW		TI_RESERVED_CONTROL	0x9008	0xC00C	RW
TI_RESERVED_CONTROL	0x801A	0xBC3C	RW		TI_RESERVED_CONTROL	0x9009	0xD333	RW
TI_RESERVED_CONTROL	0x8020	0x0200	RW		TI_RESERVED_CONTROL	0x900A	0x5E8F	RW
TI_RESERVED_CONTROL	0x8022	0x0000	RW		TI_RESERVED_CONTROL	0x900B	0xAFAF	RW
TI_RESERVED_CONTROL	0x8023	0x0190	RW		TI_RESERVED_CONTROL	0x900C	0x0800	RW
TI_RESERVED_CONTROL	0x8024	0x0000	RW		TI_RESERVED_CONTROL	0x900D	0x461A	RW
TI_RESERVED_CONTROL	0x8025	0xF000	RW		TI_RESERVED_CONTROL	0x900E	0x1723	RW
TI_RESERVED_STATUS	0x8030 - 0x8033	0x0000	RO		TI_RESERVED_CONTROL	0x900F	0x7003	RW
TI_RESERVED_STATUS	0x8035	0x0000	RO		TI_RESERVED_CONTROL	0x9010	0x0851	RW
TI_RESERVED_CONTROL	0x8050	0x0000	RW		TI_RESERVED_CONTROL	0x9011	0x1EFF	RW
TI_RESERVED_STATUS	0x8060 - 0x8067	0xFFFD	COR		TI_RESERVED_STATUS	0x9021	0xFFFD	COR
TI_RESERVED_STATUS	0x8068 - 0x806F	0xFFFD	COR		TI_RESERVED_STATUS	0x9022	0x0000	RO
TI_RESERVED_STATUS	0x8070 - 0x8077	0xFFFD	COR		TI_RESERVED_STATUS	0x9023	0x0000	RO
TI_RESERVED_STATUS	0x8078 - 0x807F	0xFFFD	COR		TI_RESERVED_STATUS	0x9024 - 0x9029	0x0000	RO
TI_RESERVED_CONTROL	0x8100	0x0000	RW		TI_RESERVED_CONTROL	0xA000	0x0000	RW
TI_RESERVED_CONTROL	0x8102	0xF280	RW		TI_RESERVED_STATUS	0xA010 - 0xA018	0x0000	RO
TI_RESERVED_CONTROL	0x8103	0x0000	RW		TI_RESERVED_CONTROL	0xA116	0x0000	RW
TI_RESERVED_CONTROL	0x9000	0x0249	RW		TI_RESERVED_CONTROL	0xA117	0x0000	RW
TI_RESERVED_CONTROL	0x9001	0x0200	RW		TI_RESERVED_STATUS	0xA118 - 0xA119	0x0000	RO

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE		UNIT
		MIN	MAX	
Supply voltage	DVDD, VDDA_LS/HS, VDDT_LS/HS, VPP, VDDD	–0.3	1.4	V
	VDDRA/B_LS/HS, VDDO[1:0]	–0.3	2.2	V
Input Voltage, V_I, (LVCMOS/CML/Analog)		–0.3	Supply + 0.3	V
Storage temperature		–65	150	°C
Operating junction temperature			105	°C
Electrostatic discharge:	HBM		1	kV
	CDM		500	V
Characterized free-air operating temperature range		–40	85	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground (VSS).

7.2 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
	Digital / analog supply voltages	VDDD, VDDA_LS/HS, DVDD, VDDT_LS/HS, VPP		0.95	1.00	1.05	V
	SERDES PLL regulator voltage	VDDRA_LS/HS, VDDRB_LS/HS	1.5V nominal	1.425	1.5	1.575	V
			1.8V nominal	1.71	1.8	1.89	
	LVCMOS I/O supply voltage	VDDO[1:0]	1.5V nominal	1.425	1.5	1.575	V
			1.8V nominal	1.71	1.8	1.89	
I_{DD}	Supply current	VDDD	10 Gbps			580	mA
		VDDA_LS/HS				600	
		DVDD + VPP				650	
		VDDT_LS/HS				600	
		VDDRA/B_LS				70	
		VDDRA/B_HS				70	
		VDDO[1:0]				10	
P_D	Power dissipation		Nominal		1.5		W
			Worst case supply voltage, temperature, and process at 10Gbps with both channels active, default swing and Clkout settings.			1.9	
I_{SD}	Shutdown current	VDDD	PD* Asserted			210	mA
		VDDA				70	
		DVDD + VPP				150	
		VDDT				65	
		VDDRA_HS/LS + VDDRB_HS/LS				7	
		VDDO				5	
T_{RISE}	REFCLK0P/N, REFCLK1P/N rise/fall time		10% to 90%	50		350	ps
J_R	REFCLK0P/N, REFCLK1P/N random jitter		12kHz to 20MHz			1	ps

7.3 High Speed Side Serial Transmitter Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(p-p)}$	TX output differential peak-to-peak voltage swing	SWING = 0000	50	130	220	mV_{pp}
		SWING = 0001	110	220	320	
		SWING = 0010	180	300	430	
		SWING = 0011	250	390	540	
		SWING = 0100	320	480	650	
		SWING = 0101	390	570	770	
		SWING = 0110	460	660	880	
		SWING = 0111	530	750	1000	
		SWING = 1000	590	830	1100	
		SWING = 1001	660	930	1220	
		SWING = 1010	740	1020	1320	
		SWING = 1011	820	1110	1430	
		SWING = 1100	890	1180	1520	
		SWING = 1101	970	1270	1610	
		SWING = 1110	1060	1340	1680	
		SWING = 1111	1090	1400	1740	
		Transmitter disabled			30	
$V_{pre/post}$	TX output pre/post cursor emphasis voltage	See register bits TWPOST1, TWPOST2, and TWPRE for de-emphasis settings. See Figure 7-2	–17.5/ –37.5%		+17.5/ +37.5%	
V_{CMT}	TX output common mode voltage	100-Ω differential termination, DC-coupled		$V_{DDT} – 0.25 × V_{OD(p-p)}$		mV
T_r, T_f	Differential output signal rise, fall time (20% to 80%), Differential load = 100Ω		24			ps
J_{T1}	Serial output total jitter				0.28	UI
J_{D1}	Serial output deterministic jitter				0.15	UI
J_{R1}	Serial output random jitter				0.15	UI
DCD	Duty Cycle Distortion	PLL multiplier = 10			0.035	UI
SDD22	Differential output return loss	50 MHz < f < 2.5 GHz			9	dB
		2.5 GHz < f < 7.5 GHz			See (1)	dB
SCC22	Common-mode output return loss	50 MHz < f < 2.5 GHz			6	dB
		2.5 GHz < f < 7.5 GHz			See (2)	dB
$T_{(LATENCY)}$	Transmit path latency			See Figure 3-7		

(1) Common-mode output return loss, SDD22 = 9 – 12 log10(f / 2500MHz)) dB
(2) Differential input return loss, SCC2 = 6 - 12 log10(f / 2500MHz)) dB

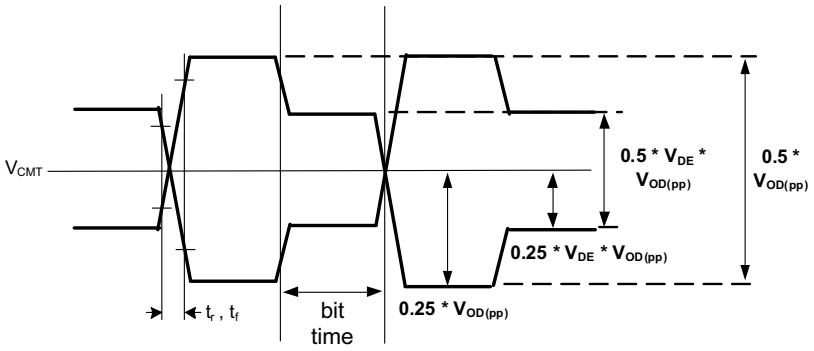
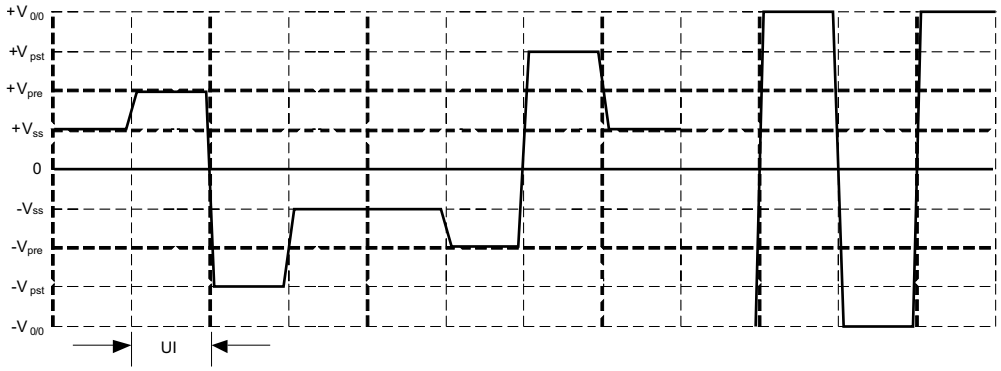


Figure 7-1. Transmit Output Waveform Parameter Definitions



h_{-1} = TWPRE (0% ≥ -17.5% for typical application) setting

h_1 = TWPOST1 (0% ≥ -37.5% for typical application) setting

$h_0 = 1 - |h_1| - |h_{-1}|$

$V_{0/0}$ = Output Amplitude with TWPRE = 0%, TWPOST = 0%.

V_{ss} = Steady State Output Voltage = $V_{0/0} * | h_1 + h_0 + h_{-1}|$

V_{pre} = PreCursor Output Voltage = $V_{0/0} * | -h_1 - h_0 + h_{-1}|$

V_{pst} = PostCursor Output Voltage = $V_{0/0} * | -h_1 + h_0 + h_{-1}|$

Figure 7-2. Pre/Post Cursor Swing Definitions

7.4 High Speed Side Serial Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	RX input differential voltage, |RXP – RXN|	Full rate, AC coupled	50		600	mV
		Half/Quarter/Eighth rate, AC coupled	50		800	
$V_{ID(pp)}$	RX input differential peak-to-peak voltage swing, 2×|RXP – RXN|	Full rate, AC coupled	100		1200	mV_{pp}
		Half/Quarter/Eighth rate, AC coupled	100		1600	
C_I	RX input capacitance				2	pF
J_{TOL}	Jitter tolerance, PRBS 31 test pattern at 10 Gbps (see Figure 7-3 for attenuation curve)	Applied sinusoidal jitter			0.115	mV_{RMS}
		Applied random jitter			0.130	
		Applied duty cycle distortion			0.035	
		Broadband noise amplitude (RMS)			5.2	
SDD11	Differential input return loss	100 MHz < f < 0.75* [Serial BIt Rate]	9			dB
		0.75*[Serial BIt Rate] < f < [Serial Bit Rate]	See (1)			
$t_{(LATENCY)}$	Receive path latency		See Figure 3-7			

(1) Differential input return loss, SDD11 = 8 – 16.6 $\log_{10}$(f / 0.75*[Serial BIt Rate])) dB

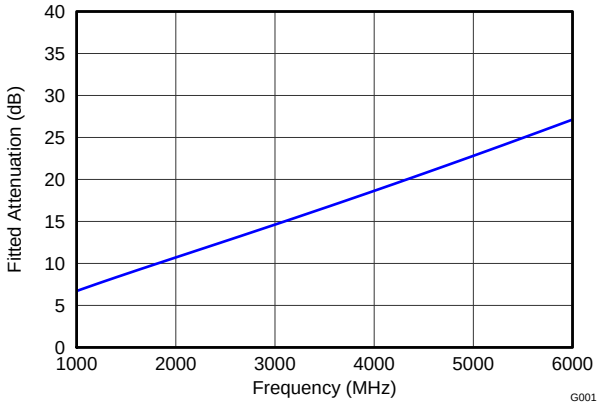


Figure 7-3. Fitted Channel Attenuation Limit

7.5 Low Speed Side Serial Transmitter Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(pp)}$	Transmitter output differential peak-to-peak voltage swing	SWING = 000	110	190	280	mV_{pp}
		SWING = 001	280	380	490	
		SWING = 010	420	560	700	
		SWING = 011	560	710	870	
		SWING = 100	690	850	1020	
		SWING = 101	760	950	1150	
		SWING = 110	800	1010	1230	
		SWING = 111	830	1050	1270	

Low Speed Side Serial Transmitter Characteristics *(continued)*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DE	Transmitter output de-emphasis voltage swing reduction	DE = 0000		0		dB
		DE = 0001		0.42		
		DE = 0010		0.87		
		DE = 0011		1.34		
		DE = 0100		1.83		
		DE = 0101		2.36		
		DE = 0110		2.92		
		DE = 0111		3.52		
		DE = 1000		4.16		
		DE = 1001		4.86		
		DE = 1010		5.61		
		DE = 1011		6.44		
		DE = 1100		7.35		
		DE = 1101		8.38		
		DE = 1110		9.54		
		DE = 1111		10.87		
V_{CMT}	Transmitter output common mode voltage	100-Ω differential termination, DC-coupled		$V_{DDT} - 0.5 \times V_{OD(p-p)}$		mV
t_R, t_F	Differential output signal rise, fall time (20% to 80%), Differential Load = 100Ω		30			ps
J_T	Serial output total jitter				0.35	UI
J_D	Serial output deterministic jitter				0.17	UI
DCD	Duty Cycle Distortion				0.035	UI

7.6 Low Speed Side Serial Receiver Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Receiver input differential voltage, |INP – INN|	Full rate, AC coupled	50		600	mV
		Half/Quarter rate, AC coupled	50		800	
$V_{ID(pp)}$	Receiver input differential peak-to-peak voltage swing 2×|INP – INN|	Full rate, AC coupled	100		1200	mV_{dfpp}
		Half/Quarter rate, AC coupled	100		1600	
C_I	Receiver input capacitance				2	pF
J_{TOL}	Jitter tolerance, total jitter at serial input (DJ + RJ) (BER 10^{-15})	Zero crossing, Half/Quarter rate			0.66	UI_{p-p}
		Zero crossing, Full rate			0.65	
J_{DR}	Serial input deterministic jitter (BER 10^{-15})	Zero crossing, Half/Quarter rate			0.50	UI_{p-p}
		Zero crossing, Full rate			0.35	
$t_{lane-skew}$	Lane-to-lane input skew				30	UI

7.7 Reference and Output Clock Characteristics (REFCLK0P/N, REFCLK1P/N)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F	Frequency		122.88		425	MHz
FHS_{offset}	Accuracy	Relative to nominal HS serial data rate	–100		100	ppm
		Relative to incoming HS serial data rate	–200		200	
FLS_{offset}	Accuracy to LS serial data	Synchronous (Multiple/Divide)	0	0	0	ppm
DC	Duty cycle	High time	45%	50%	55%	
V_{ID}	Differential input voltage		250		2000	mV_{pp}
C_{IN}	Input capacitance				1	pF
R_{IN}	Differential input impedance			100		Ω

7.8 Differential Output Clock Characteristics (CLKOUTAP/CLKOUTBP/N)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	Peak to peak	1000		2000	mV_{pp}
T_{RISE}	Output rise time	10% to 90%, 2pF lumped capacitive load, AC-coupled			350	ps
R_{TERM}	Output termination	CLKOUTA/BP/N to DVDD		50		Ω
F	Output frequency		0		500	MHz

7.9 LVCMOS Electrical Characteristics (VDDO)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = 2 mA, Driver enabled (1.8V)	VDDO – 0.45		VDDO	V
		I_{OH} = 2 mA, Driver enabled (1.5V)	0.75 × VDDO		VDDO	
V_{OL}	Low-level output voltage	I_{OL} = –2 mA, Driver enabled (1.8V)	0		0.45	V
		I_{OL} = –2 mA, Driver enabled (1.5V)	0		0.25 × VDDO	
V_{IH}	High-level input voltage		0.65 × VDDO		VDDO + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.35 × VDDO	V
I_{IH}, I_{IL}	Receiver only	Low/High input current			±170	µA
I_{OZ}	Driver only	Driver disabled			±25	µA
	Driver/Receiver with Pullup/Pulldown	Driver disabled with Pull Up/Down enabled			±195	
C_{IN}	Input capacitance				3	pF

7.10 MDIO Timing Requirements

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{period}	MDC period	See Figure 7-4	100			ns
t_{setup}	MDIO setup to ↑ MDC		10			ns
t_{hold}	MDIO hold to ↑ MDC		10			ns
T_{valid}	MDIO valid from MDC ↑		0		40	ns

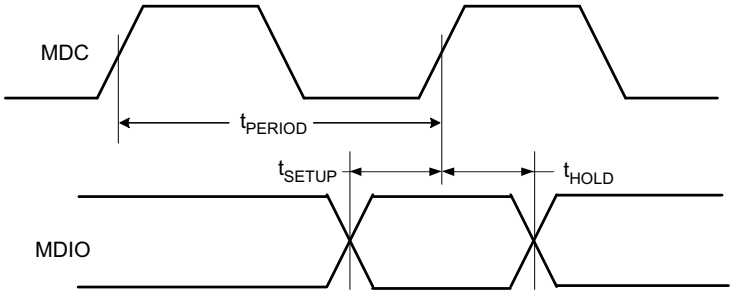


Figure 7-4. MDIO Read/Write Timing

7.11 JTAG Timing Requirements

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{PERIOD}	TCK period	See Figure 7-5	66.67			ns
T_{SETUP}	TDI/TMS/TRST_N setup to ↑ TCK		3			ns
T_{HOLD}	TDI/TMS/TRST_N hold from ↑ TCK		5			ns
T_{VALID}	TDO delay from TCK Falling		0		10	ns

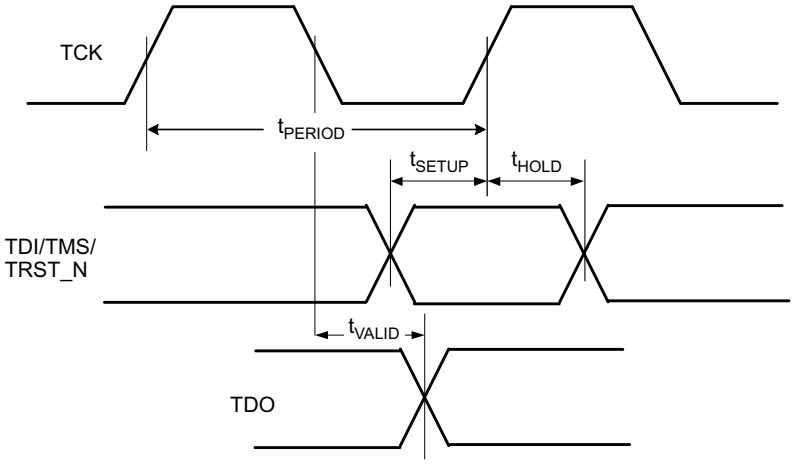


Figure 7-5. JTAG Timing

7.12 Power Sequencing Guidelines

The TLK10081 allows either the core or I/O power supply to be powered up for an indefinite period of time while the other supply is not powered up, if all of the following conditions are met:

1. All maximum ratings and recommending operating conditions are followed.
2. Bus contention while 1.5/1.8V power is applied (>0V) must be limited to 100 hours over the projected lifetime of the device.
3. Junction temperature is less than 105°C during device operation. Note: Voltage stress up to the absolute maximum voltage values for up to 100 hours of lifetime operation at junction temperature of 105°C or lower will minimally impact reliability.

The TLK10081 LVCMOS inputs are not failsafe (i.e. cannot be driven with the I/O power disabled). TLK10081 inputs should not be driven high until their associated power supplies are active.

8 MECHANICAL AND THERMAL DATA

8.1 Package Thermal Dissipation Ratings

Table 8-1 details the thermal characteristics of the TLK10081 package.

Table 8-1. Package Thermal Characteristics

JEDEC STANDARD BOARD		
PARAMETER		**VALUE**
Θ_{JA}	Theta-JA	25.5
Ψ_{JT}	Psi-JT	1.8
Ψ_{JB}	Psi-JB	13.7
CUSTOM TYPICAL APPLICATION BOARD (1)		
Θ_{JA}	Theta-JA	24.5
Ψ_{JT}	Psi-JT	0.9
Ψ_{JB}	Psi-JB	11

(1) Custom Typical Application Board Characteristics:
- 10x15 inches
- 12 layer
  - 8 power/ground layers – 95% copper (1oz)
  - 4 signal layers – 20% copper (1oz)

$\Psi_{JB} = (T_J - T_B)/(\text{Total Device Power Dissipation})$
T_J = Device Junction Temperature
T_B = Temperature of PCB 1 mm from device edge.

$\Psi_{JT} = (T_J - T_C)/(\text{Total Device Power Dissipation})$
T_J = Device Junction Temperature
T_C = Hottest temperature on the case of the package.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLK10081CTR	Active	Production	FCBGA (CTR) | 144	119 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK10081
TLK10081CTR.A	Active	Production	FCBGA (CTR) | 144	119 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-4-260C-72 HR	-40 to 85	TLK10081

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

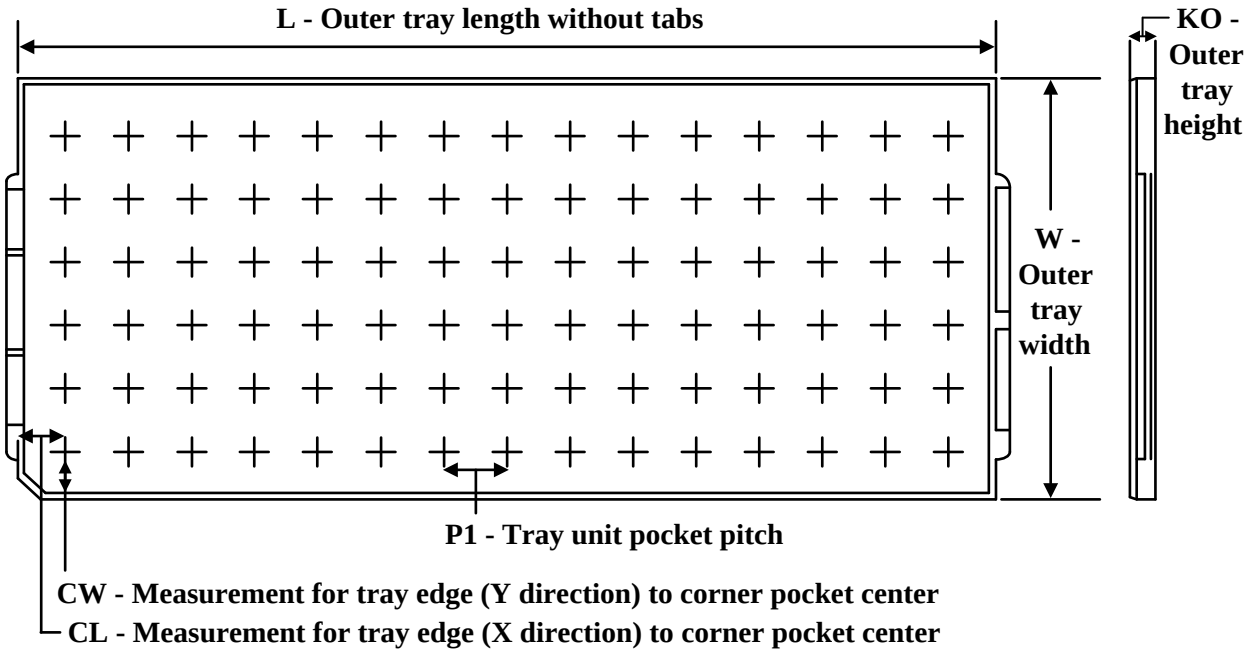
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TRAY

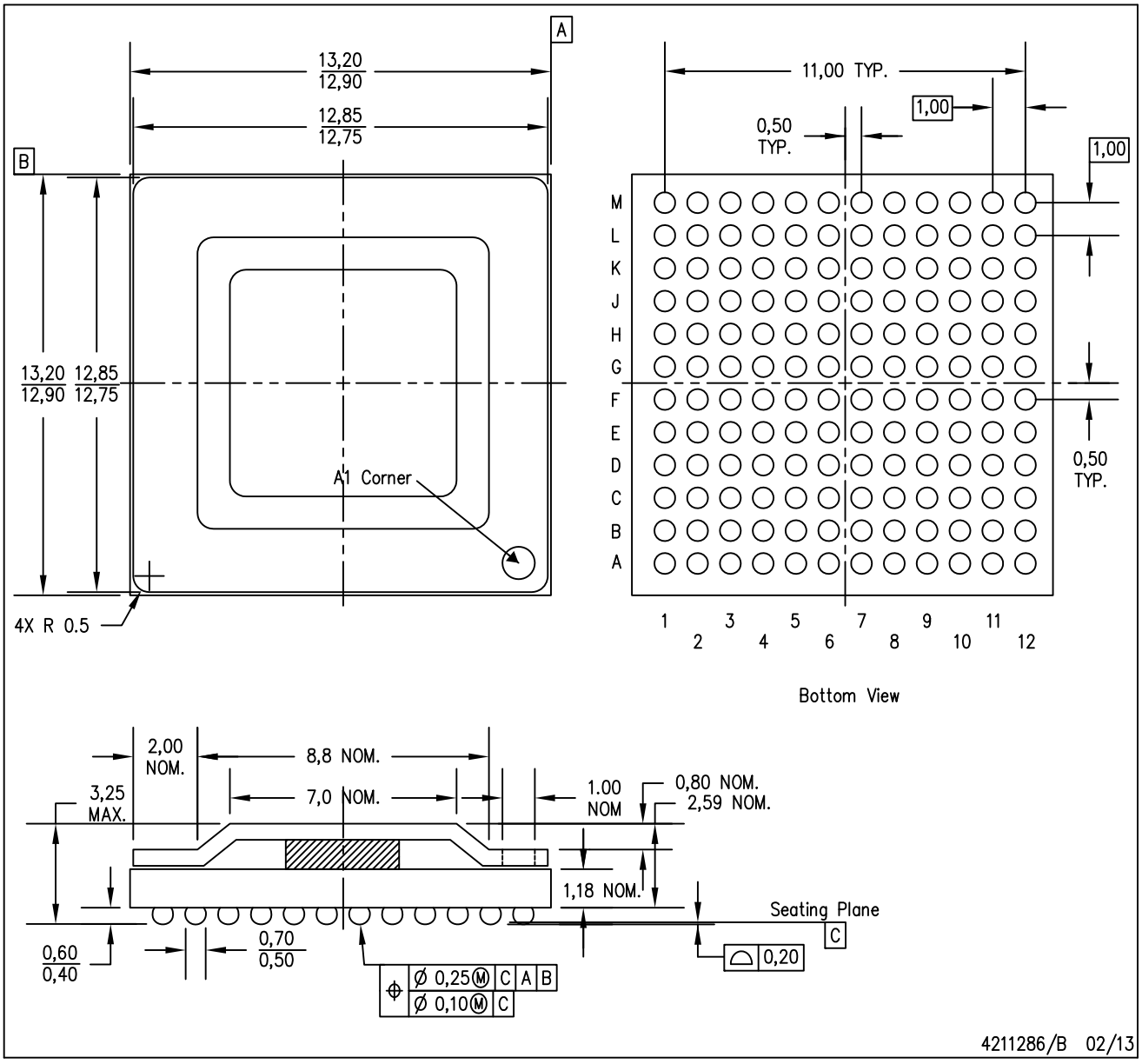


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TLK10081CTR	CTR	FCBGA	144	119	7x17	150	315	135.9	7620	18.1	12.7	12.9
TLK10081CTR.A	CTR	FCBGA	144	119	7x17	150	315	135.9	7620	18.1	12.7	12.9

CTR (S–PBGA–N144) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Flip chip application only.
D. Pb–free die bump and solder ball.

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