TLIN1028-Q1 Automotive LIN 125-mA System Basis Chip (SBC)

1 Features

- AEC-Q100 (Grade 1): Qualified for automotive applications
- Local interconnect network (LIN) physical layer specification ISO/DIS 17987–4 compliant and conforms to SAE J2602 recommended practice for LIN
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Supports 12-V applications
- Wide operating ranges
  - ±58 V LIN bus fault protection
  - LDO output supporting 3.3 V or 5 V
  - Sleep mode: Ultra-low current consumption allows wake-up event from:
    - LIN bus or local wake through EN pin
  - Power-up and down glitch-free operation
- Protection features:
  - ESD protection, V_{SUP} under-voltage protection
  - TXD dominant time out (DTO) protection, Thermal shutdown
  - Unpowered node or ground disconnection fail-safe at system level
- V_{CC} sources up to 125 mA with DRB and DDA package
- Available in SOIC (8) and HSOIC (8) packages, and leadless VSON (8) package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Hybrid, electric & powertrain systems
- Automotive infotainment and cluster
- Appliances

3 Description

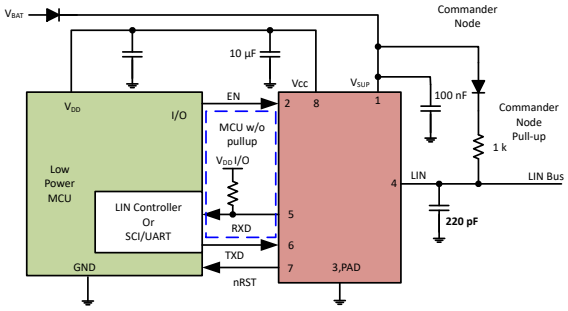
The TLIN1028-Q1 is a local interconnect network (LIN) physical layer transceiver, compliant to LIN 2.2A ISO/DIS 17987–4 standards, with an integrated low dropout (LDO) voltage regulator.

This LIN system basis chip (SBC) reduces system complexity by providing a 3.3 V or 5 V rail with up to 70 mA (D) or 125 mA (DRB and DDA) of current to power microprocessors, sensors or other devices. The TLIN1028-Q1 has an optimized current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The TLIN1028-Q1 converts the LIN protocol data stream on the TXD input into a LIN bus signal. The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin.

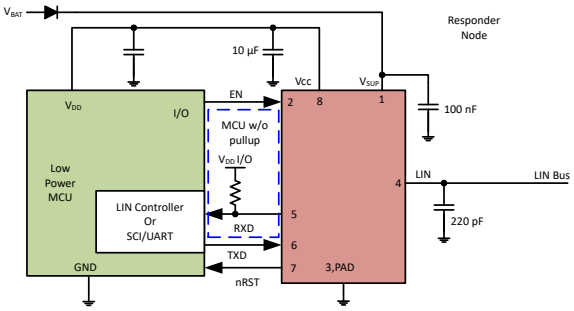
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TLIN1028D-Q1	SOIC (8)	4.90 mm x 3.91 mm
TLIN1028DDA-Q1	HSOIC (8)	4.90 mm x 3.91 mm
TLIN1028DRB-Q1	VSON (8)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematics, Commander Node(1)



Simplified Schematics, Responder Node(2)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2020) to Revision B (June 2022)	Page
• Changed all instances of legacy terminology to commander and responder where mentioned	1
• Changed *nRST is only dependent..* statement to: *nRST is dependen*t in the nRST (Reset Output) section	23
• Changed nRST: Float to nRST: GND in the sleep mode section of Figure 9-5	25

Changes from Revision * (August 2019) to Revision A (July 2020)	Page
• Changed the document status From: *Advanced Information* To: *Production* data	1
• Added *Feature*: Functional Safety-Capable	1

5 Description (continued)

Ultra-low current consumption is possible using the sleep mode which allows wake up via LIN bus or EN pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode. No external pull-up components are required for responder node applications. Commander node applications require an external pull-up resistor (1 kΩ) plus a series diode per the LIN specification

6 Pin Configuration and Functions

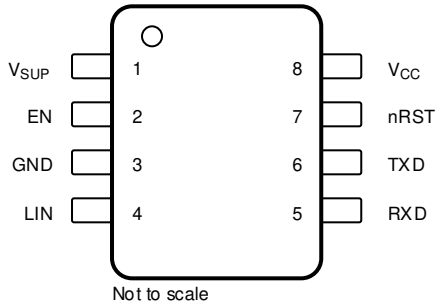


Figure 6-1. D Package, 8-Pin (SOIC), Top View

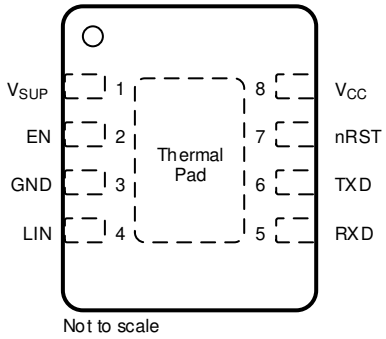


Figure 6-2. DRB Package, 8-Pin (VSON), Top View

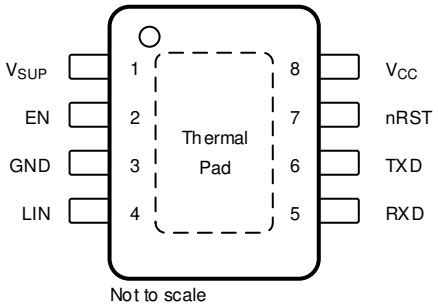


Figure 6-3. DDA Package, 8-Pin (HSOIC), Top View

Table 6-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	V_{SUP}	HV Supply In	Device supply voltage (connected to battery in series with external reverse-blocking diode)
2	EN	D I	Enable input
3	GND	GND	Ground [2] [3]
4	LIN	HV I/O	LIN bus single-wire transmitter and receiver
5	RXD	D O	RXD output (open-drain) interface reporting state of LIN bus voltage
6	TXD	D I	TXD input interface to control state of LIN output
7	nRST	D O	Reset output (active low)
8	V_{CC}	Supply Out	Output voltage from integrated LDO

(1) HV - High Voltage, DI - Digital Input, DO - Digital Output, HV I/O - High Voltage Input/Output
(2) When the thermal pad is present, it must be soldered to ground plane.
(3) If the DDA package is placed onto a D package footprint without the thermal pad soldered down, expect the performance to match the D package and not the DDA package.

7 Specifications

7.1 Absolute Maximum Ratings

(1)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range	–0.3	42	V
V_{LIN}	LIN Bus input voltage	–58	58	V
V_{CC50}	Regulated 5 V Output Supply	–0.3	6	V
V_{CC33}	Regulated 3.3 V Output Supply	–0.3	4.5	V
V_{nRST}	Reset output voltage	–0.3	V_{CC} + 0.3	V
V_{LOGIC_INPUT}	Logic input voltage	–0.3	6	V
V_{LOGIC_OUTPUT}	Logic output voltage	–0.3	6	V
I_{VCC}	V_{CC} supply current(2)		300	mA
I_O	Digital pin output current	–8	8	mA
$I_{O(nRST\_RXD)}$	Reset and RXD open-drain output current	–5	5	mA
T_J	Junction temperature	–40	165	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Device will enter thermal shutdown prior to hitting this limit. If the limit is reached the device may sustain permanent damage.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) classification level H2: V_{SUP}, LIN, and WAKE with respect to ground		±8000	V
		Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002(1)		±4000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 ESD Ratings, IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge per IEC 62228-2 (1), LIN, V_{SUP} terminal to GND	Contact discharge	±15000	V
		Indirect ESD discharge	±15000	V
$V_{(ESD)}$	Powered electrostatic discharge per SAE J2962-1(3)	Contact discharge	±8000	V
		Air discharge	±25000	
Transient	ISO 7637-2 and IEC 62215-3 transients per IEC 62228-1(2)	Pulse 1	-100	V
		Pulse 2a	75	
		Pulse 3a	-150	
		Pulse 3b	100	
Transient	ISO 7637 slow transients pulse	Per SAE J2962-1(4)	30	V

(1) IEC 62228-2 ESD testing performed at third party. Different system-level configurations may lead to different results.
(2) ISO 7637 is a system-level transient test. Different system-level configurations may lead to different results.
(3) SAE J2962-1 Testing performed at third party US3 approved EMC test facility.
(4) ISO 7637 is a system-level transient test. Results given here are specific to the SAE J2962-1 Test specification conditions. Different system-level configurations may lead to different results.

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply voltage	5.5		28	V

		MIN	NOM	MAX	UNIT
V_{LIN}	LIN bus input voltage	0		28	V
V_{LOGIC5}	Logic pin voltage	0		5.25	V
$V_{LOGIC33}$	Logic pin voltage	0		3.465	V
$I_{OH(DO)}$	Digital terminal HIGH level output current	-2			mA
$I_{OL(DO)}$	Digital terminal LOW level output current			2	mA
$C_{(VSUP)}$	V_{SUP} supply capacitance	100			nF
$C_{(VCC)}$	V_{CC} supply capacitance; 20 µA to full load	1.5			µF
$C_{(VCC)}$	V_{CC} supply capacitance; no load to full load	10			µF
ESR_{CO}	Output ESR requirements	0.001		2	Ω

7.5 Thermal Information

THERMAL METRIC(1)		TLIN1028			UNIT
		D	DRB	DDA	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.4	45.7	40.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	49.2	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.9	18.9	15.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.6	0.7	4.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.7	18.8	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.7	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Power Supply Characteristics

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
V_{SUP}	Operational supply voltage (ISO/DIS 17987 Param 10)(2)	Device is operational beyond the LIN defined nominal supply voltage range. See Figure 8-1 and Figure 8-2	5.5		36	V
V_{SUP}	Nominal supply voltage (ISO/DIS 17987 Param 10)(2)	Normal and Standby Modes: Ramp VSUP while LIN signal is a 10 kHz square wave with 50 % duty cycle and swing between 5.5 V ≤ V_{LIN} ≤ 28 V. See Figure 8-1 and Figure 8-2	5.5		28	V
		Sleep Mode	5.5		28	V
UV_{SUPR}	Under voltage V_{SUP} threshold	Ramp Up		3.5	4.2	V
UV_{SUPF}	Under voltage V_{SUP} threshold	Ramp Down	1.8	2.1	2.7	V
U_{VHYS}	Delta hysteresis voltage for V_{SUP} under voltage threshold			1.5		V
I_{SUP}	Transceiver and LDO supply current (D Package)	Transceiver normal mode dominant plus LDO output			80	mA
I_{SUP}	Transceiver and LDO supply current (DRB and DDA Packages)	Transceiver normal mode dominant plus LDO output			135	mA
$I_{SUPTRXDOM}$	Supply current transceiver only	Normal Mode: EN = V_{CC}, bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF		1.2	5	mA
		Standby Mode: EN = 0 V, bus dominant: total bus load where R_{LIN} ≥ 500 Ω and C_{LIN} ≤ 10 nF		1	2.1	mA

7.6 Power Supply Characteristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SUPTRXREC}$	Supply current transceiver only(3)	Normal Mode: EN = V_{CC}, Bus recessive: LIN = V_{SUP},		450	775	µA
		Standby Mode: EN = 0 V, LIN = recessive = V_{SUP}, I_{OH} from processor ≤ 1 µA		38	55	µA
		Added Standby Mode current through the RXD pull-up resistor with a value of 100 kΩ: EN = 0 V, LIN = recessive = VSUP, RXD = GND(1)			55	
$I_{SUPTRXSLP}$	Sleep mode supply current transceiver only	5.5 V < V_{SUP} ≤ 28 V, LIN = V_{SUP}, EN = 0 V, TXD and RXD floating		17	33	µA
REGULATED OUTPUT V_{CC}						
V_{CC}	Regulated output (D package)	V_{SUP} = 5.5 to 28 V, I_{CC} = 1 to 70 mA	–2		2	%
V_{CC}	Regulated output (DRB and DDA package)	V_{SUP} = 5.5 to 28 V, I_{CC} = 1 to 125 mA	–2		2	%
$\Delta V_{CC(\Delta VSUP)}$	Line regulation	V_{SUP} = 5.5 to 28 V, ΔV_{CC}, I_{CC} = 10 mA			50	mV
$\Delta V_{CC(\Delta VSUPL)}$	Load regulation (DRB and DDA package)	I_{CC} = 1 to 125 mA, V_{SUP} = 14 V, ΔV_{CC}			50	mV
$\Delta V_{CC(\Delta VSUPL)}$	Load regulation (D package)	I_{CC} = 1 to 70 mA, V_{SUP} = 14 V, ΔV_{CC}			50	mV
V_{DROP}	Dropout voltage (5 V LDO) (DRB and DDA package)	V_{SUP} – V_{CC}, I_{CC} = 125 mA;		300	600	mV
V_{DROP}	Dropout voltage (5 V LDO) (D package)	V_{SUP} – V_{CC}, I_{CC} = 70 mA;		300	600	mV
V_{DROP}	Dropout voltage (3.3 V LDO) (DRB and DDA package)	V_{SUP} – V_{CC}, I_{CC} = 125 mA;		350	700	mV
V_{DROP}	Dropout voltage (3.3 V LDO) (D package)	V_{SUP} – V_{CC}, I_{CC} = 70 mA;		350	700	mV
UV_{CC5R}	Under voltage 5 V V_{CC} threshold	Ramp Up		4.7	4.86	V
UV_{CC5F}	Under voltage 5 V V_{CC} threshold	Ramp Down	4.2	4.45		V
UV_{CC33R}	Under voltage 3.3 V V_{CC} threshold (3)	Ramp Up		2.9	3.1	V
UV_{CC33F}	Under voltage 3.3 V V_{CC} threshold(3)	Ramp Down	2.5	2.75		V
$t_{DET(UVCC)}$	VCC undervoltage deglitch time. An UV_{CC} event will not be recognized unless the duration is longer than this.(3)	C_{nRST} = 20pF	1		15	µs
I_{CCOUT}	Output current (D Package)	V_{CC} in regulation with 12 V V_{SUP}	0		70	mA
I_{CCOUT}	Output current (DRB and DDA package)	V_{CC} in regulation with 12 V V_{SUP}	0		125	mA
I_{CCOUTL}	Output current limit	V_{CC} short to ground			275	mA
PSRR	Power supply rejection ratio(3)	V_{RIP} = 0.5 V_{PP}, Load = 10 mA, f = 100 Hz, CO = 10 µF		60		dB
T_{SDR}	Thermal shutdown temperature	Internal junction temperature - rising	165			°C
T_{SDF}	Thermal shutdown temperature	Internal junction temperature - falling			150	°C
T_{SDHYS}	Thermal shutdown hysteresis			10		°C

(1) RXD pin is an open-drain output. In standby mode RXD is pulled low which has the device pulling current through V_{SUP} through the pull-up resisitor to V_{CC}. The value of the pull-up resistor impacts the standby mode current. A 10 kΩ resistor value can add as much as 500 µA of current.
(2) Operational supply voltage and nominal supply voltage are in relationship to the LIN transceiver. A VSUP above 28 V means the device will function but may not meet the rest of the parametric data while the nominal range means the device will meet the parametric data minus any differences provided in the test conditions.
(3) Specified by design

7.7 Electrical Charateristics

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXD OUTPUT TERMINAL (OPEN-DRAIN)						
V_{OL}	Output low voltage	Based upon a 2 kΩ to 10 kΩ external pull-up to V_{CC}			0.2	V_{CC}
I_{OL}	Low-level output current, open-drain	LIN = 0 V, RXD = 0.4 V	1.5			mA
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, RXD = V_{CC}	–5	0	5	µA

7.7 Electrical Charateristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TXD INPUT TERMINAL						
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{IH}	High-level input voltage		2		5.5	V
I_{IH}	High-level input leakage current	TXD = high	–5	0	5	µA
R_{TXD}	Internal pull-up resistor value		125	350	800	kΩ
LIN TERMINAL (REFERENCED TO V_{SUP})						
V_{OH}	High-level output voltage(1)	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 5.5 V to 36 V	0.85			V_{SUP}
V_{OL}	Low-level output voltage(1)	LIN dominant, TXD = low, V_{SUP} = 5.5 V to 36 V			0.2	V_{SUP}
V_{IH}	High-level input voltage(1)	LIN recessive, TXD = high, I_O = 0 mA, V_{SUP} = 5.5 V to 36 V	0.47		0.6	V_{SUP}
V_{IL}	Low-level input voltage(1)	LIN dominant, TXD = low, V_{SUP} = 5.5 V to 36 V	0.4		0.53	V_{SUP}
$V_{SUP\_NON\_OP}$	V_{SUP} where impact of recessive LIN bus < 5% (ISO/DIS 17987 Param 11)	TXD & RXD open, V_{LIN} = 5.5 V to 42 V, Bus Load = 60 kΩ + diode and 1.1 kΩ + diode	–0.3		42	V
I_{BUS_LIM}	Limiting current (ISO/DIS 17987 Param 12)	TXD = 0 V, V_{LIN} = 36 V, R_{MEAS} = 440 Ω, V_{SUP} = 36 V, V_{BUSdom} < 4.518 V; Figure 8-6	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Receiver leakage current, dominant (ISO/DIS 17987 Param 13)	V_{LIN} = 0 V, V_{SUP} = 12 V Driver off/recessive, R_{MEAS} = 499 Ω; Figure 8-7	–1			mA
$I_{BUS\_PAS\_rec1}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} ≥ V_{SUP}, 5.5 V ≤ V_{SUP} ≤ 36 V Driver off, R_{MEAS} = 1 kΩ; Figure 8-8			20	µA
$I_{BUS\_PAS\_rec2}$	Receiver leakage current, recessive (ISO/DIS 17987 Param 14)	V_{LIN} = V_{SUP}, Driver off, R_{MEAS} = 1 kΩ; Figure 8-8	–8		8	µA
$I_{BUS\_NO\_GND}$	Leakage current, loss of ground (ISO/DIS 17987 Param 15)	GND = V_{SUP}, V_{SUP} = 12 V, 0 V ≤ V_{LIN} ≤ 28 V, R_{MEAS} = 1 kΩ; Figure 8-9	–1		1	mA
$I_{BUS\_NO\_BAT}$	Leakage current, loss of supply (ISO/DIS 17987 Param 16)	0 V ≤ V_{LIN} ≤ 28 V, V_{SUP} = GND, R_{MEAS} = 10 kΩ; Figure 8-10			8	µA
V_{BUSdom}	Low-level input voltage (ISO/DIS 17987 Param 17)	LIN dominant (including LIN dominant for wake up); Figure 8-3, Figure 8-4			0.4	V_{SUP}
V_{BUSrec}	High-level input voltage (ISO/DIS 17987 Param 18)	LIN recessive; Figure 8-3, Figure 8-4	0.6			V_{SUP}
V_{BUS_CNT}	Receiver center threshold (ISO/DIS 17987 Param 19)	V_{BUS_CNT} = (V_{IL} + V_{IH})/2; Figure 8-3, Figure 8-4	0.475	0.5	0.525	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO/DIS 17987 Param 20)(2)	V_{HYS} = (V_{IL} - V_{IH}); Figure 8-3, Figure 8-4	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN term pull-up path (ISO/DIS 17987 Param 21)	By design and characterization	0.4	0.7	1.0	V
R_{PU}	Internal Pull-up resistor to V_{SUP} (ISO/DIS 17987 Param 26)	Normal and Standby modes	20	45	60	kΩ
I_{RSLEEP}	Pull-up current source to V_{SUP}	Sleep mode, V_{SUP} = 12 V, LIN = GND	–20		–2	µA
C_{LINPIN}	Capacitance of the LIN pin (6)				25	pF
EN INPUT TERMINAL						
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{HYS}	Hysteresis voltage	By design and characterization	30		500	mV
I_{IL}	Low-level input current	EN = Low	–6	0	6	µA
R_{EN}	Internal pull-down resistor		125	350	800	kΩ
nRST TERMINAL (OPEN DRAIN OUTPUT)						
I_{LKG}	Leakage current, high-level	LIN = V_{SUP}, nRST = V_{CC}	–6		6	µA
V_{OL}	Low-level output voltage	Based upon external pull up to V_{CC}			0.2	V_{CC}
I_{OL}	Low-level output current, open-drain	LIN = 0 V, nRST = 0.4 V	1.5			mA
DUTY CYCLE CHARACTERISTICS						

7.7 Electrical Charateristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D1	Duty Cycle 1 (ISO/DIS 17987 Param 27 and J2602 Normal battery)(3) (4)	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 50/52 µs, D1 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See Figure 8-11, Figure 8-12)	0.396			
D2	Duty Cycle 2 (ISO/DIS 17987 Param 28 and J2602 Normal battery)(3) (4)	$TH_{REC(MIN)}$ = 0.422 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.284 x V_{SUP}, V_{SUP} = 7.6 V to 18 V, t_{BIT} = 50/52 µs (20 kbps), D2 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-11, Figure 8-12)			0.581	
D3	Duty Cycle 3 (ISO/DIS 17987 Param 29 and J2602 Normal battery)(3) (4)	$TH_{REC(MAX)}$ = 0.778 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.616 x V_{SUP}, V_{SUP} = 7 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) (See Figure 8-11, Figure 8-12)	0.417			
D4	Duty Cycle 4 (ISO/DIS 17987 Param 30 and J2602 Normal battery)(3) (4)	$TH_{REC(MIN)}$ = 0.389 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.251 x V_{SUP}, V_{SUP} = 7.6 V to 18 V, t_{BIT} = 96 µs (10.4 kbps), D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-11, Figure 8-12)			0.59	
$D1_{LB}$	Duty Cycle 1 J2602 Low battery (4) (5)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 50/52 µs, $D1_{LB}$ = $t_{BUS\_rec(min)/(2\ x\ tBIT)}$ (See Figure 8-11, Figure 8-12)	0.396			
$D2_{LB}$	Duty Cycle 2 J2602 Low battery (4) (5)	T $TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 6.1 V to 7.6 V, t_{BIT} = 50/52 µs, $D2_{LB}$ = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-11, Figure 8-12)			0.581	
$D3_{LB}$	Duty Cycle 3 J2602 Low battery (4) (5)	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5.5 V to 7 V, t_{BIT} = 96 µs, $D3_{LB}$ = $t_{BUS\_rec(min)/(2\ x\ tBIT)}$ (See Figure 8-11, Figure 8-12)	0.417			
$D4_{LB}$	Duty Cycle 4 J2602 Low battery (4) (5)	T $TH_{REC(MIN)}$ = 0.496 x V_{SUP}, $TH_{DOM(MIN)}$ = 0.361 x V_{SUP}, V_{SUP} = 6.1 V to 7.6 V, t_{BIT} = 96 µs, $D4_{LB}$ = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) (See Figure 8-11, Figure 8-12)			0.59	

(1) SAE J2602 loads include: commander node: 5.5 nF; 4 kΩ and for a commander node: 5.5 nF; 875 Ω
(2) V_{HYS} is defined for both ISO 17987 and SAE J2602-1.
(3) ISO 17987 loads include 1 nF; 1 kΩ/ 6.8nF; 660 Ω/ 10 nF; 500 Ω; with t_{BIT} values of 50 µs and 96 µs
(4) SAE J2602 loads include: commander node: 5.5 nF; 4 kΩ/ 899 pF; 20 kΩ and for a responder node: 5.5 nF; 875 Ω/ 899 pF; 900 Ω; with t_{BIT} values of 52 µs and 96 µs
(5) ISO 17987 does not have a low battery specification. Using the ISO 17987 loads these low battery duty cycle parameters are covered for t_{BIT} values of 50 µs and 96 µs
(6) Specified by design

7.8 AC Switching Characteristics

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time (ISO/DIS 17987 Param 31)	R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (See Figure 8-13, Figure 8-14 and Figure 8-18)			6	µs
t_{rs_sym}	Symmetry of receiver propagation delay time Receiver rising propagation delay time (ISO/DIS 17987 Param 32)	Rising edge with respect to falling edge, (t_{rx_sym} = t_{rx_pdf} – t_{rx_pdr}), R_{RXD} = 2.4 kΩ, C_{RXD} = 20 pF (Figure 8-13, Figure 8-14 and Figure 8-18)	–2		2	µs
t_{LINBUS}	LIN wakeup time (minimum dominant time on LIN bus for wakeup)	See Figure 8-17, Figure 9-3 and Figure 9-4	25	100	150	µs

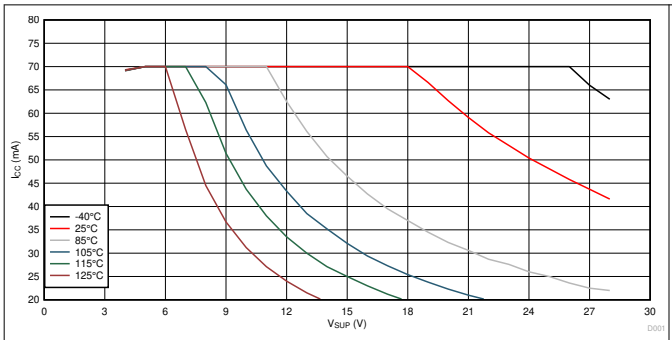
7.8 AC Switching Characteristics (continued)

parameters valid over –40°C ≤ T_J ≤ 150 °C range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CLEAR}	Time to clear false wake-up prevention logic if LIN bus had a bus stuck dominant fault (recessive time on LIN bus to clear bus stuck dominant fault)	See Figure 9-4	8	17	50	µs
t_{TXD_DTO}	Dominant state time out		20	34	80	ms
t_{EN}	Enable pin deglitch time(1)	Time of enable pin state change before initiating mode change or sampling TXD pin: See Figure 8-15	3		12	µs
t_{MODE_CHANGE}	Mode change delay time from normal mode to sleep or standby modes	Time to change from normal mode to sleep or standby after TXD pin sampling after EN pin set low: See Figure 8-15			20	µs
t_{MODE_CHANGE}	Mode change delay time from sleep mode to normal mode	Time to change from sleep mode to normal mode through EN pin and not due to a wake event; RXD pulled up to V_{CC}: See Figure 8-15			400	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid after t_{EN}: See Figure 8-15			35	µs
t_{PWR}	Power-up time	Upon power up, time it takes for nRST to go high			2	ms

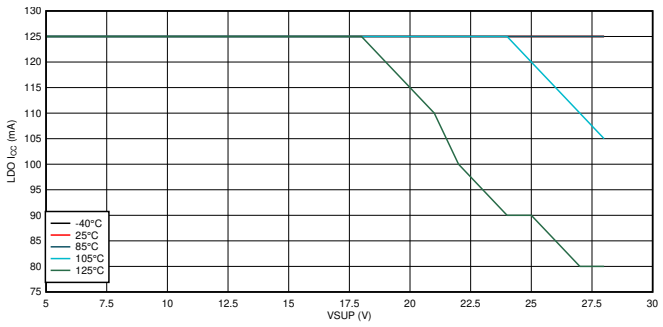
(1) Specified by design

7.9 Typical Characteristics



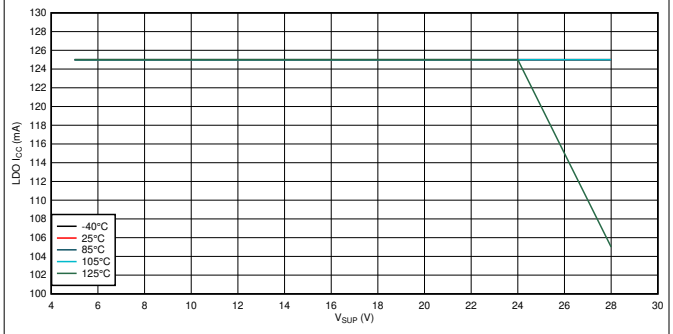
Package = D V_{CC} = 3.3 V Temp = Ambient

Figure 7-1. I_{CC} vs V_{SUP} vs Temperature



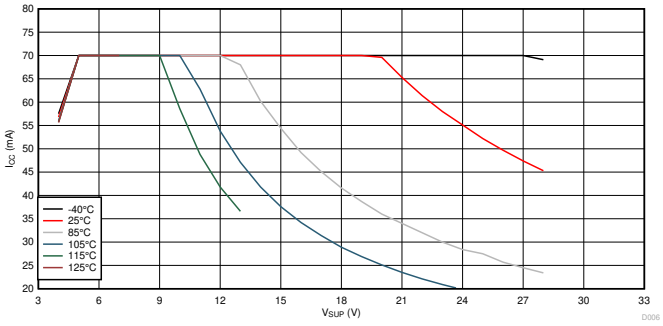
Package = DRB V_{CC} = 3.3 V Temp = Ambient

Figure 7-2. I_{CC} vs V_{SUP} vs Temperature



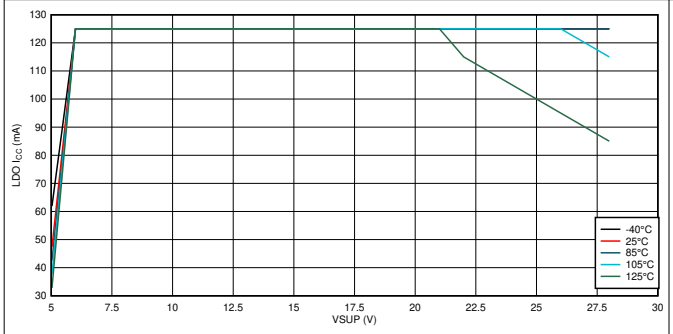
Package = DDA V_{CC} = 3.3 V Temp = Ambient

Figure 7-3. I_{CC} vs V_{SUP} vs Temperature



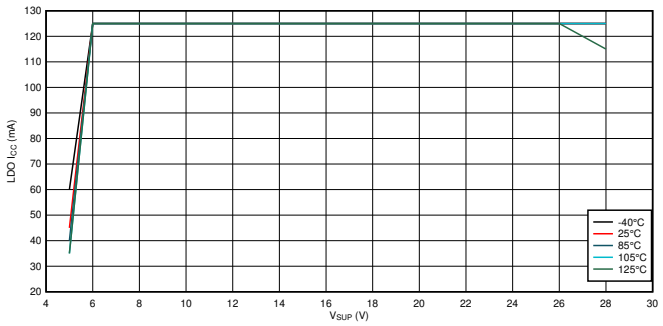
Package = D V_{CC} = 5 V Temp = Ambient

Figure 7-4. I_{CC} vs V_{SUP} vs Temperature



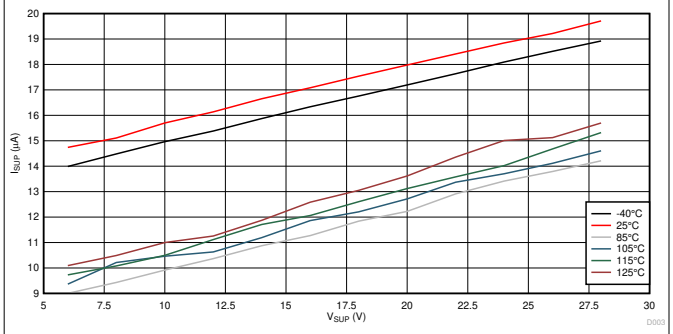
Package = DRB V_{CC} = 5 V Temp = Ambient

Figure 7-5. I_{CC} vs V_{SUP} vs Temperature



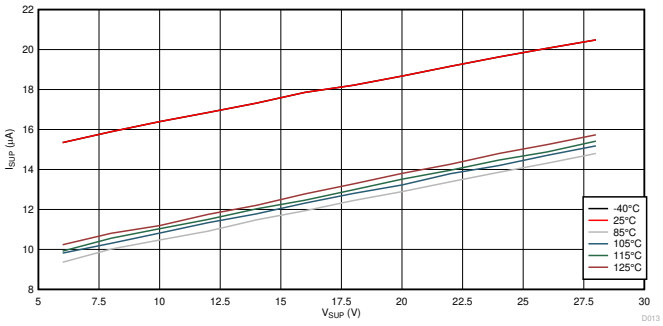
Package = DDA V_{CC} = 5 V Temp = Ambient

Figure 7-6. I_{CC} vs V_{SUP} vs Temperature



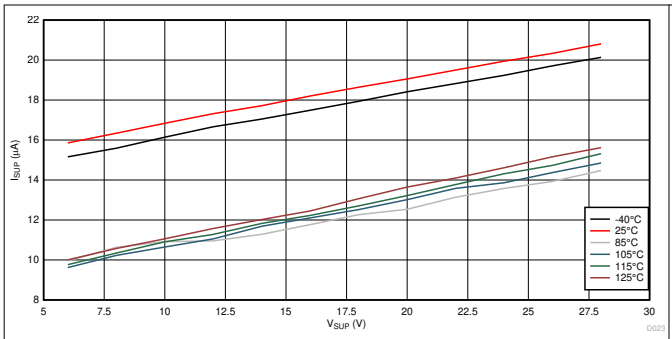
Package = D V_{CC} = 3.3 V Temp = Ambient

Figure 7-7. Sleep Mode Current Across V_{SUP} and Temperature



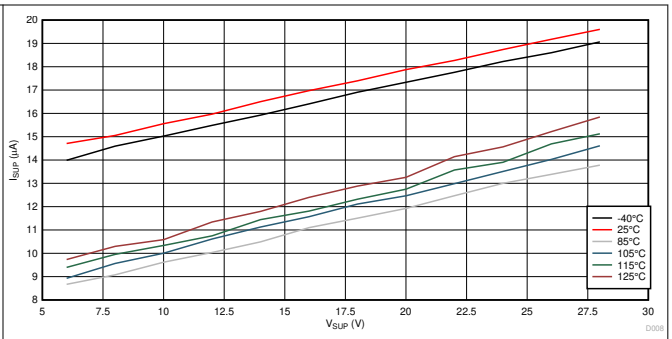
Package = DRB V_{CC} = 3.3 V Temp = Ambient

Figure 7-8. Sleep Mode Current Across V_{SUP} and Temperature



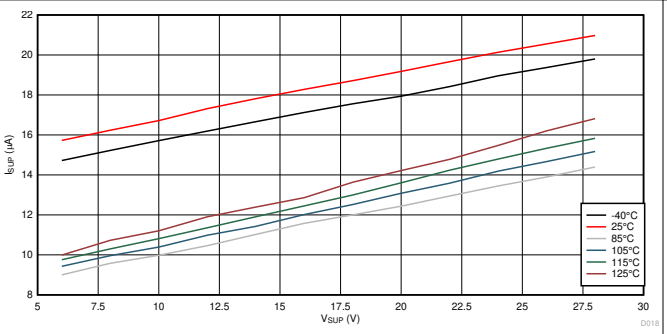
Package = DDA V_{CC} = 3.3 V Temp = Ambient

Figure 7-9. Sleep Mode Current Across V_{SUP} and Temperature



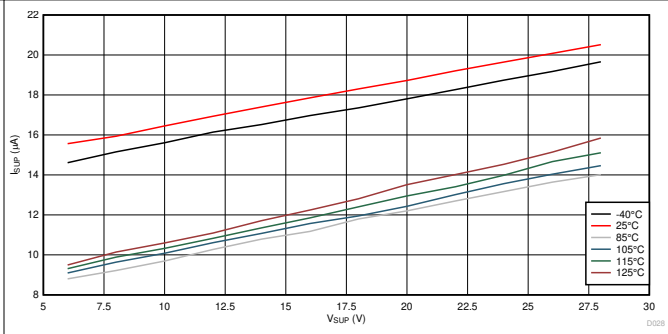
Package = D V_{CC} = 5 V Temp = Ambient

Figure 7-10. Sleep Mode Current Across V_{SUP} and Temperature



Package = DRB V_{CC} = 5 V Temp = Ambient

Figure 7-11. Sleep Mode Current Across V_{SUP} and Temperature



Package = DDA V_{CC} = 5 V Temp = Ambient

Figure 7-12. Sleep Mode Current Across V_{SUP} and Temperature

Note

For the LDO I_{CC} vs V_{SUP} vs Temperature typical curves the data was collected on a high-k EVM board using a forced air system. The curves show performance based upon thermal resistance $R_{\theta JB}$.

8 Parameter Measurement Information

8.1 Test Circuit: Diagrams and Waveforms

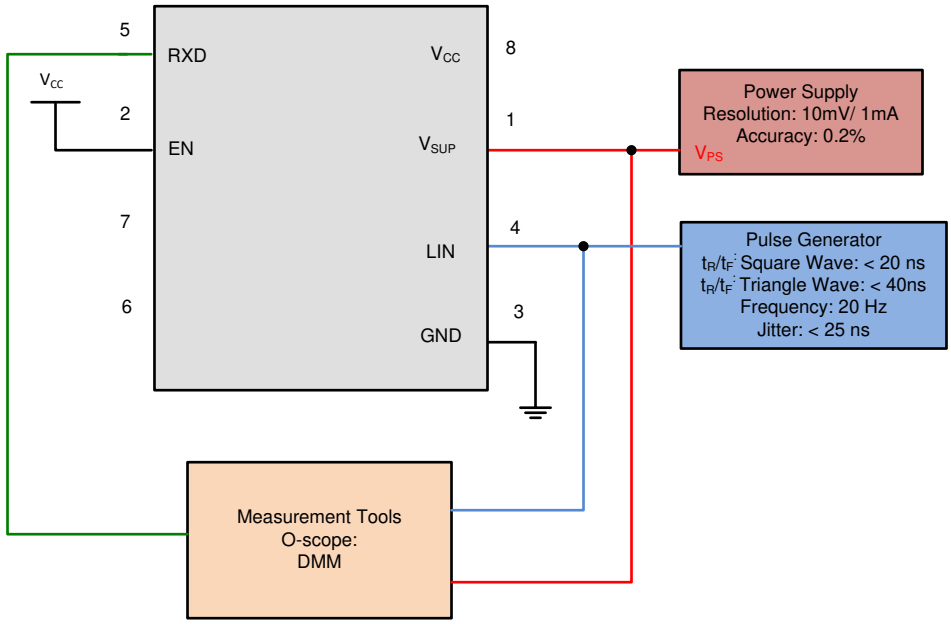


Figure 8-1. Test System: Operating Voltage Range with RX and TX Access

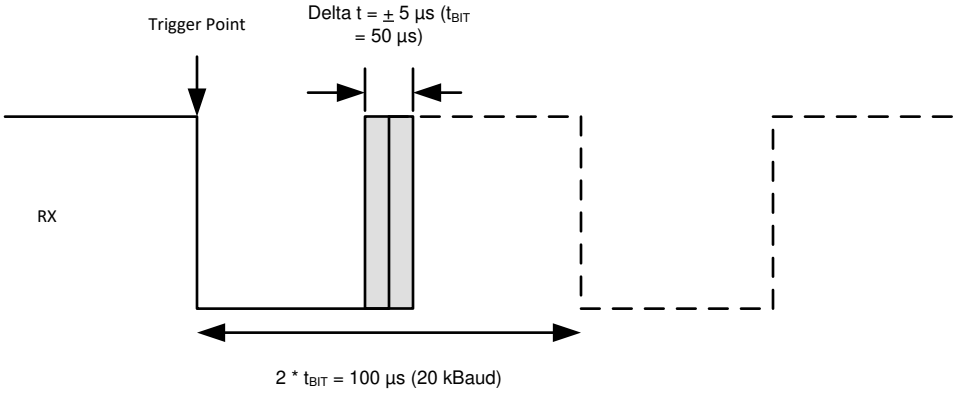


Figure 8-2. RX Response: Operating Voltage Range

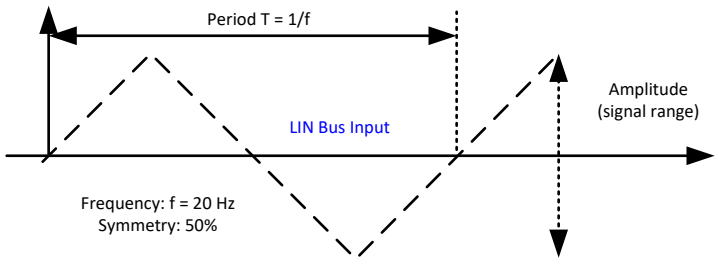


Figure 8-3. LIN Bus Input Signal

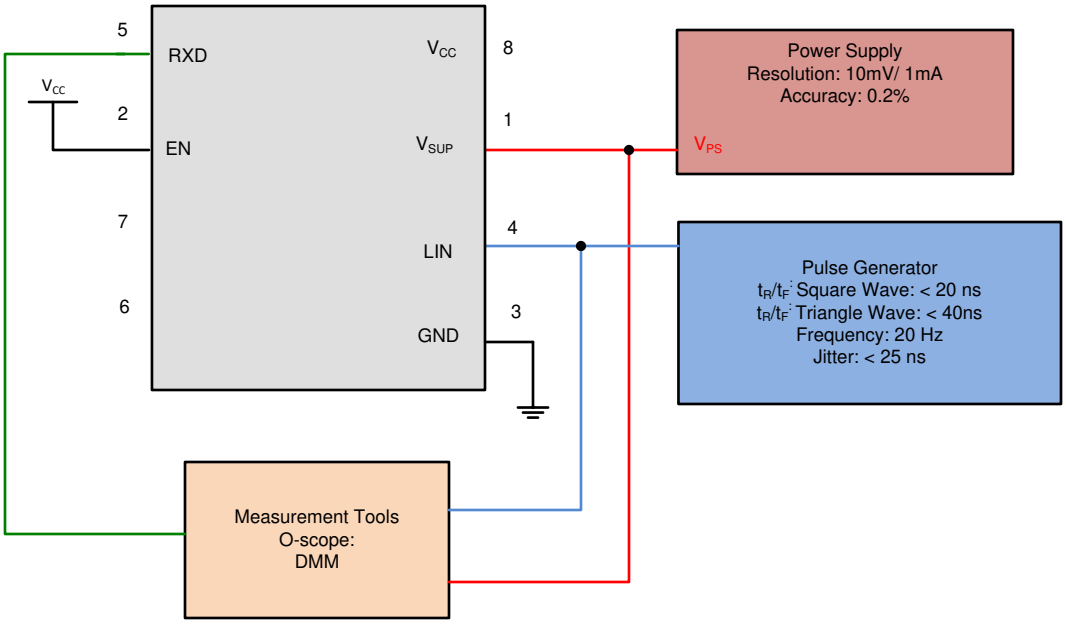


Figure 8-4. LIN Receiver Test with RX access

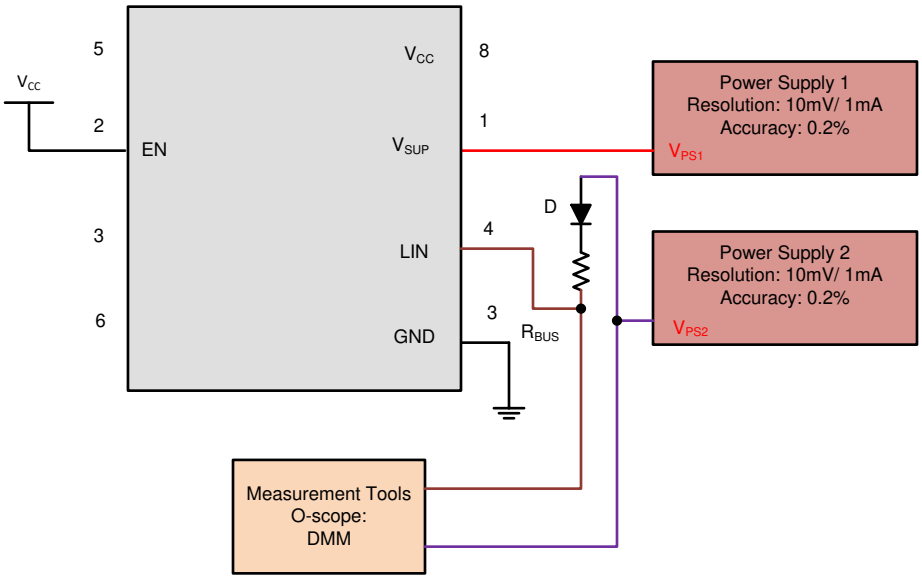


Figure 8-5. $V_{SUP\_NON\_OP}$ Test Circuit

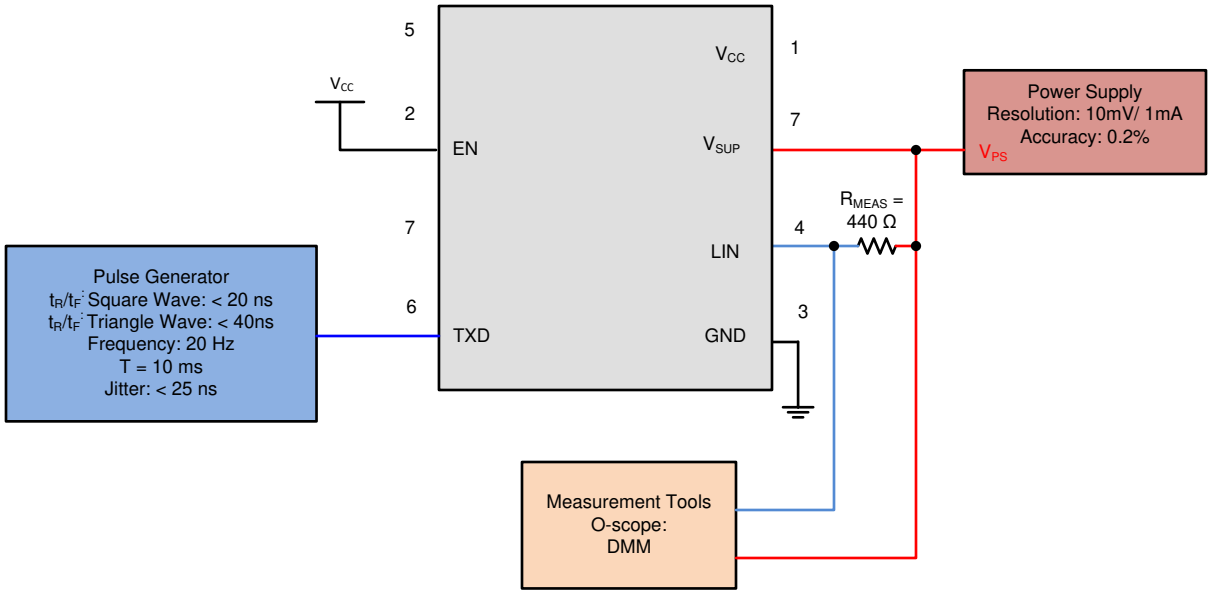


Figure 8-6. Test Circuit for I_{BUS_LIM} at Dominant State (Driver on)

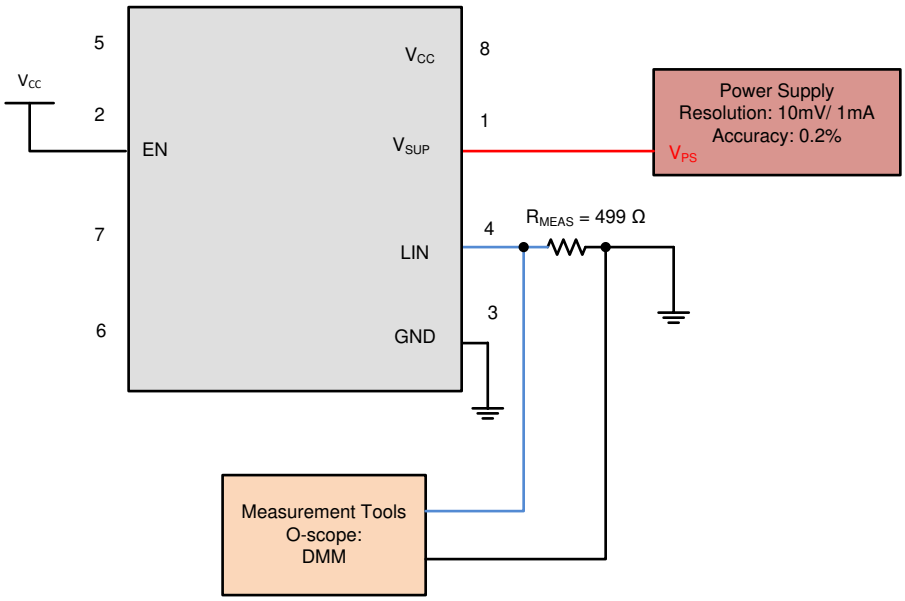


Figure 8-7. Test Circuit for $I_{BUS\_PAS\_dom}$; TXD = Recessive State V_{BUS} = 0 V

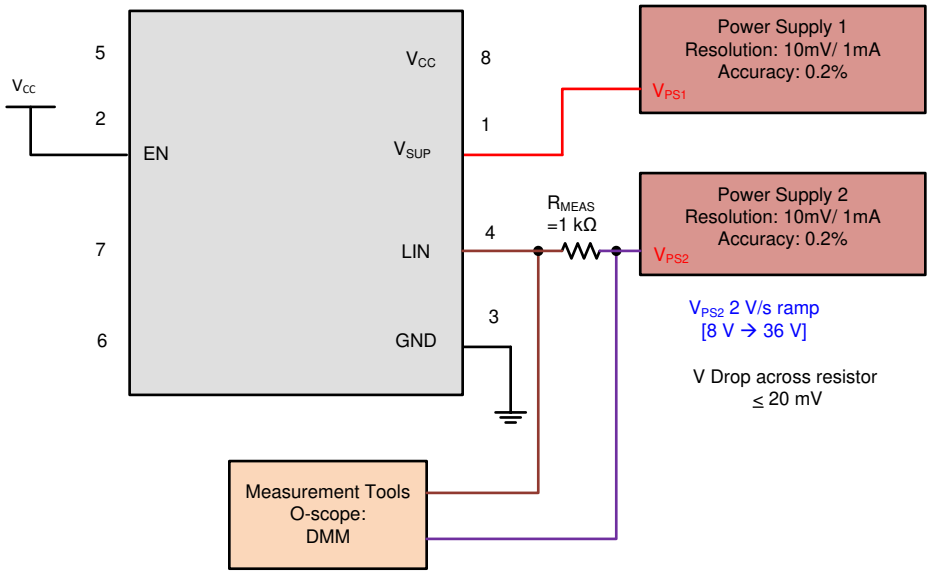


Figure 8-8. Test Circuit for $I_{BUS\_PAS\_rec}$

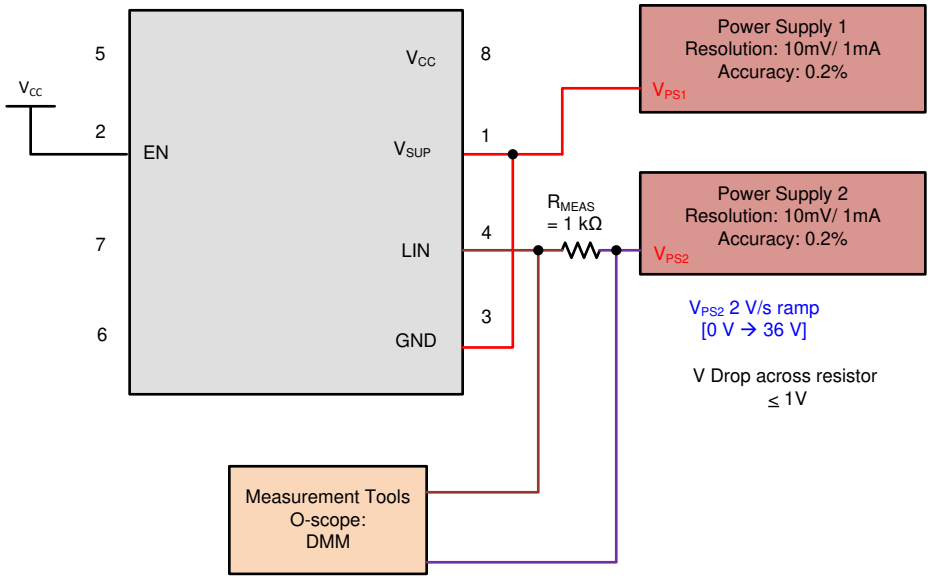


Figure 8-9. Test Circuit for $I_{BUS\_NO\_GND}$ Loss of GND

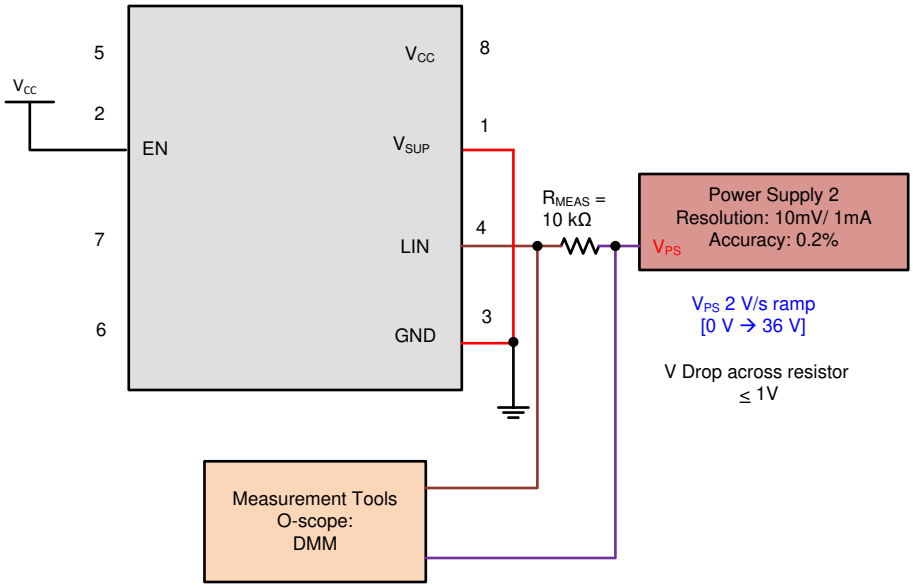


Figure 8-10. Test Circuit for $I_{BUS\_NO\_BAT}$ Loss of Battery

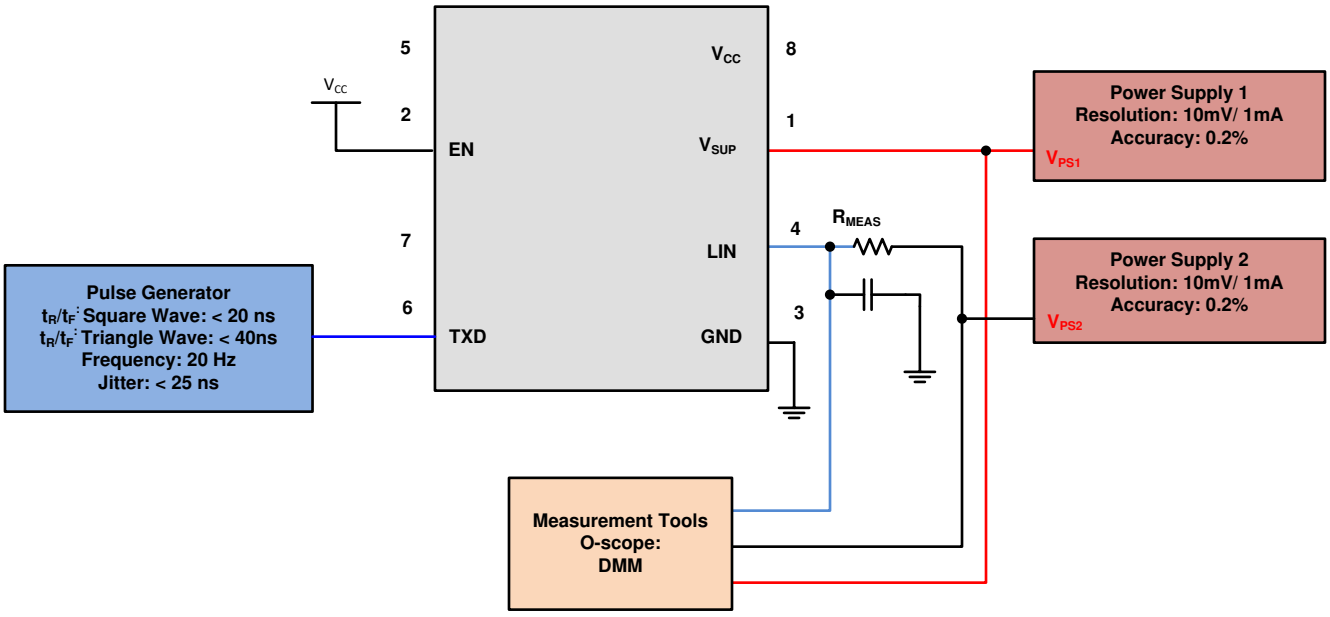


Figure 8-11. Test Circuit Slope Control and Duty Cycle

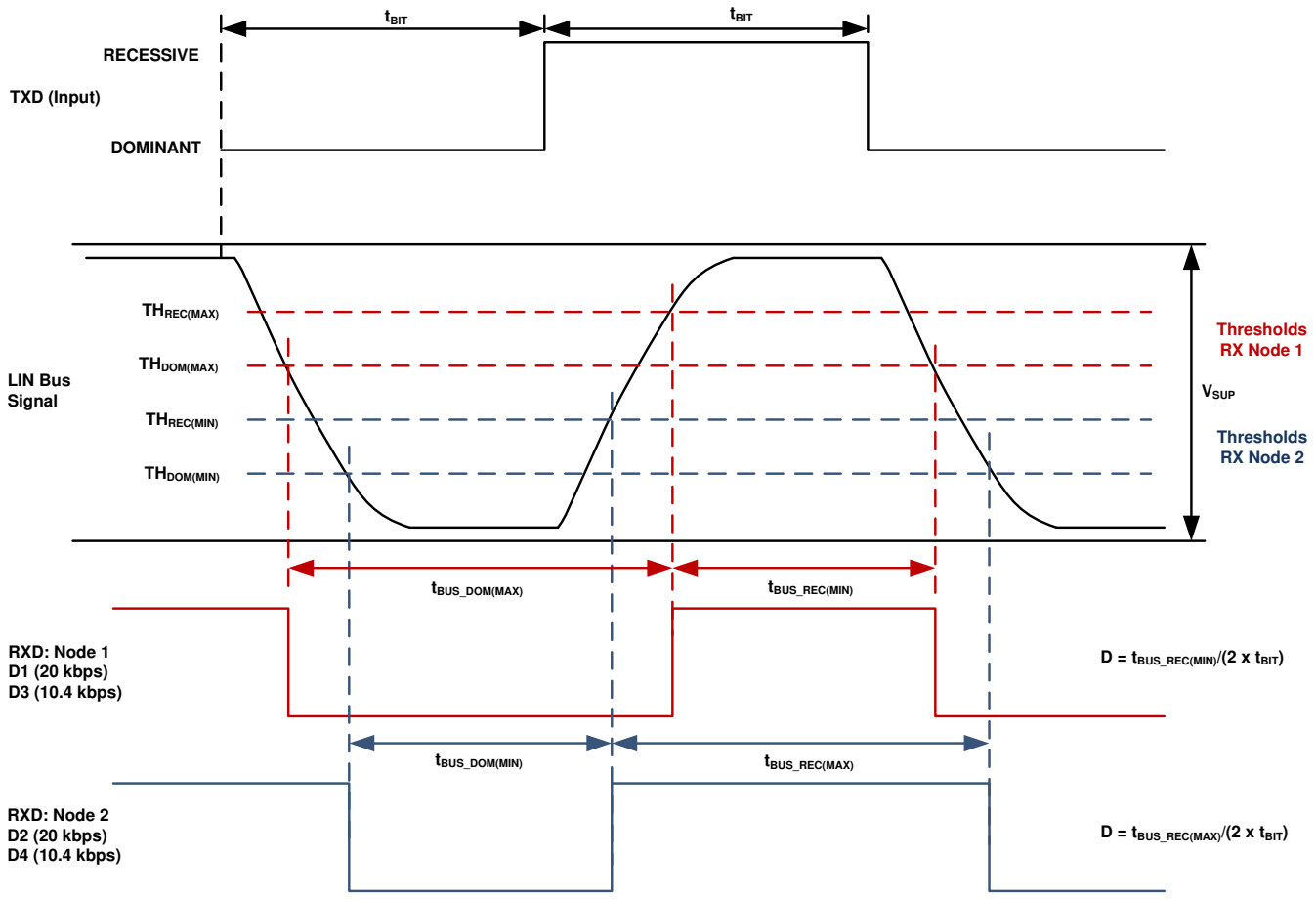


Figure 8-12. Definition of Bus Timing

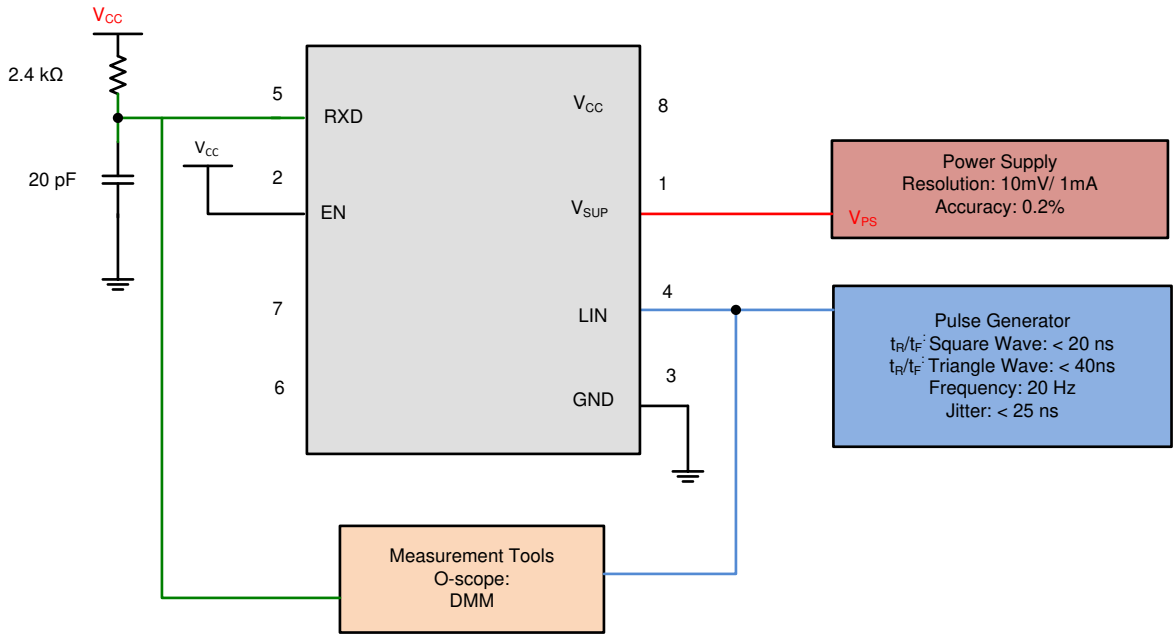


Figure 8-13. Propagation Delay Test Circuit

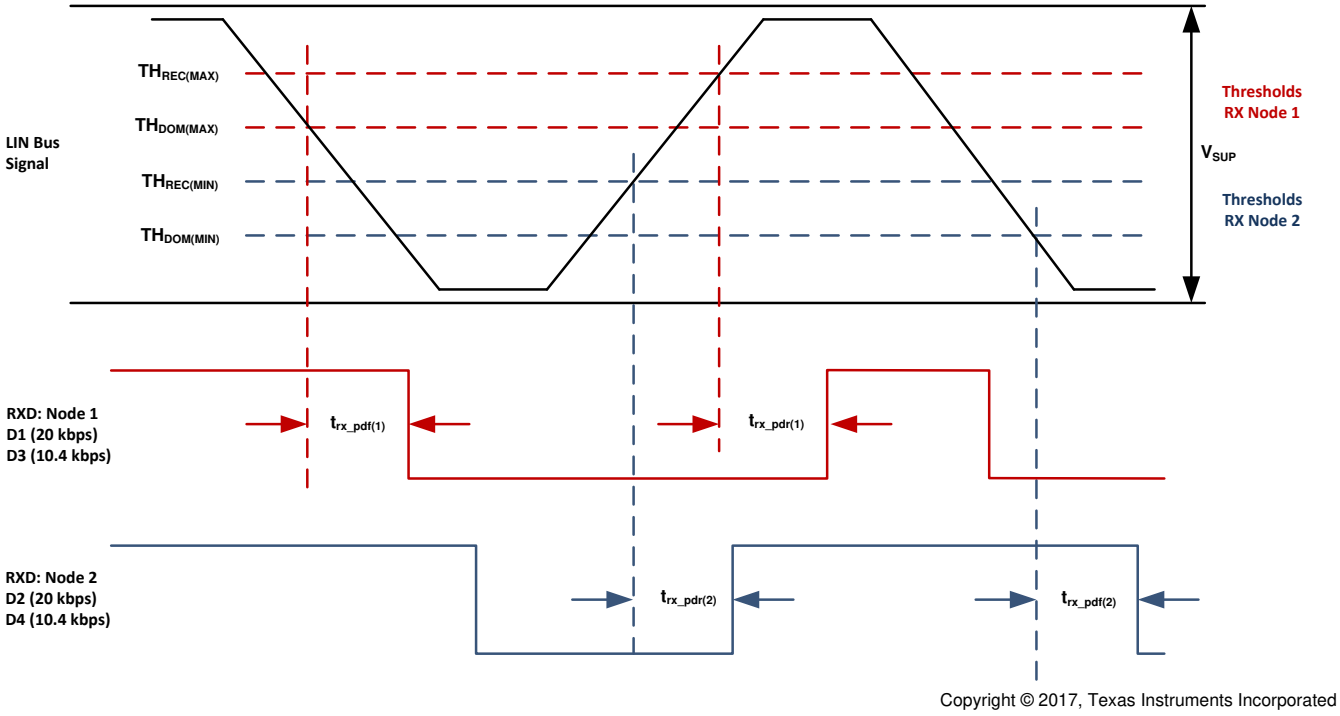


Figure 8-14. Propagation Delay

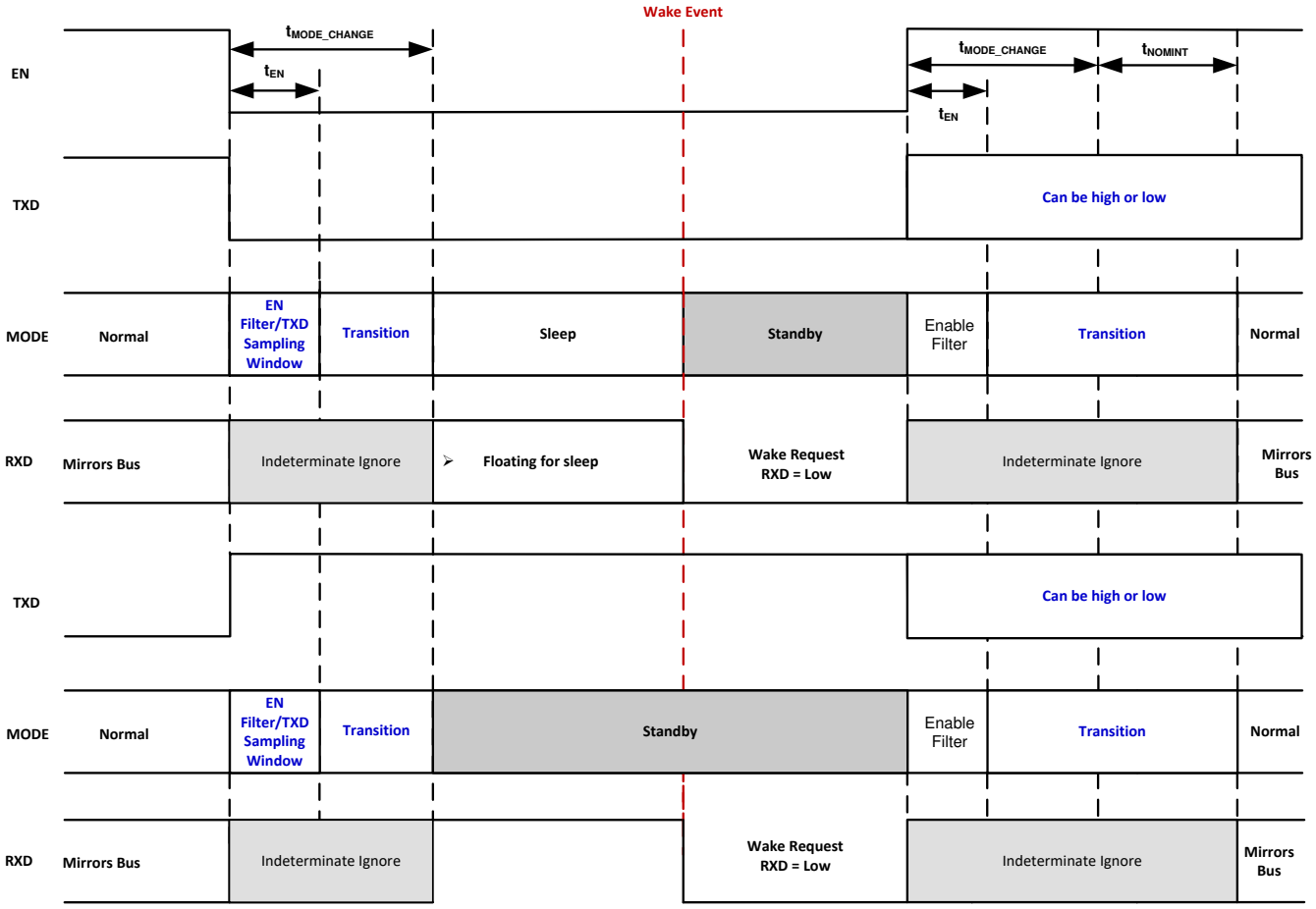


Figure 8-15. Mode Transitions

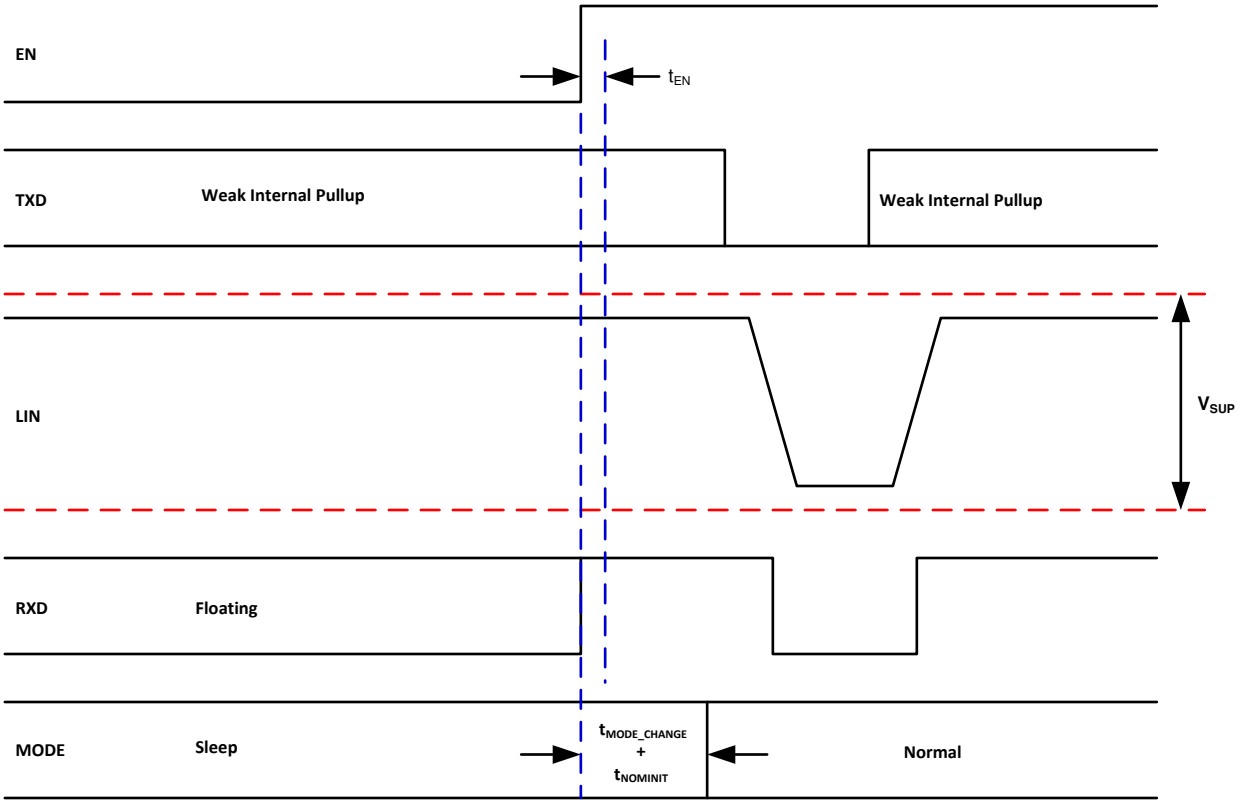


Figure 8-16. Wakeup Through EN

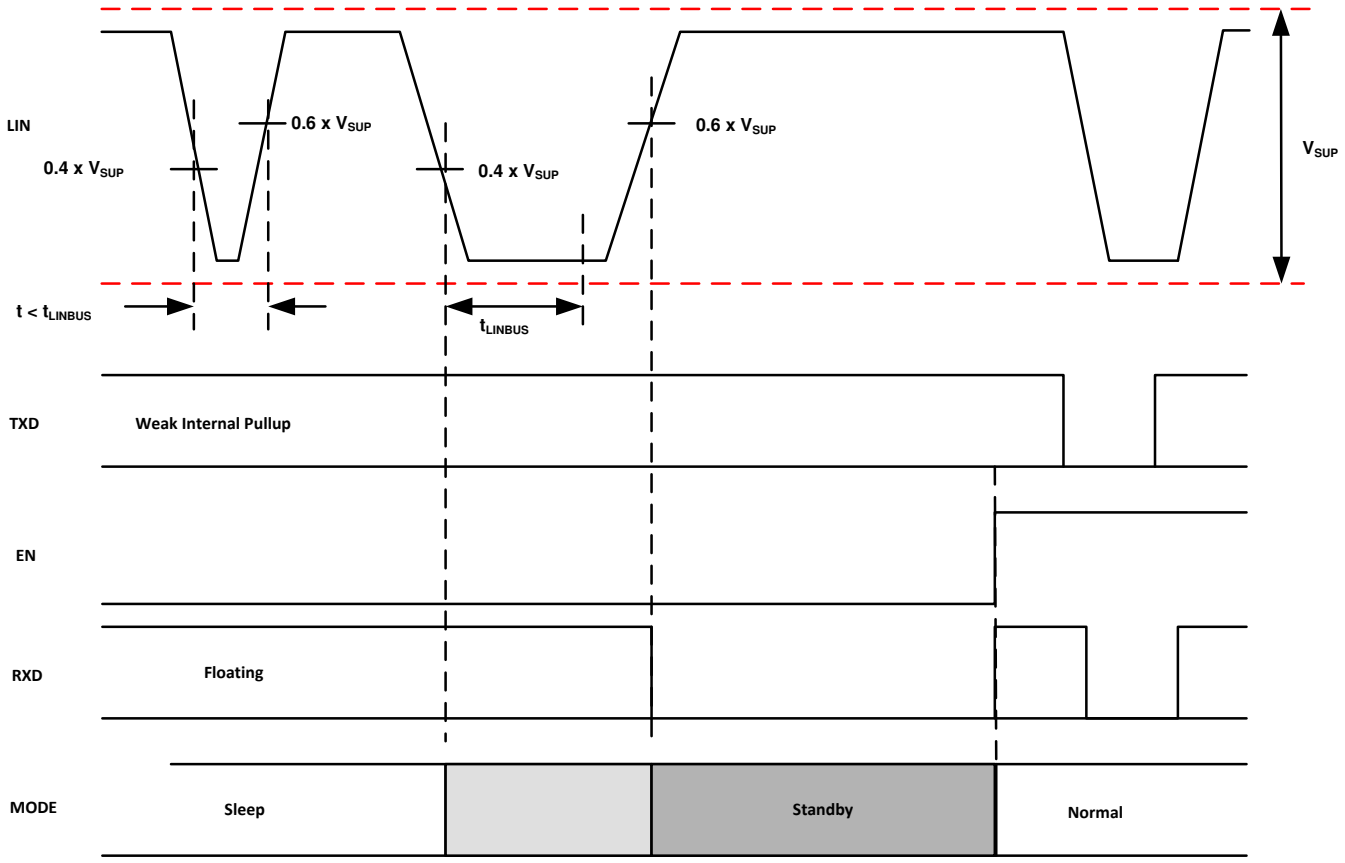


Figure 8-17. Wakeup through LIN

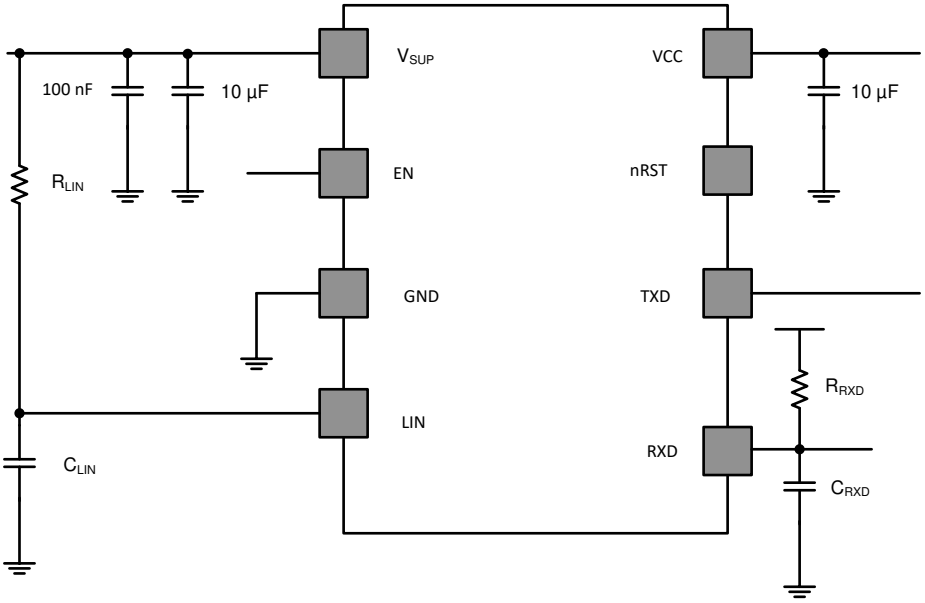


Figure 8-18. Test Circuit for AC Characteristics

9 Detailed Description

9.1 Overview

The TLIN1028-Q1 LIN transceiver is a Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and ISO/DIS 17987–4 with integrated wake-up and protection features. The LIN bus is a single-wire, bidirectional bus that typically is used in low-speed in-vehicle networks with data rates that range up to 20 kbps. The LIN receiver works up to 100 kbps supporting in-line programming. The device converts the LIN protocol data stream on the TXD input into a LIN bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic-level signals that are sent to the microprocessor through the open-drain RXD pin. The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor (45 kΩ) and a series diode.

Ultra-low current consumption is possible using the sleep mode. The TLIN1028-Q1 provides two methods to wake up from sleep mode: EN pin and LIN bus. The device integrates a low dropout voltage regulator with a wide input from V_{SUP} providing 5 V ±2% or 3.3 V ±2% with up to 125 mA of current depending upon system implementation. nRST is asserted high when V_{CC} increases above UV_{CC} and stays high as long as V_{CC} is above this threshold.

9.2 Functional Block Diagram

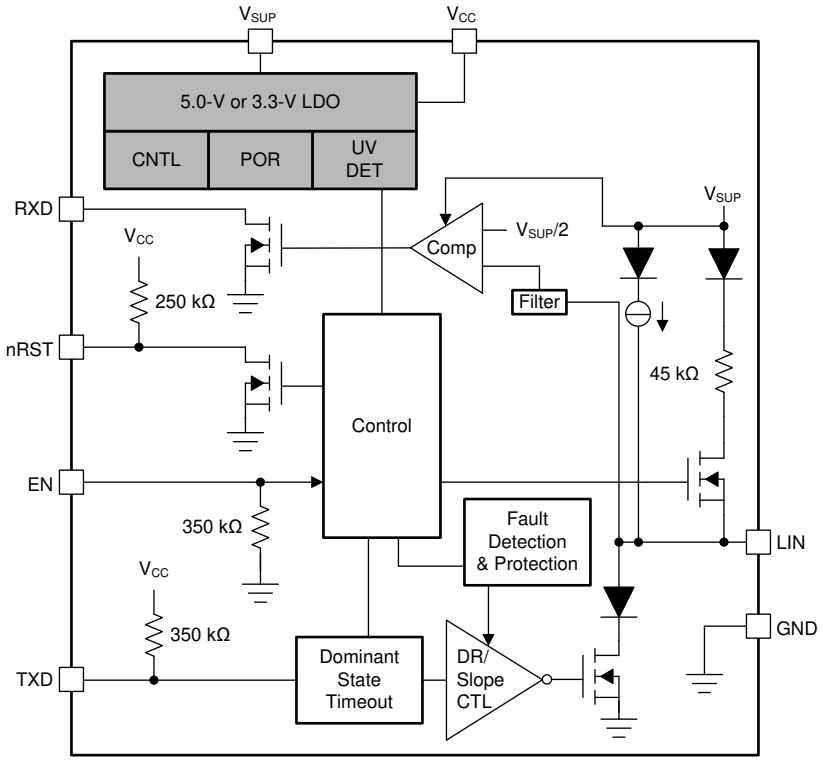


Figure 9-1. Functional Block Diagram

9.3 Feature Description

9.3.1 LIN Pin

This high-voltage input or output pin is a single-wire LIN bus transmitter and receiver. The LIN pin can survive transient voltages up to 58 V. Reverse currents from the LIN to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

9.3.1.1 LIN Transmitter Characteristics

The transmitter meets thresholds and AC parameters according to the LIN specification. The transmitter is a low-side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor and series diode to V_{SUP} must be added when the device is used for a commander node application.

9.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (> 100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the TLIN1028-Q1 to be used for high-speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

9.3.1.2.1 Termination

There is an internal pull-up resistor with a serial diode structure to V_{SUP}, so no external pull-up components are required for the LIN responder node applications. An external pull-up resistor (1 kΩ) and a series diode to V_{SUP} must be added when the device is used for commander node applications as per the LIN specification.

Figure 9-2 shows a commander node configuration and how the voltage levels are defined

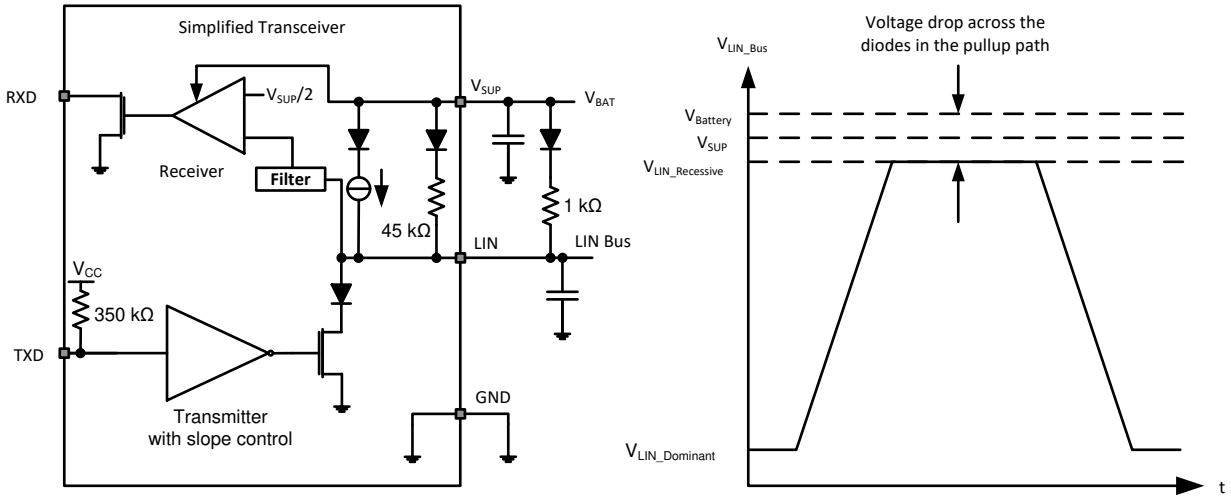


Figure 9-2. Commander Node Configuration with Voltage Levels

9.3.2 TXD (Transmit Input)

TXD is the interface to the node processor's LIN protocol controller that is used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near V_{SUP}). See Figure 9-2. The TXD input structure is compatible with processors that use 3.3 V and 5 V V_I and V_O. TXD has an internal pull-up resistor. The LIN bus is protected from being stuck dominant through a system failure driving TXD low through the dominant state time-out timer.

9.3.3 RXD (Receive Output)

RXD is the interface to the processor's LIN protocol controller, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. The RXD output structure is an open-drain output stage. This allows the device to be used with 3.3 V and 5 $V_{I/O}$ processors. If the processor's RXD pin does not have an integrated pull-up, an external pull-up resistor to the processors I and O supply voltage is required. In standby mode, the RXD pin

is driven low to indicate a wake-up request from the LIN bus from sleep mode. When going from normal mode to standby mode, the RXD pin is released and pulled-up to the voltage rail that the external pull-up resistor is connected. A LIN bus wake event will cause the RXD pin to be pulled low indicating a wake request.

9.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-battery blocking diode.

The V_{SUP} pin is a high-voltage-tolerant pin. A decoupling capacitor with a value of 100 nF is recommended to be connected close to this pin to improve the transient performance. If there is a loss of power at the ECU level, the device has ultra low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied). When V_{SUP} drops low enough the regulated output drops out of regulation. The LIN bus works with a V_{SUP} as low as 5.5 V, but at a lower voltage, the performance is indeterminate and not ensured. If V_{SUP} voltage level drops enough, it triggers the UV_{SUP}, and if it keeps dropping, at some point it passes the POR threshold.

9.3.5 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has ultra low leakage from the LIN pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

9.3.6 EN (Enable Input)

EN controls the operational modes of the device. When EN is high, the device is in normal operating mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep or standby mode and there are no transmission paths available. EN has an internal pull-down resistor to ensure the device remains in low power mode even if EN is left floating. EN should be held low until V_{SUP} reaches the expected system voltage level.

9.3.7 nRST (Reset Output)

The V_{CC} pin is monitored for under voltage events. This pin is internally pulled up to V_{CC} and when an undervoltage event takes place, this pin is pulled low. The pin returns to V_{CC} once the voltage on V_{CC} exceeds the under-voltage threshold. nRST is dependent on the value V_{CC} and not the operational mode. If UV_{CC} takes place for longer than $t_{DET(UVCC)}$ nRST is pulled to ground. If a thermal shutdown event takes place, this pin is pulled to ground.

9.3.8 V_{CC} (Supply Output)

The V_{CC} terminal can provide 5 V or 3.3 V with up to 125 mA to power up external devices when using high-k boards and thermal management best practices in order to keep the virtual junction temperature below 165 °C and avoid thermal shutdown.

9.3.9 Protection Features

The device has several protection features that are described as follows.

9.3.9.1 TXD Dominant Time Out (DTO)

During normal mode, if TXD is inadvertently driven permanently low by a hardware or software application failure, the LIN bus is protected by the dominant state time-out timer. This timer is triggered by a falling edge on the TXD pin. If the low signal remains on TXD for longer than t_{TXD_DTO}, the transmitter is disabled, thus allowing the LIN bus to return to recessive state and communication to resume on the bus. The protection is cleared and the t_{TXD_DTO} timer is reset by a rising edge on TXD. The TXD pin has an internal pull-up to ensure the device fails to a known recessive state if TXD is disconnected. During this fault, the transceiver remains in normal mode (assuming no change of state request on EN), the RXD pin reflects the LIN bus and the LIN bus pull-up termination remains on.

9.3.9.2 Bus Stuck Dominant System Fault: False Wake Up Lockout

The device contains logic to detect bus stuck dominant system faults and prevents the device from waking up falsely during the system fault. Upon entering sleep mode, the device detects the state of the LIN bus. If the bus is dominant, the wake-up logic is locked out until a valid recessive on the bus “clears” the bus stuck dominant, preventing excessive current use. Figure 9-3 and Figure 9-4 show the behavior of this protection.

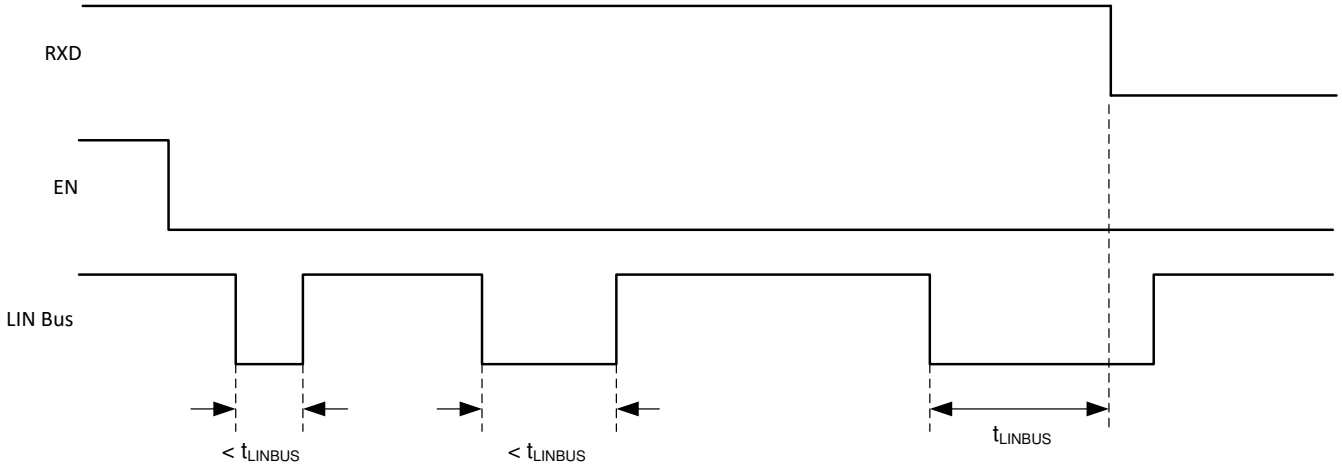


Figure 9-3. No Bus Fault: Entering Sleep Mode with Bus Recessive Condition and Wakeup

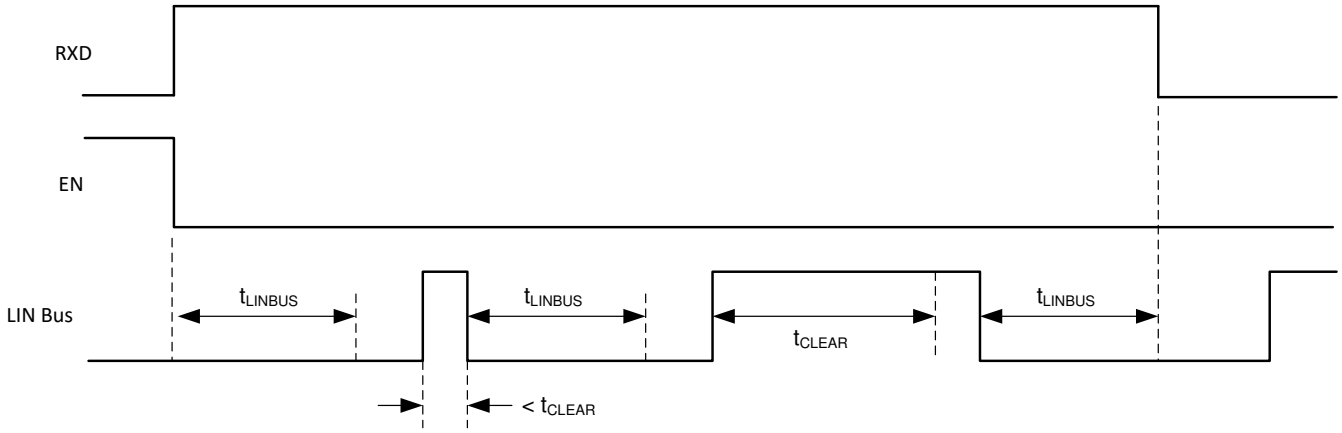


Figure 9-4. Bus Fault: Entering Sleep Mode with Bus Stuck Dominant Fault, Clearing, and Wakeup

9.3.9.3 Thermal Shutdown

The LIN transmitter is protected by current-limiting circuit; however, if the junction temperature of the device exceeds the thermal shutdown threshold, the device puts the LIN transmitter into the recessive state and turns off the V_{CC} regulator. The nRST pin is pulled to ground during a TSD event. Once the over-temperature fault condition has been removed and the virtual junction temperature has cooled beyond the hysteresis temperature, the transmitter is re-enabled. During this fault the device enters a TSD off mode. Once the junction temperature cools, the device enters standby mode as per the state diagram.

9.3.9.4 Under Voltage on V_{SUP}

The device contains a power-on reset circuit to avoid false bus messages during under voltage conditions when V_{SUP} is less than UV_{SUP}.

9.3.9.5 Unpowered Device and LIN Bus

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remain powered by the battery. The device has extremely low unpowered leakage current from the bus, so an unpowered node does not affect the network nor load it down.

9.4 Device Functional Modes

nRST: Float

The TLIN1028-Q1 has three functional modes of operation: normal, sleep, and standby. The next sections describes these modes as well as how the device moves between the different modes. Figure 9-5 graphically shows the relationship while Table 9-1 shows the state of pins.

Table 9-1. Operating Modes

Mode	EN	RXD	LIN BUS Termination	Transmitter	nRST	Comment
Sleep	Low	Floating	Weak Current pull-up	Off	Ground	nRST is internally connected to the LDO output which is pulled to ground in sleep mode.
Standby Init	Low	Floating	45 kΩ (typical)	Off	Ramping	nRST is internally connected to the LDO output which in standby init mode is pulled low until VCC raises beyond UV_{CC} threshold.
Standby from SLP	Low	Low	45 kΩ (typical)	Off	V_{CC}	Wake-up event detected, waiting on processors to set EN nRST comes on to V_{CC} once thresholds are met.
Standby from Norm	Low	High	45 kΩ (typical)	Off	V_{CC}	LDO is on and RXD is high but if a LIN bus wake event takes place RXD is pulled low.
Normal	High	LIN Bus Data	45 kΩ (typical)	On	V_{CC}	LIN transmission up to 20 kbps
TSD Off	NA	Floating	45 kΩ (typical)	Off	Ground	nRST is pulled low as the LDO is turned off which means UV_{CC} threshold has been met.

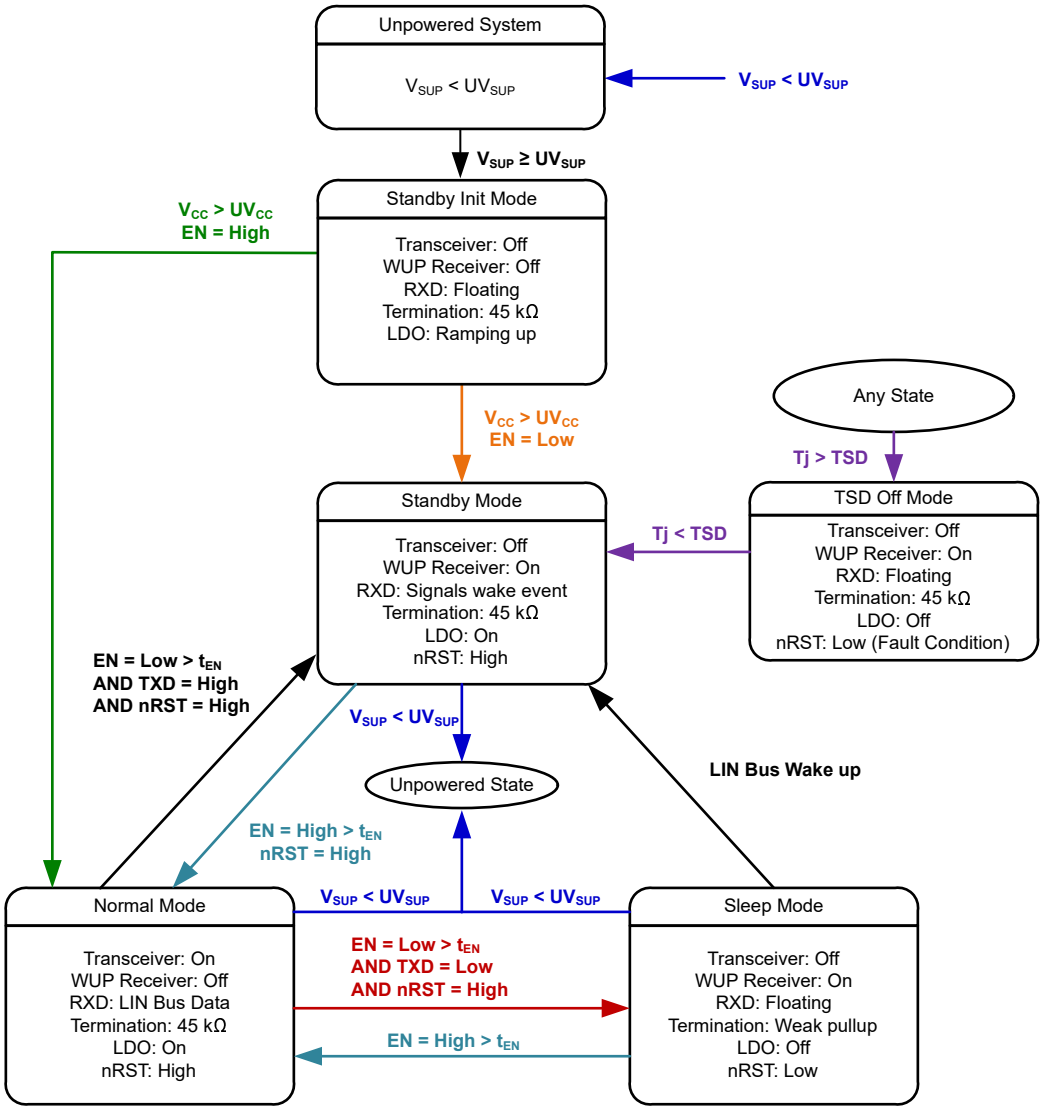


Figure 9-5. Operating State Diagram

9.4.1 Normal Mode

If the EN pin is high after the device enters standby init mode, the device enters normal mode. If EN is low, it enters standby mode. In normal operational mode, the receiver and transmitter are active and the LIN transmission up to the LIN specified maximum of 20 kbps is supported. If TXD pin is dominant at the time of entering normal mode the LIN transmitter is kept off until a recessive is applied to TXD. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller. A recessive signal on the LIN bus is a digital high and a dominant signal on the LIN bus is a digital low. The driver transmits input data from TXD to the LIN bus. Normal mode is entered as EN transitions high while the device is in sleep or standby mode for > t_{EN}. Once EN has been high for t_{EN} the device enters normal mode after t_{MODE_CHANGE} and $t_{NOMINIT}$.

9.4.2 Sleep Mode

Sleep Mode is the power saving mode for the TLIN1028-Q1. Even with extremely low current consumption in this mode, the device can still wake up from the LIN bus through a wake-up signal or if EN is set high for > t_{EN}. The wake-up events must be active for the respective time periods (t_{LINBUS}).

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short-circuited to ground). However, the weak current pull-up is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- EN input and LIN wake-up receiver are active.

9.4.3 Standby Mode

Standby mode is entered either by a wake-up event through LIN bus while the device is in sleep mode or by the EN pin from normal or standby init modes. From normal mode EN must be low for > t_{EN} and TXD and nRST are high. RXD pin in standby mode is dependent upon how standby mode was entered. If entered from normal mode or power up, RXD is high. If entered from sleep mode, RXD is pulled low to indicate a wake event. When entering standby mode from normal or standby init modes, a wake event on the LIN bus causes the RXD pin to be pulled low.

During power up, if EN is low the device goes into standby mode, and if EN is high, the device goes into normal mode. EN has an internal pull-down resistor ensuring EN is pulled low if the pin is left floating in the system.

9.4.4 Wake-Up Events

There are two ways to wake-up from sleep mode:

- Remote wake-up initiated by the falling edge of a recessive (high) to dominant (low) state transition on the LIN bus where the dominant state is held for the t_{LINBUS} filter time. After this t_{LINBUS} filter time has been met and a rising edge on the LIN bus going from dominant state to recessive state initiates a remote wake-up event eliminating false wake ups from disturbances on the LIN bus or if the bus is shorted to ground.
- Local wake-up through EN being set high for longer than t_{EN}.

9.4.4.1 Wake-Up Request (RXD)

When the TLIN1028-Q1 encounters a wake-up event from the LIN bus, RXD goes low and the device transitions to standby mode until EN is reasserted high and the device enters normal mode. Once the device enters normal mode, the RXD pin releases the wake-up request signal and the RXD pin then reflects the receiver output from the LIN bus.

9.4.5 Mode Transitions

When the device is transitioning between modes, the device needs the time t_{MODE_CHANGE} and t_{NOMINT} to allow the change to fully propagate from the EN pin through the device into the new state.

9.4.6 Voltage Regulator

The device has an integrated high-voltage LDO that operates over a 5.5 V to 28 V input voltage range for both 3.3 V and 5 V V_{CC}. The device has an output current capability of 70 mA and 125 mA depending upon package and support fixed output voltages of 3.3 V (TLIN10283-Q1) or 5 V (TLIN10285-Q1). It features thermal shutdown and short-circuit protection to prevent damage during over-temperature and over-current conditions

9.4.6.1 V_{CC}

The V_{CC} pin is the regulated output based on the required voltage. The regulated voltage accuracy is ± 2%. The output is current limited. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UV_{SUP} threshold, the regulator shuts down until the input voltage returns above the UV_{SUPR} level. The device monitors situations where V_{CC} may drop below the UV_{CC} level thus causing the nRST pin to be pulled low.

9.4.6.2 Output Capacitance Selection

For stable operation over the full temperature range and with load currents up to 125 mA on V_{CC} a certain capacitance is expected and depends upon the minimum load current. To support no load to full load a value of 10 µF and ESR smaller than 2 Ω is needed. For 20 µA to full load an 1.5 µF capacitance can be used. The low ESR recommendation is to improve the load transient performance.

9.4.6.3 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (IL) and power-switch resistor. This tracking allows for a smaller input capacitance and can possibly eliminate the need for a boost converter during cold-crank conditions.

9.4.6.4 Power Supply Recommendation

The device is designed to operate from an input-voltage supply range between 5.5 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device. The recommended minimum capacitance at the pin is 100 nF . The max voltage range is for the LIN functionality. Exceeding 24V for the LDO reduces the effective current sourcing capability due to thermal considerations.

10 Application and Implementation

Note

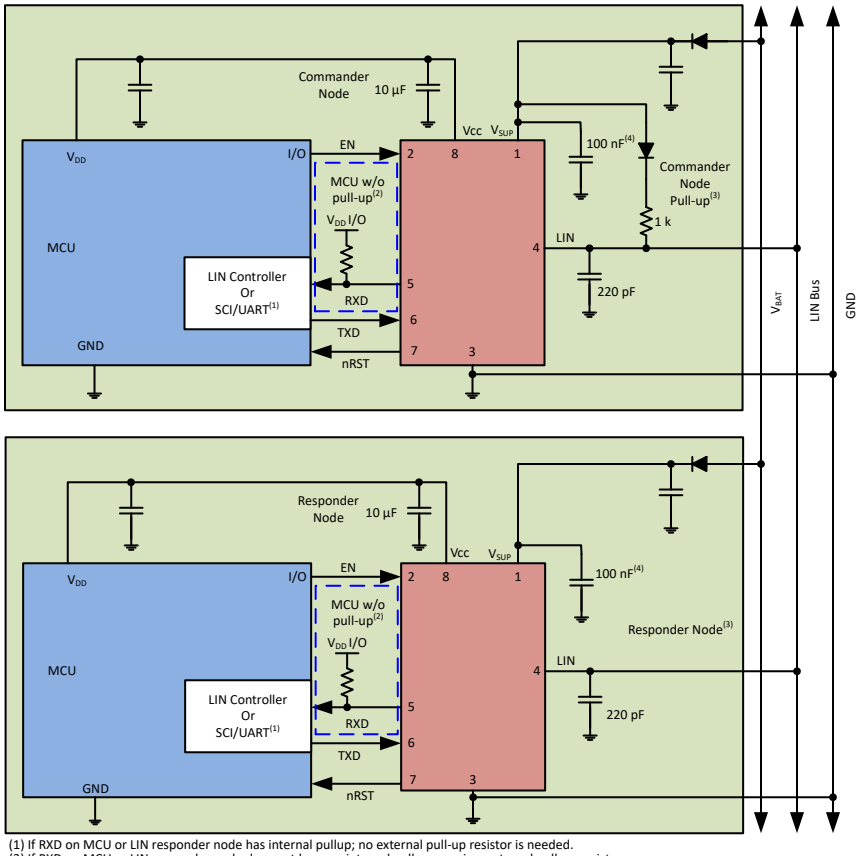
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TLIN1028-Q1 can be used as both a responder device and a commander device in a LIN network. The device comes with the ability to support a remote wake-up requests. It can provide the power to the local processor.

10.2 Typical Application

The device comes with an integrated 45 kΩ pull-up resistor and series diode for responder node applications. For commander node applications, an external 1 kΩ pull-up resistor with series blocking diode can be used. Figure 10-1 shows the device being used in both commander and responder node applications.



(1) If RXD on MCU or LIN responder node has internal pullup; no external pull-up resistor is needed.
(2) If RXD on MCU or LIN responder node does not have an internal pull-up requires external pull-up resistor.
(3) Commander node applications require and external 1 kΩ pull-up resistor and serial diode.
(4) Decoupling capacitor values are system dependent but usually have 100 nF, 1 µF and ≥10 µF

Figure 10-1. Typical LIN Bus

10.2.1 Design Requirements

10.2.1.1 Normal Mode Application Note

When using the TLIN1028-Q1 in systems which are monitoring the RXD pin for a wake-up request, special care should be taken during the mode transitions. The output of the RXD pin is indeterminate for the transition period between states as the receivers are switched. The application software should not look for an edge on the RXD pin indicating a wake-up request until t_{MODE_CHANGE}. This is shown in Figure 8-15 when transitioning to normal mode there is an initialization period shown as $t_{NOMINIT}$.

10.2.1.2 TXD Dominant State Timeout Application Note

The maximum dominant TXD time allowed by the TXD dominant state time out limits the minimum possible data rate of the device. The LIN protocol has different constraints for commander and responder node applications; thus, there are different maximum consecutive dominant bits for each application case and thus different minimum data rates.

10.2.1.3 Brownout

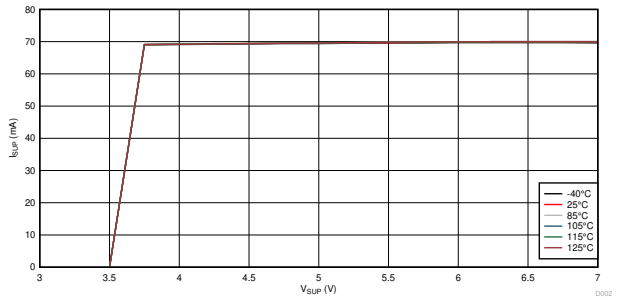
Figure 10-17 and Figure 10-18 show the behavior of the LIN, nRST and V_{CC} pins during a brownout condition. For the TLIN10283-Q1, V_{SUP} down to ~ 2.24 V has results as shown. For the TLIN10285-Q1, V_{SUP} down to ~ 2.63 V has results as shown. When V_{SUP} drops below these levels the signals are indeterminate.

10.2.2 Detailed Design Procedures

For processors or LIN responder nodes with an internal pull-up on RXD, no external pull-up resistor is needed. For processors or LIN responder nodes without internal pull-up on RXD, an external pull-up resistor is required. Commander node applications require an external 1 kΩ pull-up resistor and serial diode.

10.2.3 Application Curves

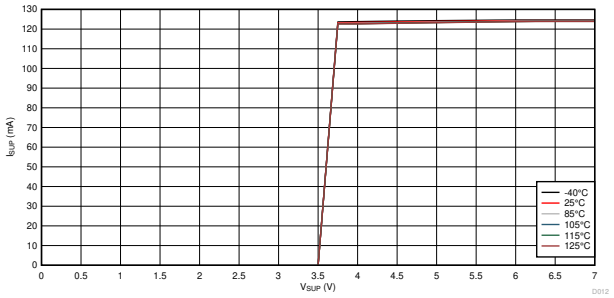
Characteristic curves below show the LDO performance ramping between 0 V and up to 7 V.



Package = D V_{CC} = 3.3 V Temperature = Ambient

I_{CC} = 70 mA

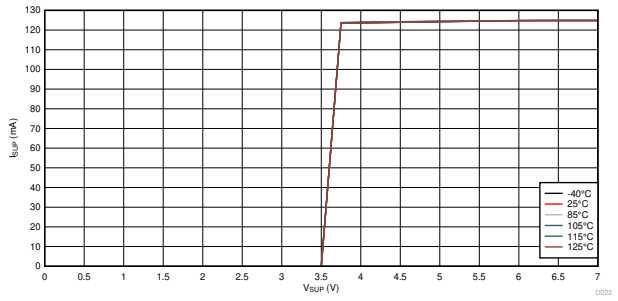
Figure 10-2. I_{SUP} vs V_{SUP} vs Temperature



Package = DRB V_{CC} = 3.3 V Temperature = Ambient

I_{CC} = 125 mA

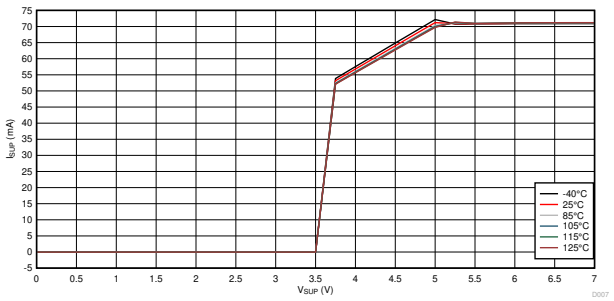
Figure 10-3. I_{SUP} vs V_{SUP} vs Temperature



Package = DDA V_{CC} = 3.3 V Temperature = Ambient

I_{CC} = 125 mA

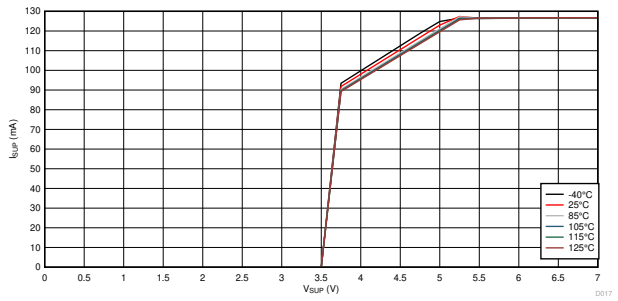
Figure 10-4. I_{SUP} vs V_{SUP} vs Temperature



Package = D V_{CC} = 5 V Temperature = Ambient

I_{CC} = 70 mA

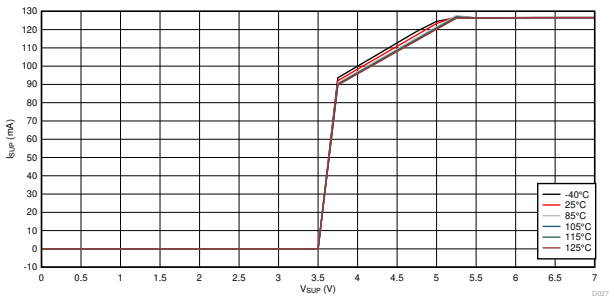
Figure 10-5. I_{SUP} vs V_{SUP} vs Temperature



Package = DRB V_{CC} = 5 V Temperature = Ambient

I_{CC} = 125 mA

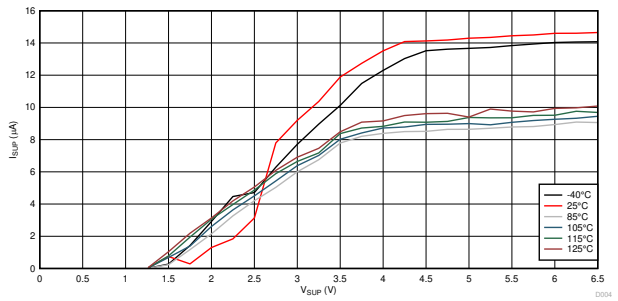
Figure 10-6. I_{SUP} vs V_{SUP} vs Temperature



Package = DDA V_{CC} = 5 V Temperature = Ambient

I_{CC} = 125 mA

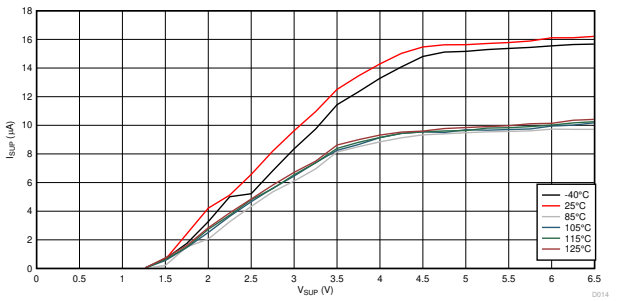
Figure 10-7. I_{SUP} vs V_{SUP} vs Temperature



Package = D 3.3 V V_{CC} = Off Temperature = Ambient

Mode = Sleep

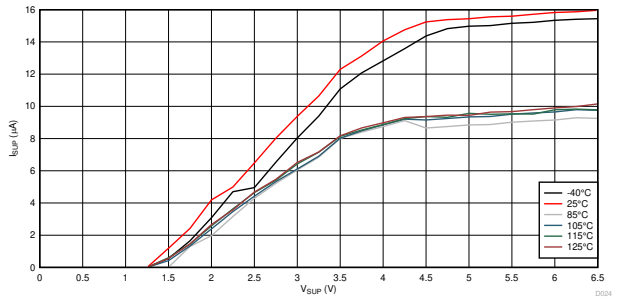
Figure 10-8. I_{SUP} vs V_{SUP} vs Temperature Ramp-down



Package = DRB 3.3 V V_{CC} = Off Temperature = Ambient

Mode = Sleep

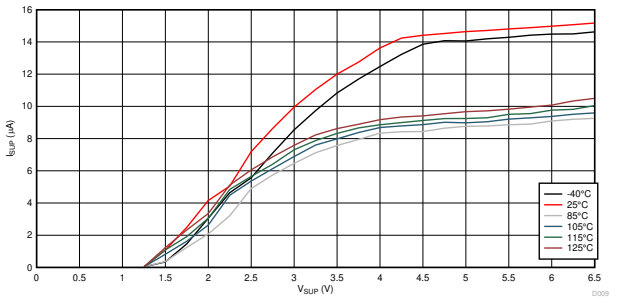
Figure 10-9. I_{SUP} vs V_{SUP} vs Temperature Ramp-down



Package = DDA 3.3 V V_{CC} = Off Temperature = Ambient

Mode = Sleep

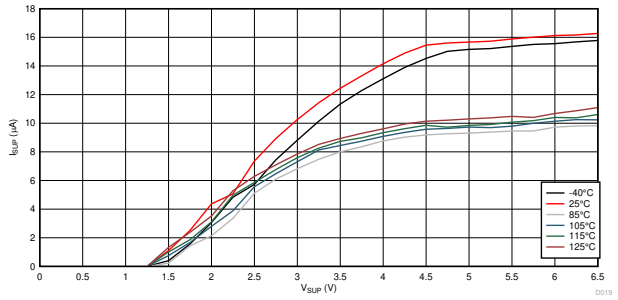
Figure 10-10. I_{SUP} vs V_{SUP} vs Temperature Ramp-down



Package = D 5 V V_{CC} = Off Temperature = Ambient

Mode = Sleep

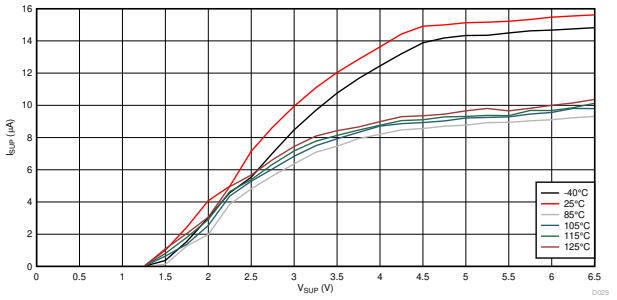
Figure 10-11. I_{SUP} vs V_{SUP} vs Temperature Ramp-down



Package = DRB 5 V V_{CC} = Off Temperature = Ambient

Mode = Sleep

Figure 10-12. I_{SUP} vs V_{SUP} vs Temperature Ramp-down



Package = DDA 5 V V_{CC} = Off Temperature = Ambient

Mode = Sleep

Figure 10-13. I_{SUP} vs V_{SUP} vs Temperature Ramp-down

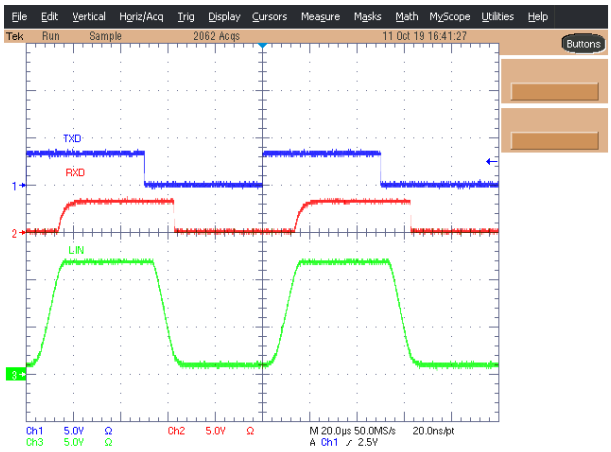


Figure 10-14. LIN Bus Performance

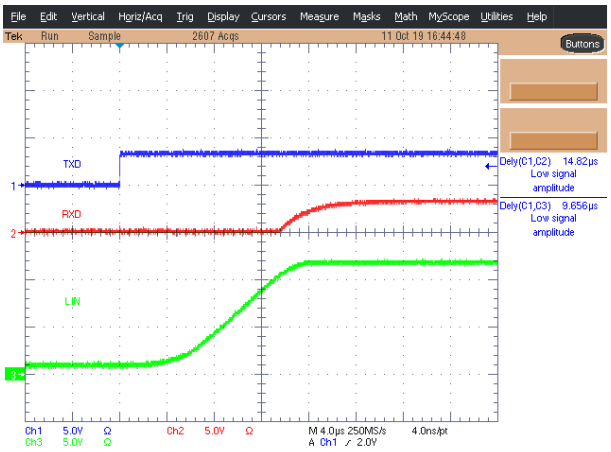


Figure 10-15. Dominant to Recessive Propagation Delay

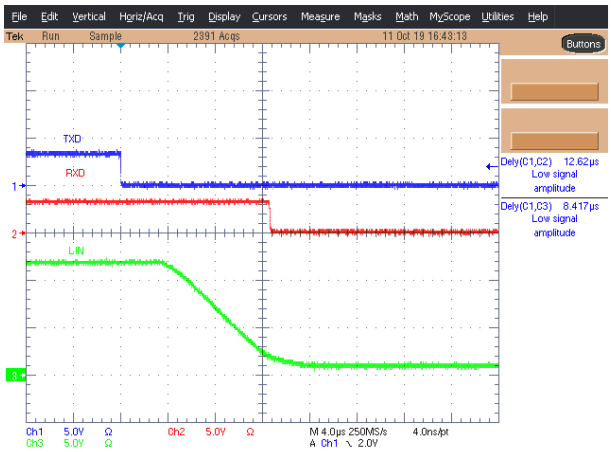


Figure 10-16. Recessive to Dominant Propagation Delay

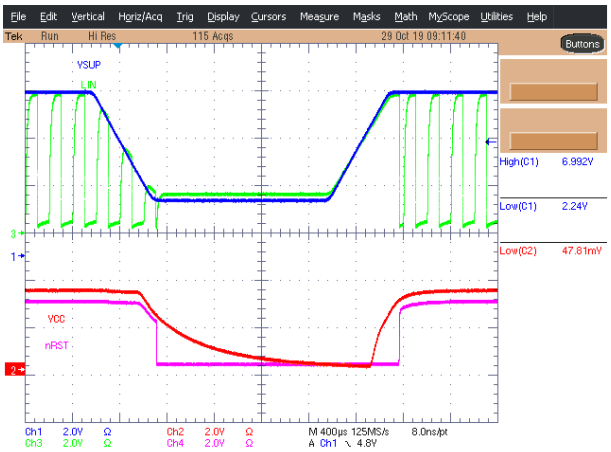


Figure 10-17. TLIN10283-Q1 Brownout

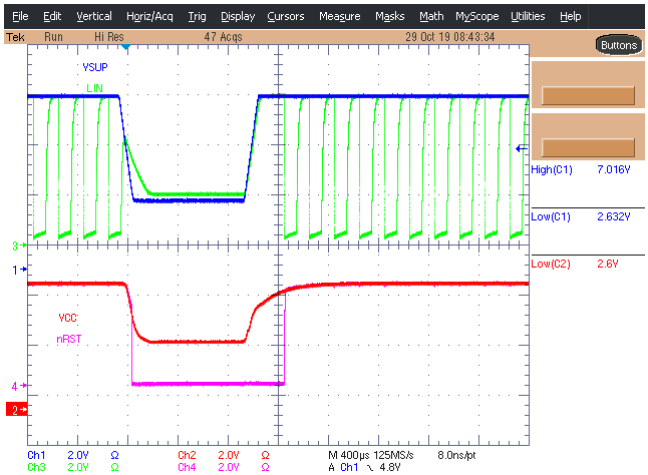


Figure 10-18. TLIN10285-Q1 Brownout

11 Power Supply Recommendations

The TLIN1028-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 5.5 V to 28 V . A 100 nF decoupling capacitor should be placed as close to the V_{SUP} pin of the device as possible.For applications where the device goes from no load to full load, a minimum decoupling capacitance to ground of 10 µF is recommended when the LDO turns on. If the device is going from 20 µA to full load then a minimum of 1.5 µF capacitance is recommended.

12 Layout

PCB design should start with understanding that frequency bandwidth from approximately 3 MHz to 3 GHz is needed thus high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

12.1 Layout Guidelines

- **Pin 1 (V_{SUP}):** This is the supply pin for the device. A 100 nF decoupling capacitor should be placed as close to the device as possible.
- **Pin 2 (EN):** EN is an input pin that is used to place the device in a low power sleep mode. If this feature is not used, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series resistor, values between 1 kΩ and 10 kΩ. Additionally, a series resistor may be placed on the pin to limit current on the digital lines in the event of an over-voltage fault.
- **Pin 3 (GND):** This is the ground connection for the device. This pin should be tied to the ground plane through a short trace with the use of two vias to limit total return inductance.
- **Pin 4 (LIN):** This pin connects to the LIN bus. For responder node applications, a 220 pF capacitor to ground is implemented. For commander node applications, an additional series resistor and blocking diode should be placed between the LIN pin and the V_{SUP} pin. See Figure 10-1
- **Pin 5 (RXD):** The pin is an open-drain output and requires and external pull-up resistor in the range of 1 kΩ to 10 kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external pull-up resistor should be placed on RXD. If RXD is connected to the V_{CC} pin a higher pull-up resistor value can be used to reduce standby current.
- **Pin 6 (TXD):** The TXD pin is the transmit input signal to the device from the processors. A series resistor can be placed to limit the input current to the device in the event of an over voltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 7 (nRST):** This pin connects to the processors as a reset out.
- **Pin 8 (V_{CC}):** Output source, either 3.3 V or 5 V depending upon the version of the device.

Note

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

12.2 Layout Example

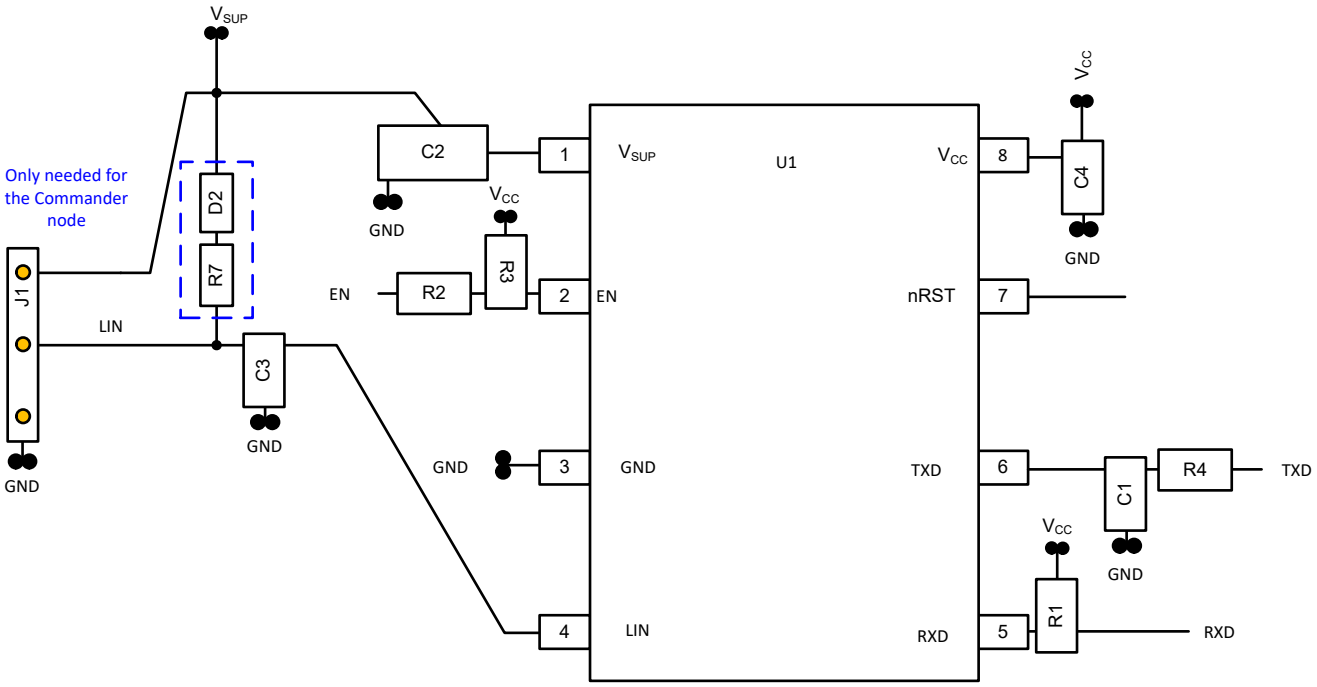


Figure 12-1. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- LIN Standards:
  - ISO/DIS 17987-1: Road vehicles -- Local Interconnect Network (LIN) -- Part 1: General information and use case definition
  - ISO/DIS 17987-4: Road vehicles -- Local Interconnect Network (LIN) -- Part 4: Electrical Physical Layer (EPL) specification 12V/24V
  - SAE J2602-1: LIN Network for Vehicle Applications
  - LIN2.0, LIN2.1, LIN2.2 and LIN2.2A specification
- EMC requirements:
  - SAE J2962-2: TBD
  - HW Requirements for CAN, LIN, FR V1.3: German OEM requirements for LIN
  - ISO 10605: Road vehicles - Test methods for electrical disturbances from electrostatic discharge
  - ISO 11452-4:2011: Road vehicles - Component test methods for electrical disturbances from narrowband radiated electromagnetic energy - Part 4: Harness excitation methods
  - ISO 7637-1:2015: Road vehicles - Electrical disturbances from conduction and coupling - Part 1: Definitions and general considerations
  - ISO 7637-3: Road vehicles - Electrical disturbances from conduction and coupling - Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines
  - IEC 62132-4:2006: Integrated circuits - Measurement of electromagnetic immunity 150 kHz to 1 GHz - Part 4: Direct RF power injection method
  - IEC 61967-4
  - CISPR25
- Conformance Test requirements:
  - ISO/DIS 17987-7: Road vehicles -- Local Interconnect Network (LIN) -- Part 7: Electrical Physical Layer (EPL) conformance test specification
  - SAE J2602-2: LIN Network for Vehicle Applications Conformance Test

TLINx441 LDO Performance, SLLA427

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLIN10283DDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TLN83
TLIN10283DDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLN83
TLIN10283DRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLN83
TLIN10283DRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLN83
TLIN10283DRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLN83
TLIN10283DRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLN83
TLIN10285DDARQ1	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	TLN85
TLIN10285DDARQ1.A	Active	Production	SO PowerPAD (DDA) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLN85
TLIN10285DRBRQ1	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLN85
TLIN10285DRBRQ1.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLN85
TLIN10285DRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLN85
TLIN10285DRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLN85

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

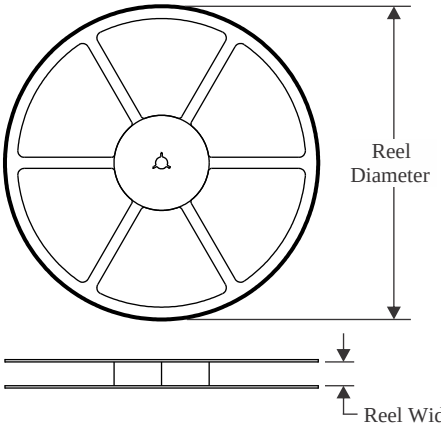
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

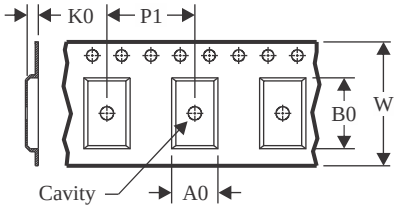
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

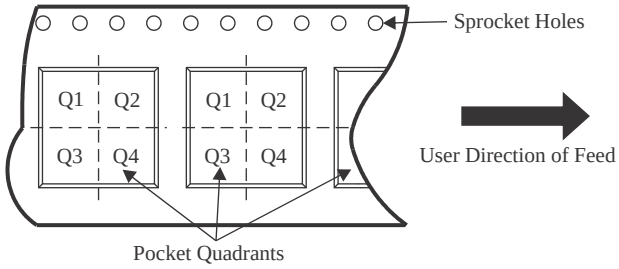


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

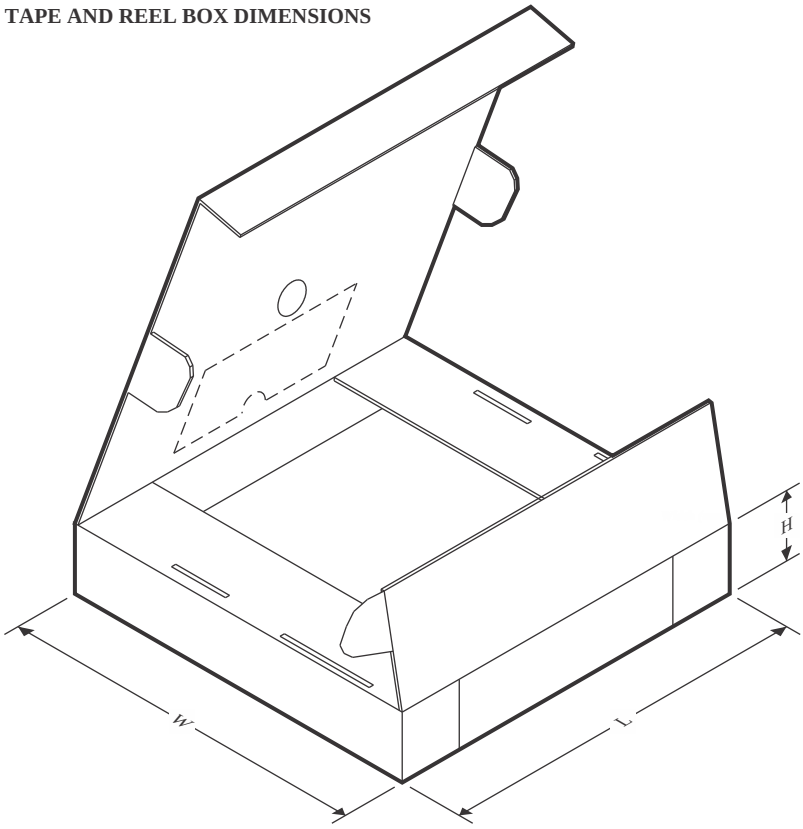
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

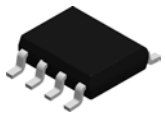
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN10283DDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TLIN10283DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TLIN10283DRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLIN10285DDARQ1	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
TLIN10285DRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
TLIN10285DRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN10283DDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TLIN10283DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN10283DRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TLIN10285DDARQ1	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
TLIN10285DRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TLIN10285DRQ1	SOIC	D	8	2500	353.0	353.0	32.0

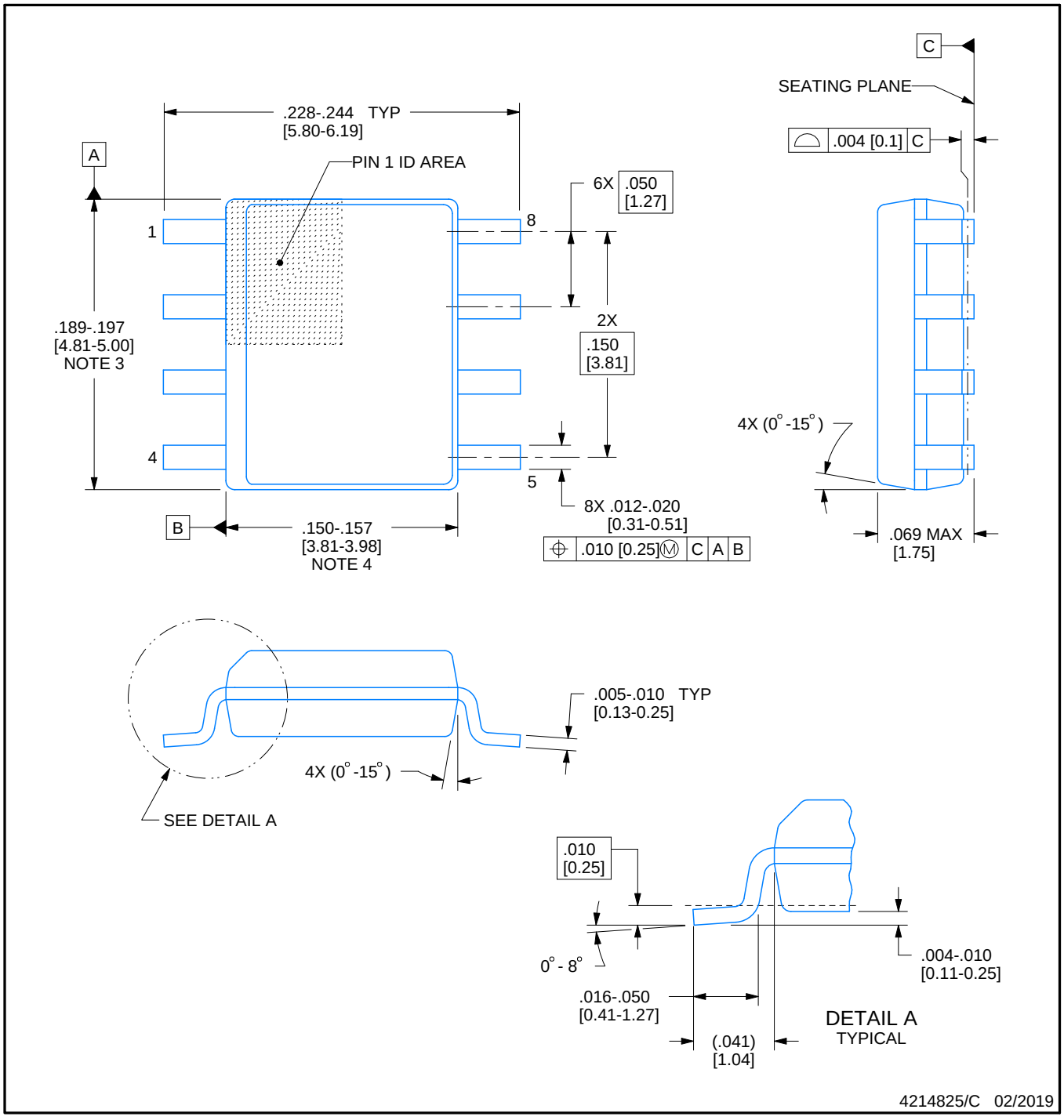


PACKAGE OUTLINE

D0008A

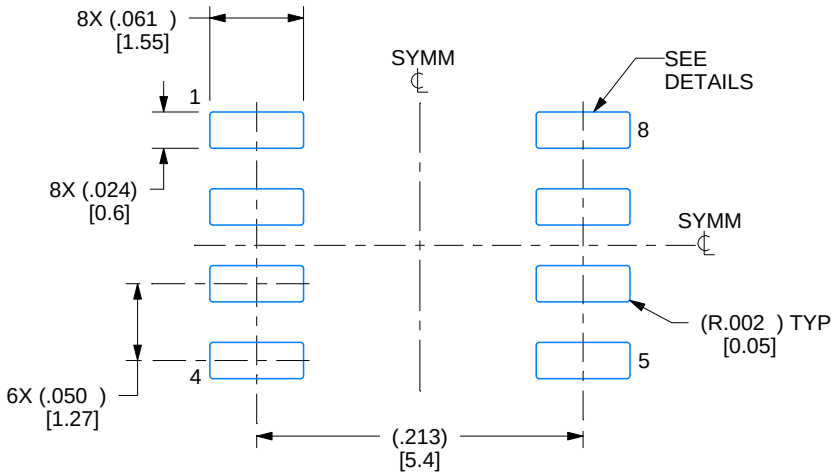
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

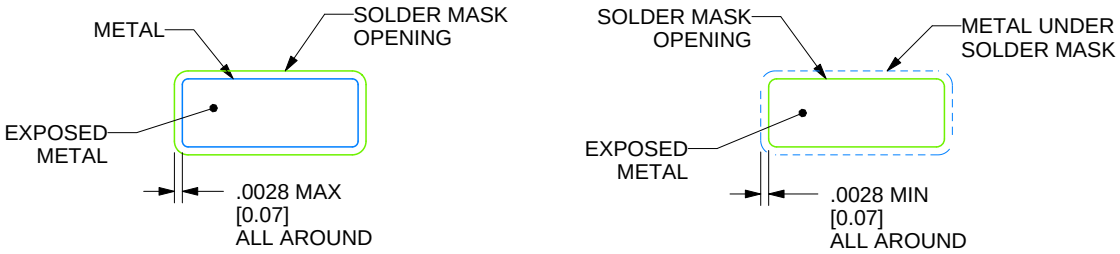


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

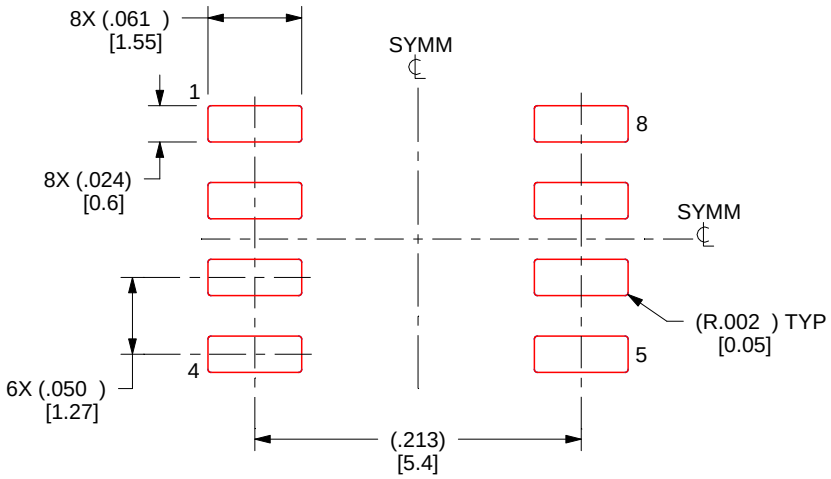
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

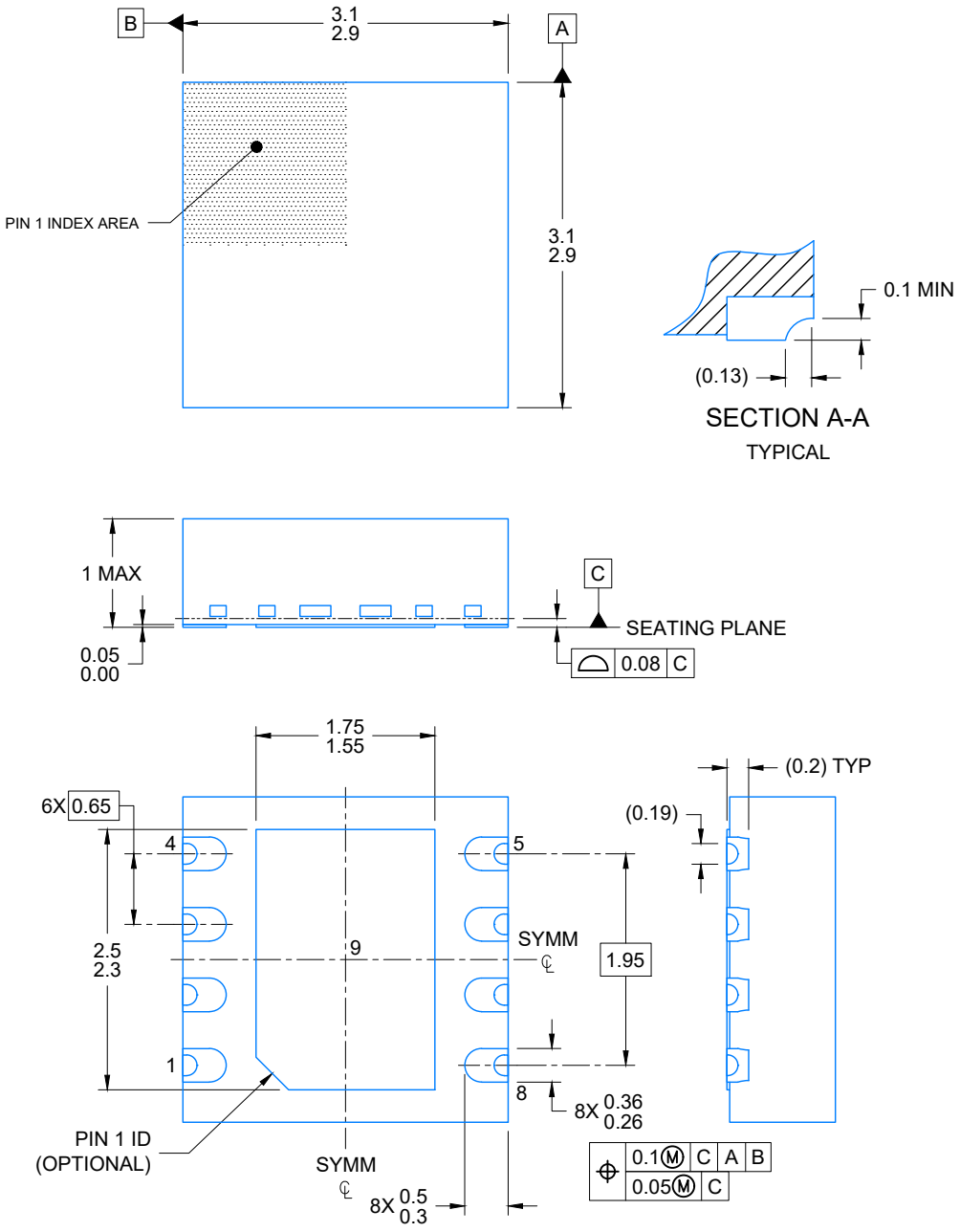
4203482/L

PACKAGE OUTLINE

DRB0008J

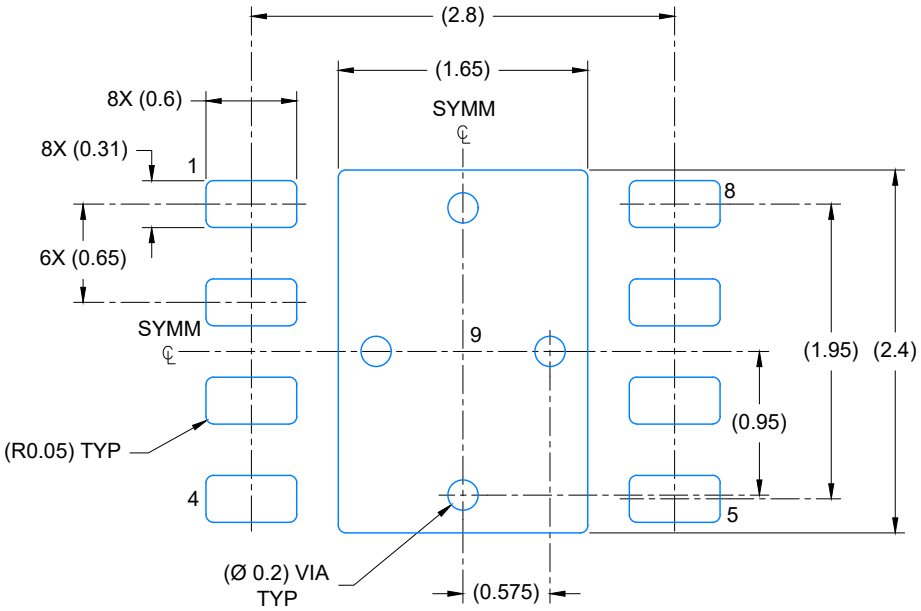
VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

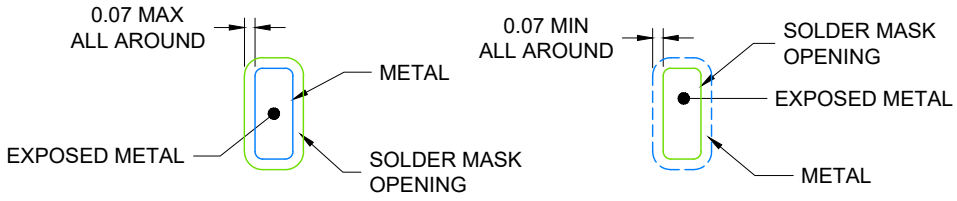


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED
(PREFERRED)

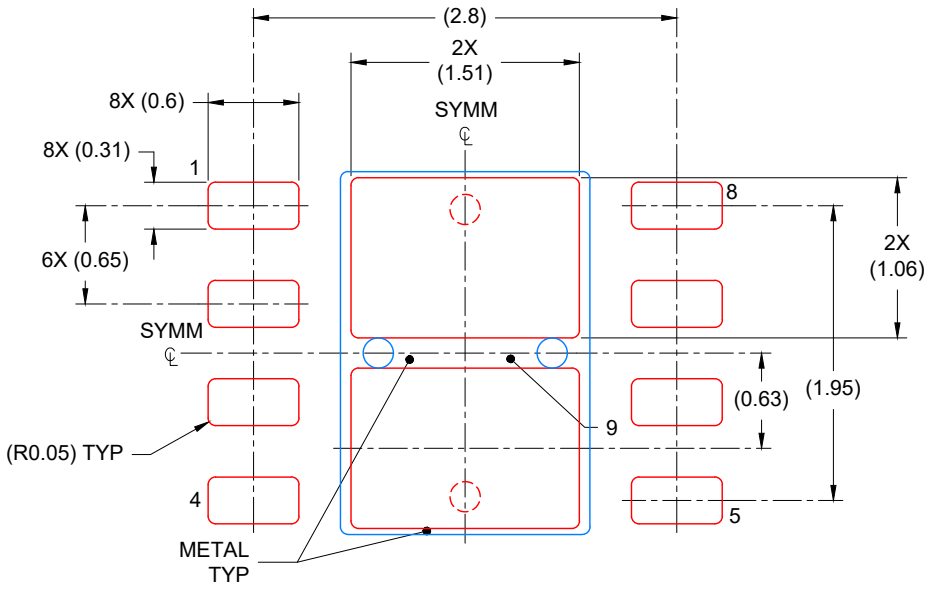
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225036/A 06/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

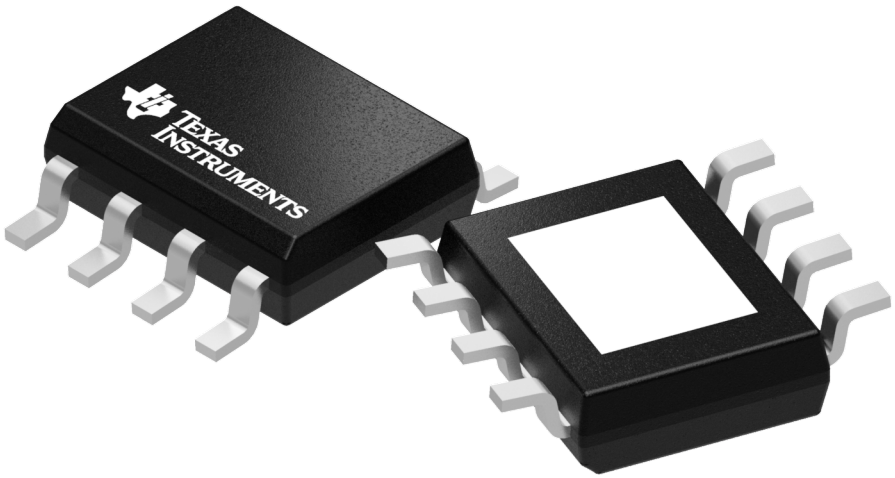
4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



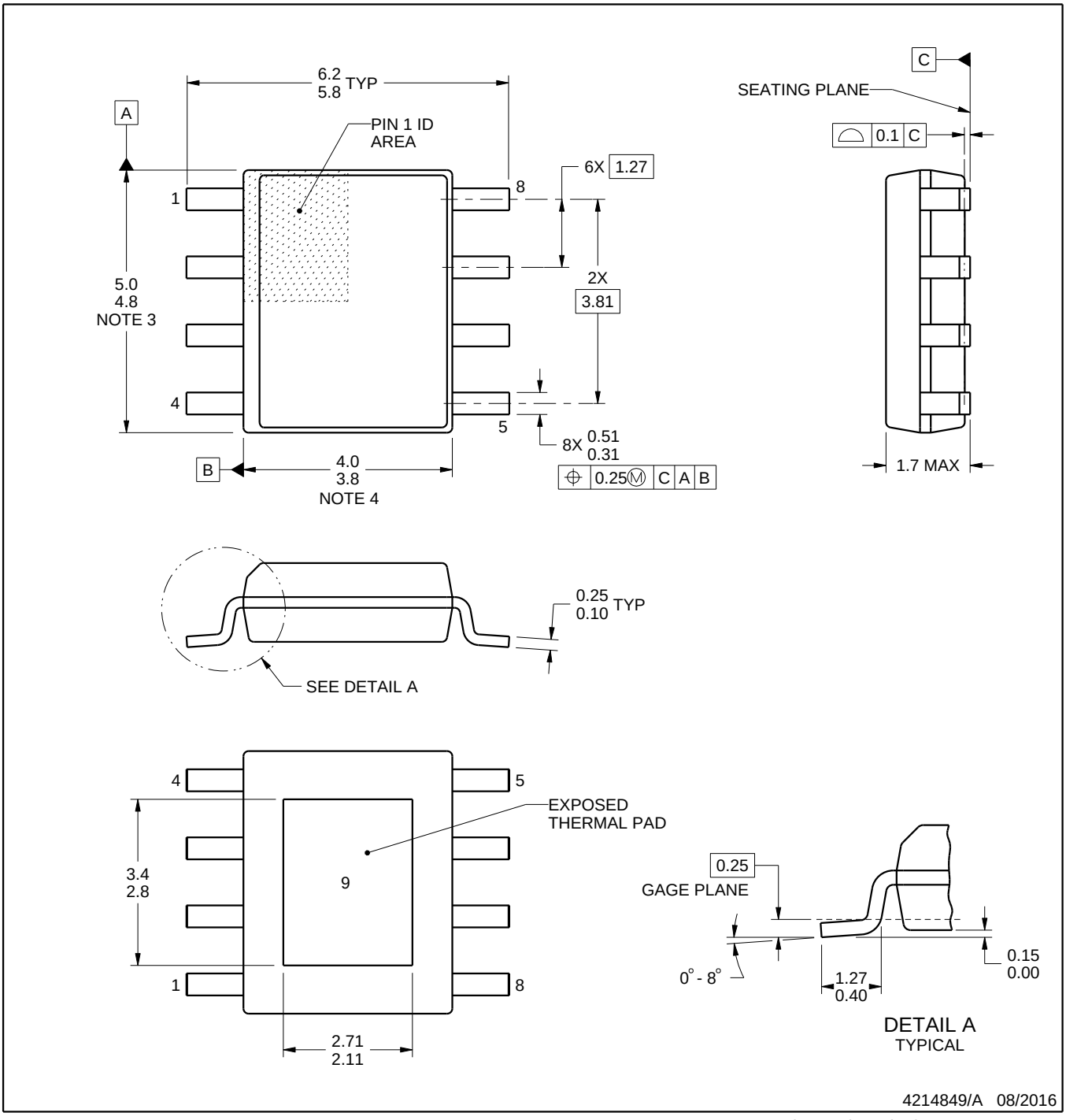
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

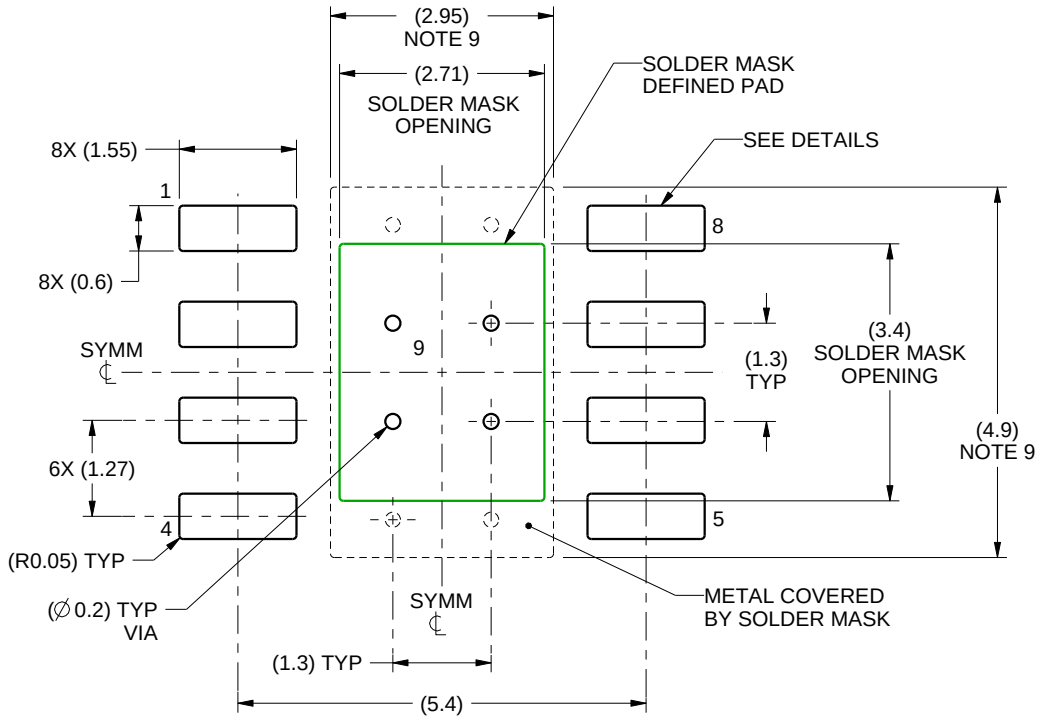
PLASTIC SMALL OUTLINE



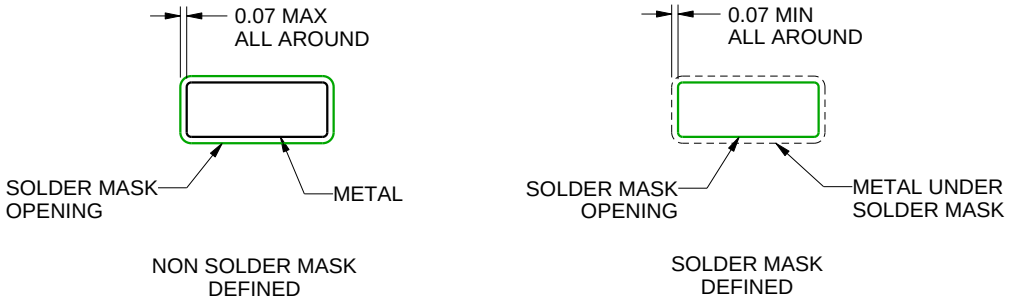
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/A 08/2016

NOTES: (continued)

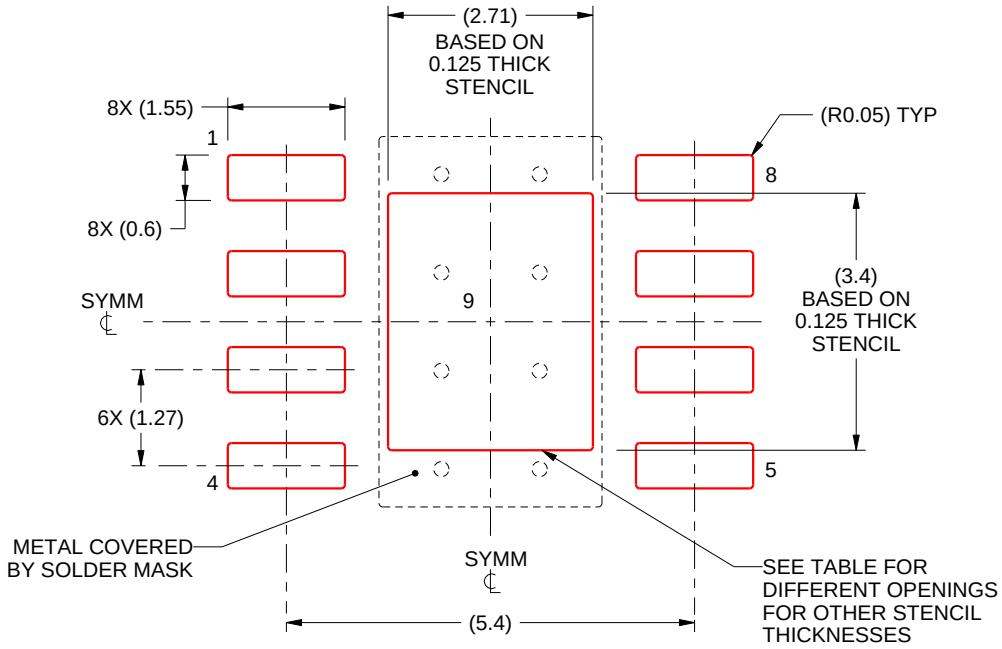
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

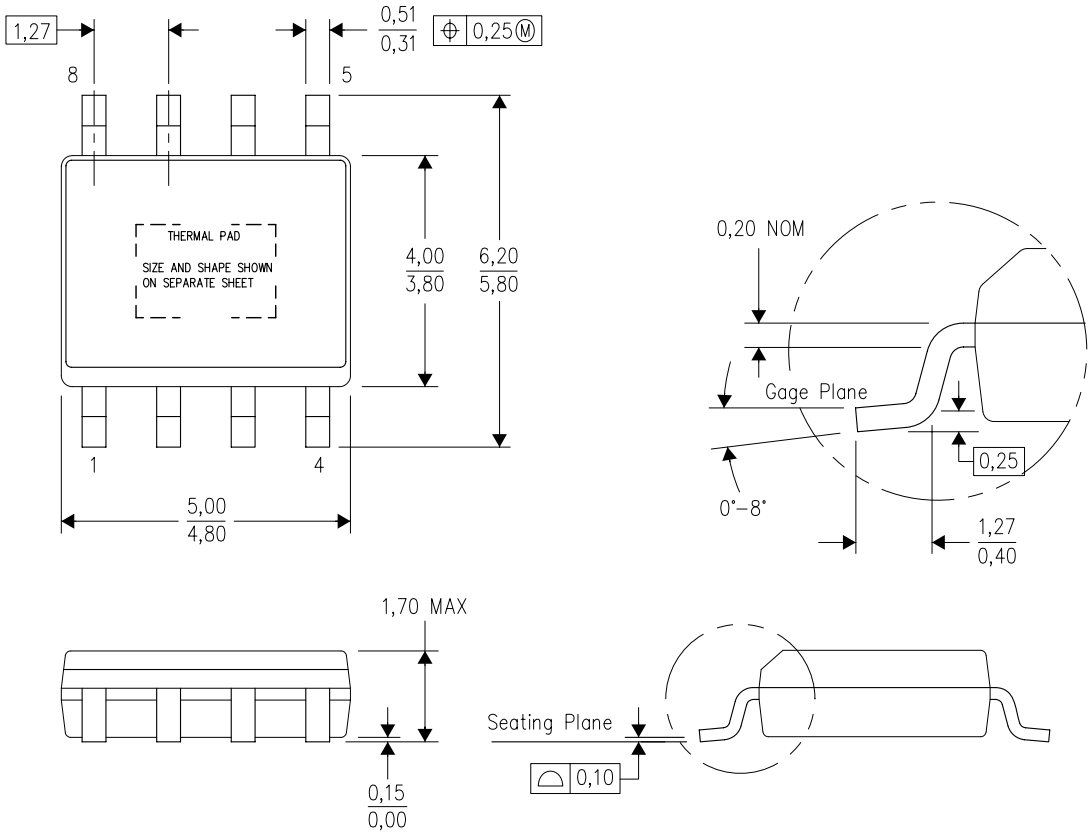
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/A 08/2016

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

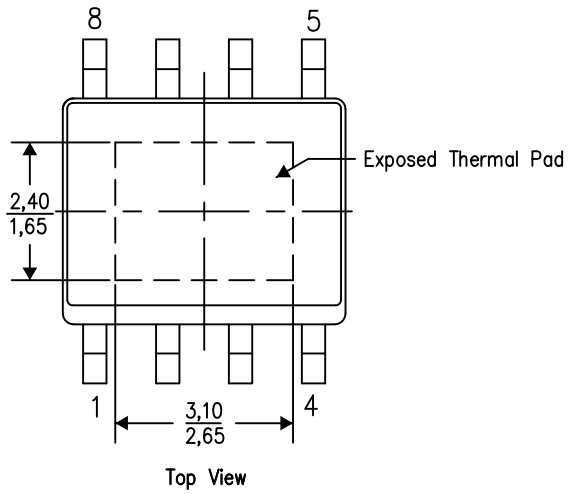
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



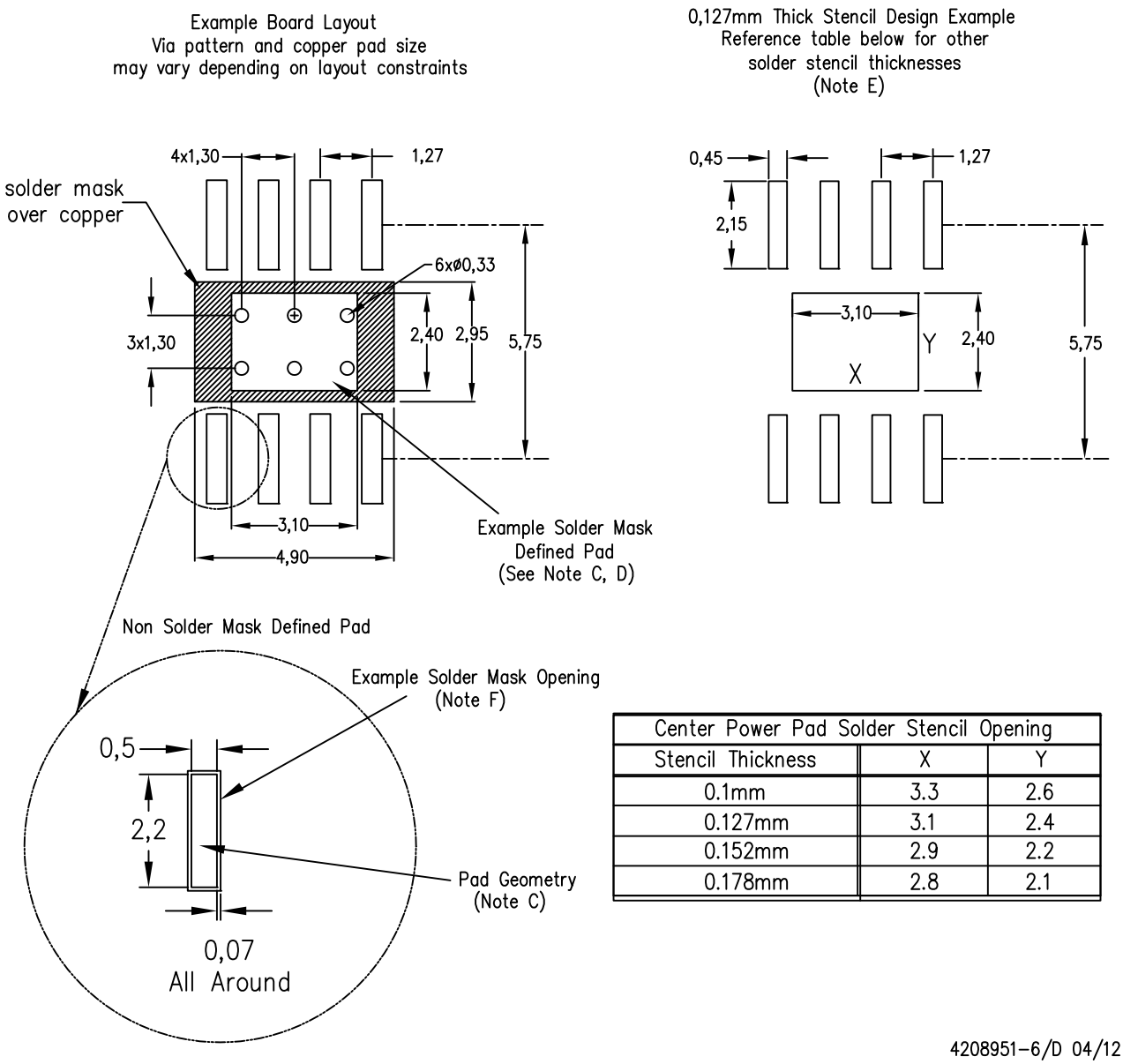
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265