

TLC69697-Q1 Automotive UART-Compatible Connectivity for TLC696[2|3][0|1|2|4|5|7|8]-Q1 Device Family

1 Features

- AEC-Q100 qualified for automotive applications
 - Grade 1: –40°C to 125°C ambient temperature
 - Device HBM classification level H2
 - Device CDM classification level C5
- Operating voltage V_{CC} range: 2.7V to 5.5V
- Control interface options
 - UART serial communication
 - Data transfer up to 4MHz
 - Support of 4 peripherals on one bus
 - CAN transceiver compatible
- LED driver SPI controller
 - Data transfer rate up to 6.6MHz
 - Programmable clock jitter for EMI enhancement
- Protection and diagnostics
 - Open-drain FAULT pin
 - UART communication loss detection
 - CRC for communication

- TLC69634Q1 and TLC69624Q1
- TLC69631Q1 and TLC69621Q1
- TLC69638Q1 and TLC69628Q1
- TLC69635Q1 and TLC69625Q1
- TLC69632Q1 and TLC69622Q1
- TLC69620Q1 and TLC69630Q1

3 Description

The TLC69697-Q1 UART-compatible connectivity enables TLC696[2|3][0|1|2|4|5|7|8]-Q1 device family to be controlled using a single UART controller. The device features an internal oscillator to generate the clock required for the SPI of the TLC696[2|3][0|1|2|4|5|7|8]-Q1 device family. The transmitted data is aligned to the clock to maintain the timing requirements of the Serial Peripheral Interface (SPI).

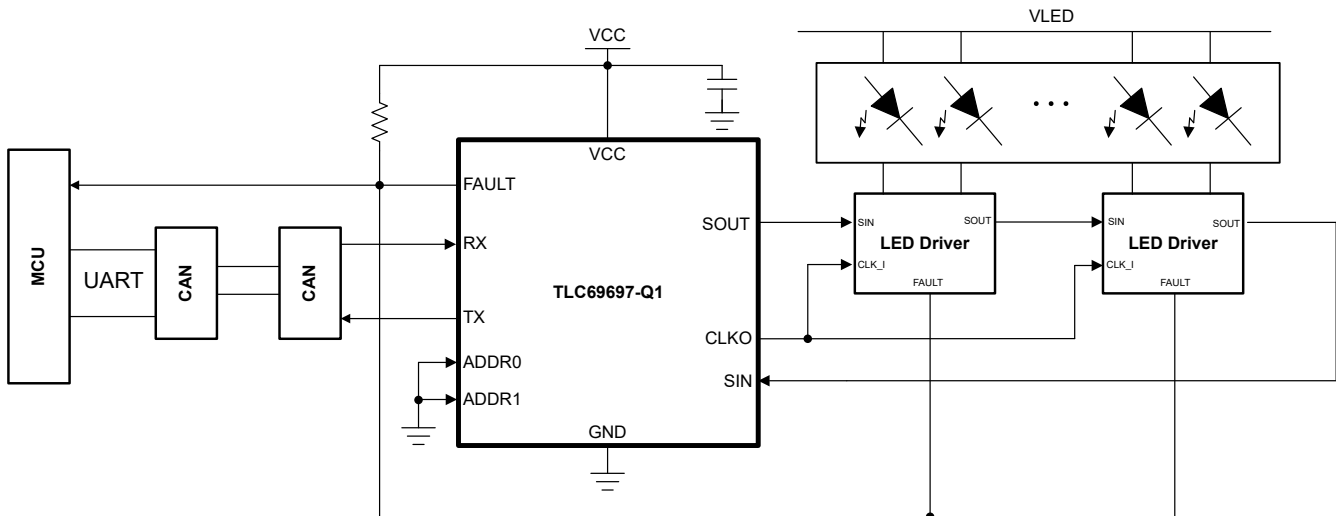
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TLC69697-Q1	SOT-23-THN (14)	4.20mm x 2.00mm

- (1) For all available packages, see the *Mechanical, Packaging, and Orderable Information* section.
- (2) The package size (length × width) is a nominal value.

2 Applications

- UART compatible connectivity for
 - TLC69637Q1 and TLC69627Q1



Typical Application Diagram



Table of Contents

1 Features	1	6.2 Support Resources.....	5
2 Applications	1	6.3 Trademarks.....	5
3 Description	1	6.4 Electrostatic Discharge Caution.....	5
4 Device Comparison Table	3	6.5 Glossary.....	5
5 Pin Configuration and Functions	4	7 Revision History	5
6 Device and Documentation Support	5	8 Mechanical, Packaging, and Orderable Information	5
6.1 Receiving Notification of Documentation Updates.....	5		

4 Device Comparison Table

PART NUMBER	MATERIAL	PACKAGE
TLC69697-Q1	TLC69697QDYRQ1	SOT-23-THN (14)

5 Pin Configuration and Functions

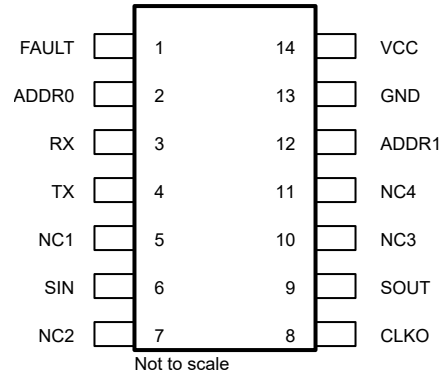


Figure 5-1. TLC69697-Q1 DYY Package, 14-Pin SOT-23-THN (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	DYY NO.		
ADDR0	2	I	Address 0 for UART interface.
ADDR1	12	I	Address 1 for UART interface.
CLKO	8	O	SPI Clock Output.
FAULT	1	O	Fault indicator open drain output.
GND	13	G	Ground pin.
NC1	5	NC	No connection.
NC2	7	NC	No connection.
NC3	10	NC	No connection.
NC4	11	NC	No connection.
RX	3	I	UART RX.
SIN	6	I	SPI Data Input.
SOUT	9	O	SPI Data Output.
TX	4	O	UART TX.
VCC	14	P	VCC Supply Input.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2026	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC69697QDYRQ1	Active	Production	SOT-23-THIN (DYY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC69697Q

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

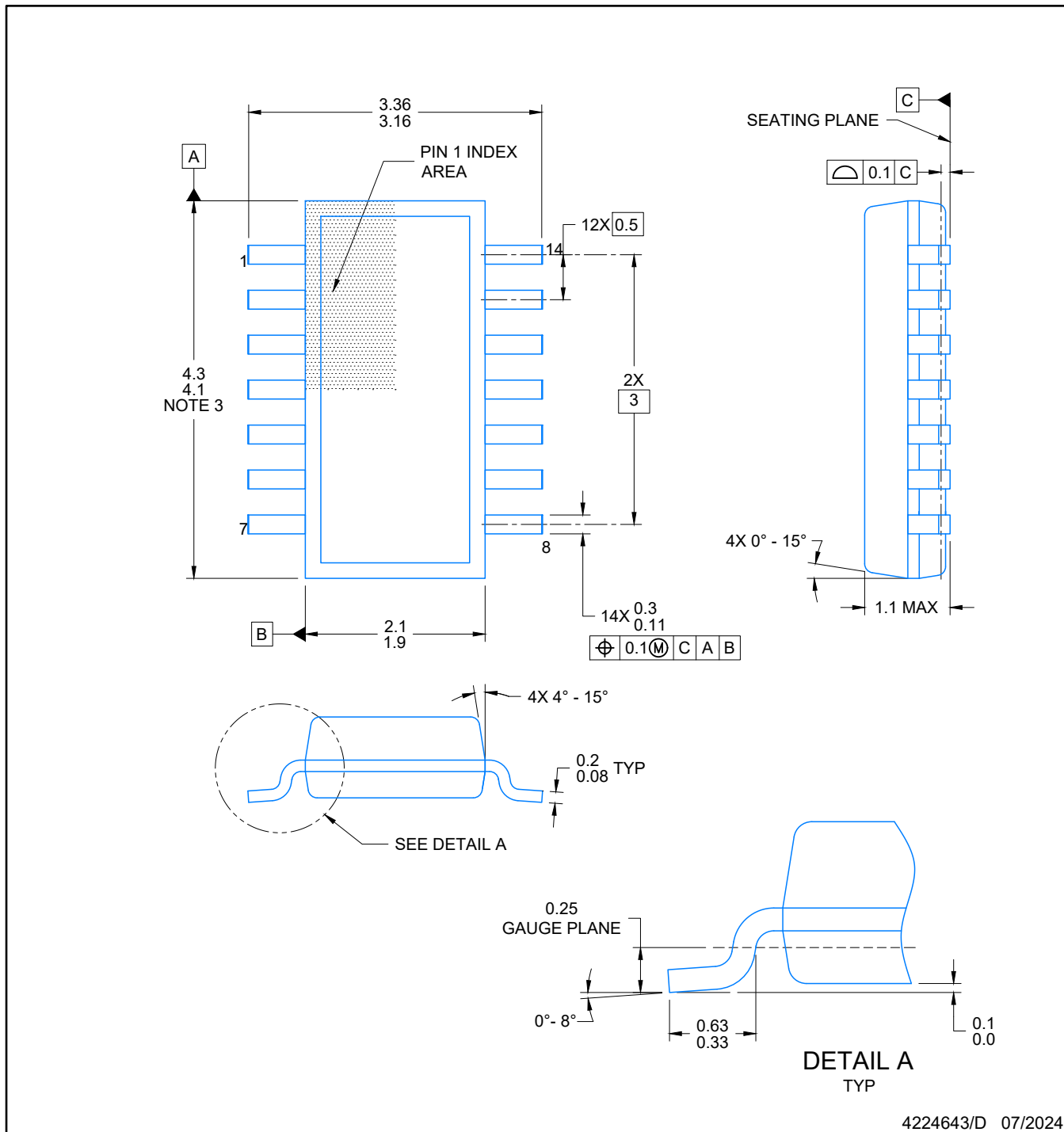
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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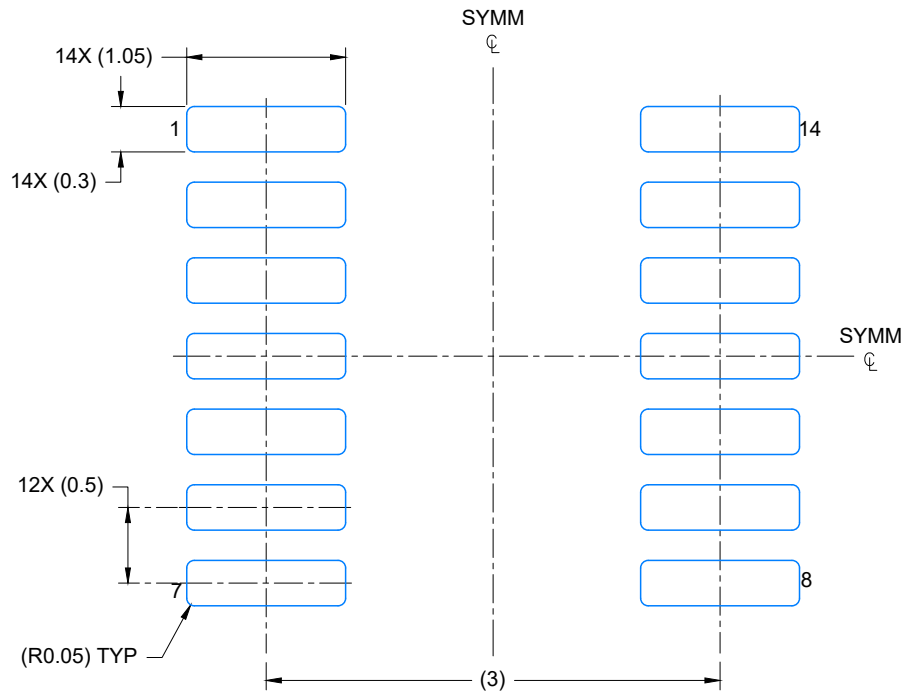
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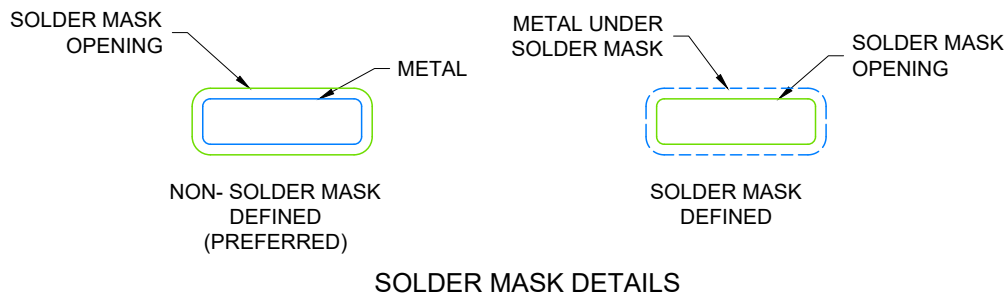
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



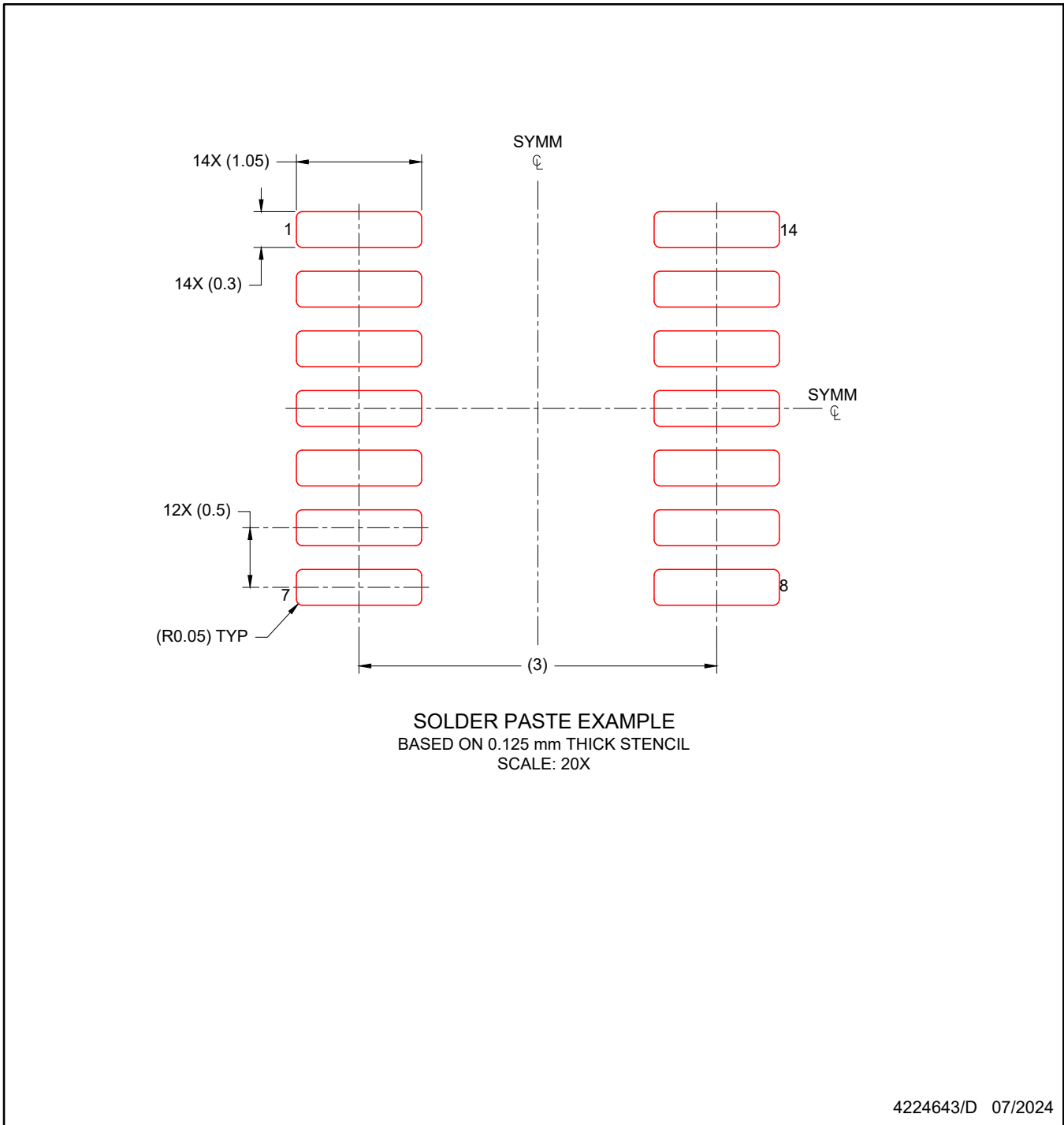
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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