16-Channel, Constant-Current LED Driver With Pre-Charge FET

1 Features

- 16-channel, constant-current sink output with on and off control
- Constant-current sink capability: 35mA (V_{CC} ≤ 3.6V), 45mA (V_{CC} > 3.6V)
- LED power-supply voltage: up to 10V
- V_{CC} = 3V to 5.5V
- Constant-current accuracy:
  - Channel-to-channel: ±1.4% (typ), ±3% (max)
  - Device-to-device: ±2% (typ), ±4% (max)
- CMOS logic level I/O
- Data transfer rate: 35MHz
- BLANK pulse width: 50ns
- Pre-charge FET for ghosting reduction
- Grouped switching delay for noise reduction
- Operating temperature: –40°C to +85°C

2 Applications

- Video displays
- Message boards

3 Description

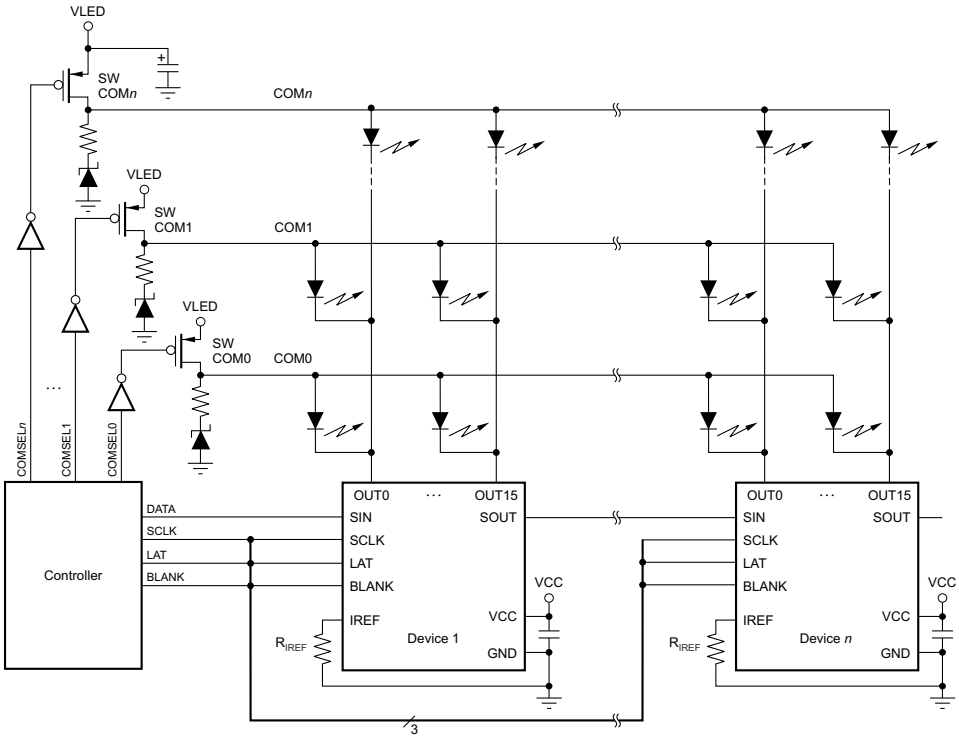
The TLC59283 is a 16-channel, constant-current sink light-emitting diode (LED) driver. Each channel can be individually controlled with a simple serial communications protocol that is compatible with 3.3V or 5V CMOS logic levels, depending on the operating VCC. When the serial data buffer is loaded, a LAT rising edge transfers the data to the OUT*n* outputs. The BLANK pin can be used to turn off all OUT*n* outputs during power-on and output data latching to prevent unwanted image displays during these times. The constant-current value of all 16 channels is set by a single external resistor.

Each constant-current output has a pre-charge field-effect transistor (FET) that can reduce ghosting on the multiplexing (dynamic) drive LED display. Multiple TLC59283s can be cascaded together to control additional LEDs from the same processor.

Package Information

PART NUMBER	PACKAGE(1)
TLC59283	DB (SSOP, 24)
	DBQ (QSOP, 24)
TLC59283	RGE (QFN, 24)

(1) For more information, see Section 12.



Typical Application Circuit (Multiple Daisy-Chained TLC59283s)

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4 Pin Configurations

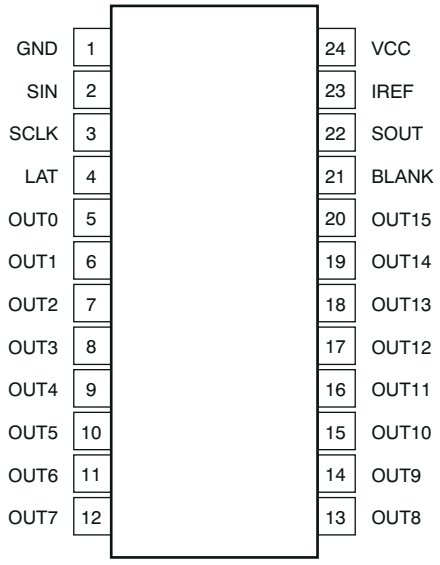


Figure 4-1. DBQ Package SSOP-24 and QSOP-24 (top view)

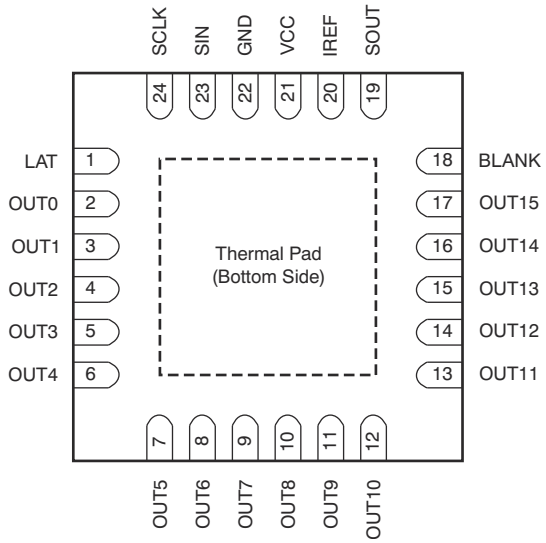


Figure 4-2. RGE Package QFN-24 (top view)

NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND with the printed circuit board (PCB) pattern.

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NUMBER			
	DBQ	RGE		
BLANK	21	18	I	All outputs empty (blank); Schmitt buffer input. When BLANK is high, all constant-current outputs (OUT0 to OUT15) are forced off and all pre-charge FETs are turned on. When BLANK is low, all constant-current outputs are controlled by the data in the output on or off data latch and all pre-charge FETs are turned off. This pin is internally pulled up to V_{CC} with a 500kΩ (typ) resistor.
GND	1	22	—	Power ground
IREF	23	20	I/O	Constant-current value setting, the OUT0 to OUT15 sink constant-current outputs are set to the desired values by connecting an external resistor between IREF and GND.
LAT	4	1	I	Level-triggered latch; Schmitt buffer input. The data in the 16-bit shift register continue to transfer to the output on or off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. This pin is internally pulled down to GND with a 500kΩ (typ) resistor.
OUT0	5	2	O	Constant-current output. Each output can be tied together with others to increase the constant-current. Different voltages can be applied to each output.
OUT1	6	3	O	Constant-current output
OUT2	7	4	O	Constant-current output
OUT3	8	5	O	Constant-current output
OUT4	9	6	O	Constant-current output
OUT5	10	7	O	Constant-current output
OUT6	11	8	O	Constant-current output
OUT7	12	9	O	Constant-current output
OUT8	13	10	O	Constant-current output
OUT9	14	11	O	Constant-current output
OUT10	15	12	O	Constant-current output
OUT11	16	13	O	Constant-current output
OUT12	17	14	O	Constant-current output
OUT13	18	15	O	Constant-current output
OUT14	19	16	O	Constant-current output
OUT15	20	17	O	Constant-current output
SCLK	3	24	I	Serial data shift clock; Schmitt buffer input. All data in the 16-bit shift register are shifted toward the MSB by a 1-bit SCLK synchronization.
SIN	2	23	I	Serial data input for driver on or off control; Schmitt buffer input. When SIN is high, the LSB is set to '1' for only one SCLK input rising edge. If two SCLK rising edges are input while SIN is high, then the 16-bit shift register LSB and LSB+1 are set to '1'. When SIN is low, the LSB is set to '0' at the SCLK input rising edge.
SOUT	22	19	O	Serial data output. This output is connected to the 16-bit shift register MSB. SOUT data changes at the SCLK rising edge.
VCC	24	21	—	Power-supply voltage

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

			VALUE		UNIT(2)
			MIN	MAX	
Voltage	V_{CC}	Supply	–0.3	+6	V
	V_{IN}	Input range, SIN, SCLK, LAT, BLANK, IREF	–0.3	V_{CC} + 0.3	V
	V_{OUT}	Output range, SOUT	–0.3	V_{CC} + 0.3	V
		Output range, OUT0 to OUT15	–0.3	+11	V
Current	I_{OUT}	Output (dc), OUT0 to OUT15		+50	mA
Temperature	$T_{J(MAX)}$	Operating junction		+150	°C
	T_{stg}	Storage range	–55	+150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.

5.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	-55	+150	°C

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±2000	

5.4 Recommended Operating Conditions

At T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER			TEST CONDITIONS	TLC59283 MIN	TLC59283 MAX	UNIT
DC CHARACTERISTICS (V_{CC} = 3 V to 5.5 V)						
V_{CC}	Supply voltage			3	5.5	V
V_O	Voltage applied to output		OUT0 to OUT15		10	V
V_{IH}	Input voltage	High	SIN, SCLK, LAT, BLANK	0.7 × V_{CC}	V_{CC}	V
V_{IL}		Low	SIN, SCLK, LAT, BLANK	GND	0.3 × V_{CC}	V
I_{OH}	Output current	High	SOUT		–2	mA
I_{OL}		Low	SOUT		2	mA
I_{OLC}	Constant output sink current		OUT0 to OUT15, 3 V ≤ V_{CC} ≤ 3.6 V	2	35	mA
			OUT0 to OUT15, 3.6 V < V_{CC} ≤ 5.5 V	2	45	mA
T_A	Temperature range	Operating free-air		–40	+85	°C
T_J		Operating junction		–40	+125	°C
AC CHARACTERISTICS (V_{CC} = 3 V to 5.5 V)						
$f_{CLK\ (SCLK)}$	Data shift clock frequency		SCLK		35	MHz
t_{WH0}	Pulse duration		SCLK	10		ns
t_{WL0}			SCLK	10		ns
t_{WH1}			LAT	20		ns
t_{WH2}			BLANK	100		ns
t_{WL2}			BLANK	50		ns
t_{SU0}	Setup time		SIN↑↓ – SCLK↑	4		ns
t_{SU1}			LAT↓ – SCLK↑	10		ns
t_{H0}	Hold time		SIN↑↓ – SCLK↑	4		ns
t_{H1}			LAT↓ – SCLK↑	10		ns

5.5 Thermal Information

THERMAL METRIC		TLC59283 DBQ 24 PINS	TLC59283 RGE 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	91.5	42.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	55.2	55.3	
θ_{JB}	Junction-to-board thermal resistance	44.9	21.7	
ψ_{JT}	Junction-to-top characterization parameter	16.8	1.9	
ψ_{JB}	Junction-to-board characterization parameter	44.5	21.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	8.8	

5.6 Electrical Characteristics

All minimum and maximum specifications are at T_A = –40°C to +85°C and V_{CC} = 3V to 5.5V, unless otherwise noted. Typical specifications are at T_A = +25°C and V_{CC} = 3.3V.

PARAMETER			TEST CONDITIONS		TLC59283 MIN	TLC59283 TYP	TLC59283 MAX	UNIT
V_{OH}	Output voltage	High	I_{OH} = –2mA at SOUT		V_{CC} – 0.4		V_{CC}	V
V_{OL}		Low	I_{OL} = 2mA at SOUT				0.4	V
V_{PCHG}	Pre-charged voltage		I_O = –10µA		V_{CC} – 2.0	V_{CC} – 1.4	V_{CC} – 0.8	V
V_{IREF}	Reference voltage output		R_{IREF} = 1.5kΩ, T_A = +25°C			1.208		V
I_{IN}	Input current		V_{IN} = V_{CC} or GND at SIN and SCLK		–1		1	µA
I_{CC0}	Supply current (V_{CC})		SIN, SCLK, LAT = GND, BLANK = V_{OUTn} = V_{CC}, R_{IREF} = open			1	2	mA
I_{CC1}			SIN, SCLK, LAT = GND, BLANK = V_{OUTn} = V_{CC}, R_{IREF} = 3kΩ (I_{OUT} = 17.6mA target)			3	4	mA
I_{CC2}			All OUT*n* = ON, SIN, SCLK, LAT, BLANK = GND, V_{OUTn} = 0.8V, R_{IREF} = 3kΩ			7	9	mA
I_{CC3}			All OUT*n* = ON, SIN, SCLK, LAT, BLANK = GND, V_{OUTn} = 0.8V, R_{IREF} = 1.5kΩ (I_{OUT} = 35.3mA target)			8	11	mA
I_{OLC}	Constant output current		All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8V, R_{IREF} = 1.5kΩ, T_A = +25°C (see Figure 6-8)		32.9	35.3	37.7	mA
I_{OLKG0}	Output leakage current		All OUT*n* = OFF, V_{OUTn} = V_{OUTfix} = 10 V, BLANK = V_{CC}, R_{IREF} = 1.5 kΩ (see Figure 6-8)	T_J = +25°C			0.1	µA
				T_J = +85°C			0.2	µA
				T_J = +125°C		0.07	0.5	µA
ΔI_{OLC0}	Constant-current error	Channel-to-channel(1)	All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8V, R_{IREF} = 1.5kΩ, T_A = +25°C (see Figure 6-8)			±1.4	±3	%
ΔI_{OLC1}		Device-to-device(2)	All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8V, R_{IREF} = 1.5kΩ, T_A = +25°C (see Figure 6-8)			±2	±4	%
ΔI_{OLC2}	Line regulation(3)		All OUT*n* = ON, V_{OUTn} = V_{OUTfix} = 0.8V, R_{IREF} = 1.5kΩ, V_{CC} = 3V to 5.5V			±0.05	±1	%/V
ΔI_{OLC3}	Load regulation(4)		All OUT*n* = ON, V_{OUTn} = 0.8V to 3V, V_{OUTfix} = 0.8V, R_{IREF} = 1.5kΩ			±0.5	±1	%/V
R_{PUP}	Resistor	Pull-up	BLANK		250	500	750	kΩ
R_{PDWN}		Pull-down	LAT		250	500	750	kΩ
R_{PCHG}	Pre-charge FET on-resistance		VCC = 5.0V, V_{OUTn} = 0V, OUT0 to OUT15, BLANK = V_{CC}, T_A = +25°C			3	6	kΩ

(1) The deviation of each output from the average of OUT0 to OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta\ (\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT14} + I_{OUT15})}{16}} - 1 \right) \times 100$$

(2) The deviation of the OUT0 to OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta\ (\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 43.8 \times \left(\frac{1.208\ V}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\ V) - (I_{OUTn} \text{ at } V_{CC} = 3\ V)}{(I_{OUTn} \text{ at } V_{CC} = 3\ V)} \right) \times \frac{100}{5.5\ V - 3\ V}$$

(4) Load regulation is calculated by the equation:

$$\Delta\ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\ V) - (I_{OUTn} \text{ at } V_{OUTn} = 1\ V)}{(I_{OUTn} \text{ at } V_{OUTn} = 1\ V)} \right) \times \frac{100}{3\ V - 1\ V}$$

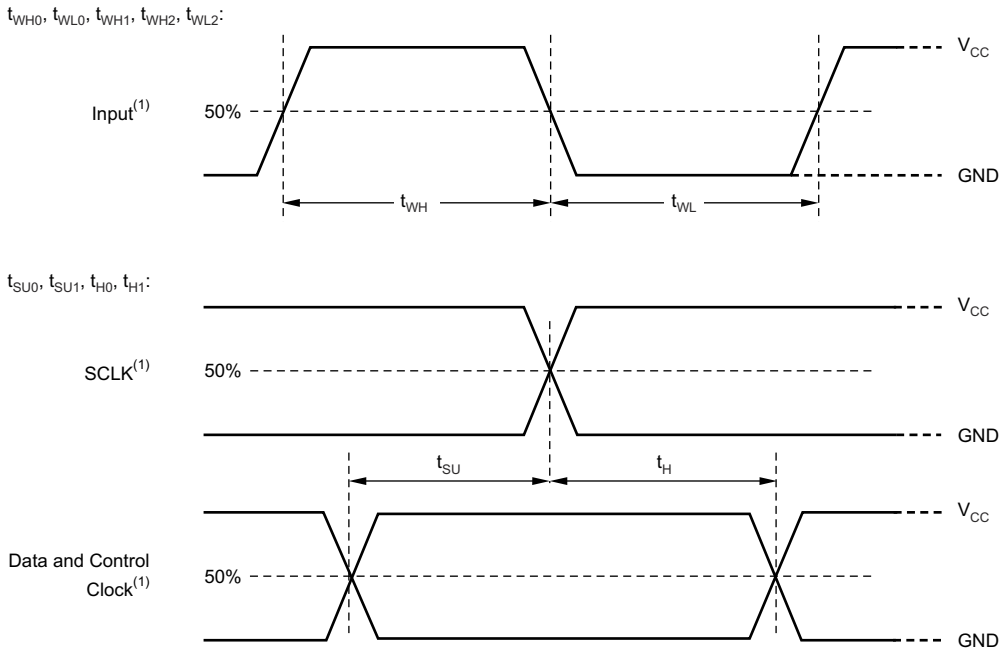
5.7 Timing Characteristics

All minimum and maximum specifications are at T_A = –40°C to +85°C, V_{CC} = 3V to 5.5V, C_L = 15pF, R_L = 110Ω, R_{IREF} = 1.5kΩ, and V_{LED} = 5.0V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 3.3V.

PARAMETER		TEST CONDITIONS	TLC59283			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	SOUT (see Figure 6-7)		3	10	ns
t_{R1}		OUT*n* (see Figure 6-6)		44		ns
t_{F0}	Fall time	SOUT (see Figure 6-7)		3	10	ns
t_{F1}		OUT*n* (see Figure 6-6)		44		ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT↑↓		11	20	ns
t_{D1}		LAT↑ or BLANK↑↓ to OUT0 on or off, T_A = +25°C		60	100	ns
t_{D2}		Grouped OUT*n* on or off to next group on or off, T_A = +25°C		2		ns
t_{ON_ERR}	Output on-time error(1)	Output on or off latch data = all '1', 50ns BLANK GND level pulse, V_{CC} = 3.3V, T_A = +25°C	–45		45	ns

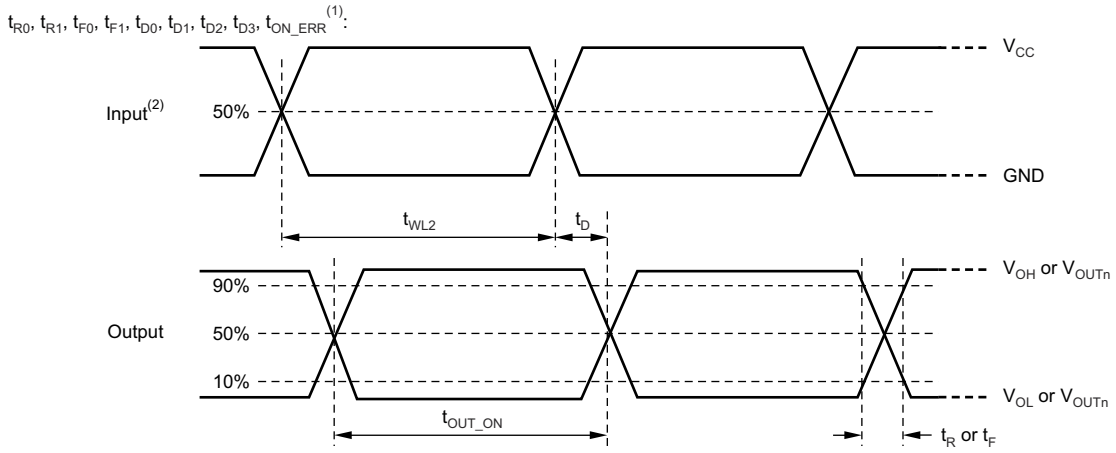
(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low level one-shot pulse width (t_{WL2}). t_{OUT_ON} indicates the actual on-time of the constant-current output.

5.8 Timing Diagrams



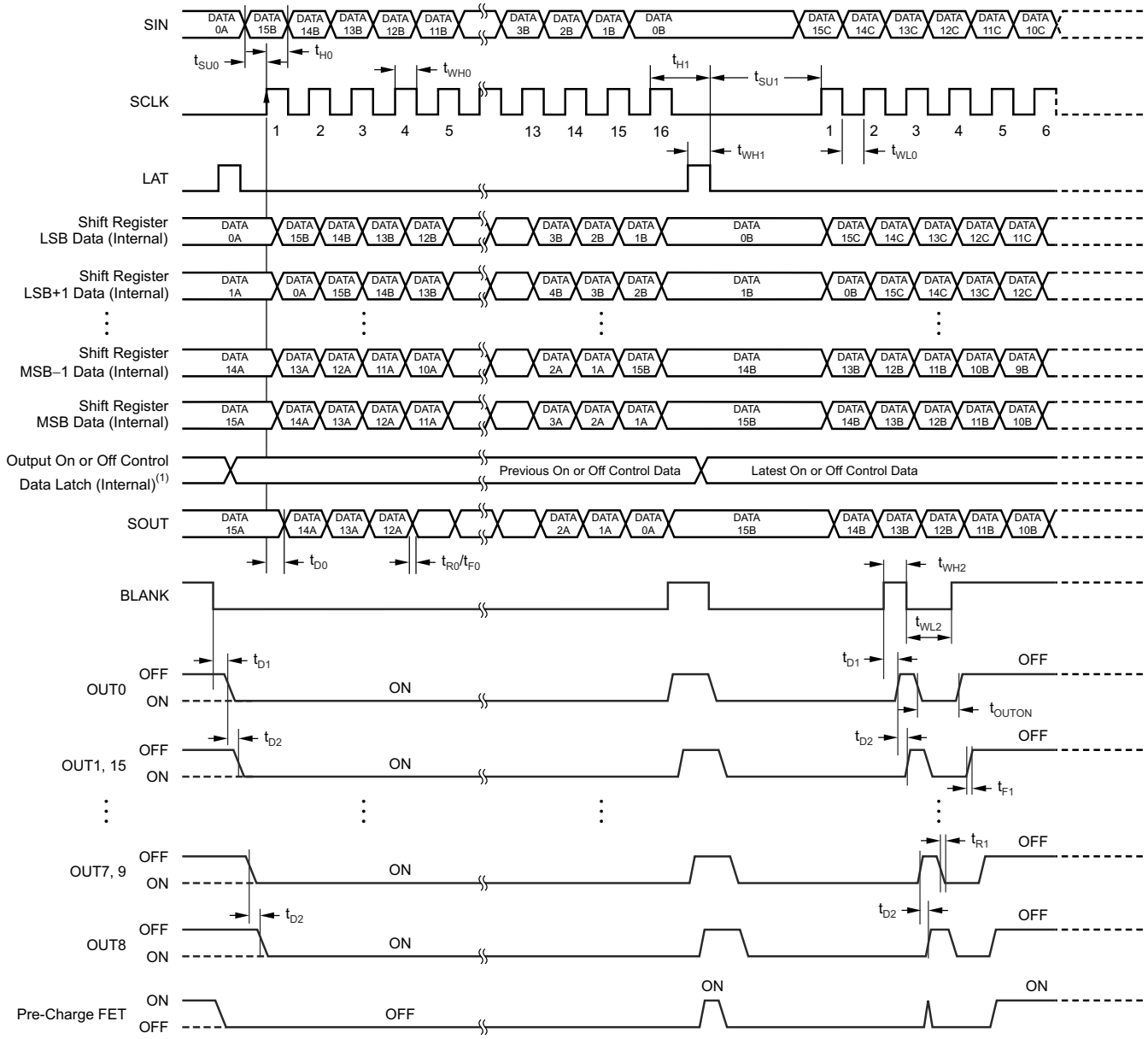
A. Input pulse rise and fall time is 1ns to 3ns.

Figure 5-1. Input Timing Diagram



A. t_{ON_ERR} is calculated by $t_{OUTON} - t_{WL2}$.
B. Input pulse rise and fall time is 1ns to 3ns.

Figure 5-2. Output Timing Diagram



A. Output on or off data = FFFFh.

B. $t_{ON\_ERR} = t_{OUTON} - t_{WL2}$.

Figure 5-3. Data Write and Output On or Off Timing Diagram

5.9 Typical Characteristics

At T_A = +25°C and V_{CC} = 3.3V, unless otherwise noted.

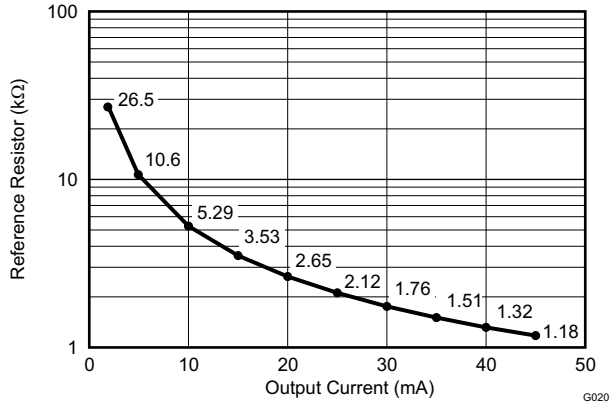


Figure 5-4. Reference Resistor vs Output Current

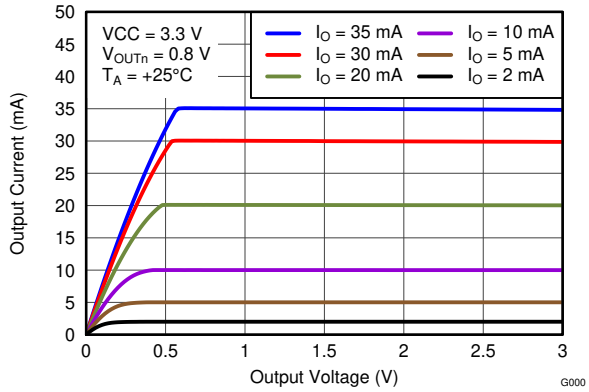


Figure 5-5. Output Current vs Output Voltage (VCC = 3.3V)

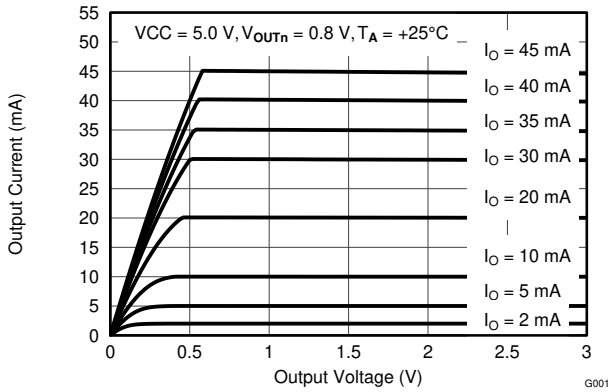


Figure 5-6. Output Current vs Output Voltage (VCC = 5.0V)

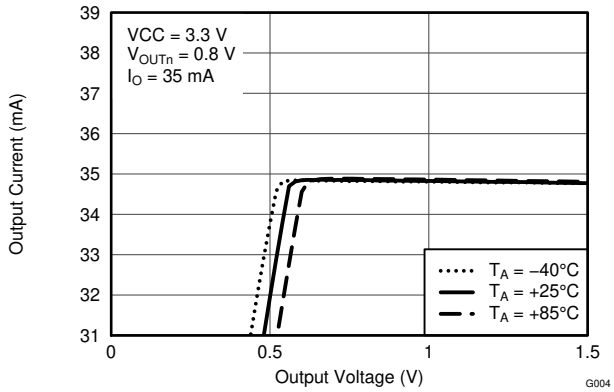


Figure 5-7. Output Current vs Output Voltage (VCC = 3.3V, Magnified)

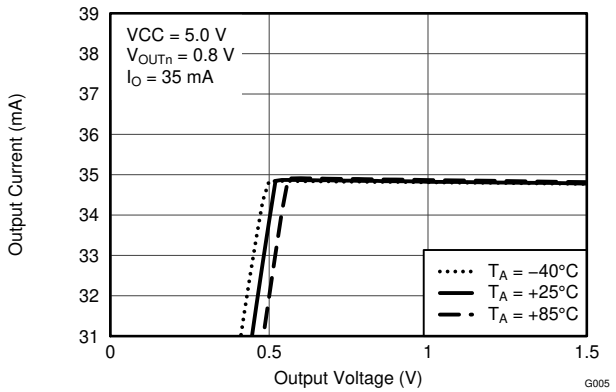


Figure 5-8. Output Current vs Output Voltage (VCC = 5.0V, Magnified)

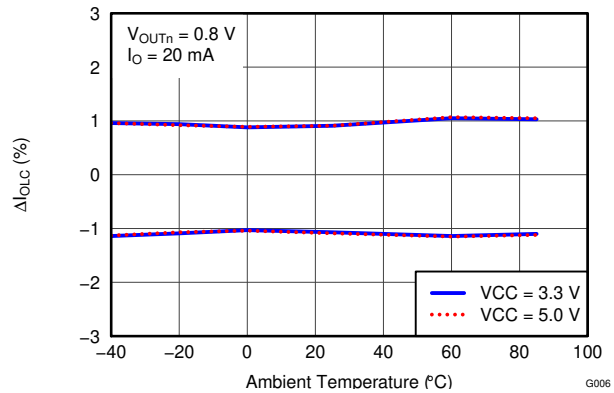


Figure 5-9. ΔI_{OLC} vs Ambient Temperature

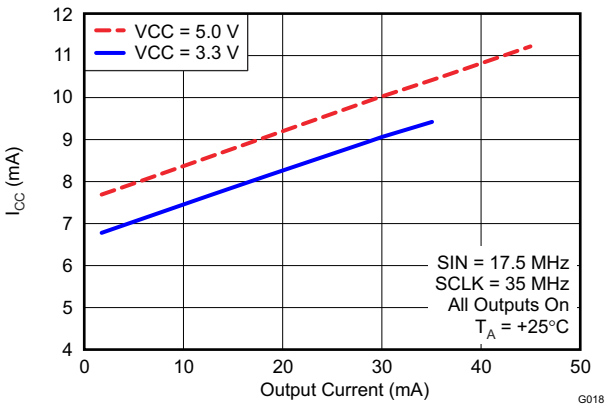


Figure 5-10. Supply Current vs Output Current

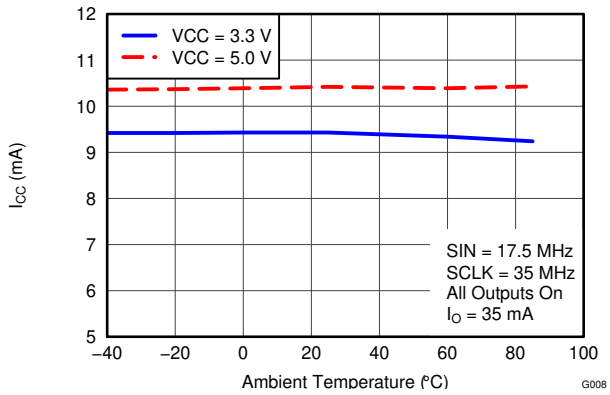


Figure 5-11. Supply Current vs Ambient Temperature

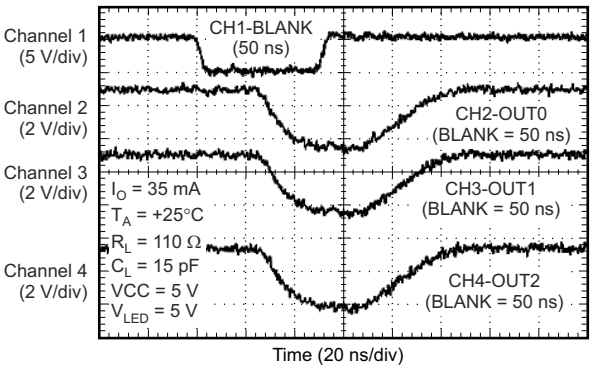


Figure 5-12. Constant-current Output Voltage Waveform

6 Parameter Measurement Information

6.1 Pin-equivalent Input and Output Schematic Diagrams

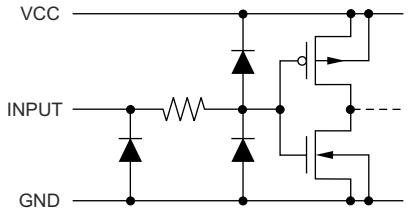


Figure 6-1. SIN and SCLK

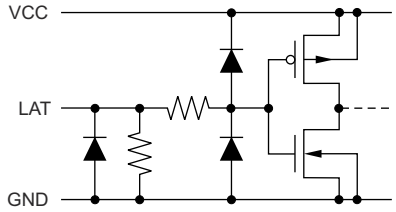


Figure 6-2. LAT

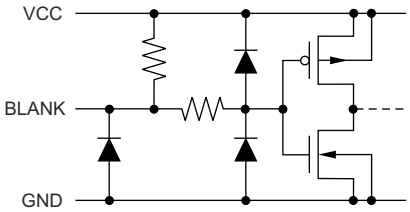


Figure 6-3. BLANK

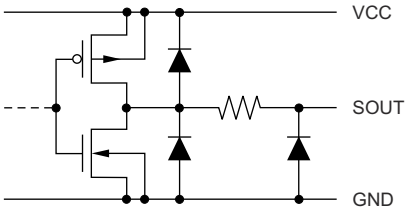
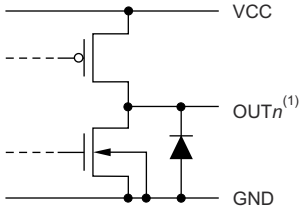


Figure 6-4. SOUT



A. n = 0 to 15.

Figure 6-5. OUT0 Through OUT15

6.2 Test Circuits

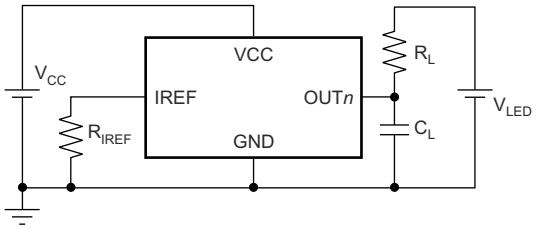


Figure 6-6. OUT*n* Rise and Fall Time Test Circuit

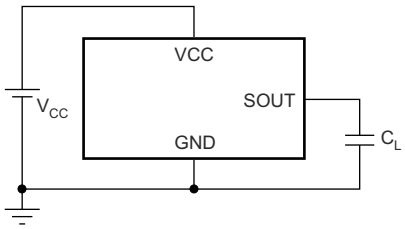


Figure 6-7. SOUT Rise and Fall Time Test Circuit

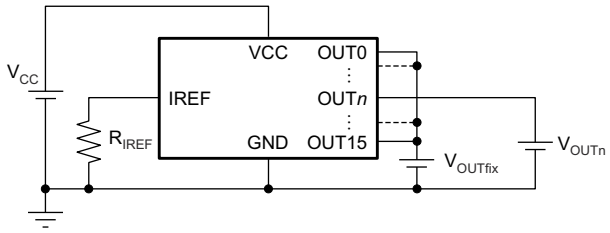


Figure 6-8. OUT*n* Constant-current Test Circuit

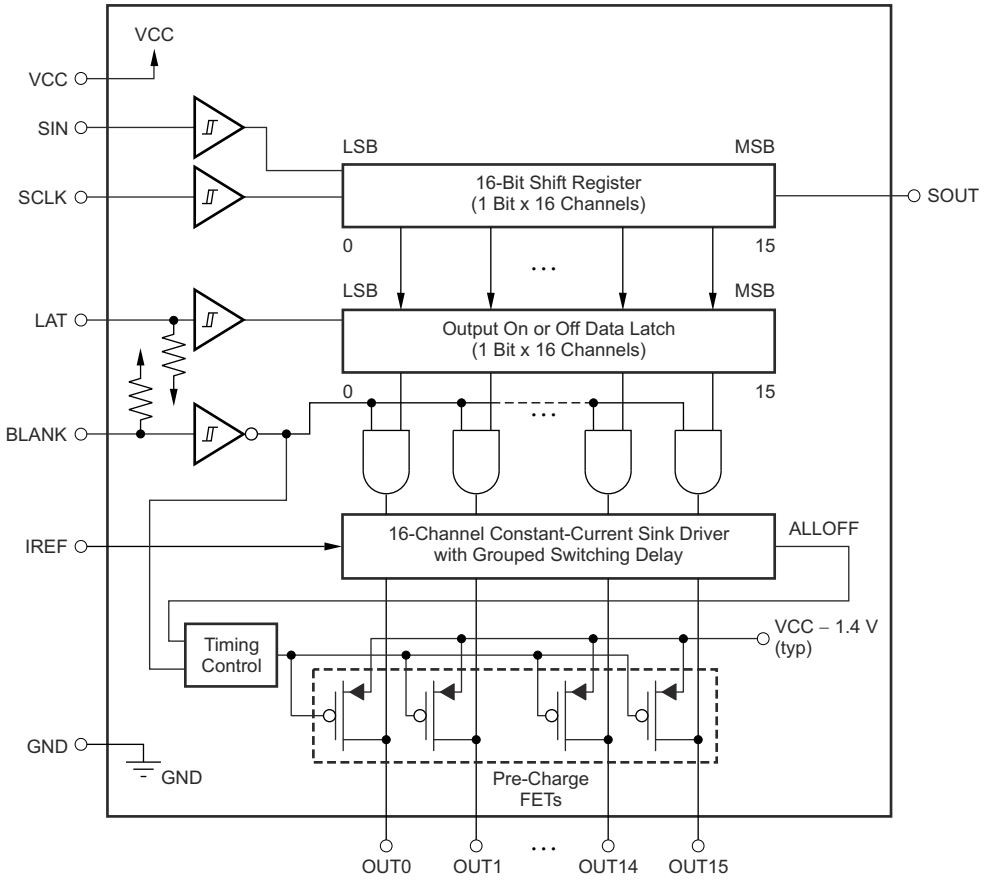
7 Detailed Description

7.1 Overview

The TLC59283 is a 16-channle, constant-current sink light-emitting diode (LED) driver. Each channel can be individually controlled with a simple serial communications protocol that is compatible with 3.3V or 5V CMOS logic levels, depending on the operating VCC. When the serial data buffer is loaded, a LAT rising edge transfers the data to the OUTn outputs. The BLANK pin can be sed to turn off all OUTn outputs during power-on and output data latching to prevent unwanted image displays during these times. The constant-current value of all 16 channels is set by a single external resistor.

Each constant-current output has a pre-charge field effect transistor (FET) that can reduce ghosting on the multiplexing (dynamic) drive LED display. Multiple TLC59283s can be cascaded together to control additional LEDs from the same processor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Constant Sink Current Value Setting

The constant-current values are determined by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by Equation 1.

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLC}\ (mA)} \times 43.8 \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (typically 1.208V)

I_{OLC} must be set in the range of 2mA to 35mA when V_{CC} is less than 3.6V. Also, when V_{CC} is equal to 3.6V or greater, I_{OLC} must be set in the range of 2mA to 45mA. The constant sink current characteristic for the external resistor value is illustrated in Figure 5-4. Table 7-1 describes the constant-current output versus external resistor value.

Table 7-1. Constant-current Output Versus External Resistor Value

I_{OLC} (mA)	R_{IREF} (kΩ, Typical)
45 (V_{CC} > 3.6V only)	1.18
40 (V_{CC} > 3.6V only)	1.32
35	1.51
30	1.76
25	2.12
20	2.65
15	3.53
10	5.29
5	10.6
2	26.5

7.3.2 Constant-current Driver On or Off Control

When BLANK is low, the corresponding output is turned on if the data in the on or off control data latch are '1' and remains off if the data are '0'. When BLANK is high, all outputs are forced off. This control is shown in Table 7-2.

Table 7-2. Output On or Off Control Data Truth Table

OUTPUT ON OR OFF DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

When the device is initially powered on, the data in the 16-bit shift register and output on or off data latch are not set to default values. Therefore, the output on or off data must be written to the data latch before turning the constant-current output on. **BLANK should be high when powered on because the constant-current may be turned on as a result of random data in the output on or off data latch.**

7.3.3 Noise Reduction

Large surge currents can flow through the device and board if all 16 outputs turn on or off simultaneously. These large current surges can induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC59283 independently turns on or off the outputs for each group with a 1ns (typ) delay time; see Figure 5-3. The 16 outputs are grouped into nine groups of either one or two outputs: group 1 (OUT0), group 2 (OUT1 and OUT15), group 3 (OUT2 and OUT14), group 4 (OUT3 and OUT13), group 5 (OUT4 and OUT12), group 6 (OUT5 and OUT11), group 7 (OUT6 and OUT10), group 8 (OUT7 and OUT9), and group 9 (OUT9). Both turn-on and turn-off times are delayed when BLANK transitions from low to high or high to low. Also when output-on and -off data are changed at the LAT rising edge while BLANK is low, both turn-on and turn-off times are delayed. However, the state of each output is controlled by the data in the output on or off data latch and the BLANK level.

7.3.3.1 Internal Pre-Charge FET

The internal pre-charge FET prevents ghosting of multiplexed LED modules. One cause of this phenomenon is the parasitic capacitance charging current of the constant-current outputs (OUT*n*) and PCB wiring connected to OUT*n* through the LED. One of the mechanisms is shown in Figure 7-1.

In Figure 7-1, the constant-current driver turns LED0-0 on at (1) and off at (2). After LED0-0 is turned off, the OUT0 voltage is pulled up to V_{CHG} by LED0-0. This OUT0 node has some parasitic capacitance (such as the constant-current driver output capacitance and the board layout capacitance shown as C0-2). After LED0-0 turns off, SWPMOS0 is turned off, SWNMOS0 is turned on for COM0, and COM0 is pulled down to GND. Because there is a parasitic capacitance between COM0 and OUT0, the OUT0 voltage is also pulled down to GND. Afterwards, SWPMOS1 is turned on for the next common line (COM1). When SWPMOS1 turns on, the OUT0 voltage is pulled up from the ground voltage to $V_{LED} – V_F$. The charge current (I_{CHRG}) flows to the parasitic capacitor (C0) through LED1-0, causing the LED to briefly turn on and creating a ghosting effect of LED1-0.

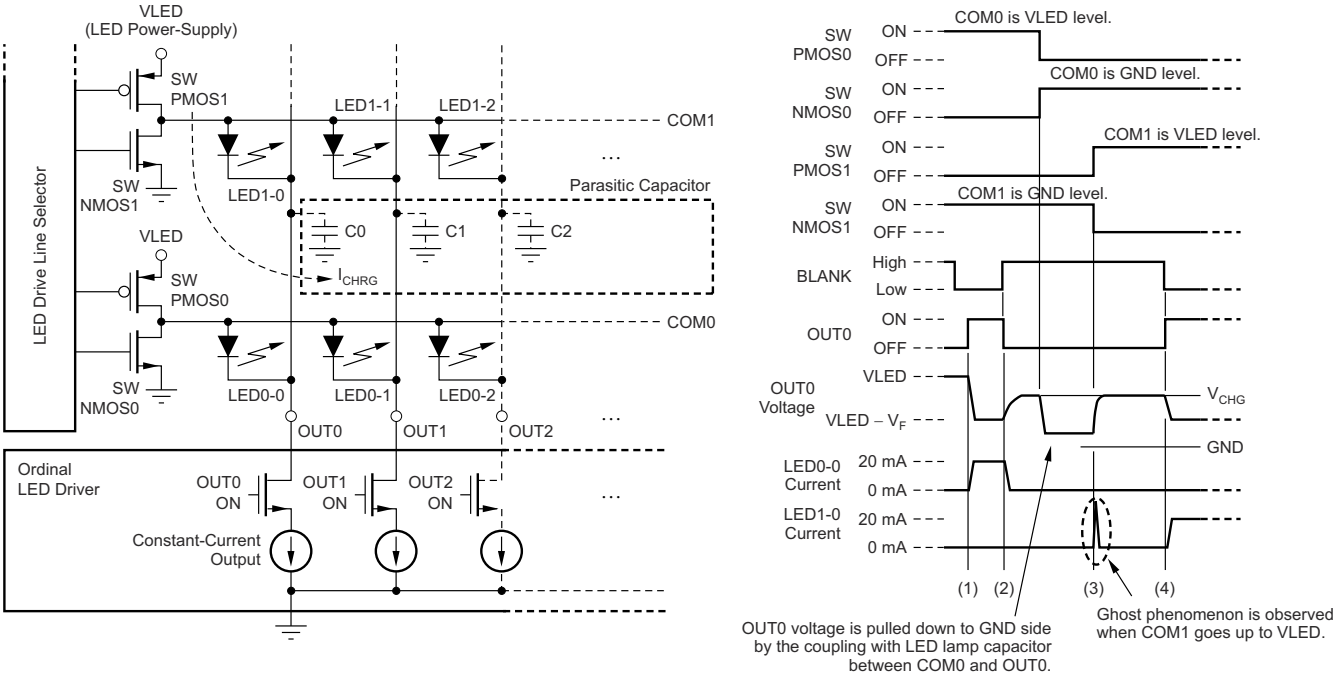


Figure 7-1. LED Ghost-Lighting Phenomenon Mechanism

The TLC59283 has an internal pre-charge FET to prevent ghosting, as shown in Figure 7-2. When a small delay after PWM control for a single common line completes, the FET pulls OUT*n* up to V_{CC}. The charge current does not flow to C0 through LED1-0 when SWMOS1 is turned on and the ghosting is eliminated at (3). However, depending on the LED anode voltage, the number of LEDs in series, the LED forward voltage, and the TLC59283 V_{CC} supply voltage, there may not be a great enough ghost-canceling effect.

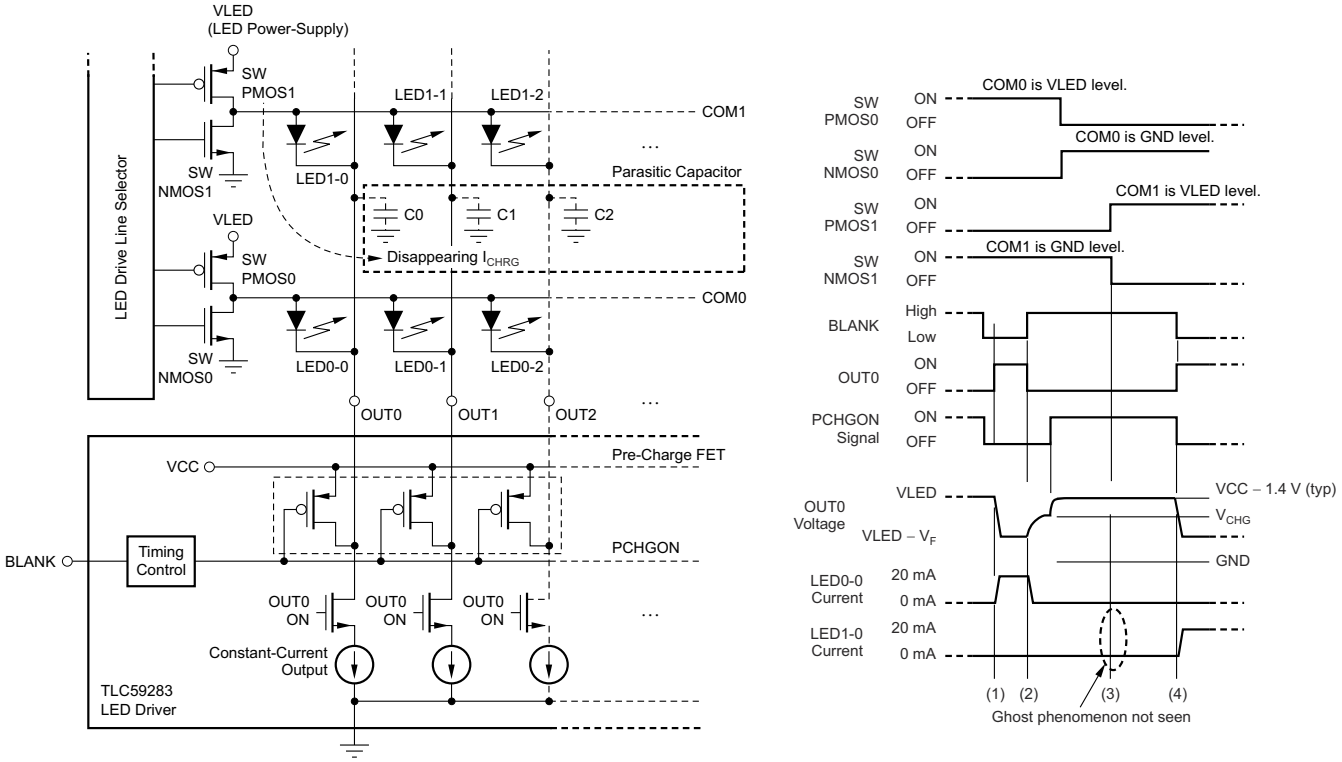


Figure 7-2. LED Ghost-lighting Mechanism by Pre-charge FET

7.3.3.2 Improve Output Control Loop Stability

Large parasitic inductances associated with the outputs of the TLC59283 have the potential of causing current loop instability that can manifest as spurious oscillations. Those parasitic inductances are most commonly associated with long traces or with the use of connectors between boards. The Application Note Improve TLC59283 Control Loop Stability for Appliance Application (SLVAFP4) describes how to minimize instability by compensating the feedback loop with small RC circuits.

8 Register Configuration

The TLC59283 has a 16-bit shift register and an output on or off data latch. Both the shift register and data latch are 16 bits long and are used to turn the constant-current outputs on and off. Figure 8-1 shows the shift register and data latch configuration. The data at the SIN pin are shifted into the 16-bit shift register LSB at the rising edge of the SCLK pin; SOUT data change at the SCLK rising edge.

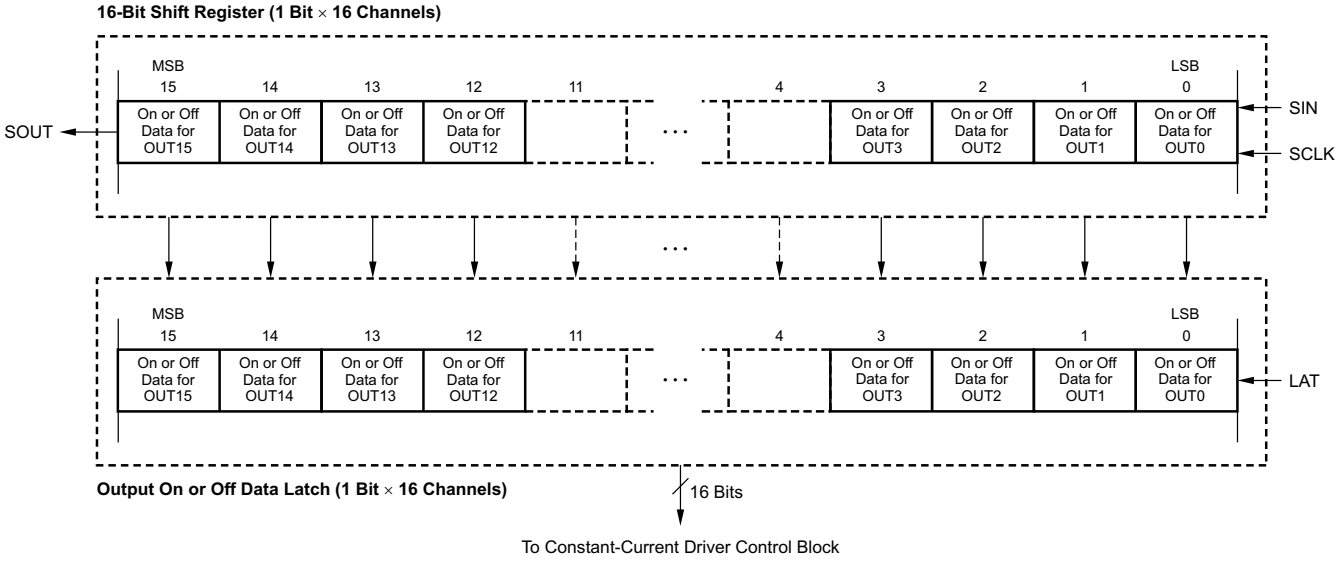


Figure 8-1. 16-Bit Shift Register and Output On or Off Data Latch Configuration

The output on or off data in the 16-bit shift register continue to transfer to the output on or off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. When the device initially powers on, the data in the output on or off shift register and latch are not set to default values; on or off control data must be written to the on or off control data latch before turning the constant-current output on. All constant-current outputs are forced off when BLANK is high. The OUT*n* on or off outputs are controlled by the data in the output on or off data latch. The writing data truth table and timing diagram are shown in Table 8-1 and Figure 8-2, respectively.

Table 8-1. Truth Table in Operation

SCLK	LAT	BLANK	SIN	OUT0…OUT7…OUT15	SOUT
↑	High	Low	Dn	Dn…Dn – 7…Dn – 15	Dn – 15
↑	Low	Low	Dn + 1	No change	Dn – 14
↑	High	Low	Dn + 2	Dn + 2…Dn – 5…Dn – 13	Dn – 13
↓	—	Low	Dn + 3	Dn + 2…Dn – 5…Dn – 13	Dn – 13
↓	—	High	Dn + 3	Off	Dn – 13

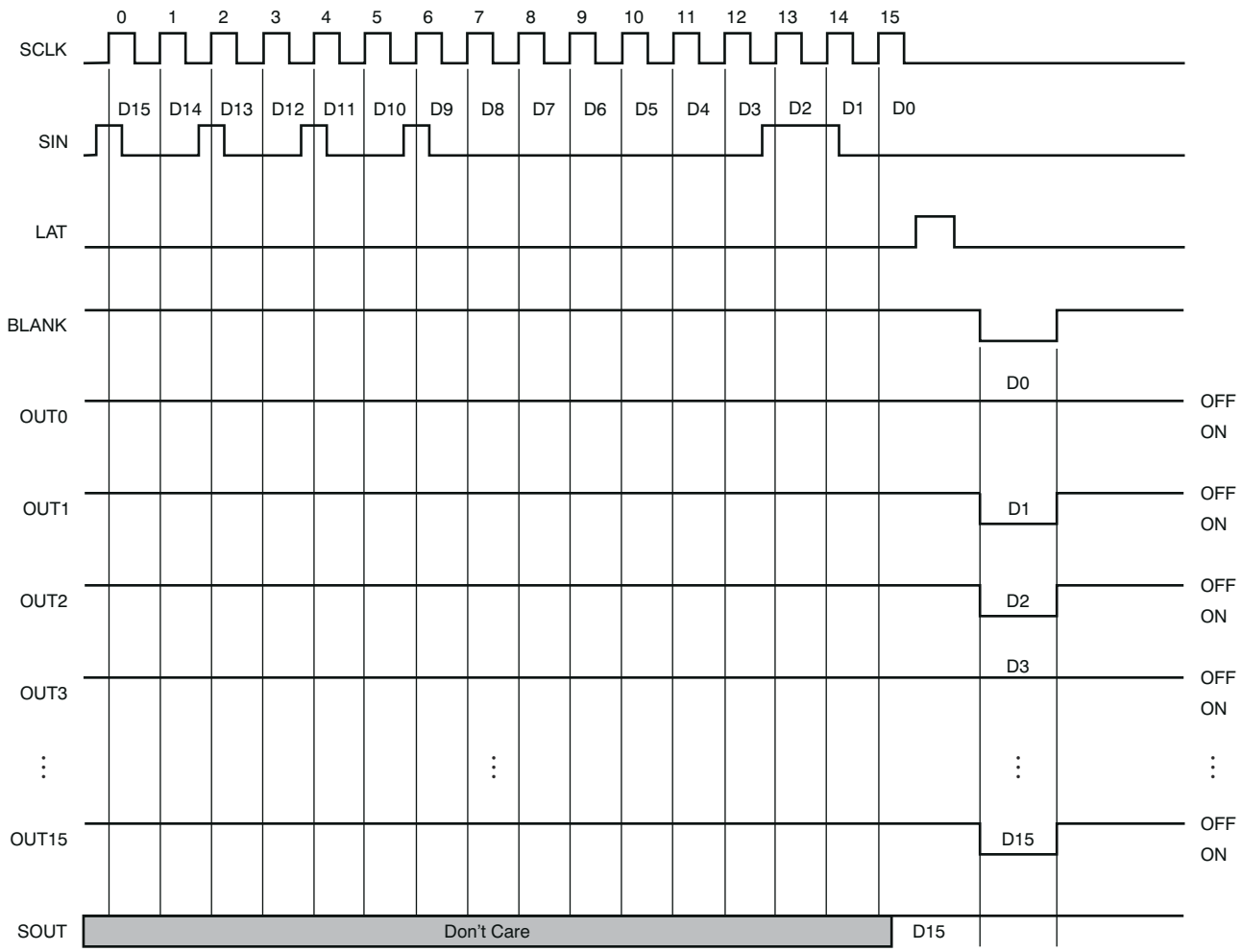


Figure 8-2. Operation Timing Diagram

9 Application and Implementation

Note

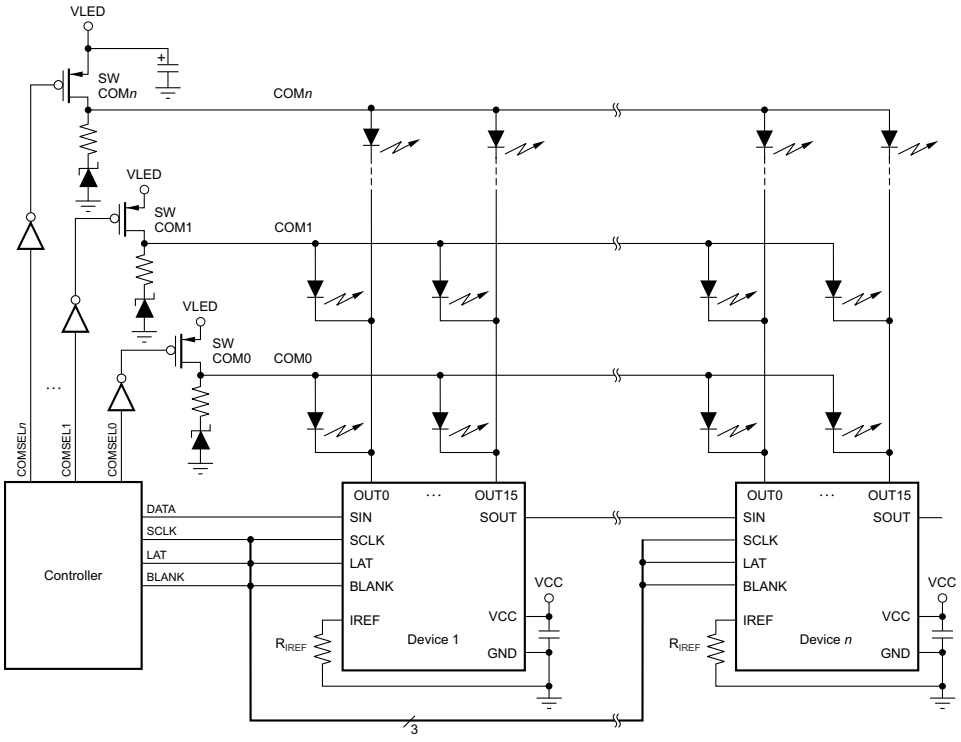
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

With the blossoming of AI (Artificial Intelligence) and IoT (Internet of Things), more and more end equipments use larger quantities of LEDs to show different statuses or functions. From the HMI (Human Machine Interface) perspective, LED indication, including LED-based seven-segment, dot-matrix displays, and a large quantity of LED indicators are bringing new dimensions of versatility and eye-pleasing visual effects to a growing number of applications. This application report showcases how to use the TLC59283 to drive seven-segment, dot-matrix displays or a large quantity of LEDs with the advantages of better brightness uniformity, smaller size, and ghosting elimination over current solutions. For additional details see Use TLC59283 for LED Indication with Better Brightness Uniformity, Smaller Size, and Ghosting Elimination

9.2 Typical Application

Typical Application Circuit (Multiple Daisy-Chained TLC59283s) shows the typical application schematic for the TLC59283.



Typical Application Circuit (Multiple Daisy-Chained TLC59283s)

9.2.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Supply Voltage	3~5.5V
Output Voltage	<10V
Output Current	<45mA
Dimming Option	No dimming option

9.2.2 Detailed Design Procedure

This section show how to use the TLC59283 to drive the LED matrix using time-multiplexing topology. To form a time-multiplexing topology, it is necessary to add external switching MOSFETs or transistors. If there is enough I/Os in the system to control the transistors, a block diagram like Figure 8-1 can be used to drive 64 LEDs.

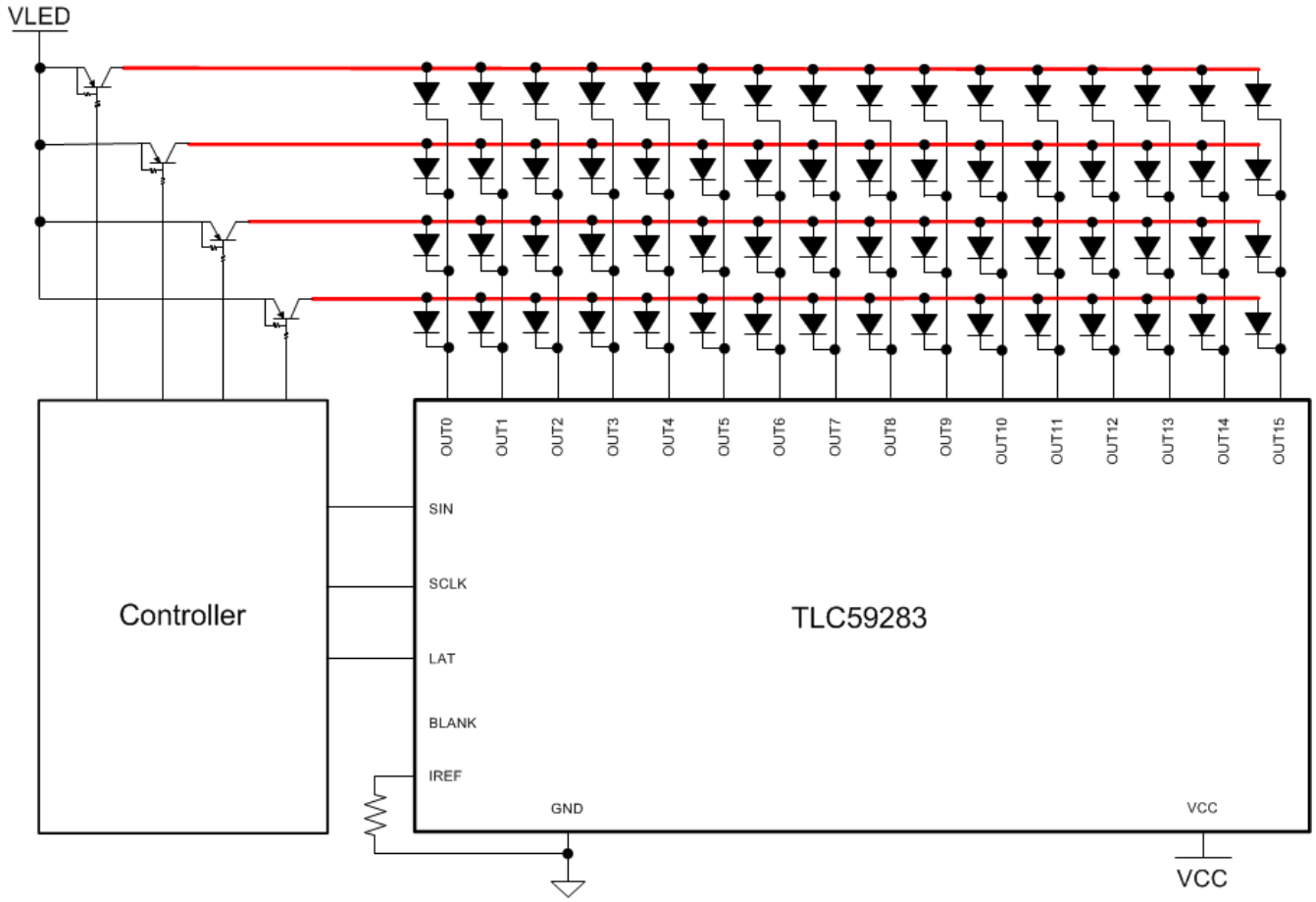


Figure 9-1. Time-multiplexing Circuit Using TLC59283 and Enough I/Os

If there are not enough I/Os in the system to control the transistors, a block diagram like Figure 8-2 can be used to drive 64 LEDs.

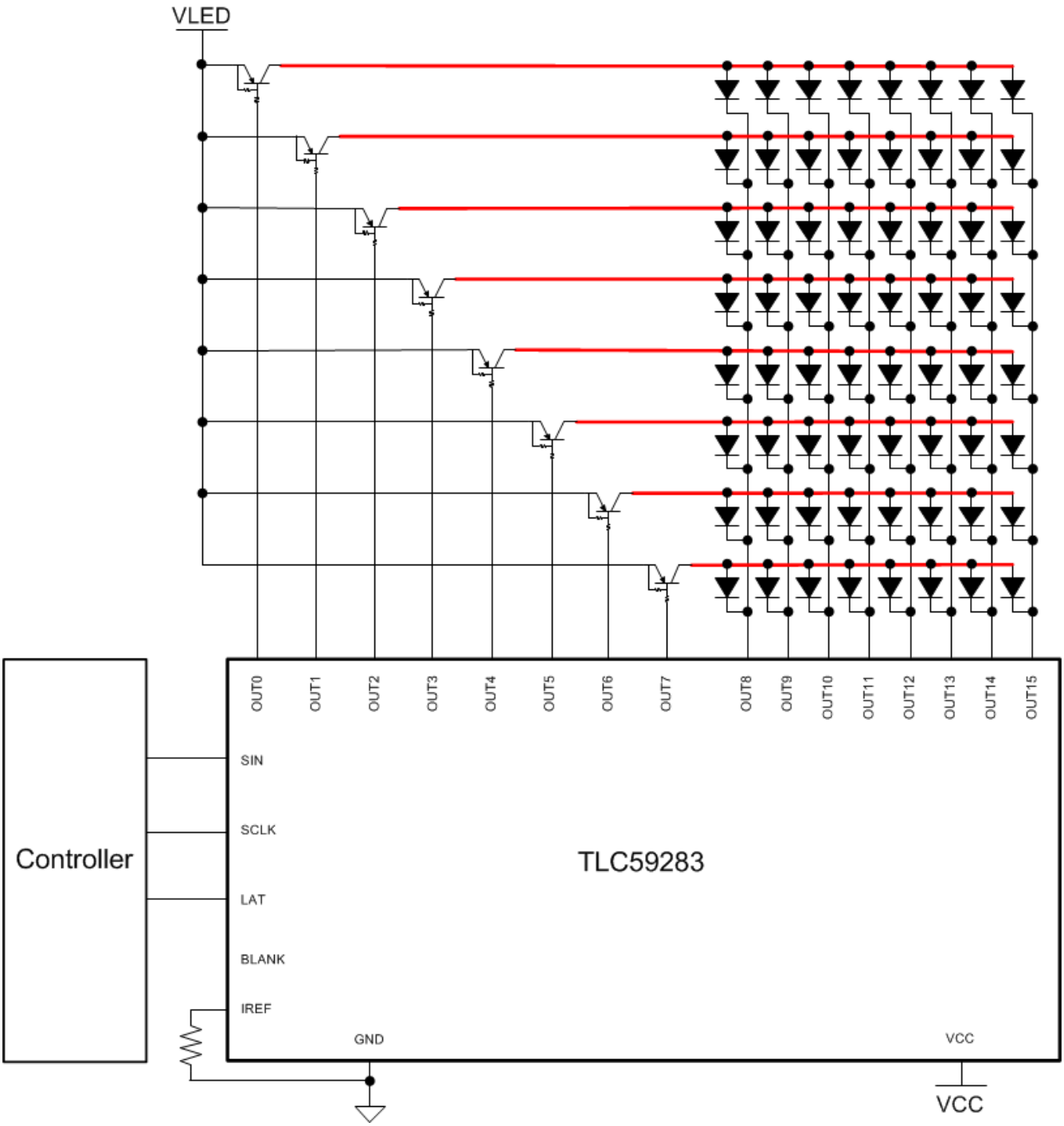


Figure 9-2. Time-multiplexing Circuit Using TLC59283 and Less I/Os

9.2.3 Application Performance Plots

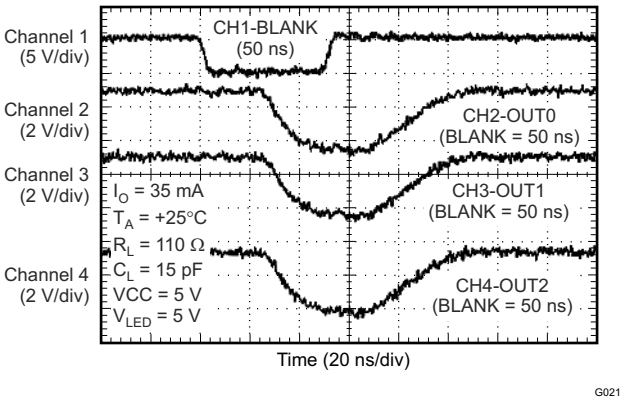


Figure 9-3. Constant-current Output Voltage Waveform

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3V to 5.5V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance is required near to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 1μF.

9.4 Layout

9.4.1 Layout Guidelines

The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple. For OUTx, path outputs must be short and wide and avoid parallel wiring and narrow trace. For better thermal performance, TI suggest to make copper polygon connected with each pin bigger.

9.4.2 Layout Example

One TLC59283 can drive up to 16 LEDs directly, so it can replace two 74HC595 and the current limit resistors if driving two seven segment displays. The below figure makes a simple comparison and the PCB size is 65% smaller using the TLC59283. If you are using the QFN package, the size is even smaller.

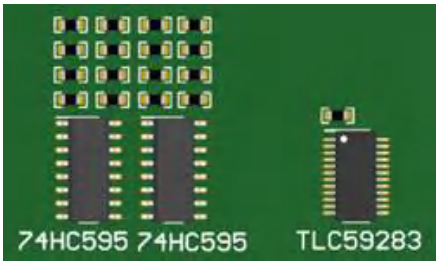


Figure 9-4. TLC59283 Layout Example

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Documentation Support

10.2.1 Related Documentation

- TLC59282 Evaluation Module
- Use TLC59283 for LED Indication with Better Brightness Uniformity, Smaller Size, and Ghosting Elimination
- Improve TLC59283 Control Loop Stability for Appliance Application

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2012) to Revision C (January 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added Improve TLC59283 Control Loop Stability for Appliance Application (SLVAFP4) .pdf link	18

Changes from Revision A (June 2012) to Revision B (October 2012)	Page
• Changed HBM ESD rating maximum specification in the Absolute Maximum Ratings table	5
• Changed I_{CC2} typical and maximum specifications in Electrical Characteristics table	7
• Changed I_{CC3} typical specification in Electrical Characteristics table	7

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC59283DBQ	Active	Production	SSOP (DBQ) | 24	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59283
TLC59283DBQ.A	Active	Production	SSOP (DBQ) | 24	50 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59283
TLC59283DBQR	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59283
TLC59283DBQR.A	Active	Production	SSOP (DBQ) | 24	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59283
TLC59283RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 59283
TLC59283RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 59283
TLC59283RGER.B	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 59283
TLC59283RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 59283
TLC59283RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC 59283

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

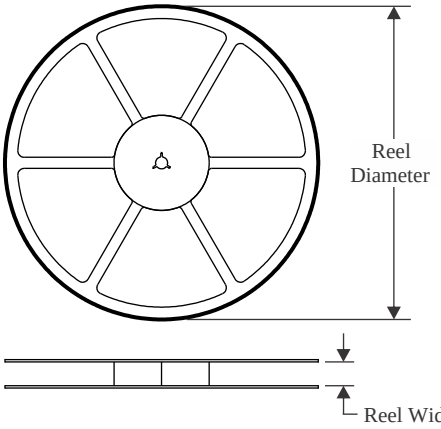
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

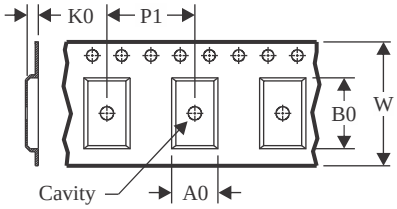
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

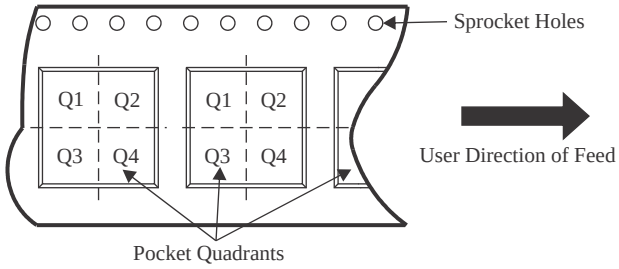


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

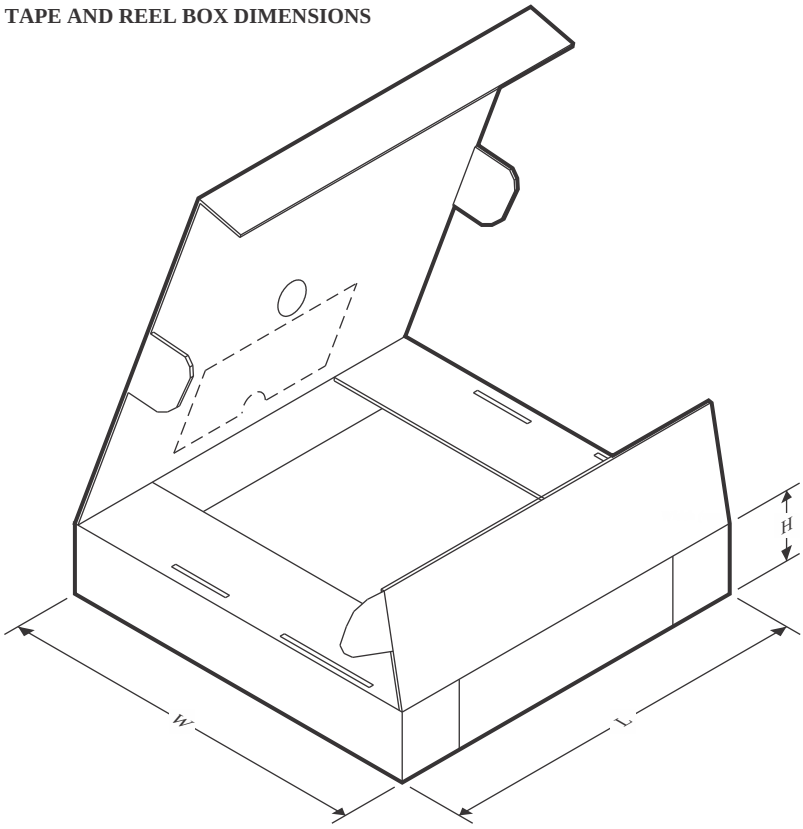
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59283DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC59283RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC59283RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

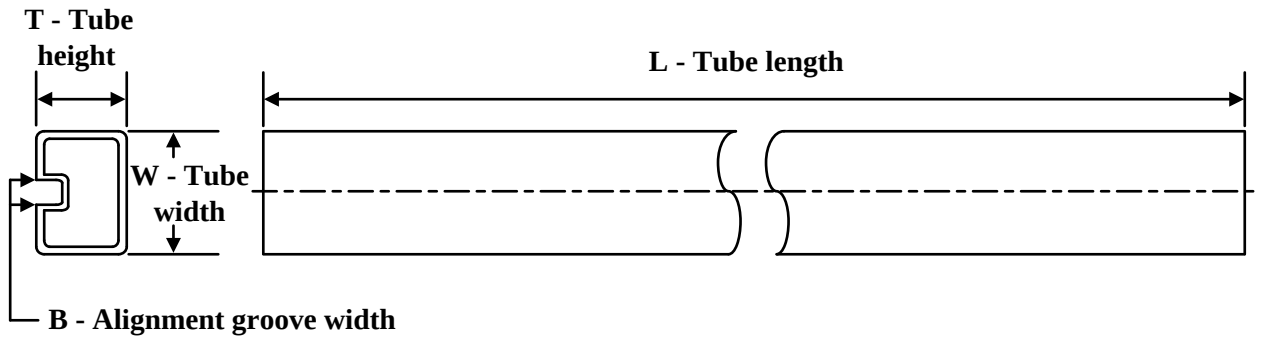
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59283DBQR	SSOP	DBQ	24	2500	353.0	353.0	32.0
TLC59283RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TLC59283RGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE



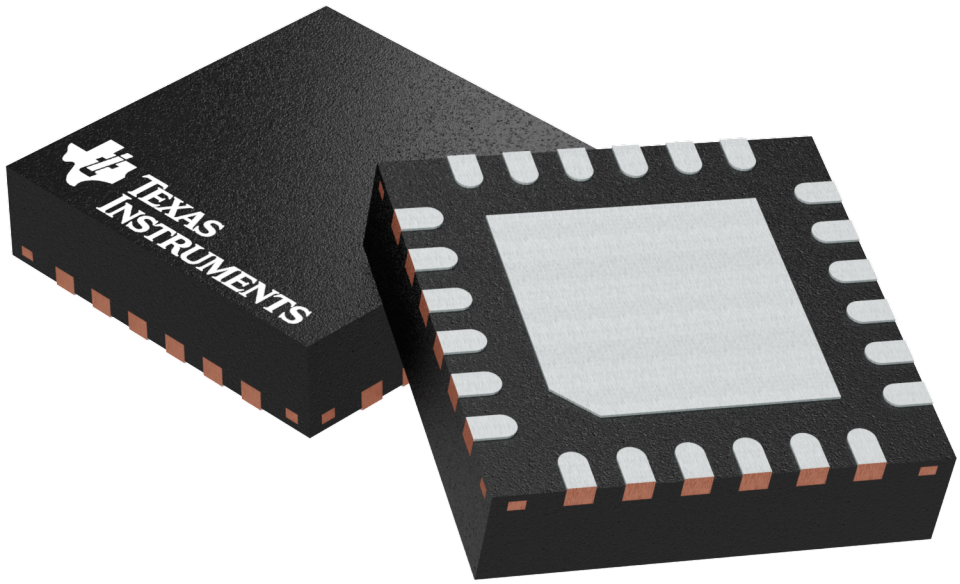
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC59283DBQ	DBQ	SSOP	24	50	506.6	8	3940	4.32
TLC59283DBQ.A	DBQ	SSOP	24	50	506.6	8	3940	4.32

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

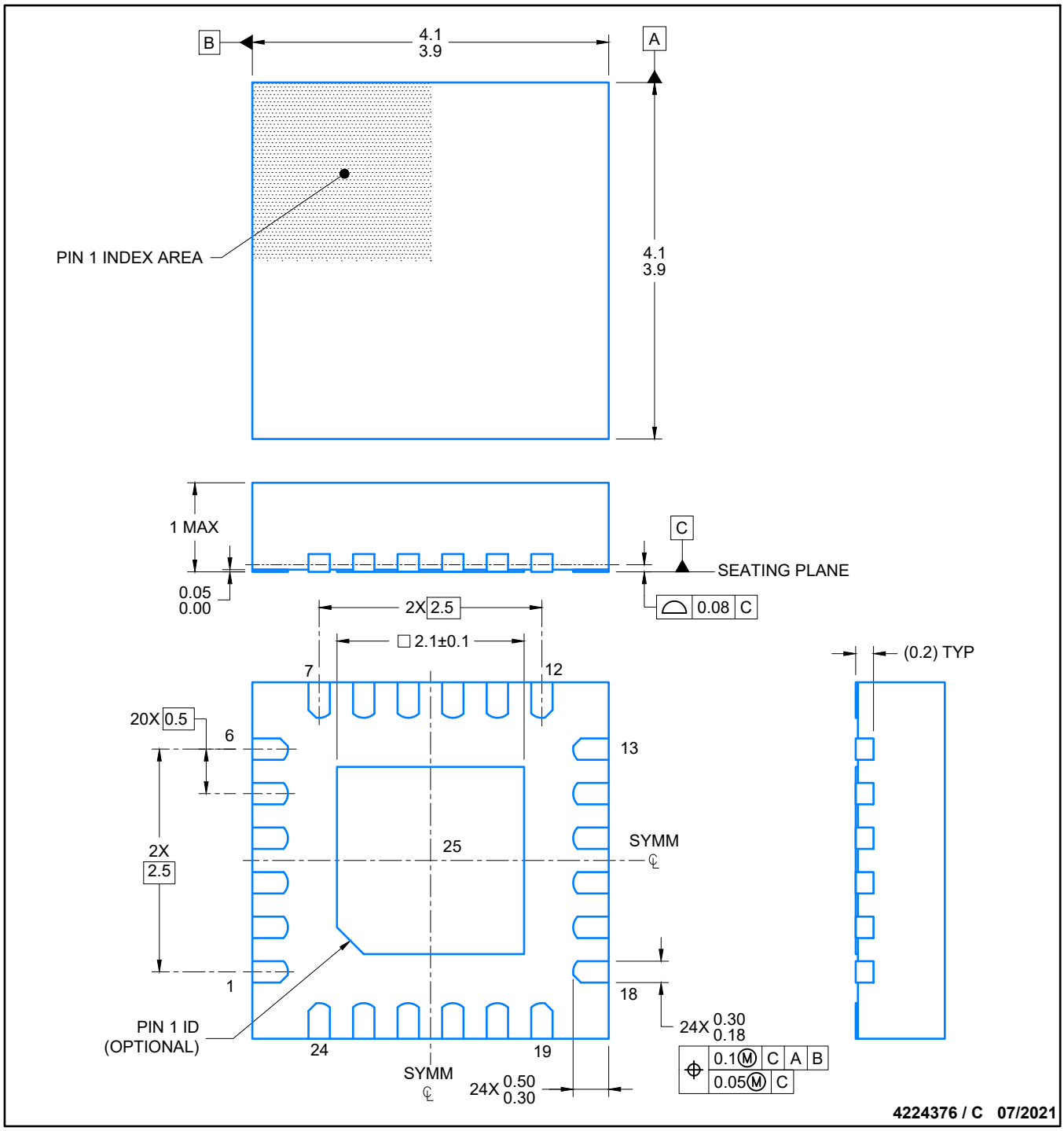
4204104/H

PACKAGE OUTLINE

RGE0024C

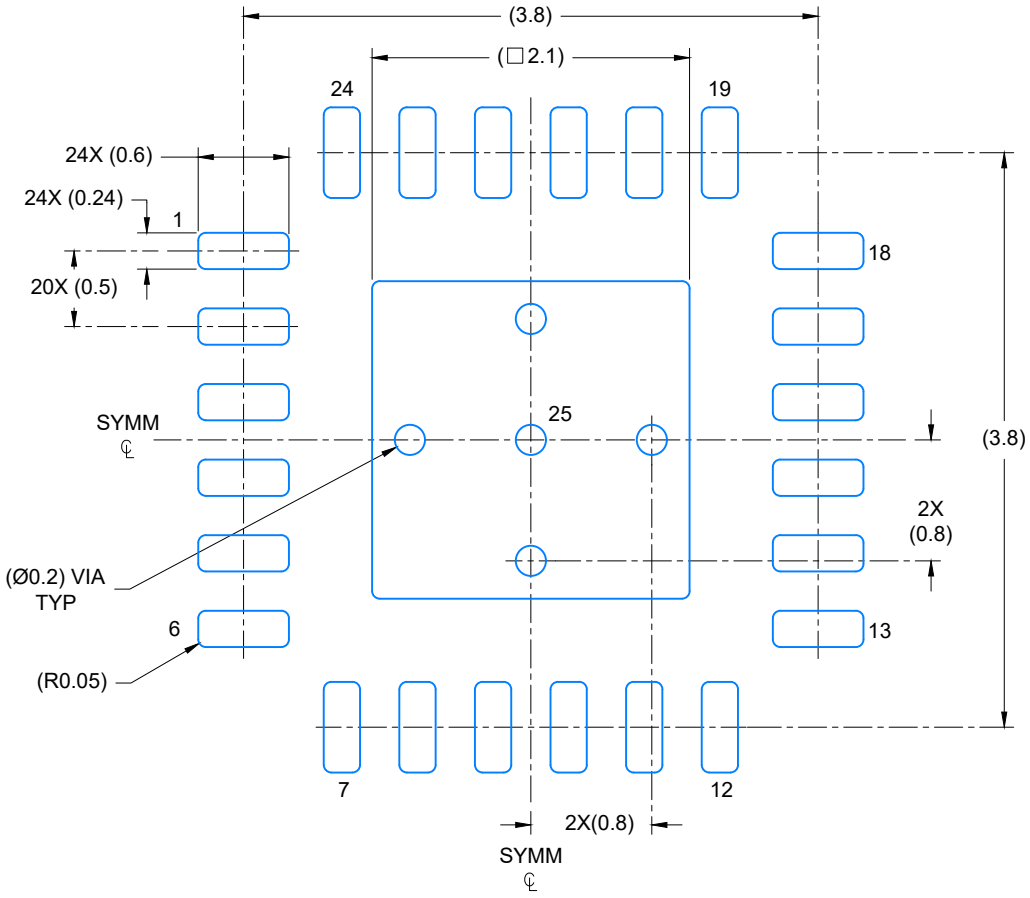
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



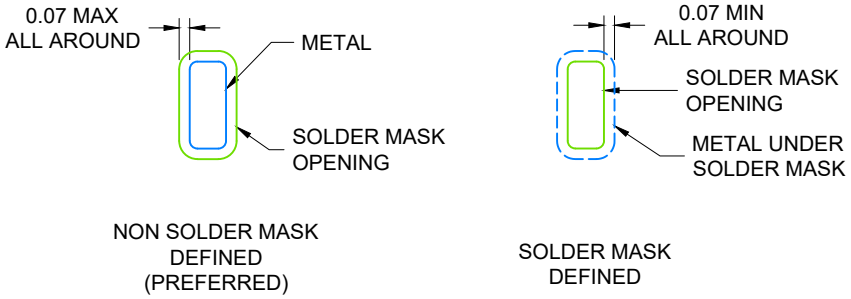
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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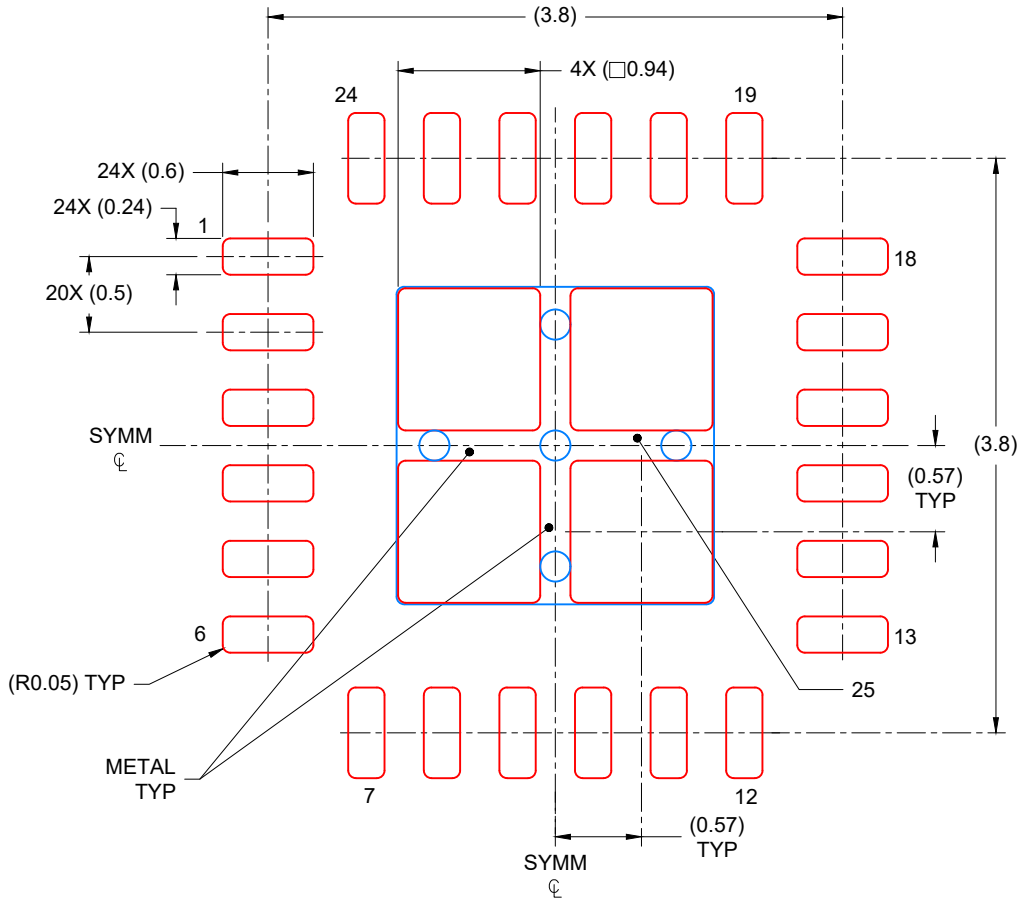
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

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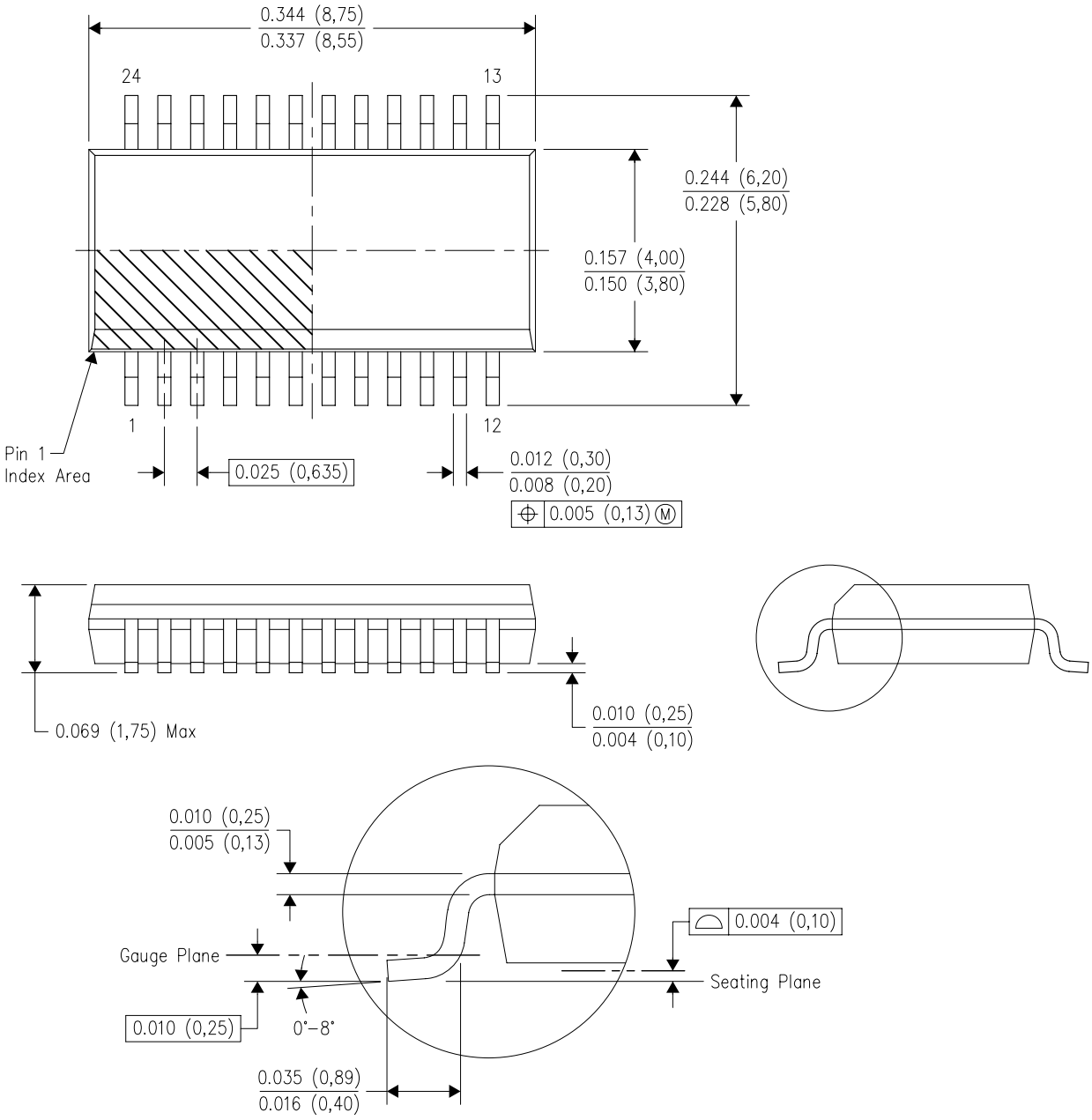
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

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