TLC59116F 16-Channel Fast-Mode Plus I²C Bus LED Driver

1 Features

- 16 LED Drivers (Each Output Programmable at OFF, ON, LED Brightness, and Group Dimming/Blinking Mixed With Individual LED Brightness)
- 16 Open-Drain Output Channels
- 256-Step (8-Bit) Linear Programmable Brightness Per LED Output Varying From Fully OFF (Default) to Maximum Brightness Using a 97-kHz PWM Signal
- 256-Step Group Brightness Control Allows General Dimming (Using a 190-Hz PWM Signal From Fully OFF to Maximum Brightness (Default)
- 256-Step Group Blinking With Frequency Programmable From 24 Hz to 10.73 s and Duty Cycle from 0% to 99.6%
- Four Hardware Address Pins Allow 14 TLC59116F Devices to be Connected to the Same I²C Bus
- Four Software-Programmable I²C Bus Addresses (One LED Group Call Address and Three LED Sub-Call Addresses) Allow Groups of Devices to be Addressed Simultaneously in Any Combination (For example, One Register Used for 'All Call' So All the TLC59116Fs on the I²C Bus Can be Addressed at the Same Time and the Second Register Used for Three Different Addresses So That 1/3 of all Devices on the Bus Can Be Addressed at the Same Time in a Group). Software Enable and Disable for I²C Bus Address.
- Software Reset Feature (SWRST Call) Allows the Device to be Reset Through the I²C Bus
- Up to 14 Possible Hardware Adjustable Individual I²C Bus Addresses Per Device so That Each Device Can be Programmed
- Output State Change Programmable on the Acknowledge or the STOP Command to Update Outputs Byte-by-Byte or All at the Same Time (Default to *Change on STOP*).
- 120-mA Maximum Output Current
- 17-V Maximum Output Voltage
- 25-MHz Internal Oscillator Requires No External Components
- 1-MHz Fast-Mode Plus (FM+) Compatible I²C Bus Interface With 30 mA High Drive Capability on SDA Output for Driving High Capacity Buses
- Internal Power-On Reset
- Noise Filter on SCL/SDA Inputs
- No Glitch on Power Up
- Active-Low Reset
- Supports Hot Insertion
- Low Standby Current
- 3.3-V or 5-V Supply Voltage
- 5.5-V Tolerant Inputs
- 28-Pin TSSOP (PW)
- –40°C to 85°C Operation

2 Applications

- Gaming
- Small Signage
- Industrial Equipment

3 Description

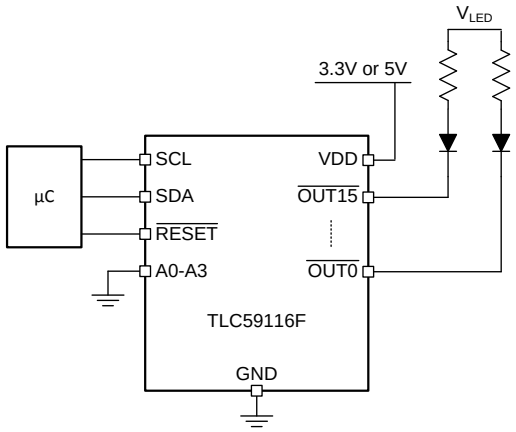
The TLC59116F is an I²C-bus controlled 16-channel LED driver optimized for red/green/blue/amber (RGBA) color mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0% to 99.6% to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0% to 99.6% that is used to either dim or blink all LEDs with the same value.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC59116F	TSSOP (28)	9.70 mm × 4.40 mm
	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2011) to Revision C — **Page**

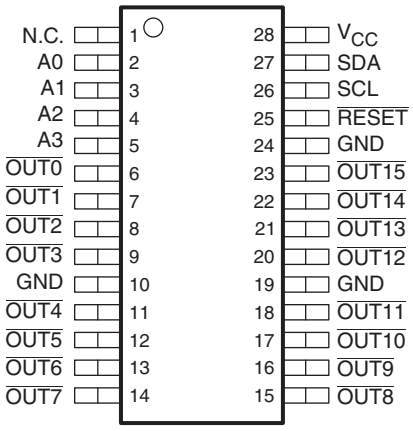
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Removed Thermal Impedence table from Specifications ... 5
- Added Figure 1 and Figure 2 to *Typical Characteristics* ... 6
- Removed Figure 9 from *Control Register* ... 16
- Added Figure 22 and Figure 23 to *Layout Examples* ... 26

Changes from Revision A (June 2010) to Revision B — **Page**

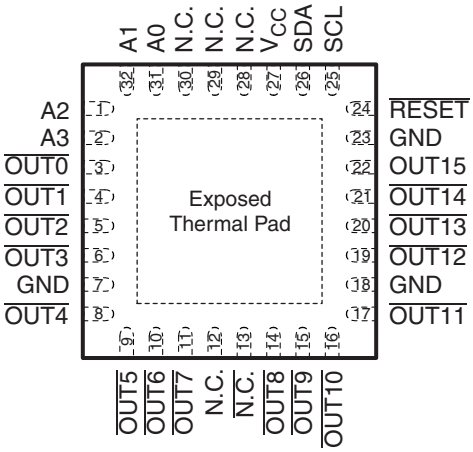
- Changed QFN PIN NO. to fix pin assignment typo. ... 3

5 Pin Configuration and Functions

PW Package
28-Pin TSSOP
Top View



RHB Package
32-Pin VQFN
Top View



If used, the exposed thermal pad must be connected as a secondary ground.

N.C. – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	QFN (RHB)	TSSOP (PW)		
A0	31	2	I	Address input 0
A1	32	3	I	Address input 1
A2	1	4	I	Address input 2
A3	2	5	I	Address input 3
GND	7, 18, 23	10, 19, 24	–	Power ground
N.C.	12, 13, 28, 29, 30	1	–	No internal connection
$\overline{OUT0}$	3–6	6–9	O	Open-drain output 0 to 3, LED ON at low
$\overline{OUT1}$				
$\overline{OUT2}$				
$\overline{OUT3}$				
$\overline{OUT4}$	8–11	11–14	O	Open-drain output 4 to 7, LED ON at low
$\overline{OUT5}$				
$\overline{OUT6}$				
$\overline{OUT7}$				
$\overline{OUT8}$	14–17	15–18	O	Open-drain output 8 to 11, LED ON at low
$\overline{OUT9}$				
$\overline{OUT10}$				
$\overline{OUT11}$				
$\overline{OUT12}$	19–22	20–23	O	Open-drain output 12 to 15, LED ON at low
$\overline{OUT13}$				
$\overline{OUT14}$				
$\overline{OUT15}$				
$\overline{RESET}$	24	25	I	Active-low reset input
SCL	25	26	I	Serial clock input
SDA	26	27	I/O	Serial data input/output
V_{CC}	27	28	–	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (see (1))

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0	7	V
V_I	Input voltage		–0.4	7	V
V_O	Output voltage		–0.5	20	V
I_O	Continuous output current per channel			120	mA
P_D	Power dissipation (T_A = 25°C, JESD 51-7)	PW package		1.6	W
T_J	Junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (see (1))

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA, $\overline{RESET}$, A0, A1, A2, A3		V_{CC} × 0.7	V_{CC}	V
V_{IL}	Low-level input voltage	SCL, SDA, $\overline{RESET}$, A0, A1, A2, A3		0	V_{CC} × 0.3	V
V_O	Output voltage	$\overline{OUT0}$–$\overline{OUT15}$			17	V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V		20	mA
			V_{CC} = 5 V		30	
I_O	Output current per channel	$\overline{OUT0}$–$\overline{OUT15}$			120	mA
T_A	Operating free-air temperature			–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

6.4 Thermal Information

THERMAL METRIC (1)		TLC59116F		UNIT
		PW (TSSOP)	RHB (VQFN)	
		28 PINS	32 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78	34.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.8	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36	8.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.5	8.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 3 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
I_L	Input/output leakage current	SCL, SDA, A0, A1, A2, A3, $\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND			±0.3	µA
	Output leakage current	$\overline{\text{OUT0}}$–$\overline{\text{OUT15}}$	V_O = 17 V, T_J = 25°C			0.5	µA
V_{POR}	Power-on reset voltage				2.5		V
I_{OL}	Low-level output current	SDA	V_{CC} = 3 V, V_{OL} = 0.4 V	20			mA
			V_{CC} = 5 V, V_{OL} = 0.4 V	30			
V_{OL}	Low-level output voltage	$\overline{\text{OUT0}}$–$\overline{\text{OUT15}}$	V_{CC} = 3 V, I_{OL} = 120 mA		200	450	mV
			V_{CC} = 4.5 V, I_{OL} = 120 mA		175	400	
r_{ON}	On resistance	$\overline{\text{OUT0}}$–$\overline{\text{OUT15}}$	V_{CC} = 3 V, I_{OL} = 120 mA		1.67	3.75	Ω
			V_{CC} = 4.5 V, I_{OL} = 120 mA		1.46	3.3	
T_{SD}	Overtemperature shutdown (2)			150	175	200	°C
T_{HYS}	Restart hysteresis				15		°C
C_i	Input capacitance	SCL, A0, A1, A2, A3, $\overline{\text{RESET}}$	$V_I = V_{CC}$ or GND		5		pF
C_{io}	Input/output capacitance	SDA	$V_I = V_{CC}$ or GND		8		pF
I_{CC}	Supply current	$\overline{\text{OUT0}}$–$\overline{\text{OUT15}}$ = OFF	V_{CC} = 5.5 V			13	mA

(1) All typical values are at T_J = 25°C.
(2) Specified by design; not production tested.

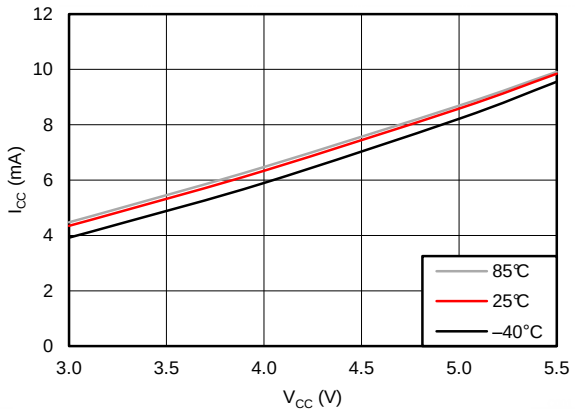
6.6 I²C Interface Bus Timing Requirements

T_A = –40°C to 85°C

PARAMETER		STANDARD-MODE I²C BUS		FAST-MODE I²C BUS		FAST-MODE PLUS I²C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
I²C Interface								
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7		1.3		0.5		µs
$t_{HD;STA}$	Hold time (repeated) START condition	4		0.6		0.26		µs
$t_{SU;STA}$	Set-up time for a (repeated) START condition	1.7		0.6		0.26		µs
$t_{SU;STO}$	Set-up time for STOP condition	4		0.6		0.26		µs
$t_{HD;DAT}$	Data hold time	0		0		0		ns
$t_{VD;ACK}$	Data valid acknowledge time (1)	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	Data valid time (2)	0.3	3.45	0.1	0.9	0.05	0.45	µs
$t_{SU;DAT}$	Data set-up time	250		100		50		ns
t_{LOW}	Low period of the SCL clock	4.7		1.3		0.5		µs
t_{HIGH}	High period of the SCL clock	4		0.6		0.26		µs
t_f	Fall times of both SDA and SCL signals (3) (4)		300	20 + 0.1C_b (5)	300		120	ns
t_r	Rise time of both SDA and SCL signals		1000	20 + 0.1C_b (5)	300		120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter (6)		50		50		50	ns
Reset								
t_W	Reset pulse width	10		10		10		ns
t_{REC}	Reset recovery time	0		0		0		ns
t_{RESET}	Time to reset (7) (8)	400		400		400		ns

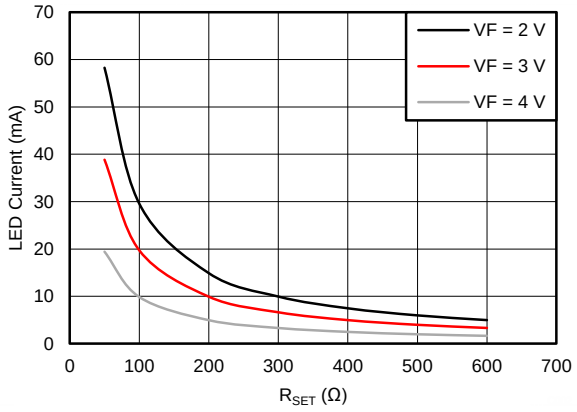
(1) $t_{VD;ACK}$ = time for acknowledgment signal from SCL low to SDA (out) low.
(2) $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL low.
(3) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
(4) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time (t_f) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(5) C_b = total capacitance of one bus line in pF.
(6) Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.
(7) Resetting the device while actively communicating on the bus may cause glitches or errant STOP conditions.
(8) Upon reset, the full delay will be the sum of t_{RESET} and the RC time constant of the SDA bus.

6.7 Typical Characteristics



All LEDs on Duty Cycle = 100%

Figure 1. I_{CC} vs V_{CC} with LEDs On



All LEDs off

Figure 2. I_{CC} vs V_{CC} with LEDs Off

7 Parameter Measurement Information

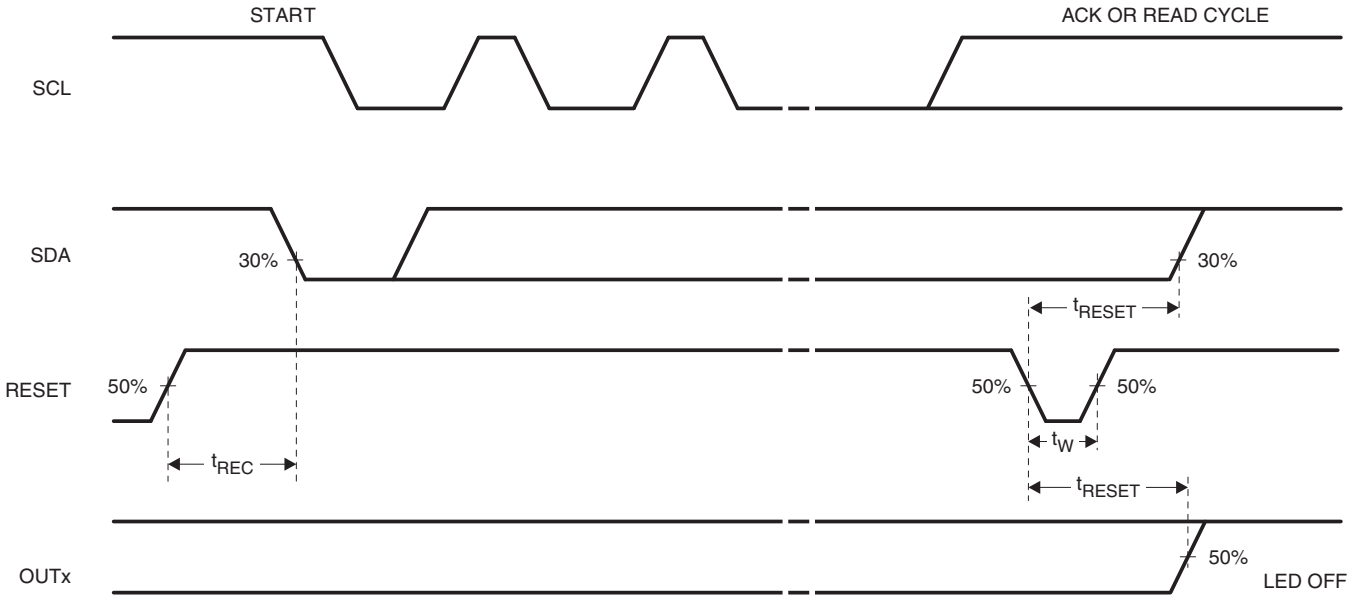


Figure 3. Definition of RESET Timing

Parameter Measurement Information (continued)

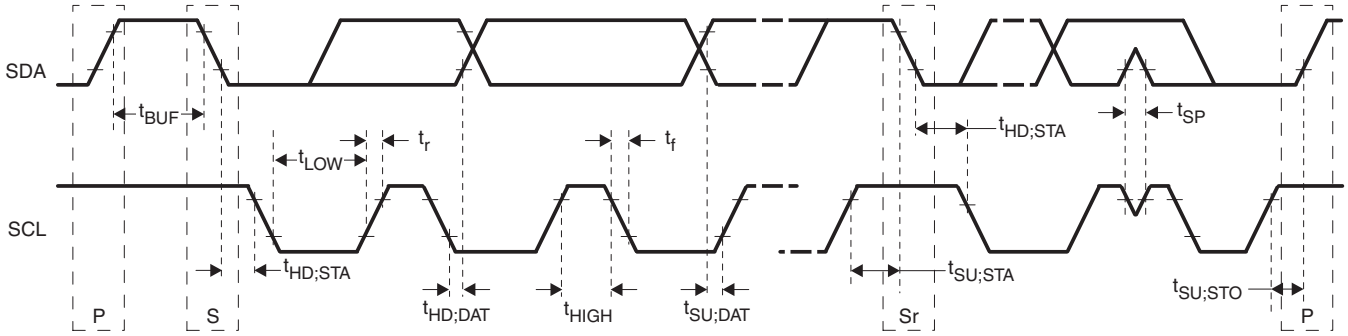
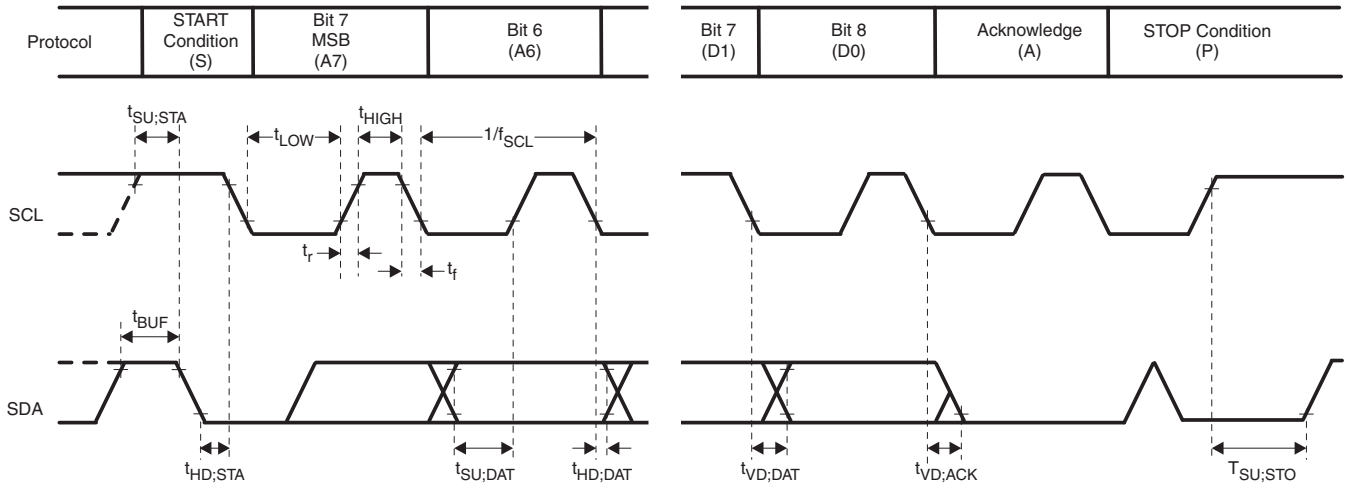
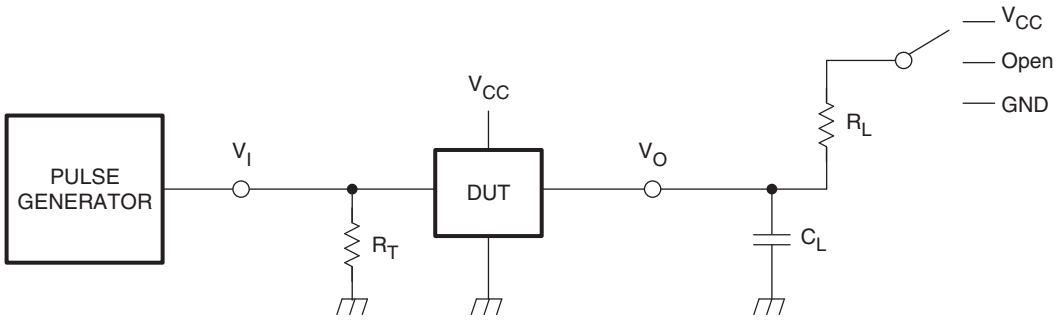


Figure 4. Definition of Timing



A. Rise and fall times refer to V_{IL} and V_{IH}.

Figure 5. I²C Bus Timing



A. Load resistor, R_L, for SDA and SCL > 1 kΩ (3 mA or less current)

B. Load capacitance, C_L, includes jig and probe capacitance

C. Termination resistance, R_T, should be equal to the output impedance Z_O of the pulse generators.

Figure 6. Test Circuit for Switching Characteristics

8 Detailed Description

8.1 Overview

The TLC59116F is an I²C-bus controlled 16-channel LED driver optimized for red/green/blue/amber (RGBA) color mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0% to 99.6% to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0% to 99.6% that is used to either dim or blink all LEDs with the same value.

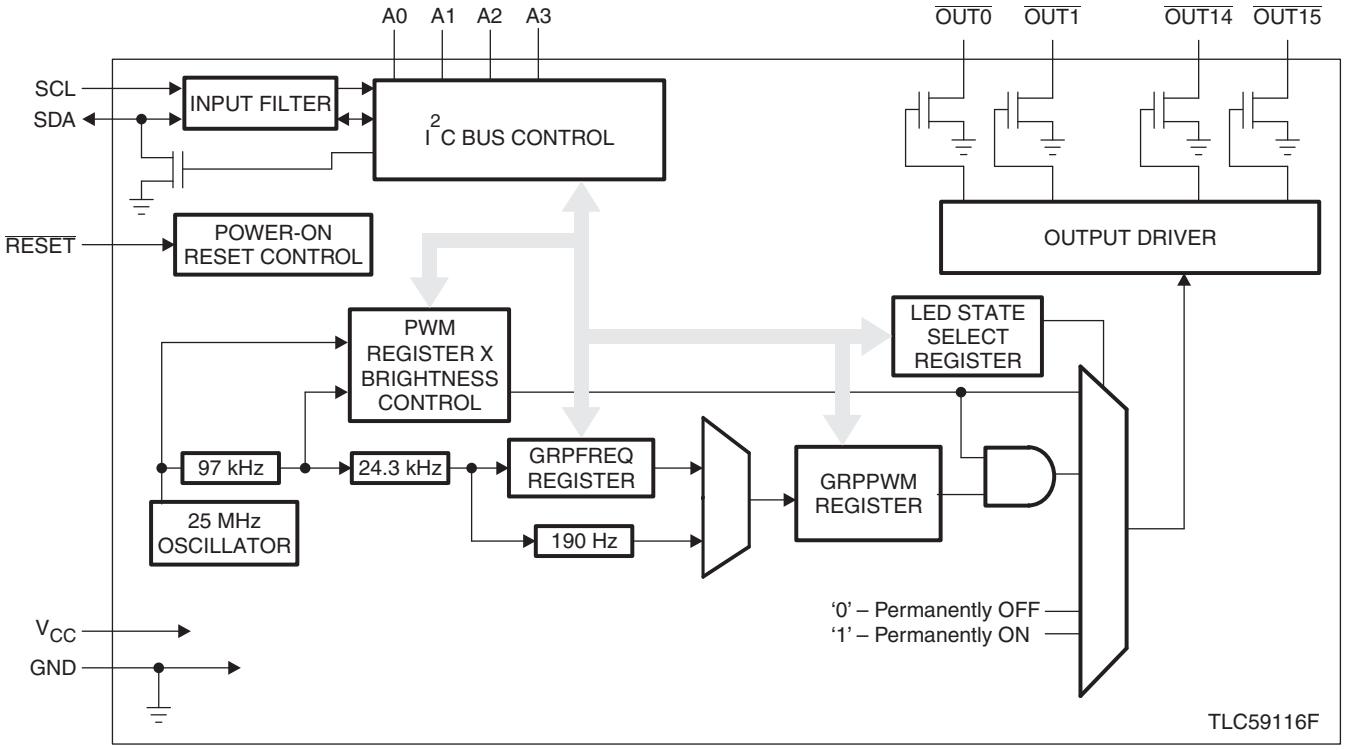
Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The TLC59116F operates with a supply voltage range of 3 V to 5.5 V and the outputs are 17-V tolerant. LEDs can be directly connected to the TLC59116F device outputs.

Software programmable LED group and three sub call I²C bus addresses allow all or defined groups of TLC59116F devices to respond to a common I²C bus address, which allows, for example, all the same color LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I²C bus commands.

Four hardware address pins allow up to 14 devices on the same bus.

The software reset (SWRST) call allows the master to perform a reset of the TLC59116F through the I²C bus, identical to the power-on reset (POR) that initializes the registers to their default state causing the outputs to be set high (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

8.2 Functional Block Diagram



Only one PWM shown for clarity.

8.3 Feature Description

8.3.1 Power-On Reset (POR)

When power is applied to V_{CC}, an internal power-on reset holds the TLC59116F in a reset condition until V_{CC} reaches V_{POR}. At this point, the reset condition is released and the TLC59116F registers and I^2C bus state machine are initialized to their default states causing all the channels to be deselected. Thereafter, V_{CC} must be lowered below 0.2 V to reset the device.

8.3.2 External Reset

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TLC59116F registers and I^2C state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again high.

This input requires a pullup resistor to V_{CC} if no active connection is used.

8.3.3 Software Reset

The software reset call (SWRST Call) allows all the devices in the I^2C bus to be reset to the power-up state value through a specific formatted I^2C bus command. To be performed correctly, it implies that the I^2C bus is functional and that there is no device hanging the bus.

The SWRST Call function is defined as the following:

- A START command is sent by the I^2C bus master.
- The reserved SWRST I^2C bus address '1101 011' with the R/$\overline{W}$ bit set to '0' (write) is sent by the I^2C bus master.
- The TLC59116F device(s) acknowledge(s) after seeing the SWRST Call address '1101 0110' (D6h) only. If the R/$\overline{W}$ bit is set to '1' (read), no acknowledge is returned to the I^2C bus master.
- Once the SWRST Call address has been sent and acknowledged, the master sends 2 bytes with 2 specific values (SWRST data byte 1 and byte 2):
  a. Byte1 = A5h: the TLC59116F acknowledges this value only. If byte 1 is not equal to A5h, the TLC59116F does not acknowledge it.
  b. Byte 2 = 5Ah: the TLC59116F acknowledges this value only. If byte 2 is not equal to 5Ah, the TLC59116F does not acknowledge it.

  If more than 2 bytes of data are sent, the TLC59116F does not acknowledge any more.
- Once the right 2 bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a STOP command to end the SWRST Call: the TLC59116F then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time (t_{BUF}).

The I^2C bus master must interpret a non-acknowledge from the TLC59116F (at any time) as a *SWRST Call Abort*. The TLC59116F does not initiate a reset of its registers. This happens only when the format of the START Call sequence is not correct.

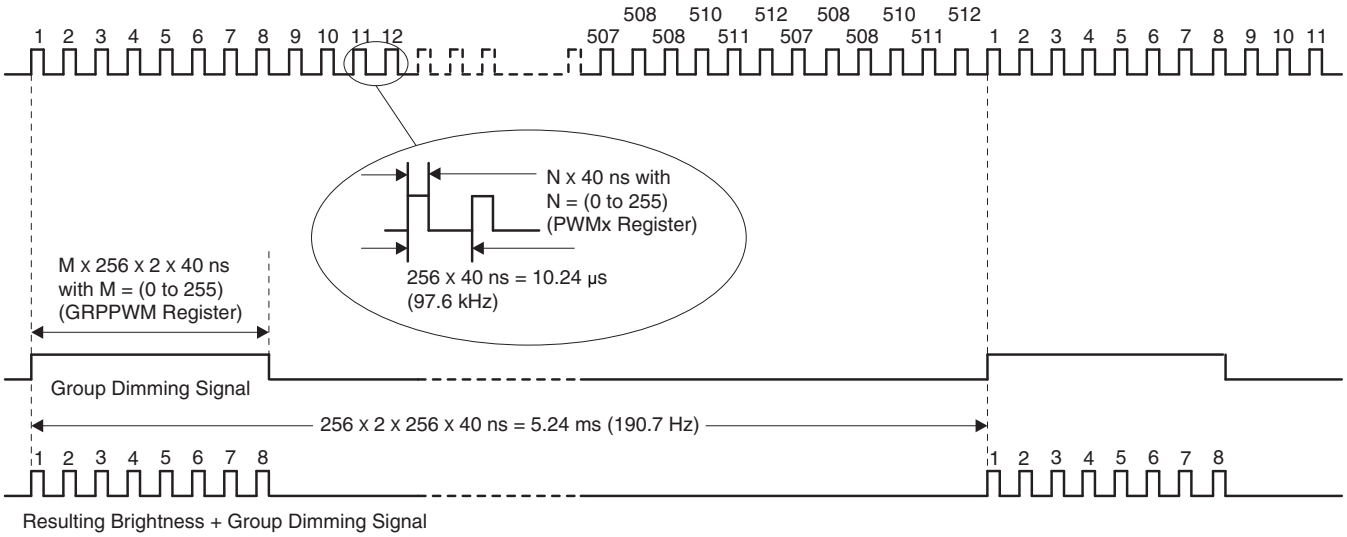
8.3.4 Individual Brightness Control With Group Dimming/Blinking

A 97-kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190-Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 s (8 bits, 256 steps) is used to provide a global blinking control.

Feature Description (continued)



A. Minimum pulse width for LEDn brightness control is 40 ns.

B. Minimum pulse width for group dimming is 20.48 µs.

C. When M = 1 (GRPPWM register value), the resulting LEDn brightness control and group dimming signal will have two pulses of the LED brightness control signal (pulse width = N × 40 ns, with N defined in the PWMx register).

D. The resulting brightness plus group dimming signal shown above demonstrate a resulting control signal with M = 4 (8 pulses).

Figure 7. Brightness and Group Dimming Signals

8.4 Device Functional Modes

8.4.1 Active

Active mode occurs when one or more of the output channels is enabled.

8.4.2 Standby

Standby mode occurs when all output channels are disabled. Standby mode may be entered either through I^2C command or by pulling the $\overline{\text{RESET}}$ pin low.

8.5 Programming

8.5.1 Device Address

Following a START condition, the bus master outputs the address of the slave it is accessing.

8.5.2 Regular I^2C Bus Slave Address

The I^2C bus slave address of the TLC59116F is shown in Figure 8. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low.

For buffer management purpose, a set of sector information data should be stored in a certain buffer.

Programming (continued)

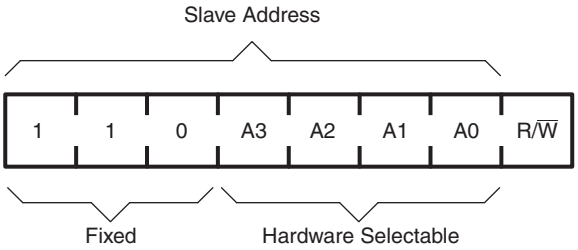


Figure 8. Slave Address

The last bit of the address byte defines the operation to be performed. When set to logic 1, a read is selected; a logic 0 selects a write operation.

8.5.3 LED All-Call I^2C Bus Address

- Default power-up value (ALLCALLADR register): D0h or 1101 000
- Programmable through I^2C bus (volatile programming)
- At power-up, LED All Call I^2C bus address is enabled. TLC59116F sends an ACK when D0h (R/$\overline{W}$ = 0) or D1h (R/$\overline{W}$ = 1) is sent by the master.

See *Register Descriptions* for more details.

NOTE

The default LED all-call I^2C bus address (D0h or 1101 000) must not be used as a regular I^2C bus slave address since this address is enabled at power-up. All the TLC59116Fs on the I^2C bus will acknowledge the address if sent by the I^2C bus master.

8.5.4 LED Sub-Call I^2C Bus Address

- Three different I^2C bus addresses can be used.
- Default power-up values:
  - SUBADR1 register: D2h or 1101 001
  - SUBADR2 register: D4h or 1101 010
  - SUBADR3 register: D8h or 1101 100
- Programmable through I^2C bus (volatile programming)
- At power-up, sub-call I^2C bus address is disabled. TLC59116F does not send an ACK when D2h (R/$\overline{W}$ = 0) or D3h (R/$\overline{W}$ = 1) or D4h (R/$\overline{W}$ = 0) or D5h (R/$\overline{W}$ = 1) or D8h (R/$\overline{W}$ = 0) or D9h (R/$\overline{W}$ = 1) is sent by the master.

See *Register Descriptions* for more details.

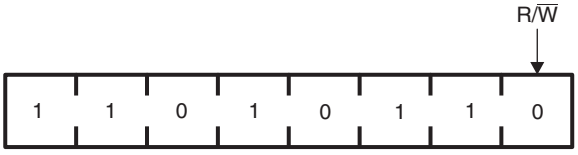
NOTE

The default LED Sub Call I^2C bus address may be used as a regular I^2C bus slave address as long as the Sub Call addresses are disabled in MODE1 (default).

8.5.5 Software Reset I^2C Bus Address

The address shown in Figure 9 is used when a reset of the TLC59116F needs to be performed by the master. The Software Reset address (SWRST Call) must be used with R/$\overline{W}$ = 0. If R/$\overline{W}$ = 1, the TLC59116F does not acknowledge the SWRST. See *Register Descriptions* for more details.

Programming (continued)



The software reset I²C bus address is reserved address and cannot be use as regular I²C bus slave address or as an LED All-Call or LED Sub-Call address.

Figure 9. Software Reset Address

8.5.6 Characteristics of the I²C Bus

The I²C bus is for two-way, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.5.6.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 10).

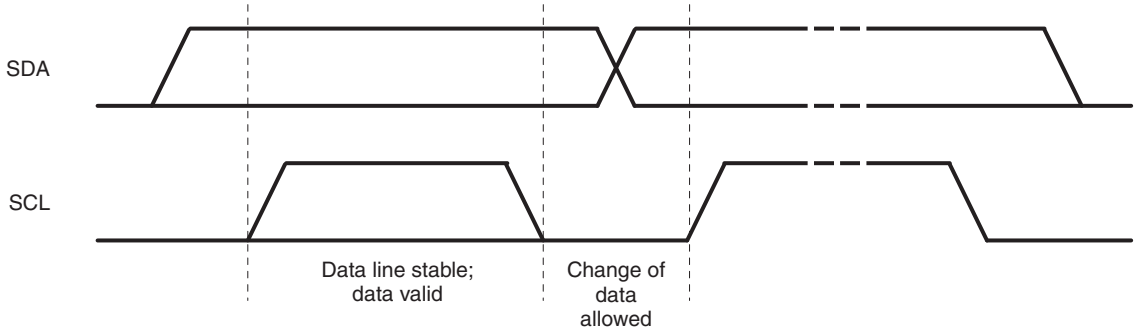


Figure 10. Bit Transfer

8.5.6.2 START and STOP Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the START condition (S). A low-to-high transition of the data line while the clock is high is defined as the STOP condition (P) (see Figure 11).

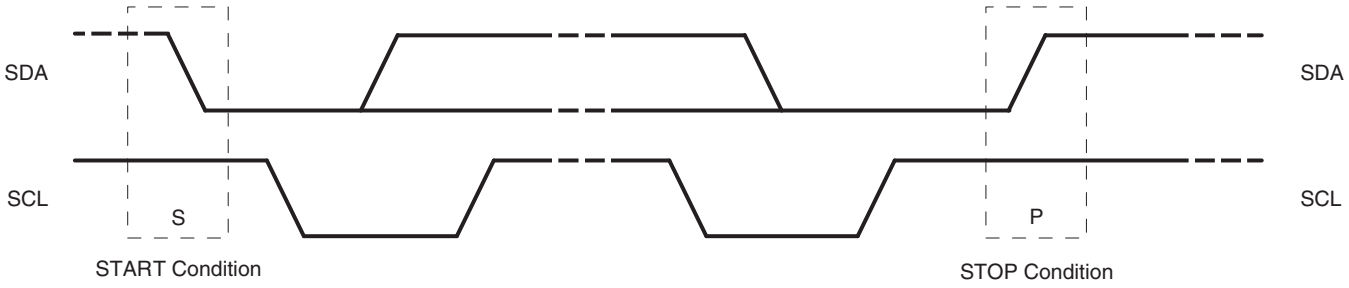


Figure 11. Definition of START and STOP Conditions

Programming (continued)

8.5.6.3 System Configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices controlled by the master are the slaves (see Figure 12).

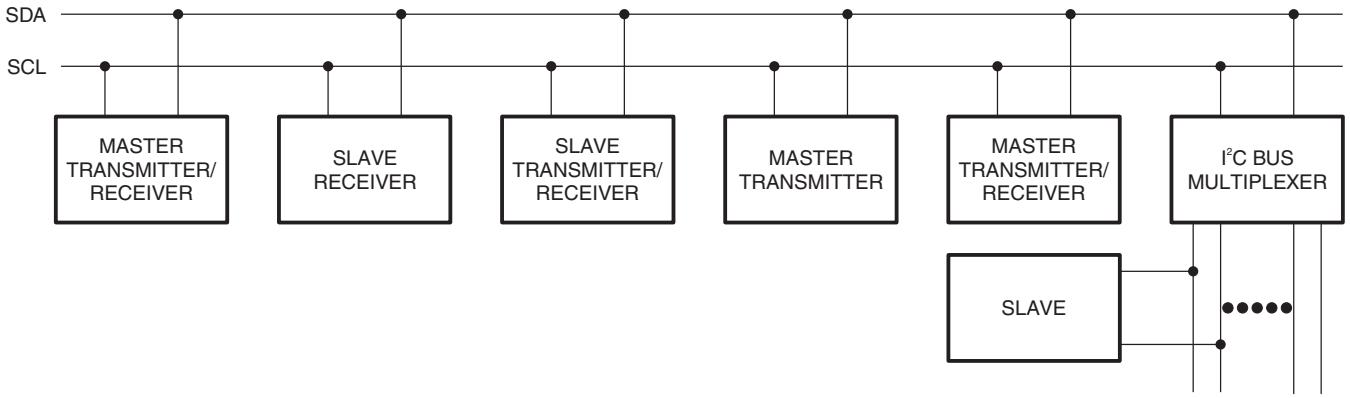


Figure 12. System Configuration

8.5.6.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a STOP condition.

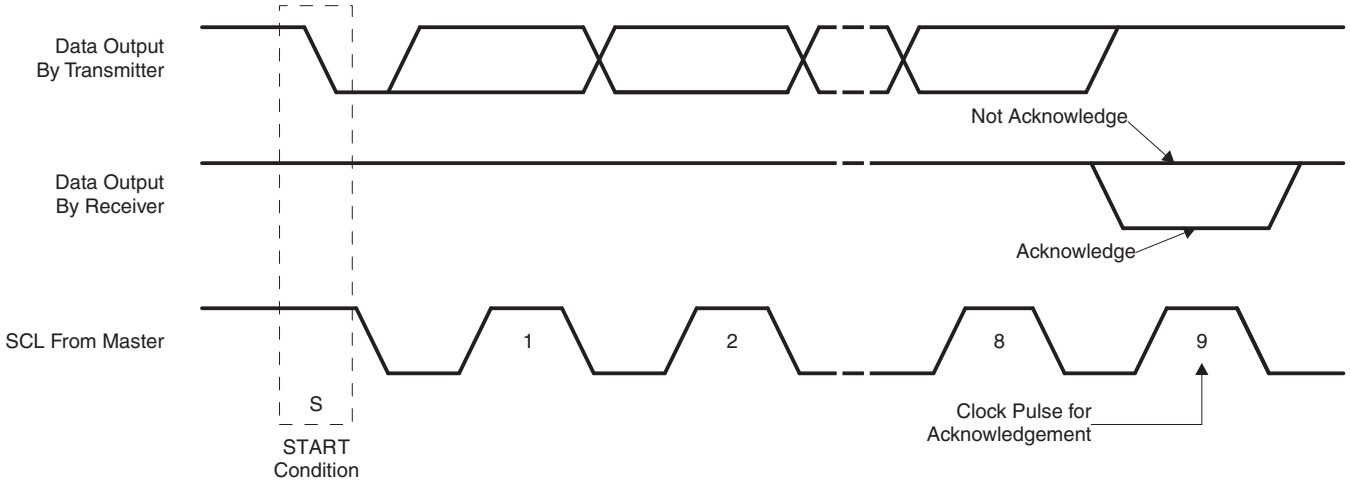


Figure 13. Acknowledge on the I²C Bus

Programming (continued)

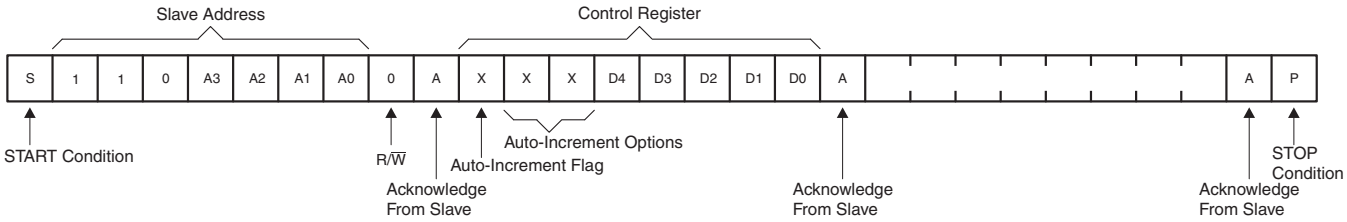


Figure 14. Write to a Specific Register

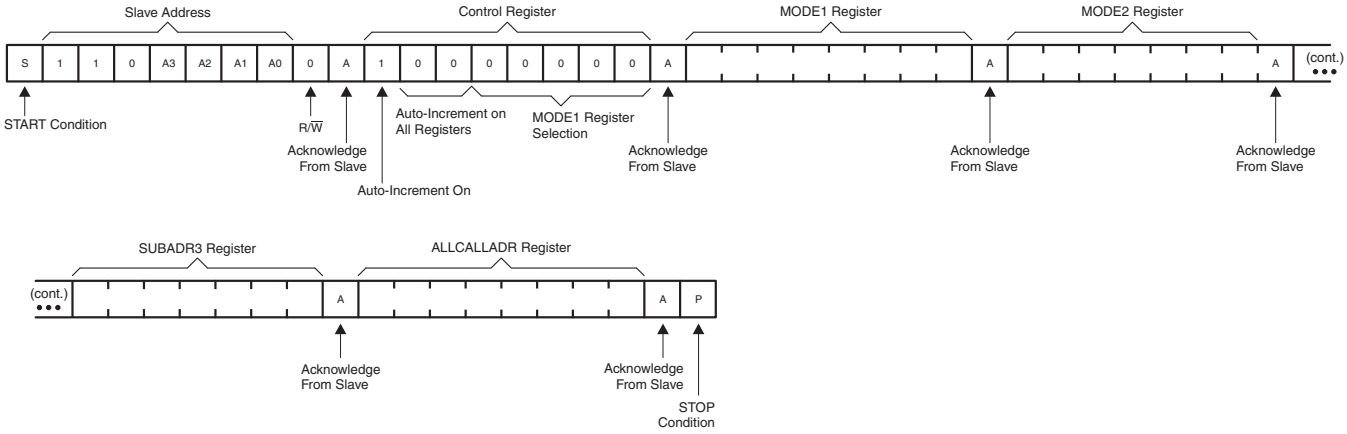


Figure 15. Write to All Registers Using the Auto-Increment Feature

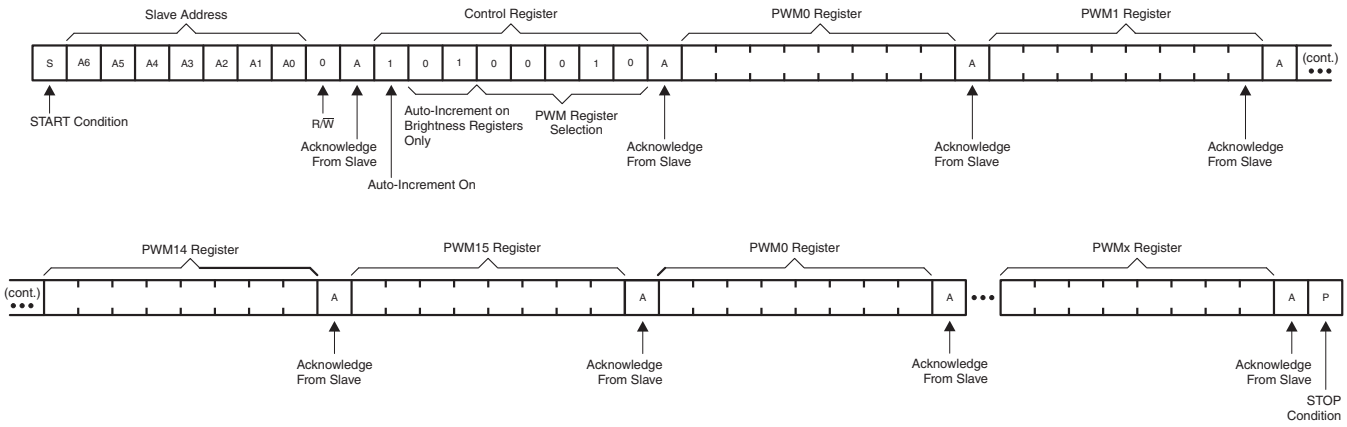


Figure 16. Multiple Writes to Individual Brightness Registers Only Using the Auto-Increment Feature

Programming (continued)

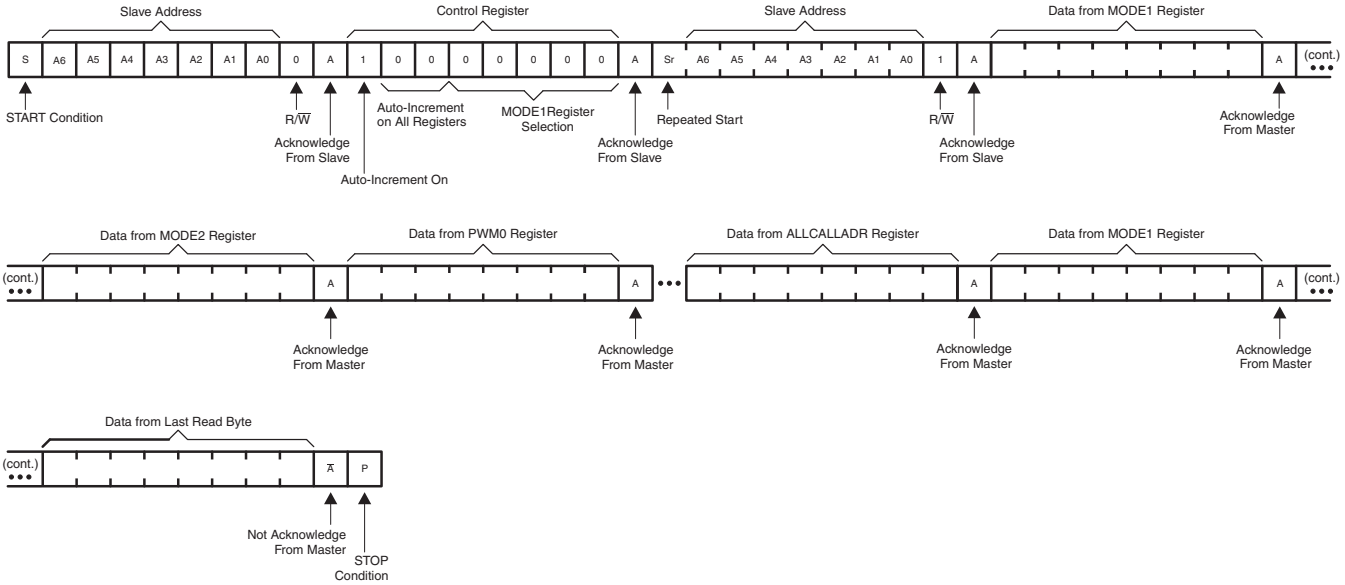
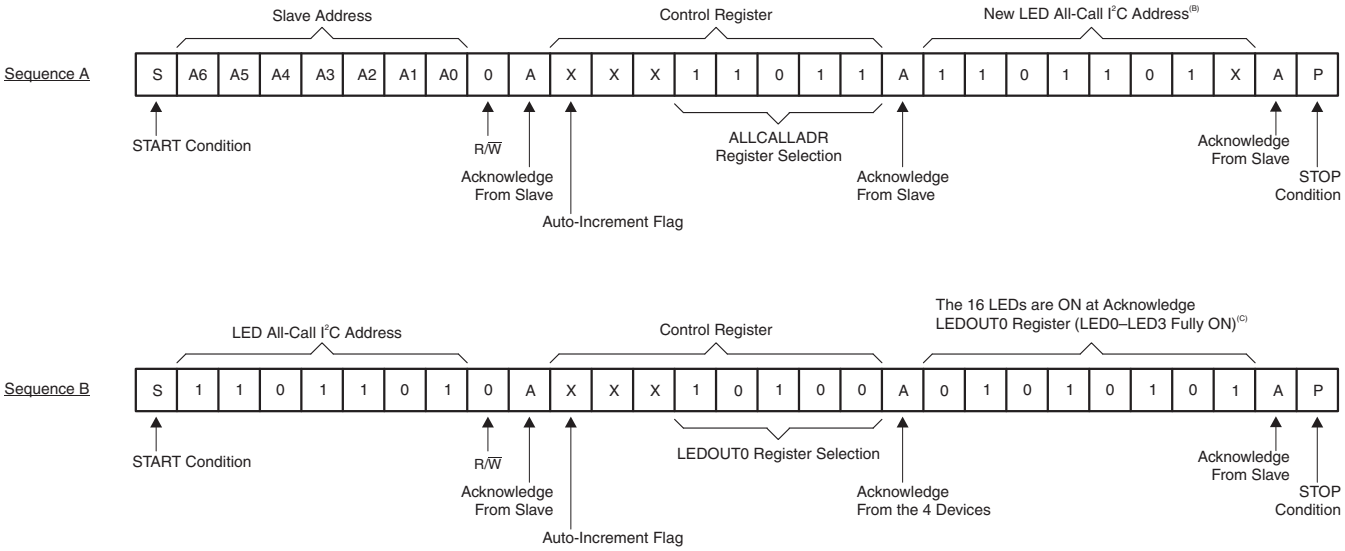


Figure 17. Read All Registers With the Auto-Increment Feature



A. In this example, four TLC59116Fs are used with the same sequence sent to each.

B. ALLCALL bit in MODE1 register is equal to 1 for this example.

C. OCH bit in MODE2 register is equal to 1 for this example.

Figure 18. LED All-Call I²C Bus Address Programming and LED All-Call Sequence Example

8.6 Register Maps

8.6.1 Control Register

Following the successful acknowledgment of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the TLC59116F, which will be stored in the Control register. The lowest 5 bits are used as a pointer to determine which register will be accessed (D[4:0]). The highest three bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).

Register Maps (continued)

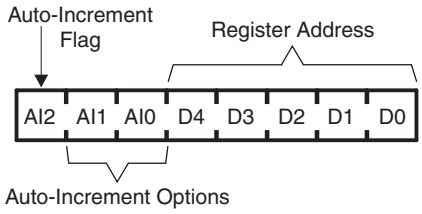


Figure 19. Control Register

When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

Table 1. Auto-Increment Options (1)

AI2	AI1	AI0	PIN DESCRIPTION
0	0	0	No auto-increment
1	0	0	Auto-increment for all registers. D[4:0] roll over to *0 0000* after the last register (1 1011) is accessed.
1	0	1	Auto-increment for individual brightness registers only. D[4:0] roll over to *0 0010* after the last register (1 0001) is accessed.
1	1	0	Auto-increment for global control registers only. D[4:0] roll over to *1 0010* after the last register (1 0011) is accessed.
1	1	1	Auto-increment for individual and global control registers only. D[4:0] roll over to *0 0010* after the last register (1 0011) is accessed.

(1) Other combinations not shown in Table 1 (AI[2:0] = 001, 010 and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I^2C bus communication (for example, changing the brightness of a single LED). Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed (for example, power-up programming).

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I^2C bus communication (for example, changing color setting to another color setting).

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I^2C bus communication (for example, global brightness or blinking change).

AI[2:0] = 111 is used when individually and global changes must be performed during the same I^2C bus communication (for example, changing color and global brightness at the same time).

Only the five least-significant bits (LSBs) D[4:0] are affected by the AI[2:0] bits.

When Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 1011 (as defined in). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See for rollover values. For example, if the Control register = 1111 0100 (F4h), then the register addressing sequence will be (in hex):

14 → … → 1B → 00 → … → 13 → 02 → … → 13 → 02 → … as long as the master keeps sending or reading data.

8.6.2 Register Descriptions

Table 2. Register Descriptions

REGISTER NUMBER (HEX)	NAME	ACCESS (1)	FUNCTION
00	MODE1	R/W	Mode register 1
01	MODE2	R/W	Mode register 2
02	PWM0	R/W	Brightness control LED0
03	PWM1	R/W	Brightness control LED1
04	PWM2	R/W	Brightness control LED2
05	PWM3	R/W	Brightness control LED3
06	PWM4	R/W	Brightness control LED4
07	PWM5	R/W	Brightness control LED5
08	PWM6	R/W	Brightness control LED6
09	PWM7	R/W	Brightness control LED7
0A	PWM8	R/W	Brightness control LED8
0B	PWM9	R/W	Brightness control LED9
0C	PWM10	R/W	Brightness control LED10
0D	PWM11	R/W	Brightness control LED11
0E	PWM12	R/W	Brightness control LED12
0F	PWM13	R/W	Brightness control LED13
10	PWM14	R/W	Brightness control LED14
11	PWM15	R/W	Brightness control LED15
12	GRPPWM	R/W	Group duty cycle control
13	GRPFREQ	R/W	Group frequency
14	LEDOUT0	R/W	LED output state 0
15	LEDOUT1	R/W	LED output state 1
16	LEDOUT2	R/W	LED output state 2
17	LEDOUT3	R/W	LED output state 3
18	SUBADR1	R/W	I^2C bus sub-address 1
19	SUBADR2	R/W	I^2C bus sub-address 2
1A	SUBADR3	R/W	I^2C bus sub-address 3
1B	ALLCALLADR	R/W	LED All Call I^2C bus address

(1) R = read, W = write

8.6.2.1 Mode Register 1 (MODE1)

Table 3. MODE1 – Mode Register 1 (Address 00h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7	AI2	R	0 (2)	Register auto-increment disabled
			1	Register auto-increment enabled
6	AI1	R	0 (2)	Auto-increment bit 1 = 0
			1	Auto-increment bit 1 = 1
5	AI0	R	0 (2)	Auto-increment bit 0 = 0
			1	Auto-increment bit 0 = 1
4	SLEEP	R/W	0	Normal mode (3)
			1 (2)	Low-power mode. Oscillator off. (4)
3	SUB1	R/W	0 (2)	TLC59116F does not respond to I^2C bus sub-address 1.
			1	TLC59116F responds to I^2C bus sub-address 1.
2	SUB2	R/W	0 (2)	TLC59116F does not respond to I^2C bus sub-address 2.
			1	TLC59116F responds to I^2C bus sub-address 2.
1	SUB3	R/W	0 (2)	TLC59116F does not respond to I^2C bus sub-address 3.
			1	TLC59116F responds to I^2C bus sub-address 3.
0	ALLCALL	R/W	0	TLC59116F does not respond to LED all-call I^2C bus address.
			1 (2)	TLC59116F responds to LED all-call I^2C bus address.

(1) R = read, W = write
(2) Default value
(3) It takes 500 µs max for the oscillator to be up and running once SLEEP bit has been set from logic 1 to 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM, or GRPFREQ registers are accessed within the 500-µs window.
(4) No LED control including ON/OFF, blinking and dimming is possible when oscillator is off. Writing to the register during SLEEP mode does not affect LED condition. It is needed to set the SLEEP bit to logic 0 when LED condition is required to change.

8.6.2.2 Mode Register 2 (MODE2)

Table 4. MODE2 – Mode Register 2 (Address 01h) Bit Description

BIT	SYMBOL	ACCESS (1)	VALUE	DESCRIPTION
7:6		R	00 (2)	Reserved
5	DMBLNK	R/W	0 (2)	Group control = dimming
			1	Group control = blinking
4		R	0 (2)	Reserved
3	OCH	R/W	0 (2)	Outputs change on STOP command (3)
			1	Outputs change on ACK
2:0		R	000 (2)	Reserved

(1) R = read, W = write
(2) Default value
(3) Change of the outputs at the STOP command allows synchronizing outputs of more than one TLC59116F. Applicable to registers from 02h (PWM0) to 17h (LEDOUT) only.

8.6.2.3 Individual Brightness Control (PWM0–PWM15) Registers

Table 5. PWM0–PWM15 – Individual Brightness Control Registers (Address 02h to 11h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE (2)	DESCRIPTION
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000	PWM0 individual duty cycle
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000	PWM1 individual duty cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000	PWM2 individual duty cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000	PWM3 individual duty cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000	PWM4 individual duty cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000	PWM5 individual duty cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000	PWM6 individual duty cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000	PWM7 individual duty cycle
0Ah	PWM8	7:0	IDC8[7:0]	R/W	0000 0000	PWM8 individual duty cycle
0Bh	PWM9	7:0	IDC9[7:0]	R/W	0000 0000	PWM9 individual duty cycle
0Ch	PWM10	7:0	IDC10[7:0]	R/W	0000 0000	PWM10 individual duty cycle
0Dh	PWM11	7:0	IDC11[7:0]	R/W	0000 0000	PWM11 individual duty cycle
0Eh	PWM12	7:0	IDC12[7:0]	R/W	0000 0000	PWM12 individual duty cycle
0Fh	PWM13	7:0	IDC13[7:0]	R/W	0000 0000	PWM13 individual duty cycle
10h	PWM14	7:0	IDC14[7:0]	R/W	0000 0000	PWM14 individual duty cycle
11h	PWM15	7:0	IDC15[7:0]	R/W	0000 0000	PWM15 individual duty cycle

(1) R = read, W = write
(2) Default value

A 97-kHz fixed frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 to LEDOUT3 registers).

$$\text{Duty cycle} = \frac{\text{IDCx[7:0]}}{256} \quad (1)$$

8.6.2.4 Group Duty Cycle Control (GRPPWM) Register

Table 6. GRPPWM – Group Duty Cycle Control Register (Address 12h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE (2)	DESCRIPTION
12h	GRPPWM	7:0	GDC0[7:0]	R/W	1111 1111	GRPPWM register

(1) R = read, W = write
(2) Default value

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190-Hz fixed frequency signal is superimposed with the 97-kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value.

NOTE

The value in GRPFREQ has to be programmed to 00h when DMBLNK = 0.

General brightness for the 16 outputs is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in percentages).

$$\text{Duty cycle} = \frac{\text{GDC[7:0]}}{256} \quad (2)$$

8.6.2.5 Group Frequency (GRPFREQ) Register

Table 7. GRPFREQ – Group Frequency Register (Address 13h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE (2)	DESCRIPTION
13h	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000	GRPFREQ register

(1) R = read, W = write
(2) Default value

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1.

NOTE

The value in GRPFREQ must be programmed to 00h when DMBLNK = 0.

Applicable to LED output programmed with LDRx = 11 (LEDOUT0 to LEDOUT3 registers). Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$\text{Global blinking period} = \frac{\text{GFRQ[7:0]} + 1}{24}\ (\text{s}) \quad (3)$$

8.6.2.6 LED Driver Output State (LEDOUT0–LEDOUT3) Register

Table 8. LEDOUT0–LEDOUT3 – LED Driver Output State Registers (Address 14h–17h) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE (2)	DESCRIPTION
14h	LEDOUT0	7:6	LDR3[1:0]	R/W	00	LED3 output state control
		5:4	LDR2[1:0]	R/W	00	LED2 output state control
		3:2	LDR1[1:0]	R/W	00	LED1 output state control
		1:0	LDR0[1:0]	R/W	00	LED0 output state control
15h	LEDOUT1	7:6	LDR7[1:0]	R/W	00	LED7 output state control
		5:4	LDR6[1:0]	R/W	00	LED6 output state control
		3:2	LDR5[1:0]	R/W	00	LED5 output state control
		1:0	LDR4[1:0]	R/W	00	LED4 output state control
16h	LEDOUT2	7:6	LDR11[1:0]	R/W	00	LED11 output state control
		5:4	LDR10[1:0]	R/W	00	LED10 output state control
		3:2	LDR9[1:0]	R/W	00	LED9 output state control
		1:0	LDR8[1:0]	R/W	00	LED8 output state control
17h	LEDOUT3	7:6	LDR15[1:0]	R/W	00	LED15 output state control
		5:4	LDR14[1:0]	R/W	00	LED14 output state control
		3:2	LDR13[1:0]	R/W	00	LED13 output state control
		1:0	LDR12[1:0]	R/W	00	LED12 output state control

(1) R = read, W = write
(2) Default value

LDRx = 00 : LED driver x is off (default power-up state).

LDRx = 01 : LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 : LED driver x is individual brightness can be controlled through its PWMx register.

LDRx = 11 : LED driver x is individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

8.6.2.7 I²C Bus Sub-Address 1 to 3 (SUBADR1–SUBADR3) Register

Table 9. SUBADR1–SUBADR3 – I²C Bus Sub-Address Registers (Address 18h–1Ah) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE (2)	DESCRIPTION
18h	SUBADR1	7:5	A1[7:5]	R	110	I²C bus sub-address 1
		4:1	A1[4:1]	R/W	1001	
		0	A1[0]	R	0	
19h	SUBADR2	7:5	A2[7:5]	R	110	I²C bus sub-address 2
		4:1	A2[4:1]	R/W	1010	
		0	A2[0]	R	0	
1Ah	SUBADR3	7:5	A3[7:5]	R	110	I²C bus sub-address 3
		4:1	A31[4:1]	R/W	1100	
		0	A3[0]	R	0	

(1) R = read, W = write
(2) Default value

Sub-addresses are programmable through the I²C bus. Default power-up values are D2h, D4h, D8h and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once sub-addresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I²C bus sub-address are valid. The LSB in SUBADRx register is a read-only bit (0).

When SUBx is set to 1, the corresponding I²C bus sub-address can be used during either an I²C-bus read or write sequence.

8.6.2.8 LED All-Call I²C Bus Address (ALLCALLADR) Register

Table 10. ALLCALLADR – All-Call I²C Bus Address Register (Address 1Bh) Bit Description

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS (1)	VALUE (2)	DESCRIPTION
1Bh	ALLCALLADR	7:5	AC[7:5]	R	110	ALLCALLADR I²C bus address register
		4:1	AC[4:1]	R/W	1000	
		0	AC[0]	R	0	

(1) R = read, W = write
(2) Default value

The LED All Call I²C bus address allows all the TLC59116Fs in the bus to be programmed at the same time (ALLCALL bit I²C-bus read or write sequence in register MODE1 must be equal to 1 (power-up default state)). This address is programmable through the I²C bus and can be used during either an I²C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I²C bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0 (MODE1), the device does not acknowledge the address programmed in register ALLCALLADR.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations for implementing this device in various applications.

9.1.1 Setting LED Current

The LED current is primarily dependent on the supply voltage, the forward voltage of the LED, and the series resistor (R_{SET}). In many applications the supply voltage and LED forward voltage cannot be adjusted. Hence, R_{SET} is utilized to adjust the LED current. This calculation is discussed in detail in the typical application example.

9.1.2 PWM Brightness Dimming

The perceived brightness of the LEDs can be adjusted by use of PWM dimming. For example, an LED driven at 50% duty cycle will appear less bright than it would at 100% duty cycle. The TLC59116F offers duty cycle control for each individual channel and also offers group duty cycle control. Refer to the Register Map for details regarding programmable duty cycle.

9.2 Typical Application

This application example provides guidance on how to set the LED current using the TLC59116F.

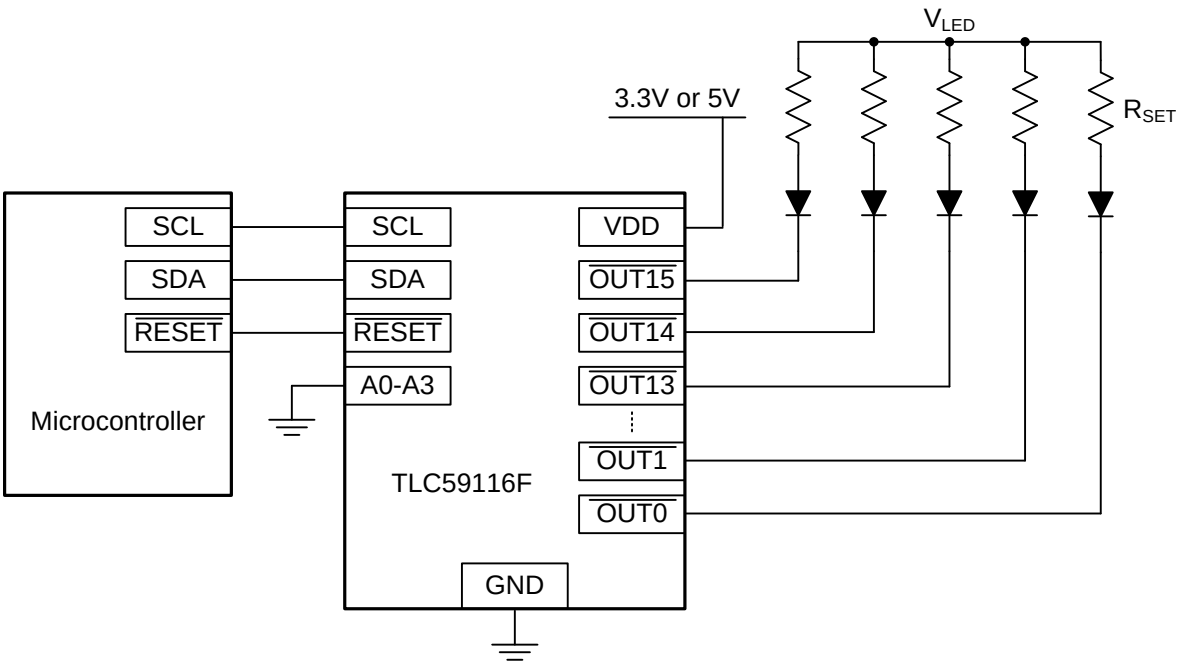


Figure 20. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 11. Design Parameters

DESIGN PARAMETER		EXAMPLE VALUE
V_{LED}	Supply voltage that powers the LED	5 V
V_F	Forward voltage across the LED	3 V
I_{LED}	Current flowing through the LED	6 mA
R_{ON}	Resistance across open-drain output	1.5 Ω

9.2.2 Detailed Design Procedure

In the LED current path, there are three voltage drops that must be considered:

- Drop across the series resistor (V_{RSET})
- Drop across the LED (V_F)
- Drop across the open-drain output channel (V_O)

The drop across the LED is defined above as VF = 3V. The drop across the open-drain output is calculated as R_{ON} x I_{LED} (1.5 Ω × 0.006 A = 0.009 V). The remaining voltage must be across the series resistor:

$5\ V = 3\ V + 0.009\ V + V_{RSET}$

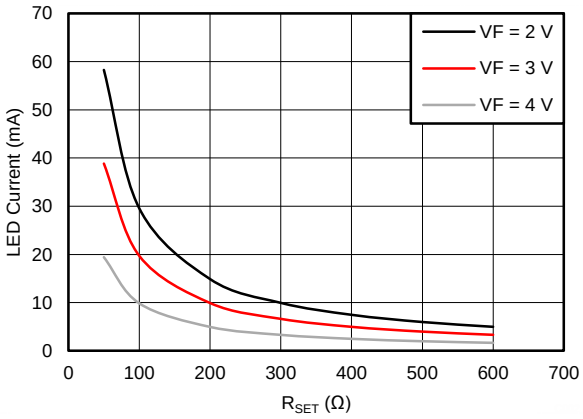
- $V_{RSET} = 1.991\ V$ (4)

After calculating V_{RSET}, we can calculate R_{SET}:

$V_{RSET} = I_{LED} \times R_{SET}$

- $1.991V = 0.006\ mA \times R_{SET}$
- $R_{SET} = 332\ \Omega$ (5)

9.2.3 Application Curve



V_{LED} = 5 V

Figure 21. Typical LED Current as a Function of R_{SET} and V_F

10 Power Supply Recommendations

TLC59116F is designed to operate from a VCC range of 3 V to 5.5 V. The system will also require a power supply for the LEDs. The supply voltage for the LEDs must be greater than the forward voltage of the LED plus the V_{OL} of the channel.

11 Layout

11.1 Layout Guidelines

The I^2C signals (SDA / SCL) should be kept away from potential noise sources.

The traces carrying power through the LEDS should be wide enough to the handle necessary current.

All LED current passes through the device and into the ground node. There must be a strong connection between the device ground and the circuit board ground. For the RHB package, the thermal pad should be connected to ground to help dissipate heat.

11.2 Layout Examples

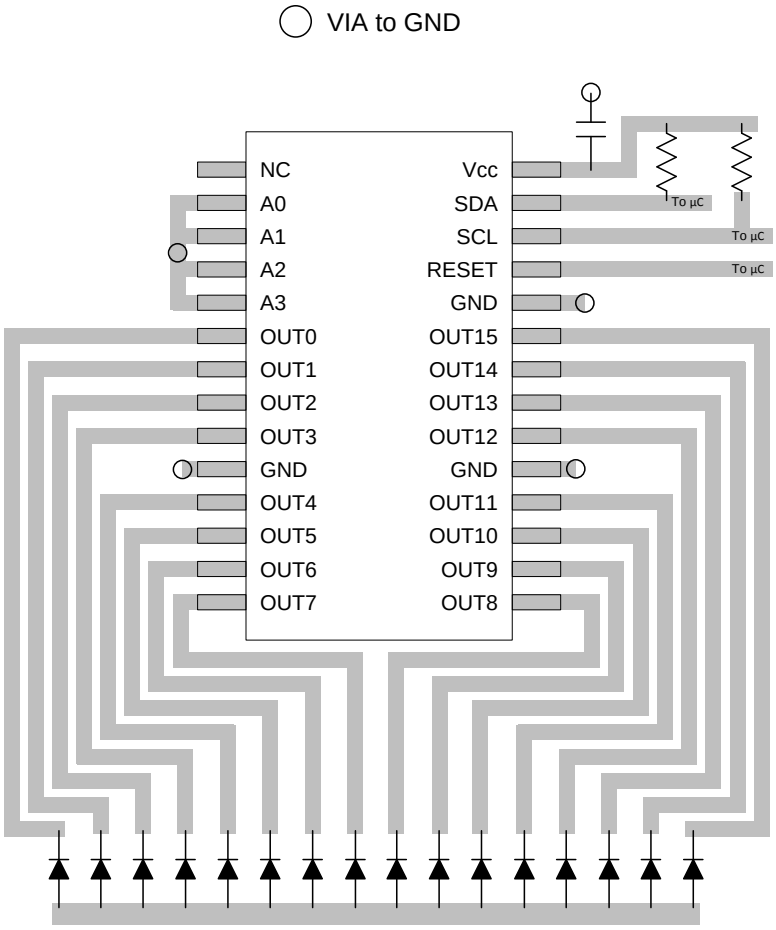


Figure 22. PW Layout Example

Layout Examples (continued)

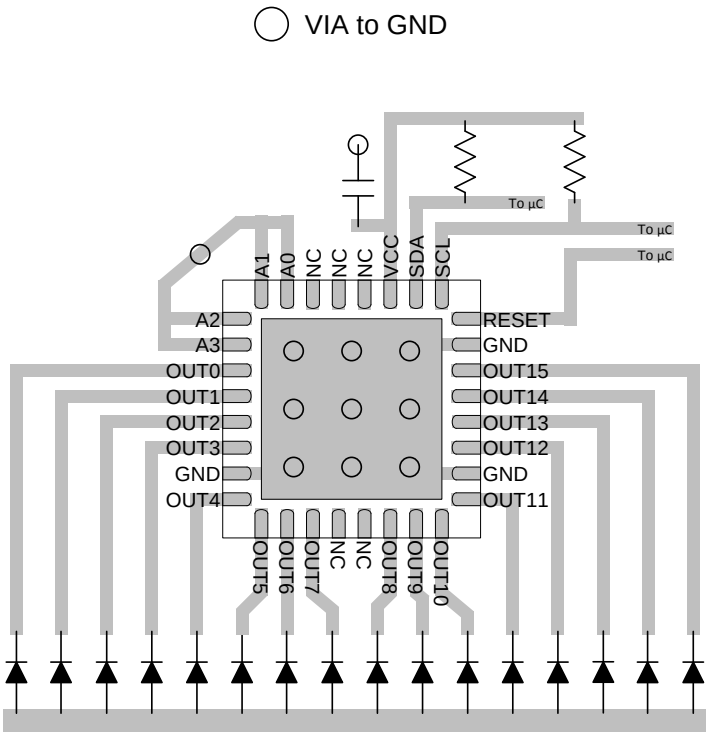


Figure 23. RHB Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC59116FIPWR	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59116F
TLC59116FIPWR.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59116F
TLC59116FIPWRG4	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59116F
TLC59116FIPWRG4.B	Active	Production	TSSOP (PW) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59116F
TLC59116FIRHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FL116F
TLC59116FIRHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FL116F
TLC59116FIRHBRG4	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FL116F
TLC59116FIRHBRG4.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FL116F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

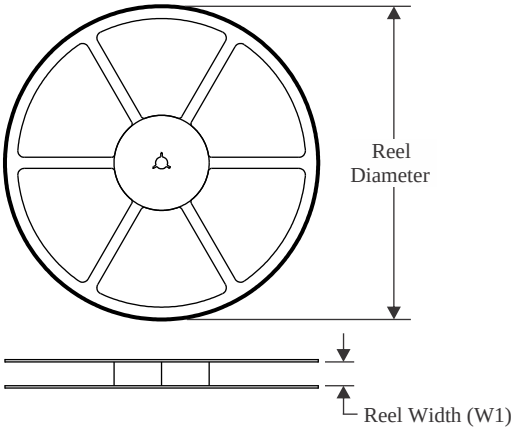
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

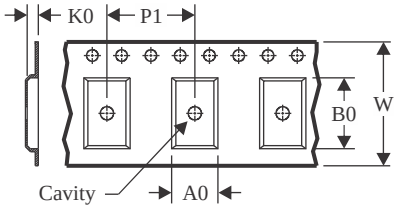
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

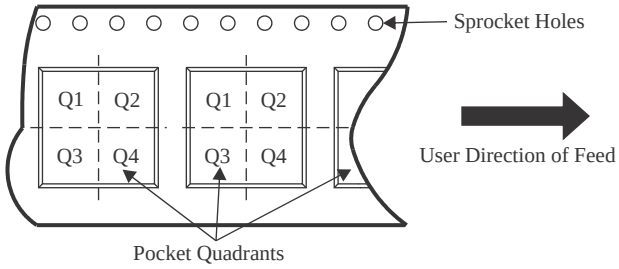


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

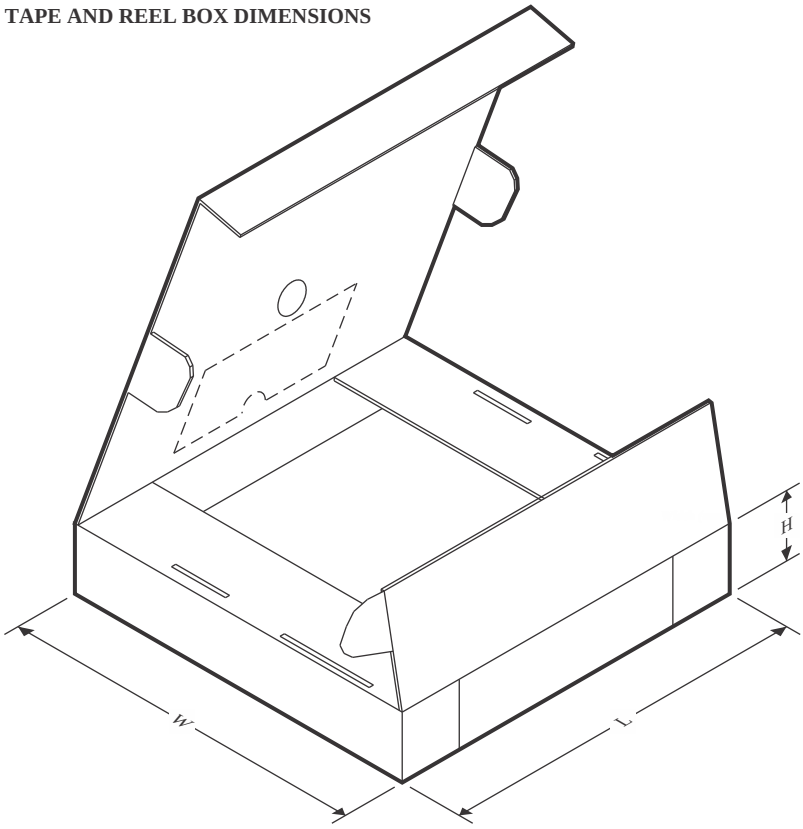
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59116FIPWR	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TLC59116FIPWRG4	TSSOP	PW	28	2000	330.0	16.4	6.75	10.1	1.8	12.0	16.0	Q1
TLC59116FIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLC59116FIRHBRG4	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

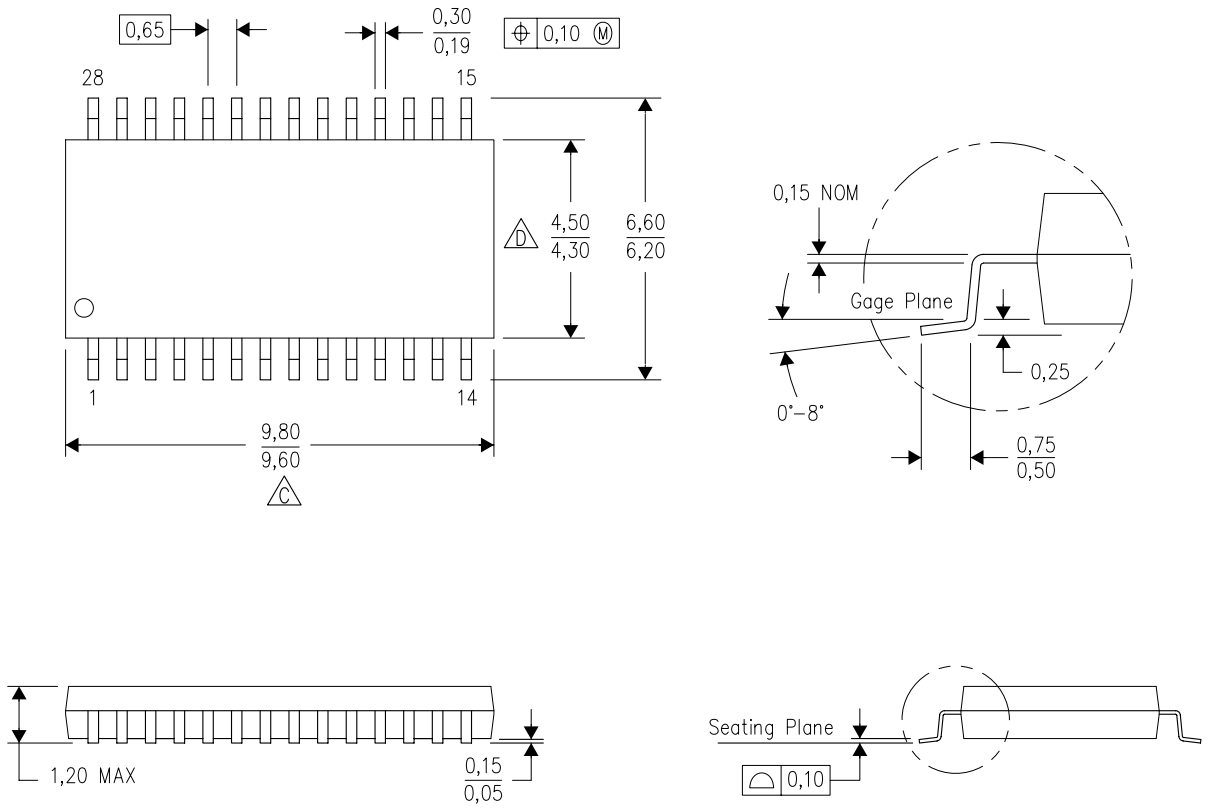
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59116FIPWR	TSSOP	PW	28	2000	353.0	353.0	32.0
TLC59116FIPWRG4	TSSOP	PW	28	2000	353.0	353.0	32.0
TLC59116FIRHBR	VQFN	RHB	32	3000	353.0	353.0	32.0
TLC59116FIRHBRG4	VQFN	RHB	32	3000	353.0	353.0	32.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

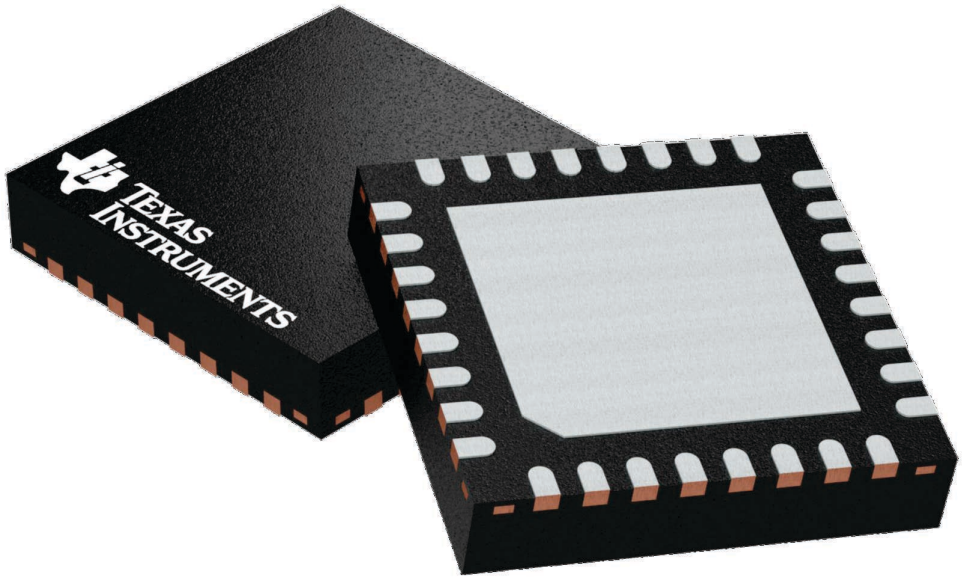
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

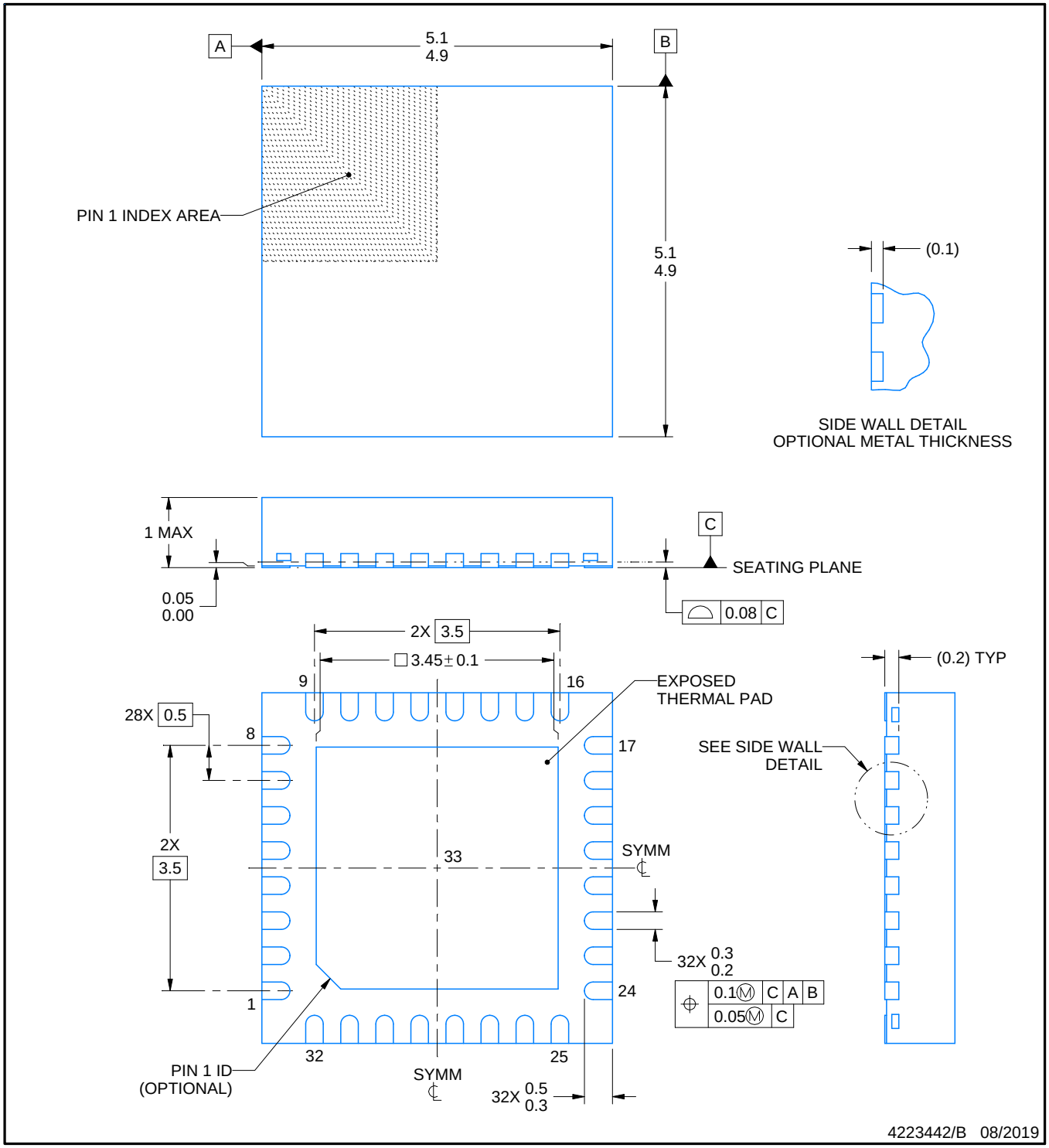
4224745/A

RHB0032E

PACKAGE OUTLINE

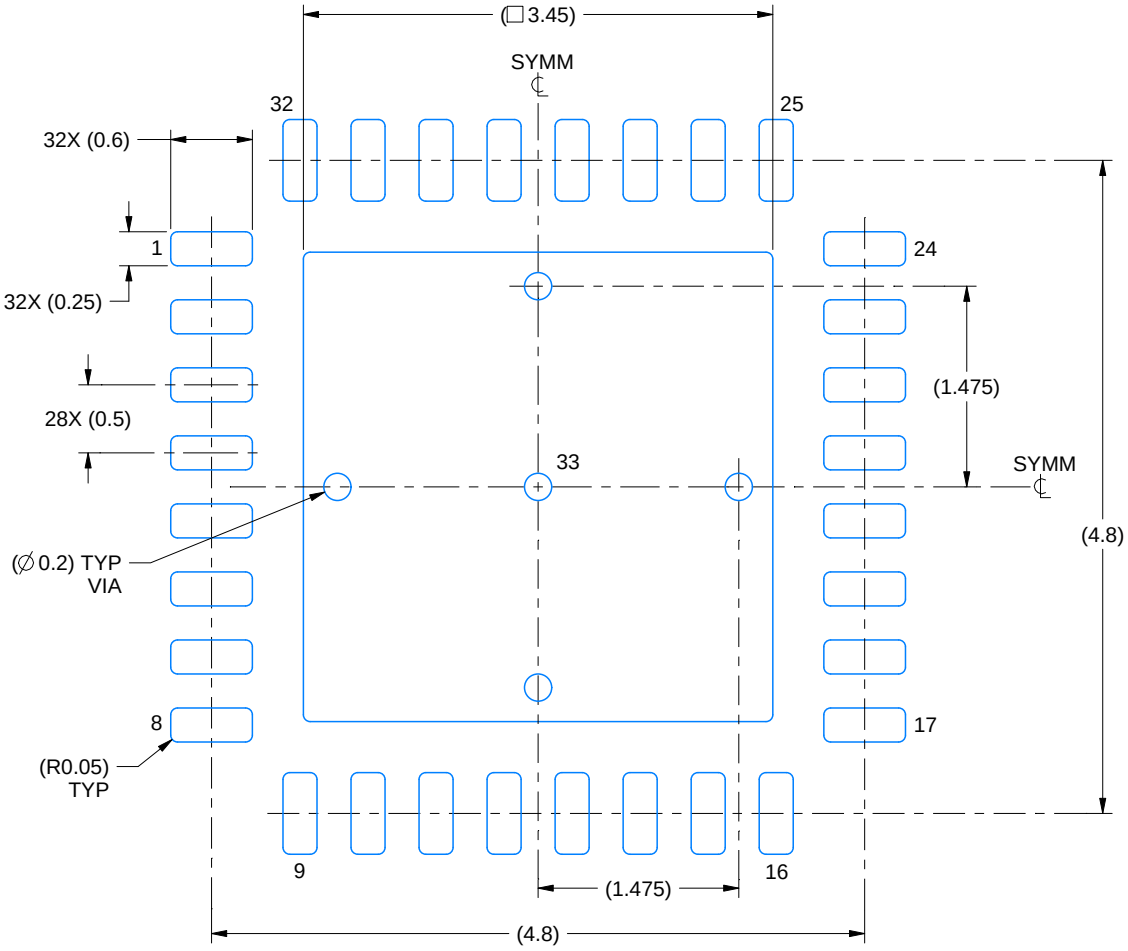
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

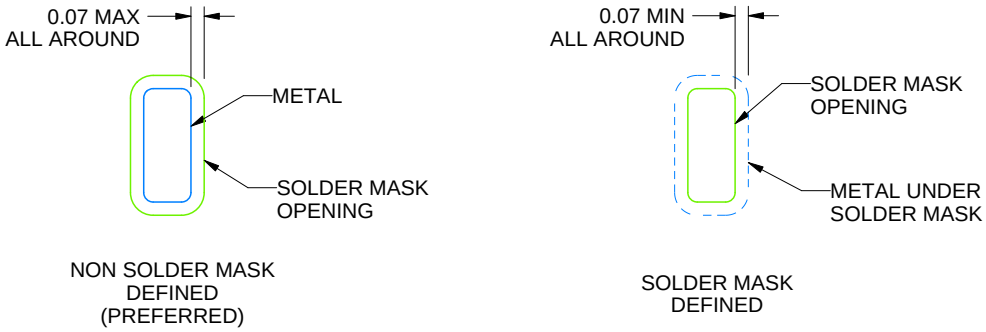


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

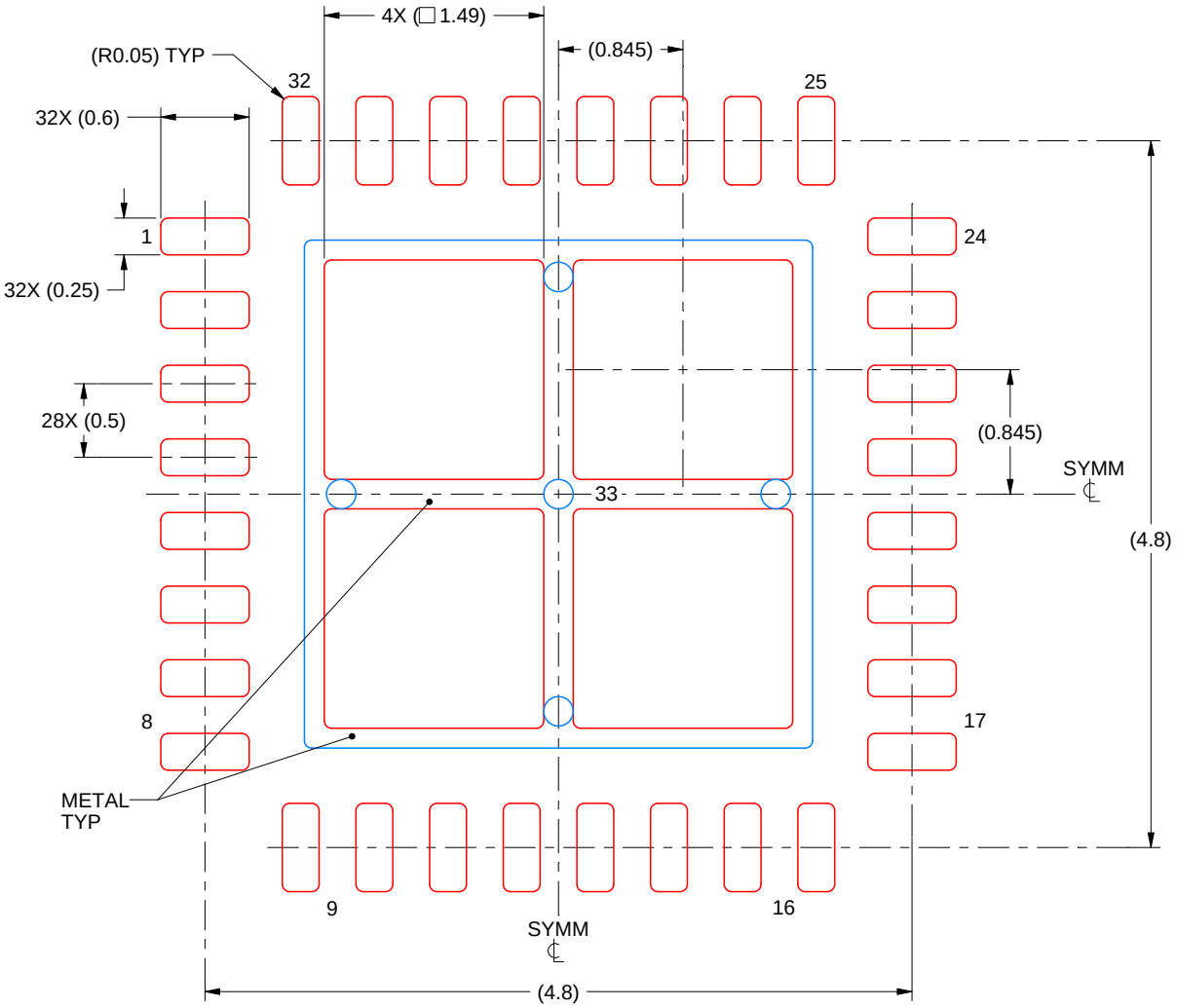


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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