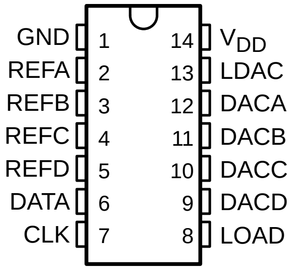
TLC5620C, TLC5620I
QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

- **Four 8-Bit Voltage Output DACs**
- **5-V Single-Supply Operation**
- **Serial Interface**
- **High-Impedance Reference Inputs**
- **Programmable 1 or 2 Times Output Range**
- **Simultaneous Update Facility**
- **Internal Power-On Reset**
- **Low-Power Consumption**
- **Half-Buffered Output**

N OR D PACKAGE
(TOP VIEW)



applications

- **Programmable Voltage Sources**
- **Digitally Controlled Amplifiers/Attenuators**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLC5620C and TLC5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

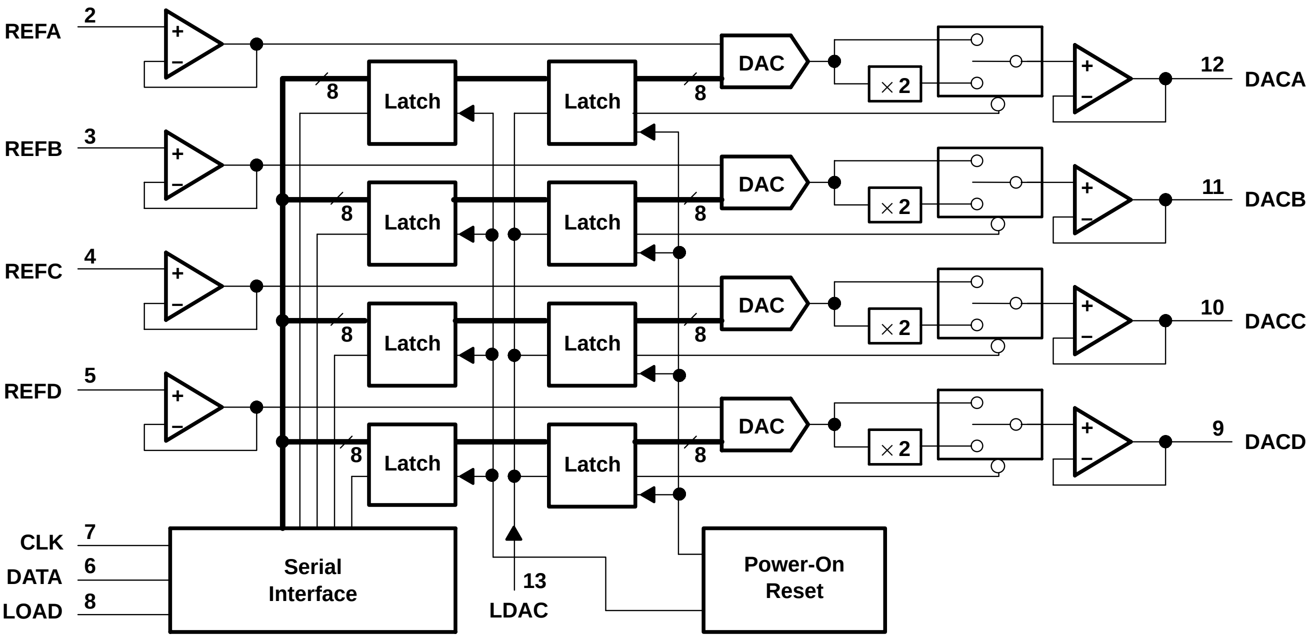
Digital control of the TLC5620C and TLC5620I are over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises eight bits of data, two DAC-select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs are updated simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLC5620C is characterized for operation from 0°C to 70°C. The TLC5620I is characterized for operation from –40°C to 85°C. The TLC5620C and TLC5620I do not require external trimming.

AVAILABLE OPTIONS

T_A	PACKAGE SMALL OUTLINE (D)	PACKAGE PLASTIC DIP (N)
0°C to 70°C	TLC5620CD	TLC5620CN
–40°C to 85°C	TLC5620ID	TLC5620IN

functional block diagram



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CLK	7	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	1	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When the LDAC signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	8	I	Serial Interface load control. When LDAC is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REFA	2	I	Reference voltage input to DAC A. This voltage defines the output analog range.
REFB	3	I	Reference voltage input to DAC B. This voltage defines the output analog range.
REFC	4	I	Reference voltage input to DAC C. This voltage defines the output analog range.
REFD	5	I	Reference voltage input to DAC D. This voltage defines the output analog range.
V_{DD}	14	I	Positive supply voltage

detailed description

The TLC5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Since the inputs are buffered, the DACs always present a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier that can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA}|\text{B}|\text{C}|\text{D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

where CODE is in the range 0 to 255 and the range (RNG) bit is 0 or 1 within the serial control word.

Table 1. Ideal Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered most significant bit (MSB) first. Data transfers using two 8-clock cycle periods are shown in Figures 3 and 4.

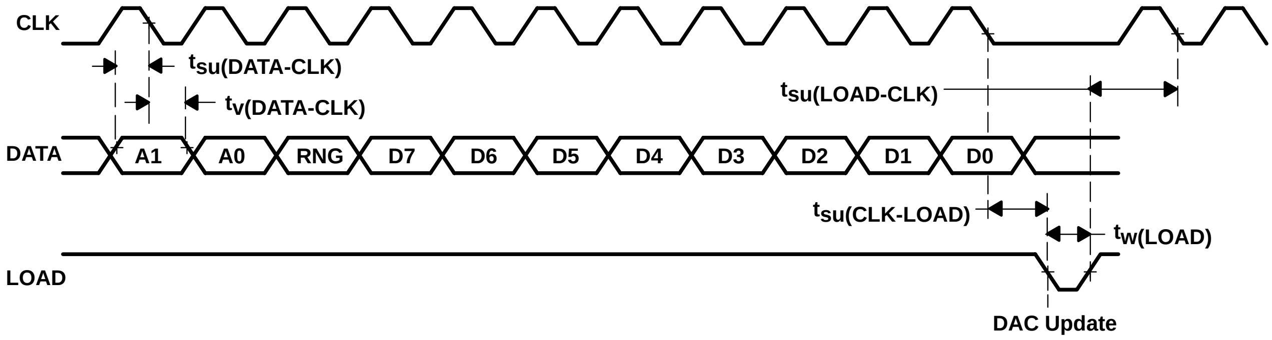


Figure 1. LOAD-Controlled Update (LDAC = Low)

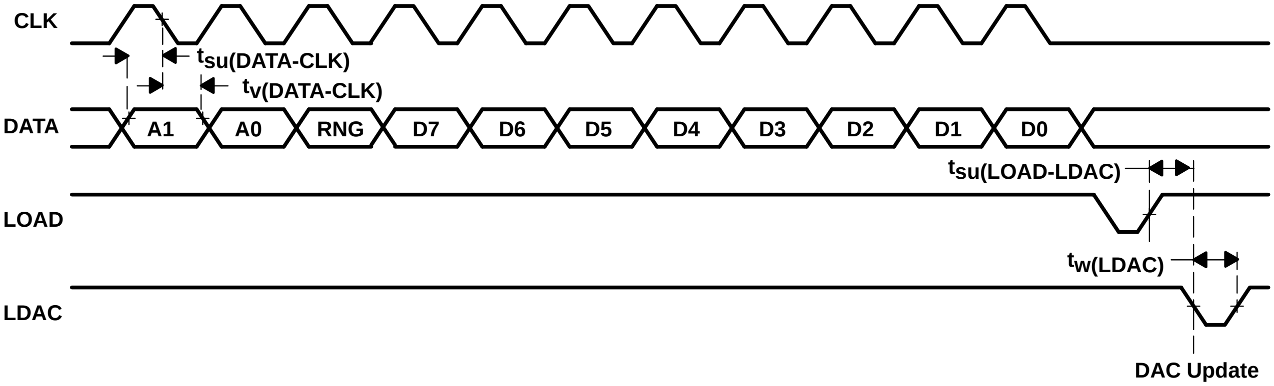


Figure 2. LDAC-Controlled Update

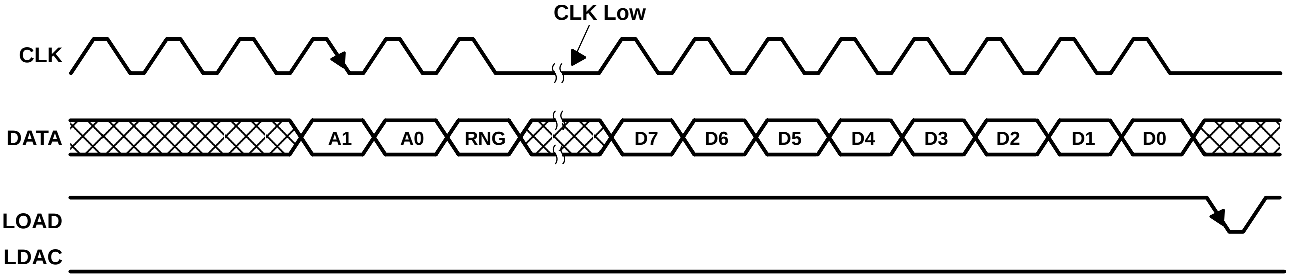


Figure 3. Load-Controlled Update Using 8-Bit Serial Word (LDAC = Low)

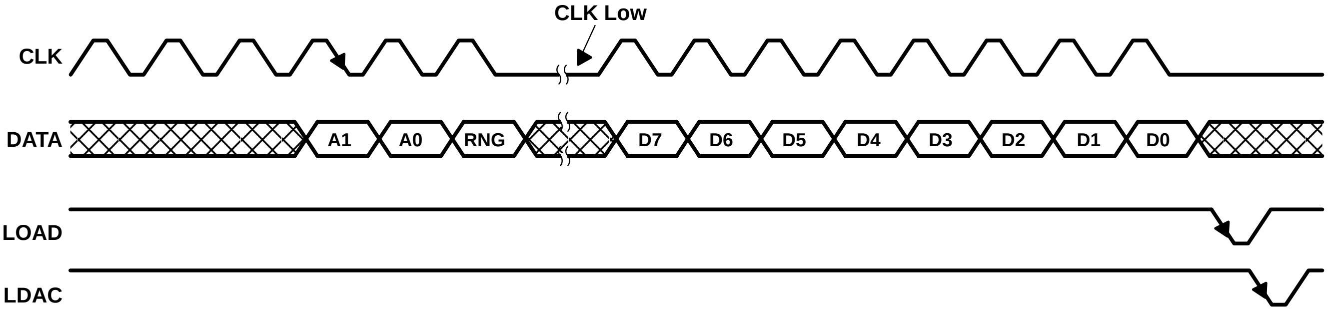


Figure 4. LDAC-Controlled Update Using 8-Bit Serial Word

Table 2 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

linearity, offset, and gain error using single-end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.

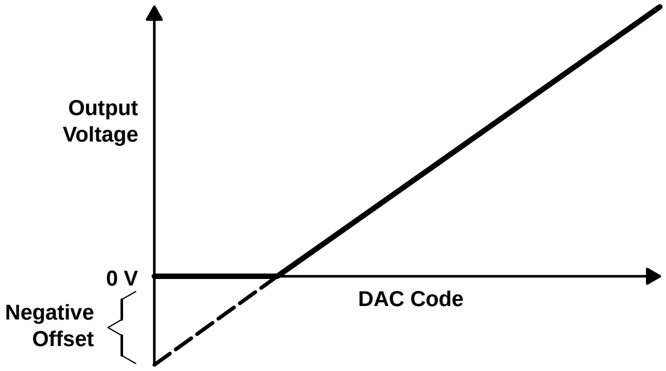
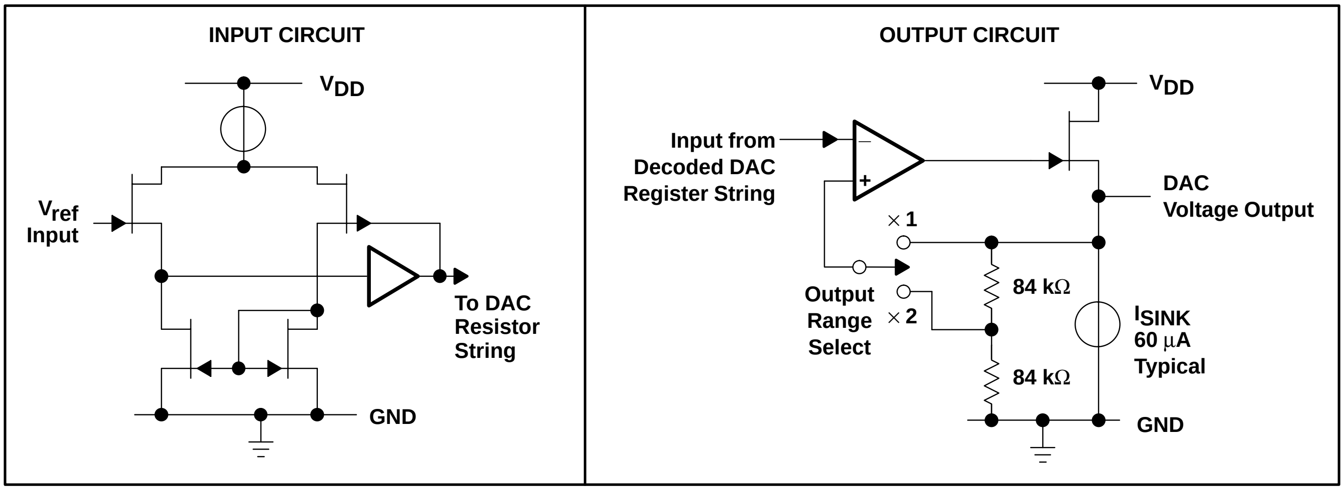


Figure 5. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset voltage.

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND)	7 V
Digital input voltage range	GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID}	GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLC5620C	0°C to 70°C
TLC5620I	–40°C to 85°C
Storage temperature range, T_{stg}	–50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		5.25	V
High-level input voltage, V_{IH}		0.8 V_{DD}			V
Low-level input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D]				V_{DD}−1.5	V
Analog full-scale output voltage, R_L = 10 kΩ			3.5		V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su(CLK-LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$ (see Figure 2)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLC5620C	0		70	°C
	TLC5620I	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	$V_I = V_{DD}$				±10	µA
I_{IL}	Low-level input current	V_I = 0 V				±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output		20			µA
$I_{O(source)}$	Output source current			2			mA
C_i	Input capacitance				15		pF
	Reference input capacitance				15		
I_{DD}	Supply current	V_{DD} = 5 V				2	mA
I_{ref}	Reference input current	V_{DD} = 5 V,	V_{ref} = 2 V			±10	µA
E_L	Linearity error (end point corrected)	V_{ref} = 2 V,	× 2 gain (see Note 1)			±1	LSB
E_D	Differential-linearity error	V_{ref} = 2 V,	× 2 gain (see Note 2)			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 2 V,	× 2 gain (see Note 3)	0		30	mV
	Zero-scale-error temperature coefficient	V_{ref} = 2 V,	× 2 gain (see Note 4)		10		µV/°C
E_{FS}	Full-scale error	V_{ref} = 2 V,	× 2 gain (see Note 5)			±60	mV
	Full-scale-error temperature coefficient	V_{ref} = 2 V,	× 2 gain (see Note 6)		±25		µV/°C
PSRR	Power-supply rejection ratio	See Notes 7 and 8			0.5		mV/V

NOTES:
1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale-error temperature coefficient is given by: ZSETC = $[ZSE(T_{max}) – ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale-error temperature coefficient is given by: FSETC = $[FSE(T_{max}) – FSE\ (T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
7. Zero-scale-error rejection ratio (ZSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Full-scale-error rejection ratio (FSE RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To ±0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		µs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES:
9. Settling time is the time between a LOAD falling edge and the DAC output reaching full scale voltage within +/– 0.5 LSB starting from an initial output voltage equal to zero.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{pp} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{pp} and with a full-scale digital-input code.

PARAMETER MEASUREMENT INFORMATION

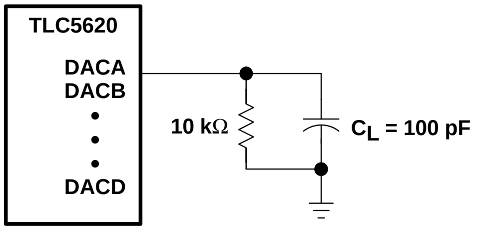


Figure 6. Slew, Settling Time, and Linearity Measurements

TYPICAL CHARACTERISTICS

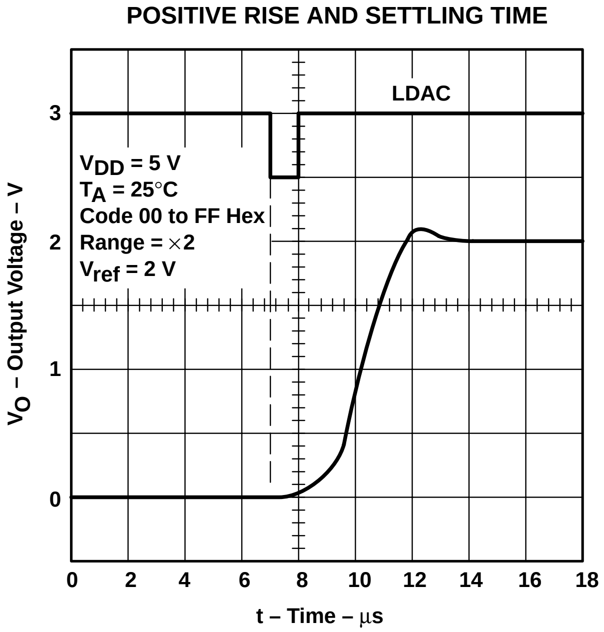


Figure 7

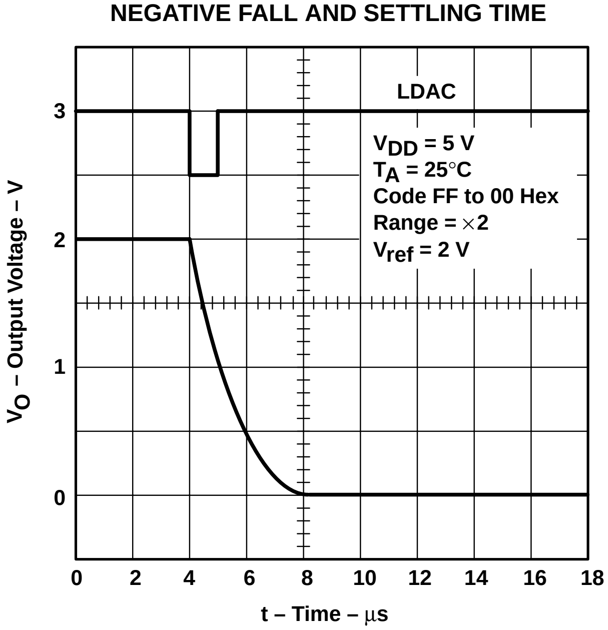


Figure 8

TYPICAL CHARACTERISTICS

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

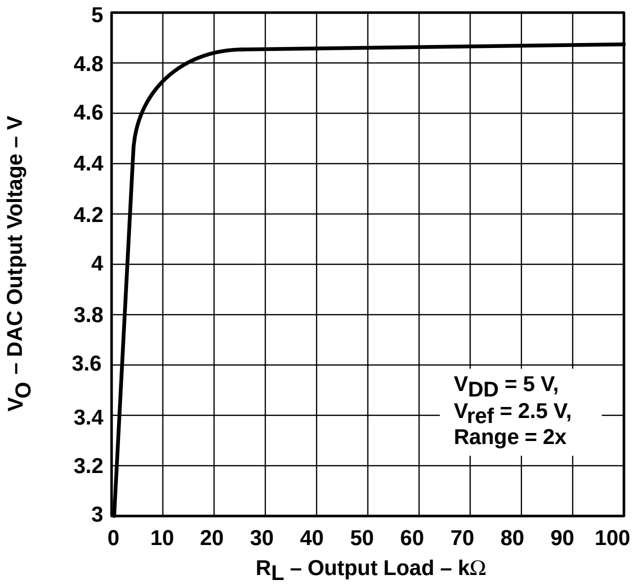


Figure 9

DAC OUTPUT VOLTAGE
vs
OUTPUT LOAD

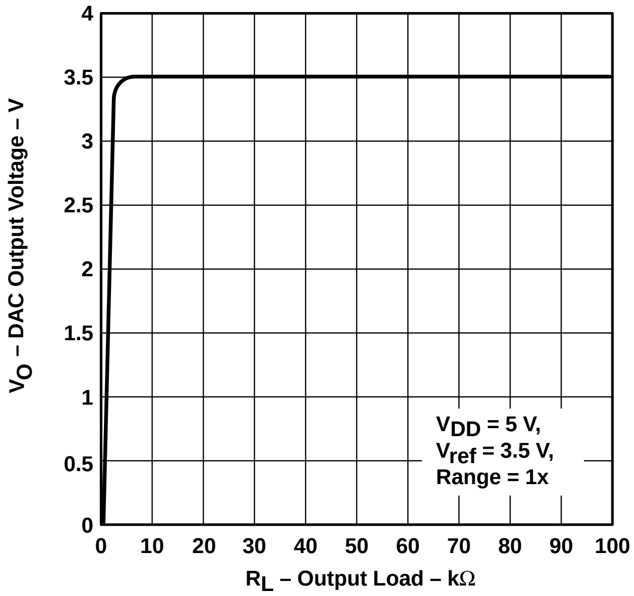


Figure 10

OUTPUT SOURCE CURRENT
vs
OUTPUT VOLTAGE

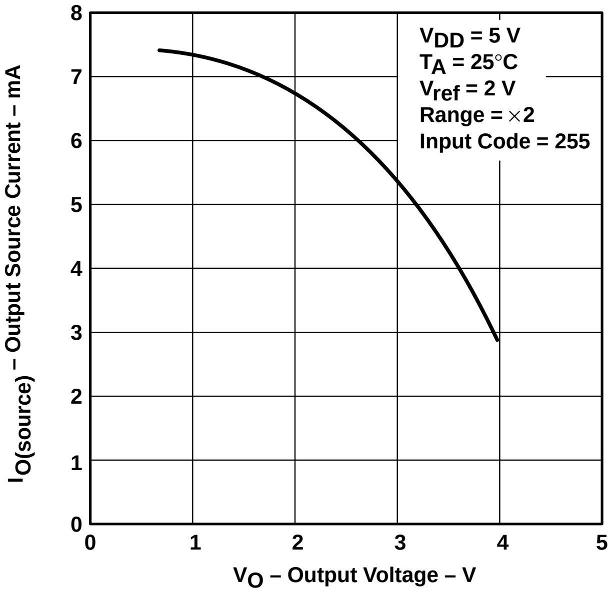


Figure 11

SUPPLY CURRENT
vs
TEMPERATURE

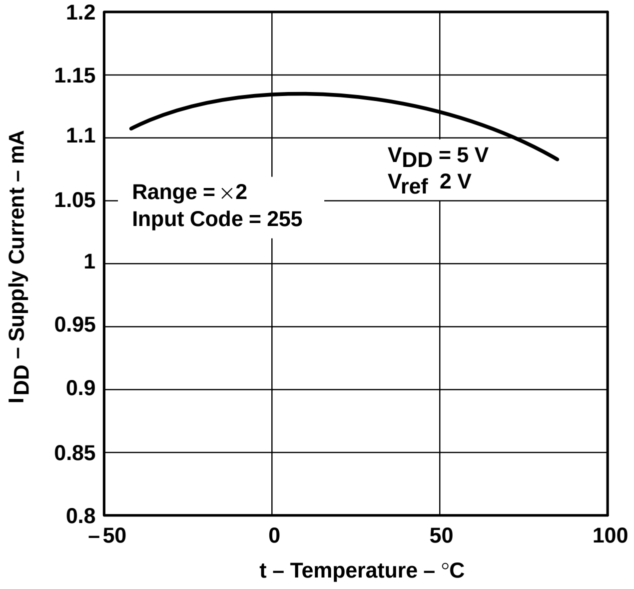


Figure 12

TYPICAL CHARACTERISTICS

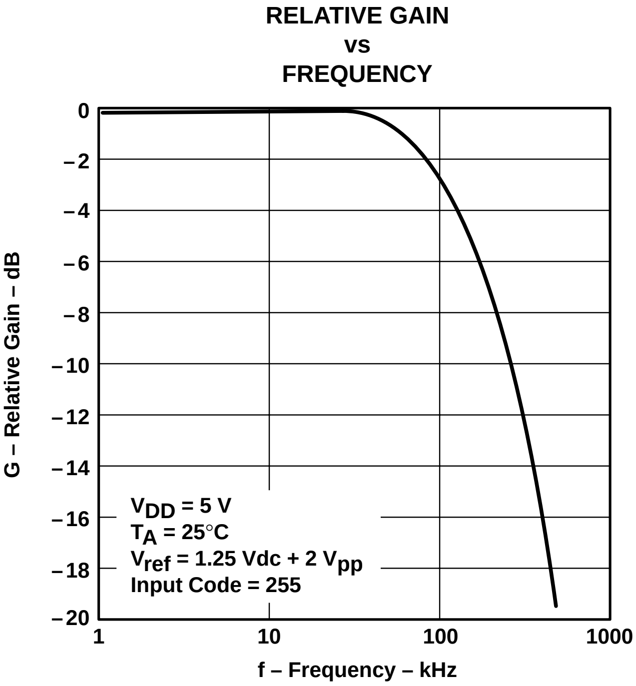


Figure 13

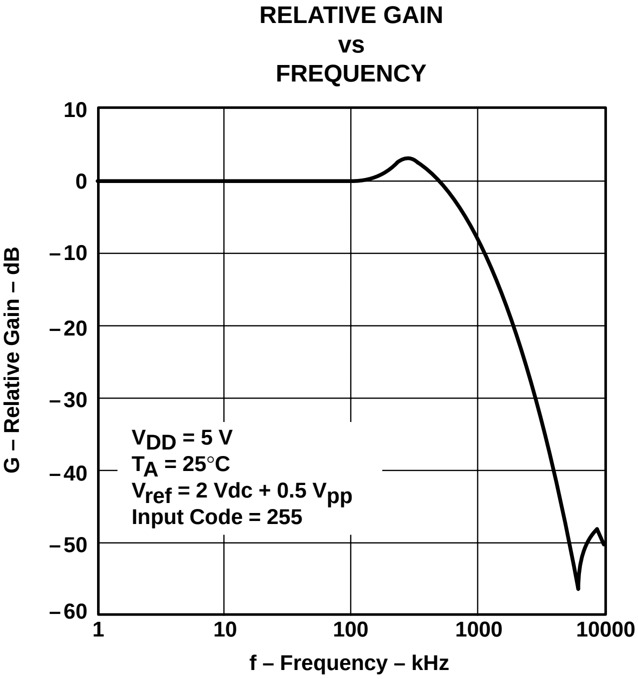
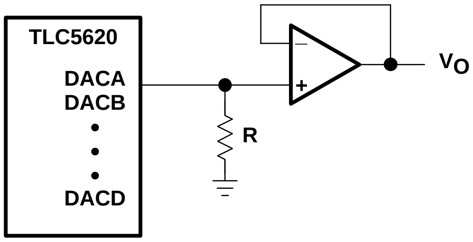


Figure 14

APPLICATION INFORMATION



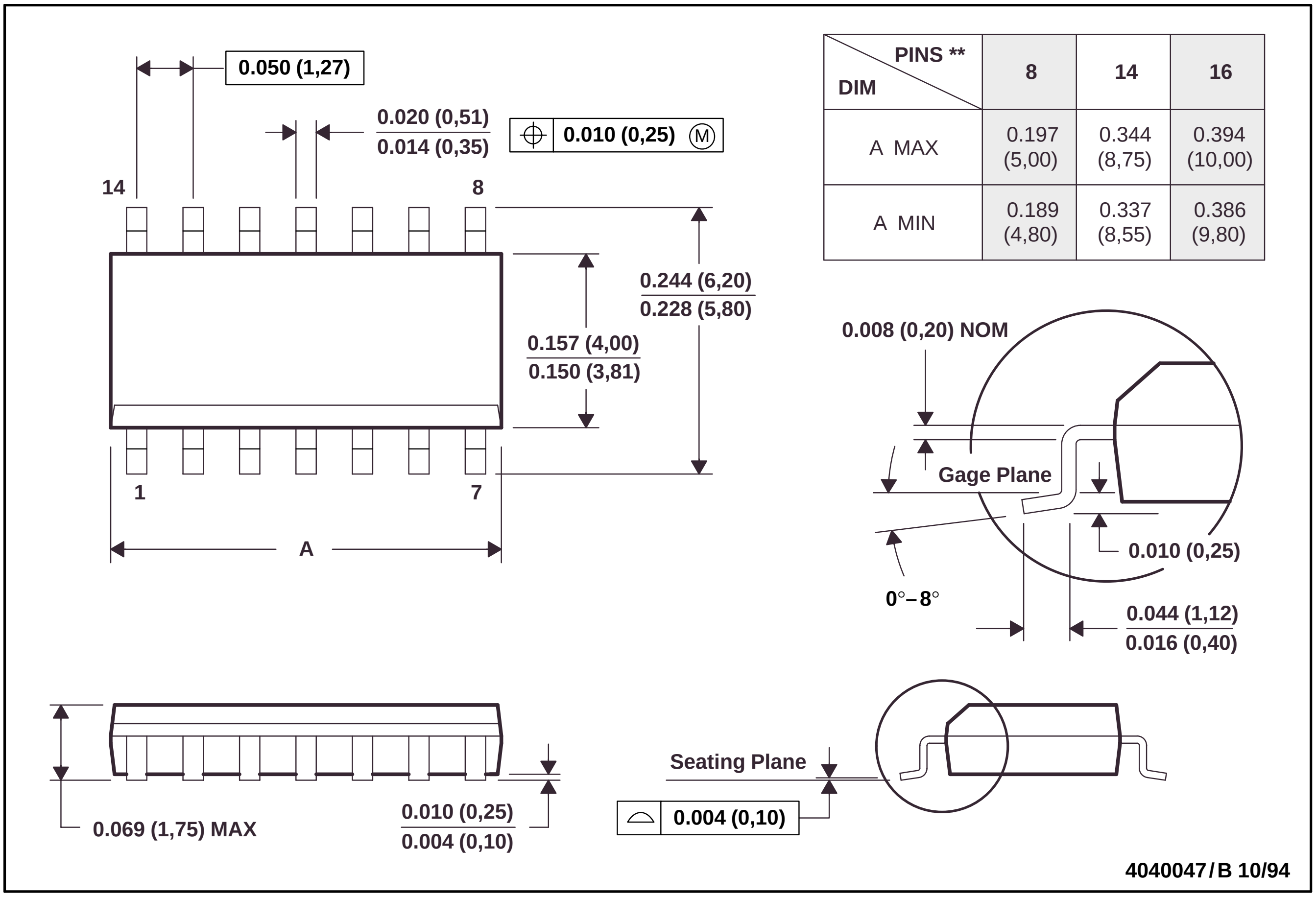
NOTE A: Resistor R ≥ 10 kΩ

Figure 15. Output Buffering Scheme

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

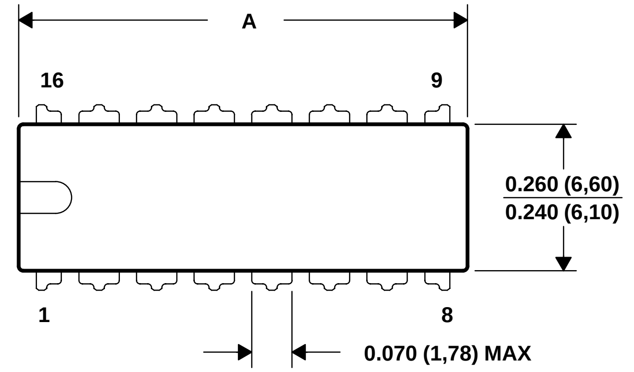
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Four center pins are connected to die mount pad.
- E. Falls within JEDEC MS-012

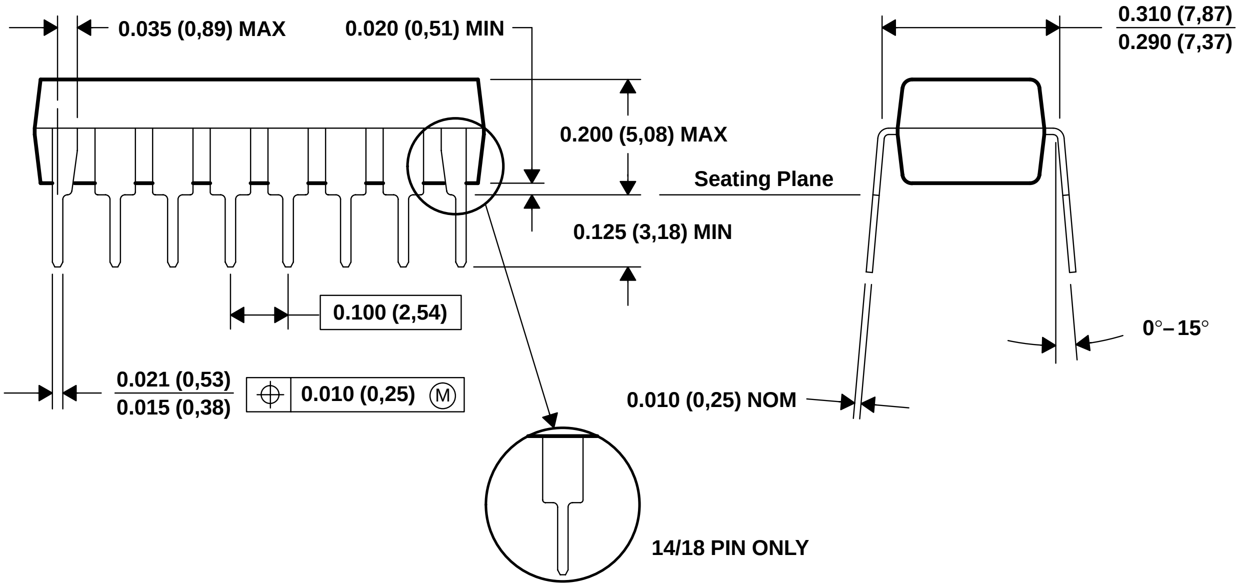
MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)





4040049/C 08/95

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC5620CD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC5620C
TLC5620CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC5620C
TLC5620CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC5620CN
TLC5620ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC5620I
TLC5620IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC5620I
TLC5620IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC5620IN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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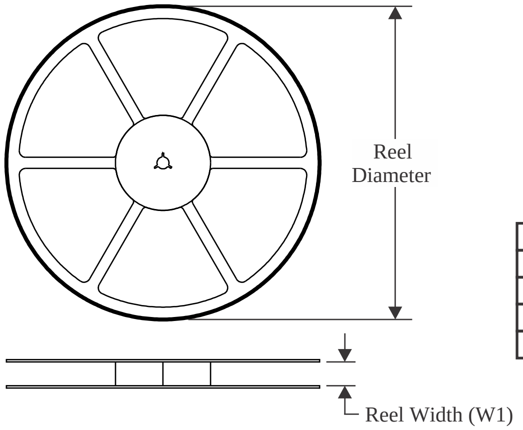
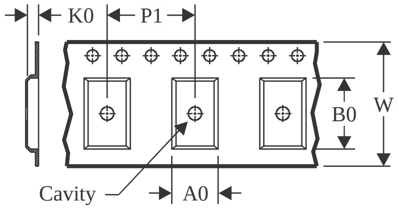
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

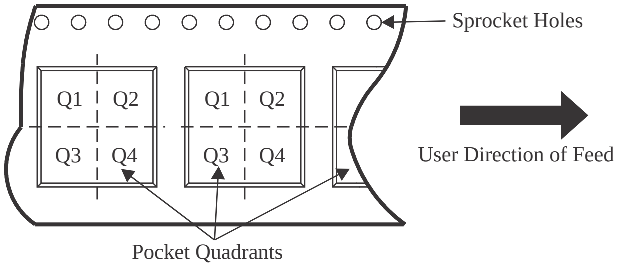


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

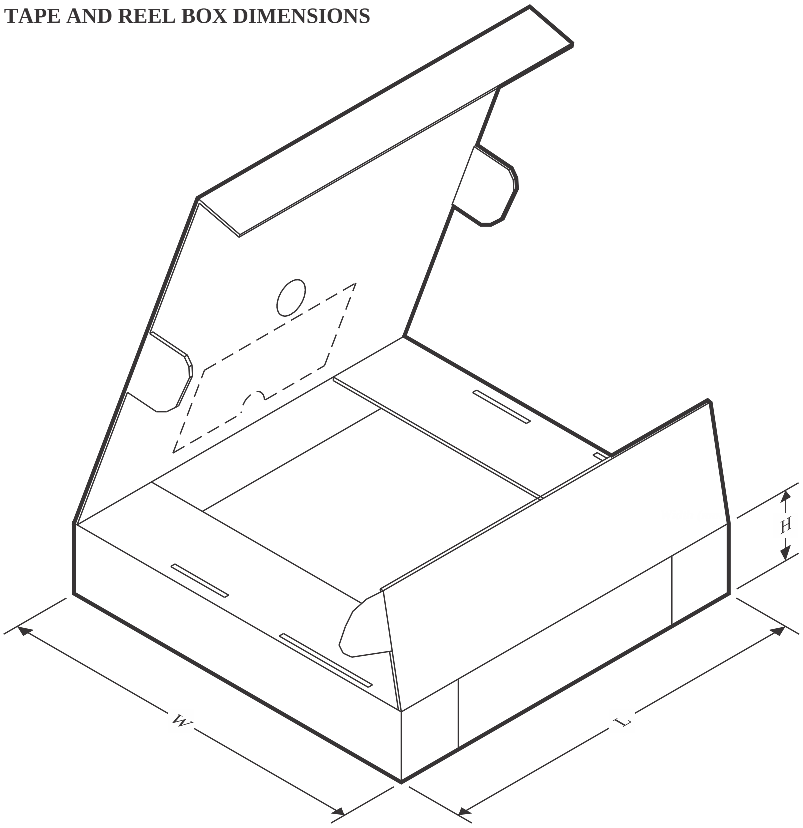
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5620CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5620IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

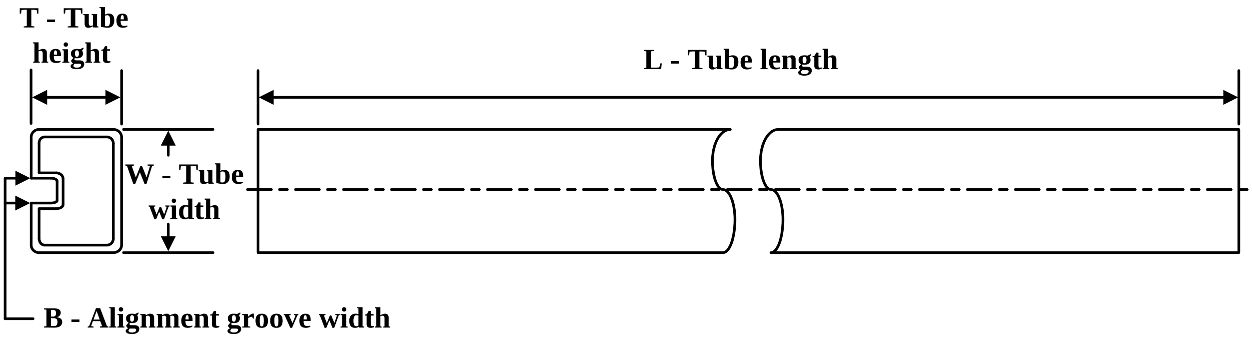
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5620CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC5620IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5620CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC5620CDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC5620CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC5620ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC5620IDG4	D	SOIC	14	50	505.46	6.76	3810	4
TLC5620IN	N	PDIP	14	25	506	13.97	11230	4.32

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