











TLC3702-Q1

SGLS156F-MARCH 2003-REVISED DECEMBER 2016

TLC3702-Q1 Dual Micropower LinCMOS™ Voltage Comparators

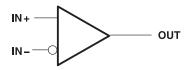
Features

- **Qualified for Automotive Applications**
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to +125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Devce CDM ESD Classification Level C4B
- Push-Pull CMOS Output Drives Capacitive Loads Without Pullup Resistor, $I_0 = \pm 8 \text{ mA}$
- Very Low Power...100 µW Typical at 5 V
- Fast Response Time... $t_{PLH} = 2.7 \mu s$ Typical With 5-mV Overdrive
- Single-Supply Operation...3 V to 16 V
- On-Chip ESD Protection

Applications

- Transmission Control Unit
- **Braking**
- **Engine Control**

Symbol (Each Comparator)



3 Description

The TLC3702-Q1 consists of two independent micropower voltage comparators. Compared to similar devices, the TLC3702-Q1 uses one-twentieth of the power for similar response times. This allows the device to react quickly to fast changing signals while extending the battery life.

The push-pull CMOS output stage drives capacitive loads directly without a power consuming pullup resistor to achieve the stated response time. Eliminating the pullup resistor not only reduces power dissipation but also saves board space component cost. Additionally, the output stage is fully compatible with all TTL and CMOS requirements.

Texas Instruments' LinCMOS™ process superior analog performance versus standard CMOS processes. Along with the standard advantages of low power without sacrificing speed, high input impedance and low bias currents, the LinCMOS process offers extremely stable input/offset voltages with large differential input voltages. This characteristic makes it possible to build reliable CMOS comparators.

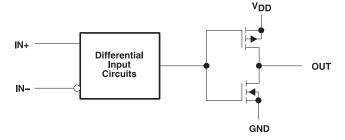
The TLC3702-Q1 has a wide supply range from 3 V to 16 V, allowing design flexibility. The voltage range also allows the device to handle start-stop applications and be connected directly to a standard 12-V battery. All of these features make the TLC3702-Q1 suitable for HEV/EV and powertrain system such as transmission control unit (TCU) and engine control.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)		
TI C2702 O4	SOIC (8)	4.90 mm × 3.91 mm		
TLC3702-Q1	TSSOP (8)	3.00 mm × 4.40 mm		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram (Each Comparator)



Page



Table of Contents

1	Features 1		8.3 Feature Description	13
2	Applications 1		8.4 Device Functional Modes	15
3	Description 1	9	Application and Implementation	16
4	Revision History2		9.1 Application Information	16
5	Pin Configuration and Functions3		9.2 Typical Applications	16
6	Specifications	10	Power Supply Recommendations	20
•	6.1 Absolute Maximum Ratings	11	Layout	20
	6.2 ESD Ratings		11.1 Layout Guidelines	20
	6.3 Recommended Operating Conditions		11.2 Layout Example	20
	6.4 Thermal Information	12	Device and Documentation Support	<mark>2</mark> 1
	6.5 Electrical Characteristics		12.1 Receiving Notification of Documentation Update	es <mark>21</mark>
	6.6 Switching Characteristics 5		12.2 Community Resources	<mark>21</mark>
	6.7 Typical Characteristics 6		12.3 Trademarks	21
7	Parameter Measurement Information 10		12.4 Electrostatic Discharge Caution	<mark>21</mark>
8	Detailed Description		12.5 Glossary	21
-	8.1 Overview 13	13	Mechanical, Packaging, and Orderable Information	21
	8.2 Functional Block Diagram 13		morniquoi!	21

4 Revision History

Changes from Revision E (August 2012) to Revision F

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

•	Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.	. 1
•	Deleted Ordering Information table; see POA at the end of the datasheet.	. 1
•	Changed the Description section	. 1
•	Changed Equation 2 in Detailed Design Procedure from "R2 + R1//R" to "R1 + R2//R"	17
•	Changed "Output is high" to "Output is low"	17
•	Deleted Enhanced Supply Supervisor schematics and Pulse-Width-Modulated Motor Speed Controller schematic	17
•	Added missing resistors to <i>Two-Phase Non-Overlapping Clock Generator</i> schematic and changed in NOTES A: from "1.85" to "2 × 1.71"	18
•	Deleted the Micropower Switching Regulator image	19

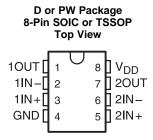
C	nanges from Revision D (February 2012) to Revision E	Page
•	Changed part numbers from TLC3702 to TLC3702-Q1	······································
•	Changed units for I _{IB} from dB to pA and nA	4

Submit Documentation Feedback

Copyright © 2003–2016, Texas Instruments Incorporated



5 Pin Configuration and Functions



Pin Functions

PIN I/O		1/0	DESCRIPTION
NAME	NO.		
1IN+	3	I	Non-Inverting input channel 1
1IN-	2	I	Inverting input channel 1
2IN+	5	1	Non-Inverting input channel 2
2IN-	6	1	Inverting input channel 2
1OUT	1	0	Output, Channel 1
1OUT	7	0	Output, Channel 2
GND	4	-	Negative (lowest) power supply
VDD	8	-	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V _{DD} ⁽²⁾		-0.3	18	V
Differential input voltage, V _{ID} ⁽³⁾		±18	V	
Input voltage, V _I	-0.3	V_{DD}	٧	
Output voltage, V _O	-0.3	V_{DD}	٧	
Input current, I _I			±5	mA
Output current, I _O (each output)		±20	mA	
Total supply current into V _{DD}			40	mA
Total current out of GND			40	mA
Continuous total power dissipation		See Therma	al Information	
Operating free-air temperature, T _A		-40	125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10	D package		260	°C
seconds	PW package		260	
Storage temperature, T _{stg}		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to GND.

(3) Differential voltages are at IN+ with respect to IN-.

Copyright © 2003–2016, Texas Instruments Incorporated



6.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	All pins	±2000	
		Charged-device model (CDM), per AEC	All pins except 1, 4, 5, and 8	±500	V
		Q100-011	Pins 1, 4, 5, and 8	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4	5	16	V
V _{IC}	Common-mode input voltage	0		V _{DD} - 1.5	V
I _{OH}	High-level output current			-20	mA
I _{OL}	Low-level output current			20	mA
T _A	Operating free-air temperature	-40		125	°C

6.4 Thermal Information

		TLC37	702-Q1	
	THERMAL METRIC ⁽¹⁾	D (SOIC)	PW (TSSOP)	UNIT
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.7	181.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.9	49.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.8	110.1	°C/W
ΨЈТ	Junction-to-top characterization parameter	15.3	2.4	°C/W
ΨЈВ	Junction-to-board characterization parameter	57.3	108.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	_	_	°C/W

For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at specified operating free-air temperature range, $V_{DD} = 5 \text{ V}$ (unless otherwise noted). See $^{(1)}$

	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
		V 5 V to 10 V	25°C		1.2	5	
V _{IO}	Input offset voltage	$V_{DD} = 5 \text{ V to } 10 \text{ V},$ $V_{IC} = V_{ICR} \text{min, See}$ (2)	-40°C to +125°C			10	mV
	land effect coment	V 05.V	25°C		1		A
I _{IO}	Input offset current	$V_{IC} = 2.5 \text{ V}$	125°C			15	pА
	Innut hing gurrant	V 25V	25°C		5		рА
I _{IB}	Input bias current	V _{IC} = 2.5 V	125°C			30	nA
			25°C	0 to V _{DD} - 1			
V _{ICR}	Common-mode input voltage range		-40°C to +125°C	0 to V _{DD} - 1.5			V
			25°C		84		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$	125°C		83		dB
			-40°C		82		
			25°C		85		
k _{SVR}	Supply-voltage rejection ratio	$V_{DD} = 5 \text{ V to } 10 \text{ V}$	125°C		85		dB
			-40°C		82		

(1) All characteristics are measured with zero common-mode voltage unless otherwise noted.

(2) The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

Submit Documentation Feedback

Copyright © 2003–2016, Texas Instruments Incorporated



Electrical Characteristics (continued)

at specified operating free-air temperature range, $V_{DD} = 5 \text{ V}$ (unless otherwise noted). See $^{(1)}$

	1 0	3 , DD (•			
	PARAMETER	TEST CONDITIONS	T _A	MIN	TYP	MAX	UNIT
	High level output voltege		25°C	4.5			
V _{OH}	High-level output voltage	$V_{ID} = 1 \text{ V}, I_{OH} = -4 \text{ mA}$	125°C	4.2			V
\/	Low lovel output voltage	V _{ID} = 1 V, I _{OH} = −4 mA	25°C		210	300	m\/
V _{OL}	Low-level output voltage		125°C			500	mV
	Overally source at the th		25°C		19	40	
I _{DD}	Supply current (both comparators)	Outputs low, No load	-40°C to +125°C			90	μΑ

6.6 Switching Characteristics

at recommended operating conditions, $V_{DD} = 5 \text{ V}$, $T_A = 25 ^{\circ}\text{C}$ (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS	MIN TYP	MAX	UNIT
			Overdrive = 2 mV	4.5		
			Overdrive = 5 mV	2.7		
	Propagation response time, low-to-high-level	f = 10 kHz, $C_L = 50 \text{ pF}$	Overdrive = 10 mV	1.9		μs
t _(PLH)	output (1)	OL = 30 pi	Overdrive = 20 mV	1.4		
			Overdrive = 40 mV	1.1		
		V _I = 1.4 V step at IN+		1.1		
	Propagation response time, high-to-low-level	f = 10 kHz, C _L = 50 pF	Overdrive = 2 mV	4		μs
			Overdrive = 5 mV	2.3		
			Overdrive = 10 mV	1.5		
t _(PHL)	output (1)		Overdrive = 20 mV	0.95		
			Overdrive = 40 mV	0.65		
		V _I = 1.4 V step at IN+		0.15		
t _f	Fall time	f = 10 kHz, C _L = 50 pF	Overdrive = 50 mV	50		ns
t _r	Rise time	f = 10 kHz, C _L = 50 pF	Overdrive = 50 mV	125		ns

⁽¹⁾ Simultaneous switching of inputs causes degradation in output response.

Copyright © 2003–2016, Texas Instruments Incorporated

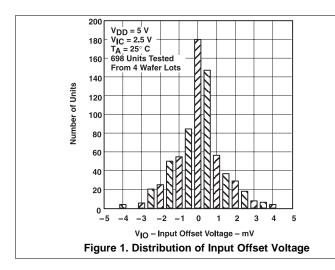


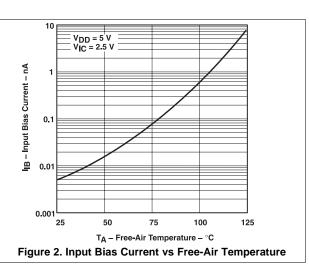
6.7 Typical Characteristics

Table 1. Table of Graphs

			FIGURE
V _{IO}	Input offset voltage	Distribution	Figure 1
I _{IB}	Input bias current	vs Free-air temperature	Figure 2
CMRR	Common-mode rejection ratio	vs Free-air temperature	Figure 3
k _{SVR}	Supply-voltage rejection ratio	vs Free-air temperature	Figure 4
V _{OH}	High-level output current	vs Free-air temperature	Figure 5
		vs High-level output current	Figure 6
V _{OL}	Low-level output voltage	vs Low-level output current	Figure 7
		vs Free-air temperature	Figure 8
t _t	Transition time	vs Load capacitance	Figure 9
	Supply current response	vs Time	Figure 10
	Low-to-high-level output response	Low-to-high level output propagation delay time	Figure 11
	High-to-low level output response	High-to-low level output propagation delay time	Figure 12
t _{PLH}	Low-to-high level output propagation delay time	vs Supply voltage	Figure 13
t _{PHL}	High-to-low level output propagation delay time	vs Supply voltage	Figure 14
		vs Frequency	Figure 15
I_{DD}	Supply current	vs Supply voltage	Figure 16
		vs Free-air temperature	Figure 17

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.





Submit Documentation Feedback

Copyright © 2003–2016, Texas Instruments Incorporated



Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.

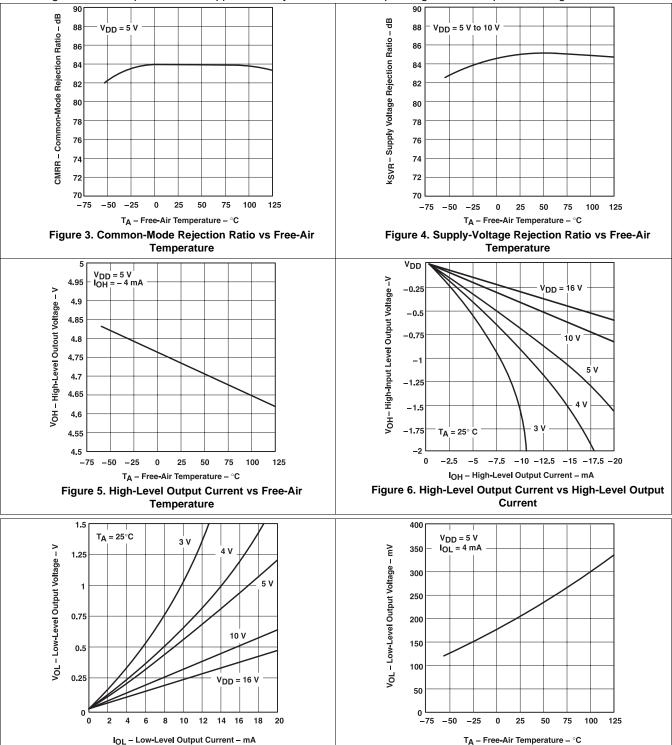


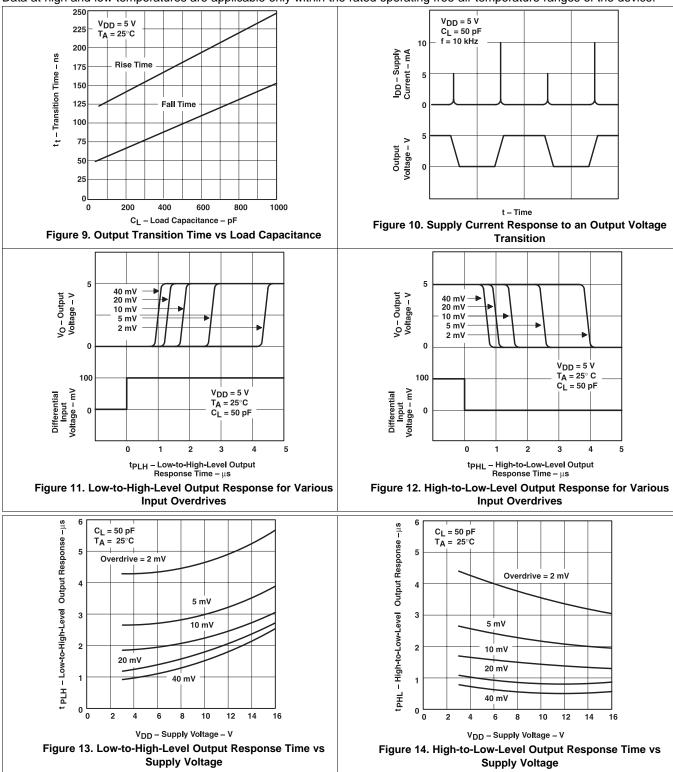
Figure 8. Low-Level Output Voltage vs Free-Air Temperature

Figure 7. Low-Level Output Voltage vs Low-Level Output

Current

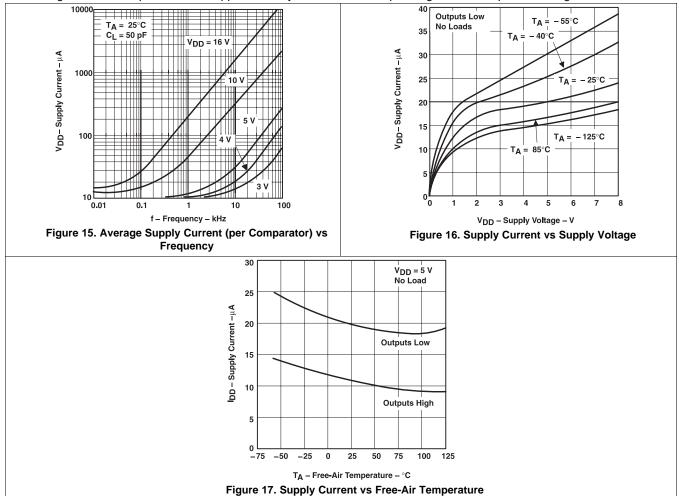


Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.





Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the device.



7 Parameter Measurement Information

CAUTION

The TLC3702-Q1 contains a digital output stage which, if held in the linear region of the transfer curve, can cause damage to the device.

Conventional operational amplifier and comparator testing incorporates the use of a servo loop which is designed to force the device output to a level within this linear region. Because the servo-loop method of testing cannot be used, the following alternatives are offered for measuring parameters such as input offset voltage, common-mode rejection, and so forth.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 18(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed to provide greater accuracy, as shown in Figure 18(b) for the V_{ICR} test. This slewing is done instead of changing the input voltages.

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal, but opposite in polarity, to the input offset voltage, the output changes states.

Figure 19 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching mode servo loop in which IC1a generates a triangular waveform of approximately 20-mV amplitude. IC1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test, while the noninverting input is driven by the output of the integrator formed by IC1c through the voltage divider formed by R8 and R9. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R8 and R9 provide an increase in input offset voltage by a factor of 100 to make measurement easier. The values of R5, R7, R8, and R9 can significantly influence the accuracy of the reading; therefore, TI recommends that their tolerance level be one percent or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

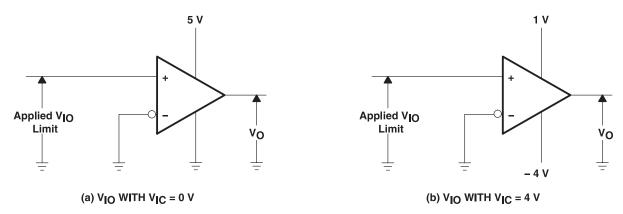


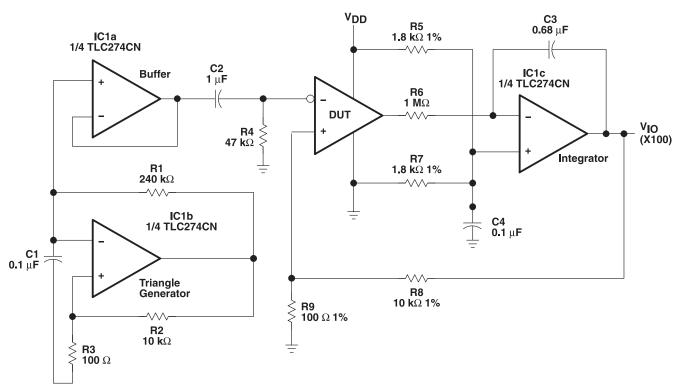
Figure 18. Method for Verifying That Input Offset Voltage Is Within Specified Limits

Submit Documentation Feedback

Copyright © 2003–2016, Texas Instruments Incorporated



Parameter Measurement Information (continued)



Copyright © 2016, Texas Instruments Incorporated

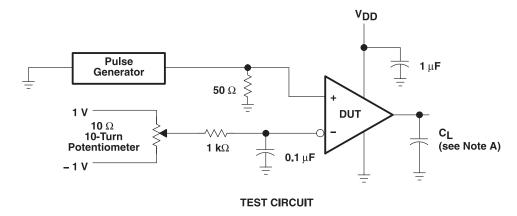
Figure 19. Circuit for Input Offset Voltage Measurement

Response time is defined as the interval between the application of an input step function and the instant when the output reaches 50% of its maximum value. Response time for the low-to-high-level output is measured from the leading edge of the input pulse, while response time for the high-to-low-level output is measured from the trailing edge of the input pulse. Response time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input as shown in Figure 20, so that the circuit is just at the transition point. A low signal, for example 105-mV or 5-mV overdrive, causes the output to change state

Copyright © 2003–2016, Texas Instruments Incorporated



Parameter Measurement Information (continued)



Overdrive Overdrive 100 mV Input 100 mV Input 90% 90% Low-to-High **High-to-Low** 50% **Level Output Level Output** 10% 10% ^tPLH ^tPHL

NOTE A: C_L includes probe and jig capacitance.

Figure 20. Response, Rise, and Fall Times Circuit and Voltage Waveforms

VOLTAGE WAVEFORMS

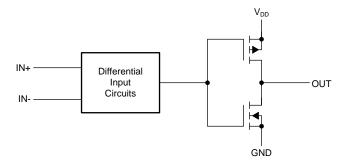


8 Detailed Description

8.1 Overview

The TLC3702-Q1 push-pull output comparator features a low quiescent current 20 uA and operation from 4 V to 16 V. The push-pull CMOS output stage drives capacitive loads directly without a power consuming pull-up resistor to achieve the stated response time.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 LinCMOS™ Process

The LinCMOS process is a linear polysilicon-gate CMOS process. Primarily designed for single-supply applications, LinCMOS products facilitate the design of a wide range of high-performance analog functions from operational amplifiers to complex mixed-mode converters.

While digital designers are experienced with CMOS, MOS technologies are relatively new for analog designers. This short guide is intended to answer the most frequently asked questions related to the quality and reliability of LinCMOS products. Further questions should be directed to the nearest TI field sales office.

8.3.2 Electrostatic Discharge

CMOS circuits are prone to gate oxide breakdown when exposed to high voltages even if the exposure is only for very short periods of time. Electrostatic discharge (ESD) is one of the most common causes of damage to CMOS devices. It can occur when a device is handled without proper consideration for environmental electrostatic charges, for example, during board assembly. If a circuit in which one amplifier from a dual op amp is being used and the unused pins are left open, high voltages tend to develop. If there is no provision for ESD protection, these voltages may eventually punch through the gate oxide and cause the device to fail. To prevent voltage buildup, each pin is protected by internal circuitry.

Standard ESD-protection circuits effectively shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltages but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting transistors during normal operation after an ESD voltage has occurred. Although these currents are small, on the order of tens of nanoamps, CMOS amplifiers are often specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed the patented ESD-protection circuit shown in Figure 21. This circuit can withstand several successive 2-kV ESD pulses, while reducing or eliminating leakage currents that may be drawn through the input pins. A more detailed discussion of the operation of the TI ESD-protection circuit is presented in the following sections.

All input and output pins on LinCMOS and Advanced LinCMOS products have associated ESD-protection circuitry that undergoes qualification testing to withstand 2000 V discharged from a 100-pF capacitor through a $1500-\Omega$ resistor (human body model) and 200 V from a 100-pF capacitor with no current-limiting resistor (charged device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

Copyright © 2003–2016, Texas Instruments Incorporated Submit Doc



Feature Description (continued)

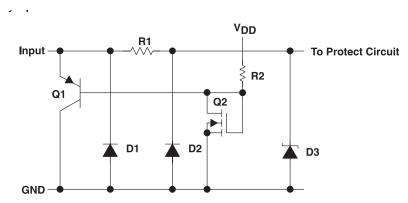


Figure 21. LinCMOS™ ESD-Protection Schematic

8.3.3 Input Protection Circuit Operation

TI's patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterized by extremely fast rise times and usually low energies, and can occur both when the device has all pins open and when it is installed in a circuit.

8.3.4 Positive ESD Transients

Initial positive charged energy is shunted through Q1 to V_{SS} . Q1 turns on when the voltage at the input rises above the voltage on the V_{DD} pin by a value equal to the V_{BE} of Q1. The base current increases through R2 with input current as Q1 saturates. The base current through R2 forces the voltage at the drain and gate of Q2 to exceed its threshold level ($V_T \sim 22$ to 26 V) and turn Q2 on. The shunted input current through Q1 to V_{SS} is now shunted through the N-channel enhancement-type MOSFET Q2 to V_{SS} . If the voltage on the input pin continues to rise, the breakdown voltage of the zener diode D3 is exceeded and all remaining energy is dissipated in R1 and D3. The breakdown voltage of D3 is designed to be 24 V to 27 V, which is well below the gate-oxide voltage of the circuit to be protected.

8.3.5 Negative ESD Transients

The negative charged ESD transients are shunted directly through D1. Additional energy is dissipated in R1 and D2 as D2 becomes forward biased. The voltage seen by the protected circuit is −0.3 V to −1 V (the forward voltage of D1 and D2).

8.3.6 Circuit-Design Considerations

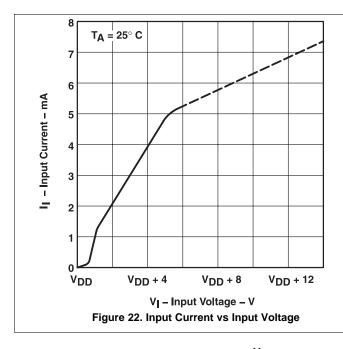
LinCMOS products are being used in actual circuit environments that have input voltages that exceed the recommended common-mode input voltage range and activate the input protection circuit. Even under normal operation, these conditions occur during circuit power up or power down, and in many cases, when the device is being used for a signal conditioning function. The input voltages can exceed V_{ICR} and not damage the device only if the inputs are current limited. The recommended current limit shown on most product data sheets is ± 5 mA. Figure 22 and Figure 23 show typical characteristics for input voltage versus input current.

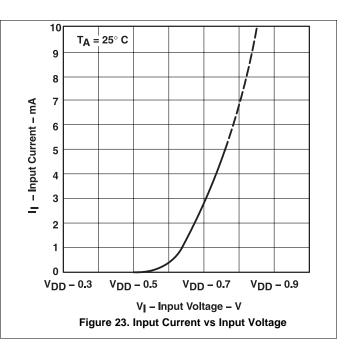
Normal operation and correct output state can be expected even when the input voltage exceeds the positive supply voltage. Again, the input current should be externally limited even though internal positive current limiting is achieved in the input protection circuit by the action of Q1. When Q1 is on, it saturates and limits the current to approximately 5-mA collector current by design. When saturated, Q1 base current increases with input current. This base current is forced into the V_{DD} pin and into the device I_{DD} or the V_{DD} supply through R2 producing the current limiting effects shown in Figure 22. This internal limiting lasts only as long as the input voltage is below the V_T of Q2.

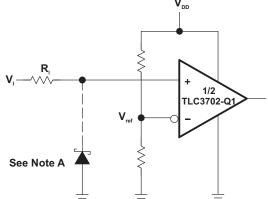


Feature Description (continued)

When the input voltage exceeds the negative supply voltage, normal operation is affected and output voltage states may not be correct. Also, the isolation between channels of multiple devices (duals and quads) can be severely affected. External current limiting must be used since this current is directly shunted by D1 and D2 and no internal limiting is achieved. If normal output voltage states are required, an external input voltage clamp is required (see Figure 24).







Positive Voltage Input Current Limit:

$$R_{_{I}} \ = \ \frac{V_{_{I}} - V_{_{DD}} - 0.3 \ V}{5 \ mA}$$

Negative Voltage Input Current Limit:

$$R_{_{I}} = \frac{-V_{_{I}} - V_{_{DD}} - (-0.3 \text{ V})}{5 \text{ mA}}$$

Copyright © 2016, Texas Instruments Incorporated

A. If the correct input state is required when the negative input exceeds GND, a Schottky clamp is required.

Figure 24. Typical Input Current-Limiting Configuration for a LinCMOS™ Comparator

8.4 Device Functional Modes

The TLC3702-Q1 is powered on when the supply is connected. The device can operate with single or dual supply, depending on the application. The device is in its full performance once the supply is above the recommended value.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The inputs should always remain within the supply rails to avoid forward biasing the diodes in the electrostatic discharge (ESD) protection structure. If either input exceeds this range, the device is not damaged as long as the input is limited to less than 5 mA. To maintain the expected output state, the inputs must remain within the common-mode range. For example, at 25°C with $V_{DD} = 5$ V, both inputs must remain between -0.2 V and 4 V to ensure proper device operation.

To ensure reliable operation, the supply should be decoupled with a capacitor (0.1 μ F) that is positioned as close to the device as possible.

The TLC3702-Q1 has internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

9.2 Typical Applications

9.2.1 Achieving Greater Noise Immunity

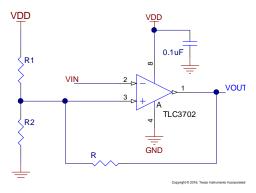


Figure 25. Application Adding Hysteresis to the TLC3702-Q1

9.2.1.1 Design Requirements

Figure 25 shows a typical topology used to introduce additional hysteresis. The additional hysteresis depends on the external resistors value and the supply voltage VDD.

Table 2. Design Parameters

PARAMETER	VALUE
Supply voltage	5 V
VIN	2.5 V and 50 mV noise on top
Ceramic capacitor	XR5 or XR7 50V
Hysteresis V+(H) - V+(-)	70 mV
R1, R2	27K 1%
R	1ΜΩ 1%

Product Folder Links: TLC3702-Q1



9.2.1.2 Detailed Design Procedure

This circuit is designed for stabilizing the output in a noisy environment by adding external hysteresis. The hysteresis is added by connecting a feedback resistor between positive input V+ and output VOUT. Output is high and VOUT = VDD, the positive input V+(H) = VDD

$$\frac{R2}{R2 + R1//R} \text{ VDD} \tag{1}$$

Output is low and VOUT = GND, the positive input V+(L) =

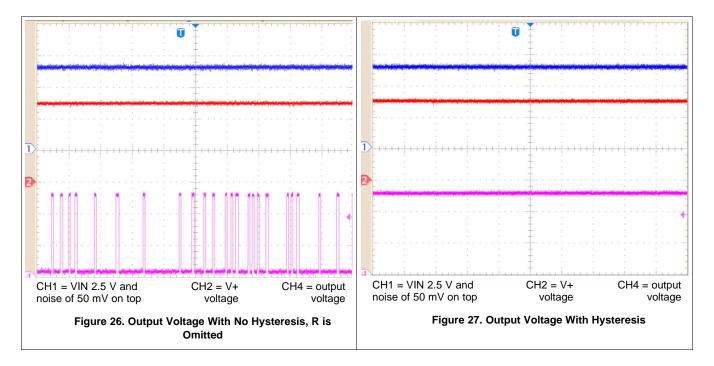
$$\frac{R2//R}{R1+R2//R} VDD \tag{2}$$

From Equation 1 and Equation 2:

$$\frac{R}{R1} = \frac{V + (L)}{V + (H) - V + (L)}$$
(3)

$$\frac{R2}{R1} = \frac{V + (L)}{VDD - V + (H)} \tag{4}$$

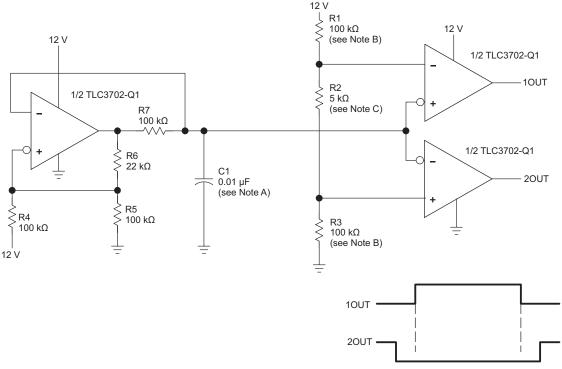
9.2.1.3 Application Curves



Copyright © 2003–2016, Texas Instruments Incorporated

TEXAS INSTRUMENTS

9.2.2 Two-Phase Non-Overlapping Clock Generator



NOTES: A. Adjust C1 for a change in oscillator frequency where: $1/f = 2 \times 1.71 (100 \text{ k}\Omega)\text{C1}$

- B. Adjust R1 and R3 to change duty cycle
- C. Adjust R2 to change deadtime

Copyright © 2016, Texas Instruments Incorporated

Figure 28. Two-Phase Non-Overlapping Clock Generator

9.2.2.1 Design Requirements

Table 3 lists the design parameters.

Table 3. Design Parameters

PARAMETER	VALUE				
Supply voltage	3 V to 12 V				
Ceramic capacitor	XR5 or XR7 50 V				
Resistors	1%				

9.2.2.2 Detailed Design Procedure

The first stage is a window comparator with positive feedback by connecting R6 between the comparator output and the positive input. That creates an external hysteresis depending on resistors R4, R5, R6 value and the supply voltage VDD.

Comparator output is high gives V+(H) =

$$\frac{R5}{R5 + R4 / /R6} VDD \tag{5}$$

Comparator output is low gives V+(L) =

$$\frac{R5 \, / \, /R6}{R4 + R5 \, / \, /R6} \, VDD$$

(6)



The negative feedback between capacitor C1 and the comparator negative input allows the capacitor to charge between 2 threshold V+(H) and V+(L). The charging and discharging is exponential with time constant of R7C1. The charging and discharging have the same duration.

C1 is charging during the time when output is high and the voltage across it is:

$$Vc(t) = VDD \left(1 - e^{-\frac{t}{R7C1}}\right)$$
(7)

The charging time is:

$$R7C1 \times Ln\left(\frac{VDD - V + (L)}{VDD - V + (H)}\right)$$
(8)

The charging and discharging time is:

$$T = 2 \times R7C1 \times Ln\left(\frac{VDD - V + (L)}{VDD - V + (H)}\right)$$
(9)

and the oscillator frequency is:

$$F = \frac{1}{2 \times R7C1 \times Ln\left(\frac{VDD - V + (L)}{VDD - V + (H)}\right)}$$
(10)

For the circuit of Figure 28, V+(L) = 1.83 V, V+(H) = 10.17 V and period T = 3.43 mS

This circuit can also be used for Frequency Dithering in switch mode power supply to pass EMC compliance.

The second stage forms 2 window comparators with complementary outputs. One output 10UT is high when

$$Vc > \frac{R2 + R3}{R1 + R2 + R3} VDD$$
 (11)

VDD and 2OUT is high when

$$Vc < \frac{R3}{R1+R2+R3}VDD \tag{12}$$

Copyright © 2003–2016, Texas Instruments Incorporated

10 Power Supply Recommendations

The TLC3702-Q1 comparator is specified for use on a single supply from 3 V to 16 V (or a dual supply from ± 1.5 V to ± 8 V) over a temperature range of -40° C to $\pm 125^{\circ}$ C. The device continues to function below this range, but performance is not specified. Place bypass capacitors close to the power supply pins to reduce noise coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

For any high-speed comparator or amplifier, proper design and printed-circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.

- Minimizing resistance from the signal source to the comparator input is necessary in order to minimize the
 propagation delay of the complete circuit. The source resistance along with input and stray capacitance
 creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency
 signals. The input capacitance of the TLC3702-Q1 device along with stray capacitance from an input pin to
 ground results in several picofarads of capacitance.
- The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2-μF tantalum capacitor do not need to be as close to the device as the 0.1-μF capacitor, and may be shared with other devices. The 2.2-μF capacitor buffers the power-supply line against ripple, and the 0.1-μF capacitor provides a charge for the comparator during high frequency switching.
- In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.
- Figure 29 shows an evaluation layout for the TLC3702-Q1 SOIC-8 package. C1 and C2 are power-supply bypass capacitors. Place the 0.1-µF capacitor closest to the comparator. Figure 25 shows a schematic of this circuit.

11.2 Layout Example

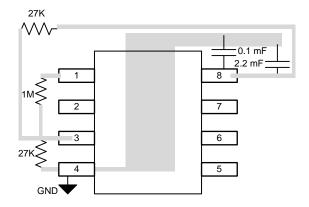


Figure 29. Layout Example



12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

LinCMOS, E2E are trademarks of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: TLC3702-Q1

Copyright © 2003-2016, Texas Instruments Incorporated

www.ti.com 4-Nov-2025

PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TLC3702QDRQ1	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702Q1
TLC3702QDRQ1.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3702Q1
TLC3702QPWRQ1	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3702Q1
TLC3702QPWRQ1.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	3702Q1

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents Tl's knowledge and belief as of the date that it is provided. Tl bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. Tl has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. Tl and Tl suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC3702-Q1:

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

www.ti.com 4-Nov-2025

● Enhanced Product : TLC3702-EP

Military : TLC3702M

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

● Enhanced Product - Supports Defense, Aerospace and Medical Applications

• Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC3702QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC3702QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2025



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC3702QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
TLC3702QPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0



SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale, TI's General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025