TLC27L1x Low-Power Operational Amplifiers

1 Features

- Input offset voltage drift: typically 0.1μV/month, including the first 30 days
- Wide range of supply voltages over specified temperature range:
  - 0°C to 70°C: 3V to 16V
  - −40°C to +85°C: 4V to 16V
- Single-supply operation
- Common-mode input voltage range extends below the negative rail
- Low noise: 68nV/√Hz, typically at f = 1kHz
- Output voltage range includes negative rail
- High input impedance: $10^{12}\Omega$, typical
- ESD-protection circuitry
- Small-outline package option also available in tape and reel
- Designed-in latch-up immunity

2 Applications

- Smoke and heat detector
- Field transmitter and sensor
  - Flow transmitter
  - Pressure transmitter
  - Temperature transmitter
  - Level transmitter
- Motion detector

3 Description

The TLC27L1x operational amplifiers combine a wide range of input offset-voltage grades with low offset-voltage drift and high input impedance. In addition, the TLC27L1x is a low-bias version of the TLC271 programmable amplifier. These devices use the Texas Instruments silicon-gate LinCMOS technology, which provides offset-voltage stability far exceeding the stability available with conventional metal-gate processes.

Two offset-voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC27L1 (10mV) to the TLV27L1A (5mV) low-offset version. The extremely high input impedance and low bias currents, in conjunction with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

In general, many features associated with bipolar technology are available in LinCMOS operational amplifiers, without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are all easily designed with the TLC27L1x. The devices also exhibit low-voltage, single-supply operation, making them an excellent choice for remote and inaccessible battery-powered applications. The common-mode input-voltage range includes the negative rail.

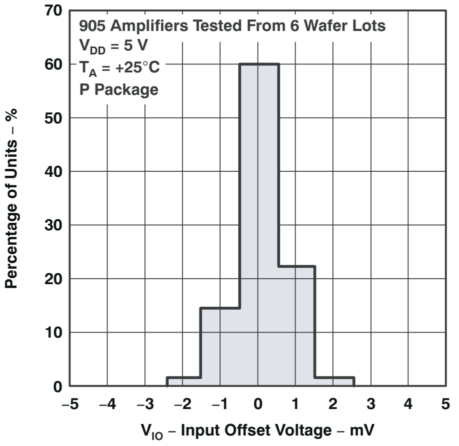
The TLC27L1x incorporate internal electrostatic-discharge (ESD) protection circuits that prevent functional failures at voltages up to 2000V as tested under MIL-STD-883C, Method 3015.2. However, exercise care when handling these devices because exposure to ESD can result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to +85°C.

Device Information

PART NUMBER	V_{IOmax} AT 25°C	PACKAGE[1]
TLC27L1	10mV	D (SOIC, 8)
		P (PDIP, 8)
TLC27L1A	5mV	P (PDIP, 8)

[1] For more information, see Section 10.



Sample Distribution of Input Offset Voltage

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4 Pin Configuration and Functions

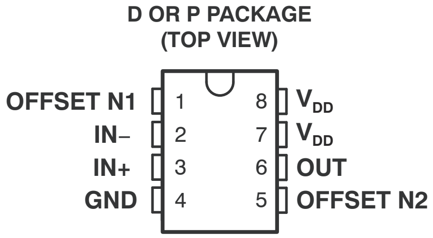


Figure 4-1. D Package,8-Pin SOIC, or P Package, 8-Pin PDIP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	4	Ground	Ground or negative (lowest) power supply
IN+	3	Input	Noninverting input
IN–	2	Input	Inverting input
OFFSET N1	1	Input	On legacy silicon: IN– offset adjustment pin (bias-select). On new silicon: NC, non internally connected pin
OFFSET N2	5	Input	On legacy silicon: IN+ offset adjustment pin (bias-select). On new silicon: NC, non internally connected pin
OUT	6	Output	Output
V_{DD}	7, 8	Power	Positive (highest) power supply

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted(1)

			MIN	MAX	UNIT
V_{DD} (2)	Supply voltage			18	V
V_{ID} (3)	Differential input voltage			$\pm V_{DD}$	V
V_I (any input)	Input voltage		–0.3	V_{DD}	V
I_I	Input current			±5	mA
I_O	Output current			±30	mA
	Duration of short-circuit current at (or less than) T_A = 25°C(4)		Unlimited		
	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature	C suffix	0	70	°C
		I suffix	–40	85	
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds			260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground.
(3) Differential voltages are at the IN+ with respect to IN–.
(4) The output is able to be shorted to either supply. Limit temperature, supply voltages, or both to not exceed the maximum dissipation ratings (see Section 7.1.6).

5.2 Dissipation Ratings

PACKAGE	$T_A \leq 25°C$ POWER RATING	$T_A > 25°C$ DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8 mW/°C	640 mW	520 mW

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage	C suffix	3	16	V
		I suffix	4	16	
V_{IC}	Common-mode input voltage	V_{DD} = 5V	–0.2	3.5	V
		V_{DD} = 10V	–0.2	8.5	
T_A	Operating free-air temperature	C suffix	0	+70	°C
		I suffix	–40	+85	

5.4 Electrical Characteristics, C Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L1C, TLC27L1AC						UNIT
				V_{DD} = 5V			V_{DD} = 10V			
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}V_{IO}$	Input offset voltage	TLC27L1C, V_O = 1.4V, V_{IC} = 0V, R_S = 50Ω, R_I = 1MΩ	25°C		1.1	10		1.1	10	mV
			0°C to 70°C			12			12	mV
		TLC27L1AC, V_O = 1.4V, V_{IC} = 0V, R_S = 50Ω, R_I = 1MΩ	25°C		0.9	5		0.9	5	mV
			0°C to 70°C			6.5			6.5	mV
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current[1] [2]	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.5	60		0.5	60	pA
			70°C		7	300		8	300	pA
I_{IB}	Input bias current[1] [2]	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6	60		0.7	60	pA
			70°C		40	600		50	600	pA
V_{ICR}	Common-mode input voltage range[3]		25°C	–0.2 to +4	–0.2 to +4.2		–0.2 to +9	–0.2 to +9.2		V
			0°C to 70°C	–0.2 to +3.5			–0.2 to +8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100mV, R_L = 1MΩ	25°C	3.2	4.1		8	8.9		V
			0°C	3	4.1		7.8	8.9		V
			70°C	3	4.2		7.8	8.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100mV, I_{OL} = 0mA	25°C		1	50		5	50	mV
			0°C		1	50		5	50	mV
			70°C		1	50		5	50	mV
A_{VD}	Large-signal differential voltage amplification	R_L = 1MΩ[4]	25°C	50	520		50	870		V/mV
			0°C	50	700		50	1030		V/mV
			70°C	50	380		50	660		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	87		65	94		dB
			0°C	60	85		60	93		dB
			70°C	60	85		60	93		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		70	97		dB
			0°C	60	97		60	97		dB
			70°C	60	98		60	98		dB
$I_{I(SEL)}$	Offset adjustment pin input current (BIAS SELECT)	$V_{I(SEL)}$ = V_{DD}, legacy silicon	25°C		65			95		nA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, no load	25°C		10	17		14	23	μA
			0°C		12	21		18	33	μA
			70°C		8	14		11	20	μA

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.
(4) At V_{DD} = 5V, V_O = 0.25V to 2V; at V_{DD} = 10V, V_O = 1V to 6V.

5.5 Operating Characteristics, V_{DD} = 5V, C Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L1C, TLC27L1AC			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{I(PP)}$ = 1V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.03		V/µs
			0°C		0.04		
			70°C		0.03		
		$V_{I(PP)}$ = 2.5V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.03		
			0°C		0.03		
			70°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2	25°C		68		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20pF, R_L = 1MΩ, see Figure 6-1	25°C		5		kHz
			0°C		6		
			70°C		4.5		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3	25°C		85		kHz
			0°C		100		
			70°C		65		
φ_m	Phase margin	V_I = 10mV, f = B_1, C_L = 20pF, see Figure 6-3	25°C		34		°
			0°C		36		
			70°C		30		

5.6 Operating Characteristics, V_{DD} = 10V, C Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L1C, TLC27L1AC			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{I(PP)}$ = 1V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.05		V/µs
			0°C		0.05		
			70°C		0.04		
		$V_{I(PP)}$ = 5.5V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.04		
			0°C		0.05		
			70°C		0.04		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2	25°C		68		$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20pF, R_L = 1MΩ, see Figure 6-1	25°C		1		kHz
			0°C		1.3		
			70°C		0.9		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3	25°C		110		kHz
			0°C		110		
			70°C		90		
φ_m	Phase margin	V_I = 10mV, f = B_1, C_L = 20pF, see Figure 6-3	25°C		38		°
			0°C		40		
			70°C		34		

5.7 Electrical Characteristics, I Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L1I						UNIT
				V_{DD} = 5V			V_{DD} = 10V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4V, V_{IC} = 0V, R_S = 50Ω, R_I = 1MΩ	25°C		1.1	10		1.1	10	mV
			–40°C to +85°C			13			13	mV
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current[(1)](2)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.5	60		0.5	60	pA
			85°C		24	1000		26	1000	pA
I_{IB}	Input bias current[(1)](2)	V_O = V_{DD}/2, V_{IC} = V_{DD}/2	25°C		0.6	60		0.7	60	pA
			85°C		200	2000		220	2000	pA
V_{ICR}	Common-mode input voltage range(3)		25°C	–0.2 to +4	–0.2 to 4.2		–0.2 to +9	–0.2 to +9.2		V
			–40°C to +85°C	–0.2 to +3.5			–0.2 to +8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100mV, R_L = 1MΩ	25°C	3	4.1		8	8.9		V
			–40°C	3	4.1		7.8	8.9		V
			85°C	3	4.2		7.8	8.9		V
V_{OL}	Low-level output voltage	V_{ID} = −100mV, I_{OL} = 0mA	25°C		1	50		5	50	mV
			–40°C		1	50		5	50	mV
			85°C		1	50		5	50	mV
A_{VD}	Large-signal differential voltage amplification	R_L = 1MΩ(4)	25°C	50	520		50	870		V/mV
			–40°C	50	900		50	1550		V/mV
			85°C	50	330		50	585		V/mV
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	65	87		65	94		dB
			–40°C	60	85		60	93		dB
			85°C	60	85		60	93		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5V to 10V, V_O = 1.4V	25°C	70	97		70	97		dB
			–40°C	60	97		60	97		dB
			85°C	60	98		60	98		dB
$I_{I(SEL)}$	Offset adjustment pin input current (BIAS SELECT)	$V_{I(SEL)}$ = V_{DD}, legacy silicon	25°C		65			95		nA
I_{DD}	Supply current	V_O = V_{DD}/2, V_{IC} = V_{DD}/2, no load	25°C		10	17		14	23	μA
			–40°C		16	27		25	43	μA
			85°C		17	13		10	18	μA

(1) Typical values of input bias current and input offset current less than 5pA determined mathematically.
(2) Values specified by characterization.
(3) This range also applies to each input individually.
(4) At V_{DD} = 5V, V_O = 0.25V to 2V; at V_{DD} = 10V, V_O = 1V to 6V.

5.8 Operating Characteristics, V_{DD} = 5V, I Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L1I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{I(PP)}$ = 1V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.03		V/µs
			–40°C		0.04		
			85°C		0.03		
		$V_{I(PP)}$ = 2.5V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.03		
			–40°C		0.04		
			85°C		0.02		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20pF, R_L = 1MΩ, see Figure 6-1	25°C		5		kHz
			–40°C		7		
			85°C		4		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3	25°C		85		kHz
			–40°C		110		
			85°C		55		
φ_m	Phase margin	V_I = 10mV, f = B_1, C_L = 20pF, see Figure 6-3	25°C		34		°
			–40°C		38		
			85°C		28		

5.9 Operating Characteristics, V_{DD} = 10V, I Suffix

at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	TLC27L1I			UNIT
				MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{I(PP)}$ = 1V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.05		V/µs
			–40°C		0.06		
			85°C		0.03		
		$V_{I(PP)}$ = 5.5V, R_L = 1MΩ, C_L = 20pF, see Figure 6-1	25°C		0.04		
			–40°C		0.05		
			85°C		0.03		
V_n	Equivalent input noise voltage	f = 1kHz, R_S = 20Ω, see Figure 6-2	25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20pF, R_L = 1MΩ, see Figure 6-1	25°C		1		kHz
			–40°C		1.4		
			85°C		0.8		
B_1	Unity-gain bandwidth	V_I = 10mV, C_L = 20pF, see Figure 6-3	25°C		110		kHz
			–40°C		110		
			85°C		80		
φ_m	Phase margin	V_I = 10mV, f = B_1, C_L = 20pF, see Figure 6-3	25°C		38		°
			–40°C		42		
			85°C		32		

5.10 Typical Characteristics

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

Table of Graphs

TYPICAL CHARACTERISTIC			FIGURE
V_{IO}	Input offset voltage	Distribution	Figure 5-1, Figure 5-2
αV_{IO}	Temperature coefficient	Distribution	Figure 5-3, Figure 5-4
V_{OH}	High-level output voltage	vs High-level output current	Figure 5-5, Figure 5-6
		vs Supply voltage	Figure 5-7
		vs Free-air temperature	Figure 5-8
V_{OL}	Low-level output voltage	vs Common-mode input voltage	Figure 5-9, Figure 5-10
		vs Differential input voltage	Figure 5-11
		vs Free-air temperature	Figure 5-12
		vs Low-level output current	Figure 5-13, Figure 5-14
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage	Figure 5-15
		vs Free-air temperature	Figure 5-16
		vs Frequency	Figure 5-25, Figure 5-26
I_{IB}	Input bias current	vs Free-air temperature	Figure 5-17
I_{IO}	Input offset current	vs Free-air temperature	Figure 5-17
V_I	Maximum input voltage	vs Supply voltage	Figure 5-18
I_{DD}	Supply current	vs Supply voltage	Figure 5-19
		vs Free-air temperature	Figure 5-20
SR	Slew rate	vs Supply voltage	Figure 5-21
		vs Free-air temperature	Figure 5-22
	Bias-select current	vs Supply voltage	Figure 5-23
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	Figure 5-24
φ_m	Phase margin	vs Supply voltage	Figure 5-27
		vs Free-air temperature	Figure 5-28
		vs Capacitive load	Figure 5-29
V_n	Equivalent input noise voltage	vs Frequency	Figure 5-30
	Phase shift	vs Frequency	Figure 5-25, Figure 5-26

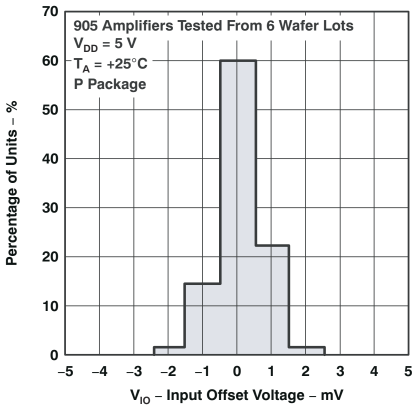


Figure 5-1. Distribution of TLC27L1 Input Offset Voltage

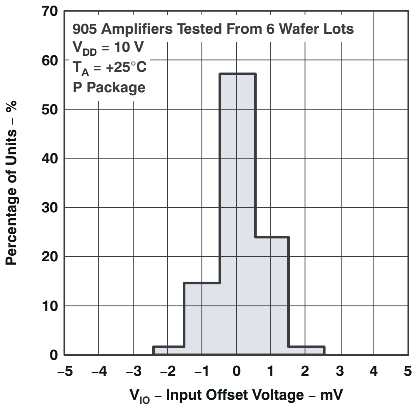


Figure 5-2. Distribution of TLC27L1 Input Offset Voltage

5.10 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

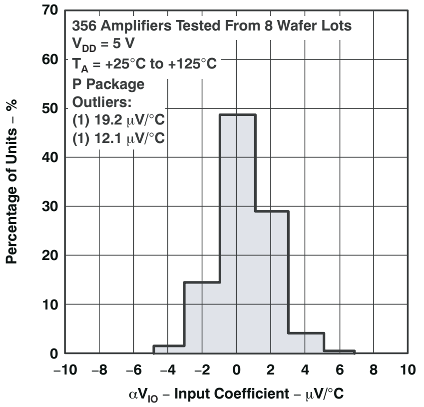


Figure 5-3. Distribution of TLC27L1 Input Offset Voltage Temperature Coefficient

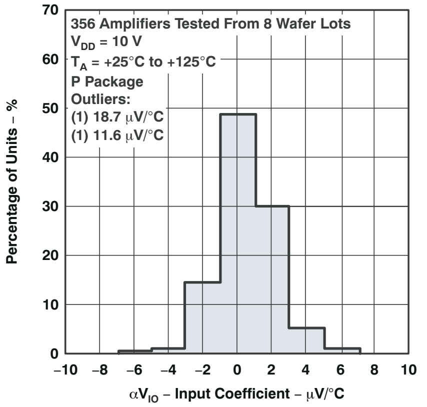


Figure 5-4. Distribution of TLC27L1 Input Offset Voltage Temperature Coefficient

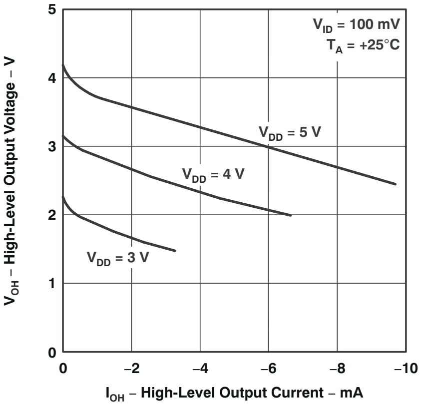


Figure 5-5. High-Level Output Voltage vs High-Level Output Current

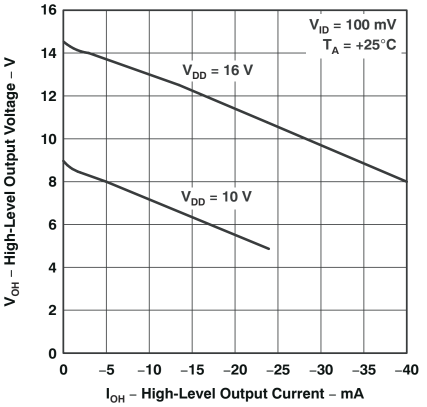


Figure 5-6. High-Level Output Voltage vs High-Level Output Current

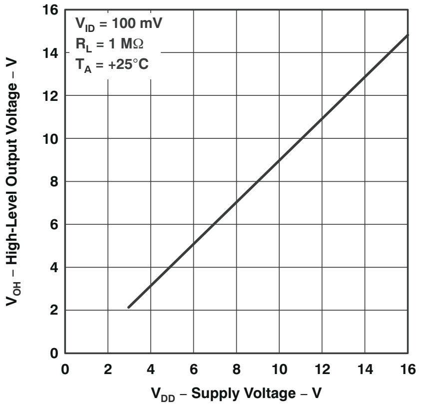


Figure 5-7. High-Level Output Voltage vs Supply Voltage

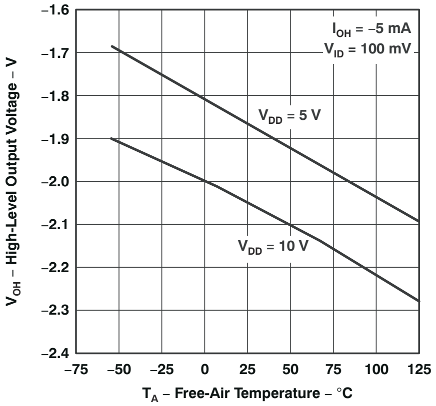


Figure 5-8. High-Level Output Voltage vs Free-Air Temperature

5.10 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

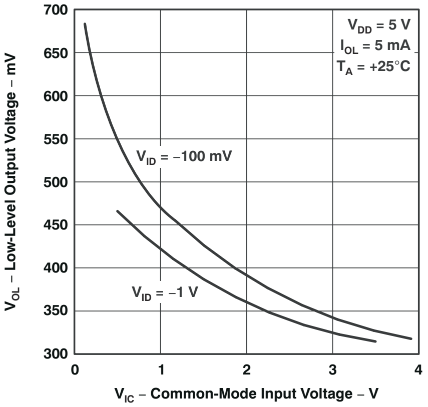


Figure 5-9. Low-Level Output Voltage vs Common-Mode Input Voltage

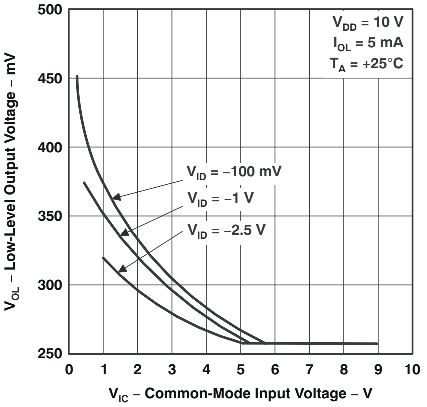


Figure 5-10. Low-Level Output Voltage vs Common-Mode Input Voltage

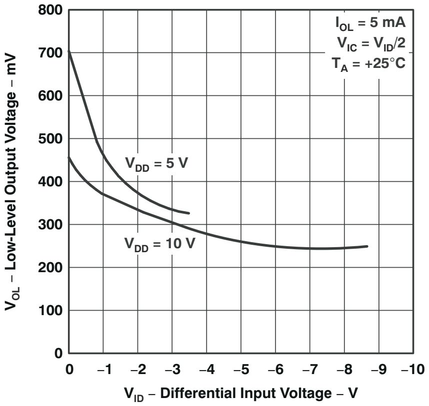


Figure 5-11. Low-Level Output Voltage vs Differential Input Voltage

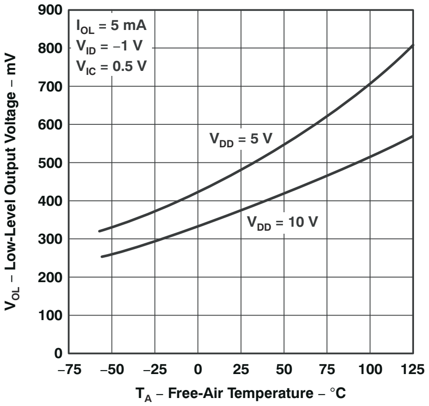


Figure 5-12. Low-Level Output Voltage vs Free-Air Temperature

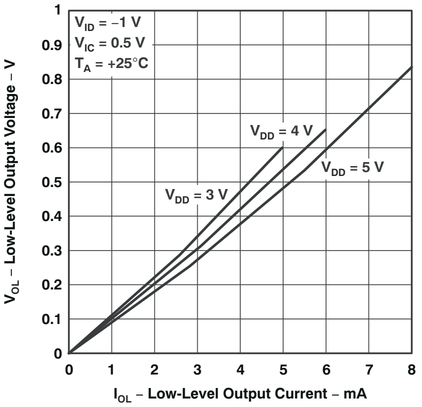


Figure 5-13. Low-Level Output Voltage vs Low-Level Output Current

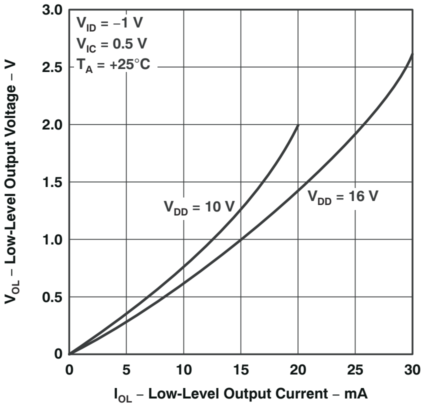


Figure 5-14. Low-Level Output Voltage vs Low-Level Output Current

5.10 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

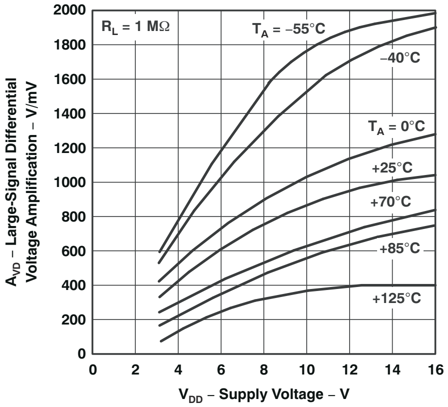


Figure 5-15. Large-Signal differential Voltage Amplification vs Supply Voltage

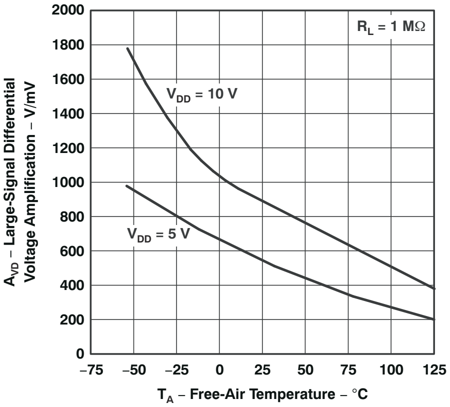
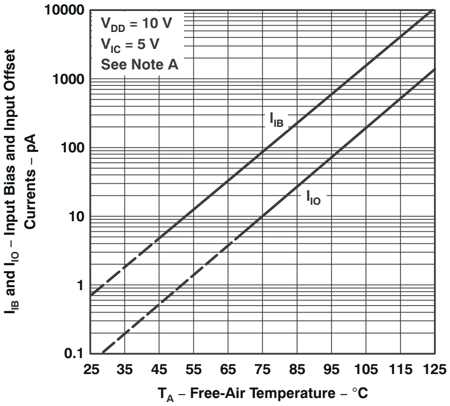


Figure 5-16. Large-Signal Differential Voltage Amplification vs Free-Air Temperature



Typical values of input bias current and input offset current less than 5pA determined mathematically

Figure 5-17. Input Bias and Input Offset Currents vs Free-Air Temperature

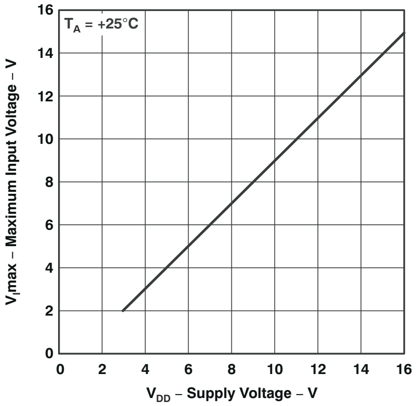


Figure 5-18. Maximum Input Voltage vs Supply Voltage

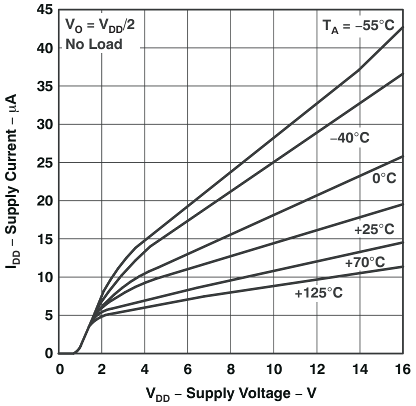


Figure 5-19. Supply Current vs Supply Voltage

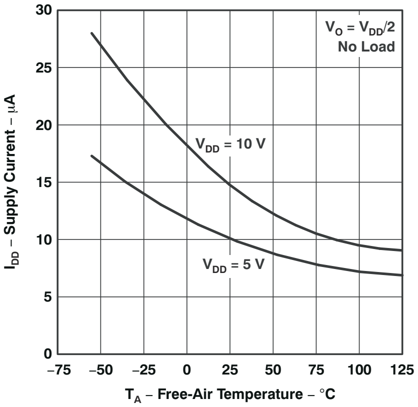


Figure 5-20. Supply Current vs Free-Air Temperature

5.10 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

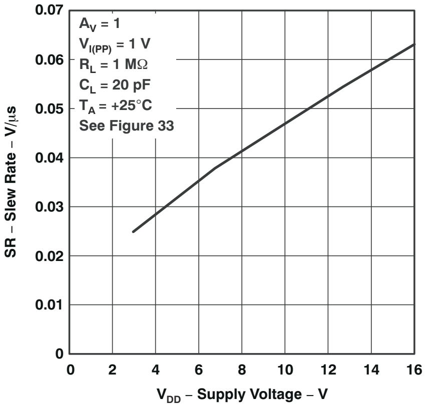


Figure 5-21. Slew Rate vs Supply Voltage

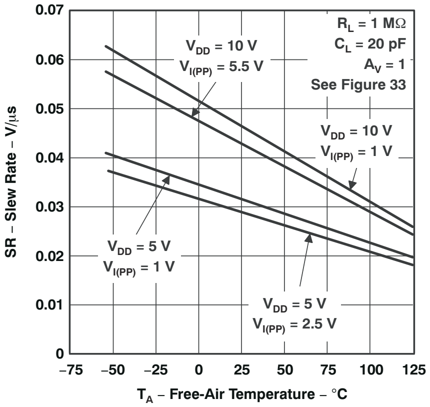


Figure 5-22. Slew Rate vs Free-Air Temperature

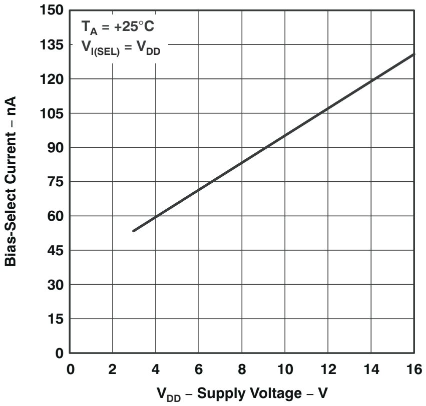


Figure 5-23. Bias-Select Current vs Supply Voltage

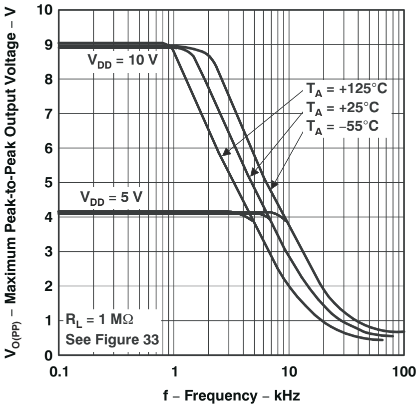


Figure 5-24. Maximum Peak-to-Peak Output Voltage vs Frequency

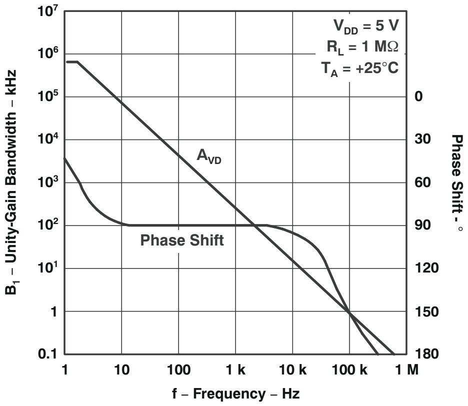


Figure 5-25. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

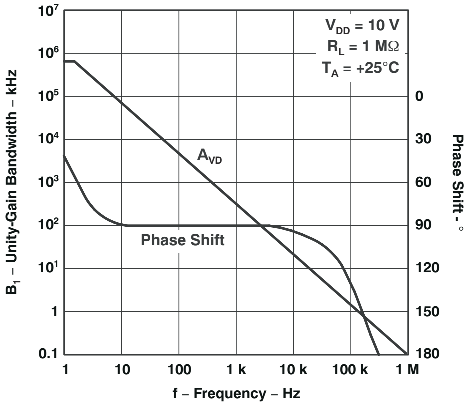


Figure 5-26. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

5.10 Typical Characteristics (continued)

data at high and low temperatures applicable only within rated operating free-air temperature ranges of the various devices

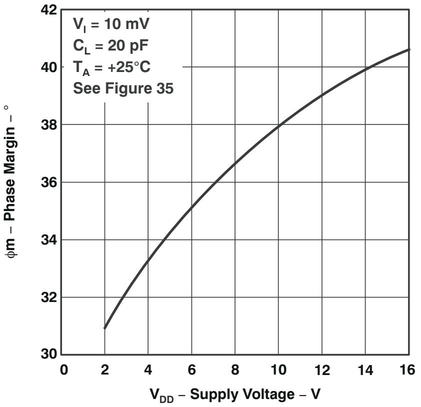


Figure 5-27. Phase Margin vs Supply Voltage

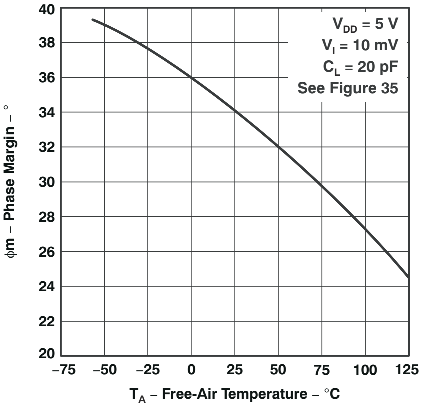


Figure 5-28. Phase Margin vs Free-Air Temperature

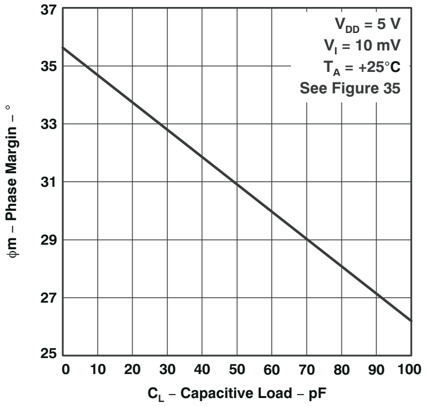


Figure 5-29. Phase Margin vs Capacitive Load

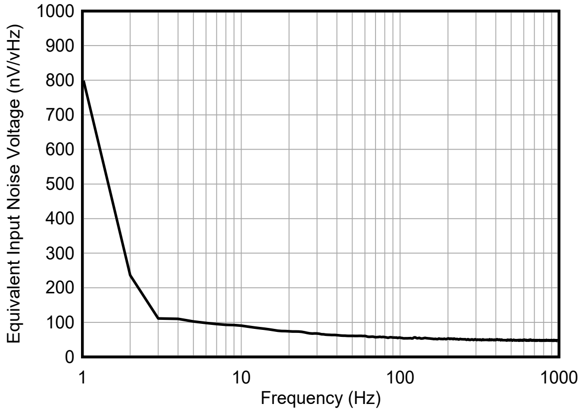
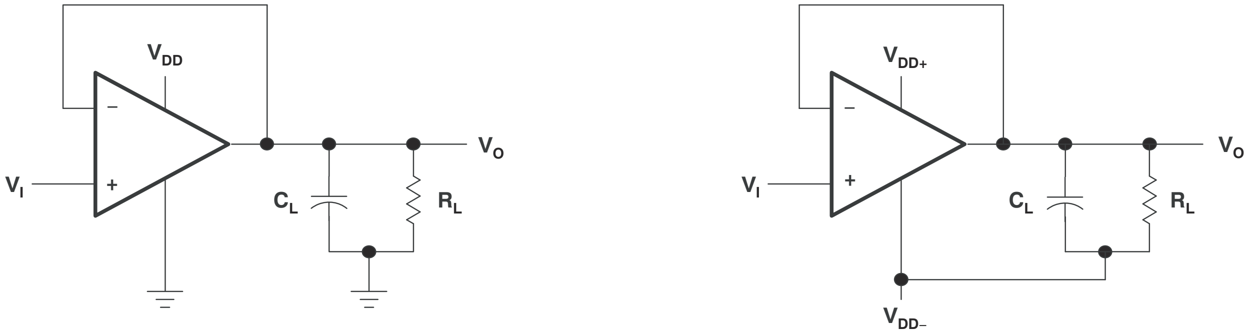


Figure 5-30. Equivalent Input Noise Voltage vs Frequency

6 Parameter Measurement Information

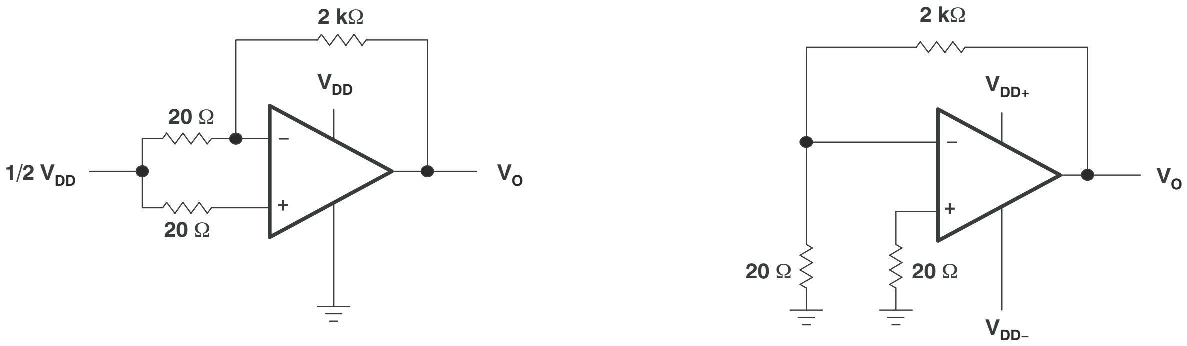
6.1 Single-Supply Versus Split-Supply Test Circuits

Because the TLC27L1 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, is offset from ground. Avoid this inconvenience by testing the device with split supplies and the output load tied to the negative rail. The following figures show a comparison of single-supply versus split-supply test circuits. The use of either circuit gives the same result.



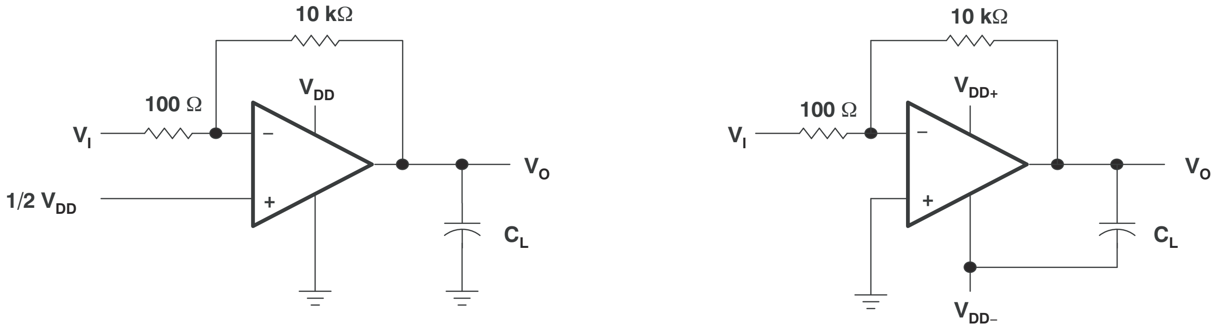
(a) SINGLE SUPPLY **(b) SPLIT SUPPLY**

Figure 6-1. Unity-Gain Amplifier



(a) SINGLE SUPPLY **(b) SPLIT SUPPLY**

Figure 6-2. Noise-Test Circuit



(a) SINGLE SUPPLY **(b) SPLIT SUPPLY**

Figure 6-3. Gain-of-100 Inverting Amplifier

6.2 Input Bias Current

Because of the high input impedance of the TLC27L1 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 6-4). Leakages that can otherwise flow to the inputs are shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

Many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

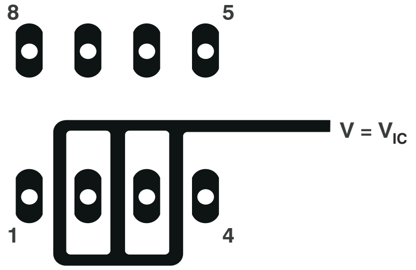


Figure 6-4. Isolation Metal Around Device Inputs (P package)

6.3 Low-Level Output Voltage

To obtain low-level supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output voltage being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, observe these two conditions. If conditions other than these are to be used, see the *Typical Characteristics* in Section 5.10.

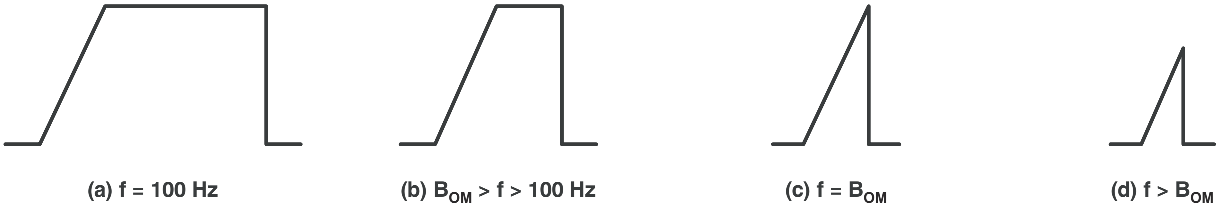
6.4 Input Offset Voltage Temperature Coefficient

Erroneous readings often result from attempts to measure the temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is less than freezing, moisture is able to collect on both the device and the test socket. This moisture results in leakage and contact resistance that potentially causes erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage because the moisture also covers the isolation metal, thereby rendering the techniques useless. Perform these measurements at temperatures greater than freezing to minimize error.

6.5 Full-Power Response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is typically measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal. When the output shows significant distortion, the input frequency is noted as the full-linear bandwidth. The full-peak response is defined as the maximum output frequency, without regard to distortion, at which the full peak-to-peak output swing is maintained. When the output frequency is greater than the full-peak response bandwidth, or maximum output-swing bandwidth, the full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet, and is measured using the circuit in Figure 6-1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 6-5). A square wave allows a more accurate determination of the point at which the maximum peak-to-peak output is reached.


(a) f = 100 Hz

(b) B_{OM} > f > 100 Hz

(c) f = B_{OM}

(d) f > B_{OM}

Figure 6-5. Full-Power-Response Output Signal

6.6 Test Time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than bipolar and BiFET devices. The problem becomes more pronounced with reduced supply levels and lower temperatures.

7 Application and Implementation

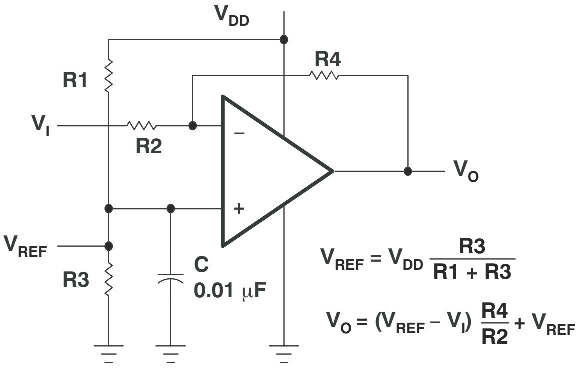
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Single-Supply Operation

While the TLC27L1 performs well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This optimization includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS. For maximum dynamic range, 16V single-supply operation is recommended.



$$V_{REF} = V_{DD}\frac{R3}{R1 + R3}$$

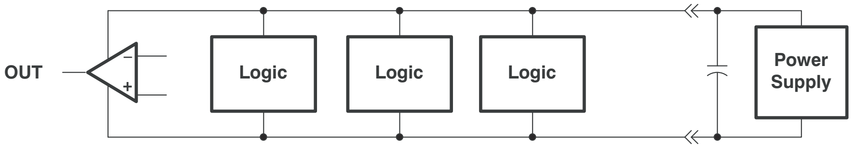
$$V_O = (V_{REF} - V_I)\frac{R4}{R2} + V_{REF}$$

Figure 7-1. Inverting Amplifier With Voltage Reference

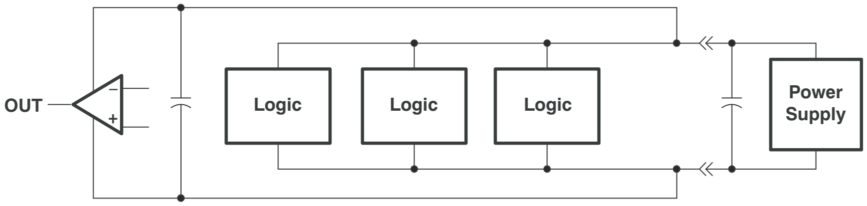
Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is typically sufficient to establish this reference level (see Figure 7-1). The low-input bias-current consumption of the TLC27L1 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC27L1 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, take the following recommended precautions:

1. Power linear devices from separate bypassed supply lines (see Figure 7-2); otherwise, linear device supply rails potentially fluctuate as a result of voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling is probably necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 7-2. Common Versus Separate Supply Rails

7.1.2 Input Characteristics

The TLC27L1 is specified with a minimum and a maximum input voltage that, if exceeded at either input, possibly causes the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. The lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} − 1V at T_A = 25°C and at V_{DD} − 1.5V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the legacy TLC27L1 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time is calculated to be typically 0.1µV/month, including the first month of operation.

The legacy TLC27L1 previously offered external input-offset null control. Migration from the legacy 150mm LinCMOS process to a 300mm diameter wafer process has brought associated improvements to input offset voltage precision, eliminating the need for the offset adjustment or "bias select" pins. These pins are non-internally-connected on new silicon devices, and can be left floating or biased to a fixed voltage. The new silicon also features improved slew rate, supply-voltage rejection ratio, and voltage noise. However, this change does introduce a new crossover region, where shifts in input offset (typically 300µV–400µV) occur as the input common-mode voltage approaches the V_{DD} rail. Figure 7-3 and Figure 7-4 plot the mean and standard deviation of this characteristic at various temperatures for a 10V supply.

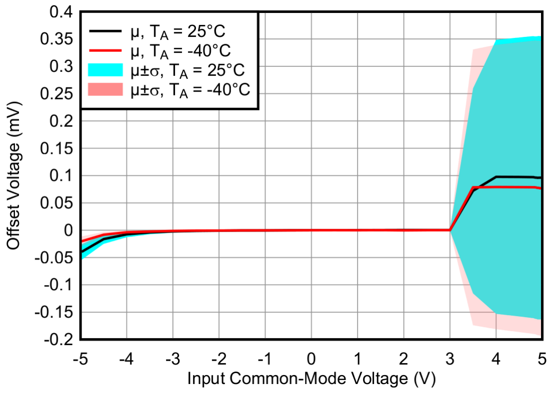


Figure 7-3. Offset Voltage vs Input Common-mode Voltage

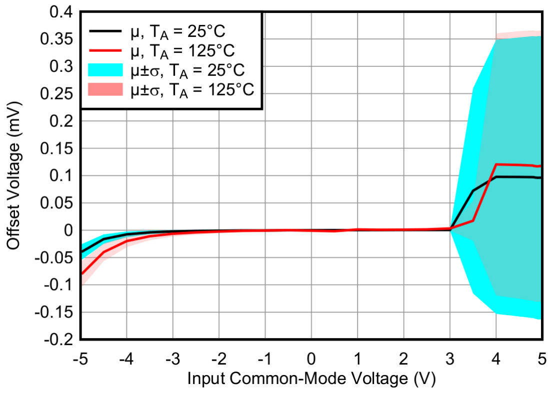
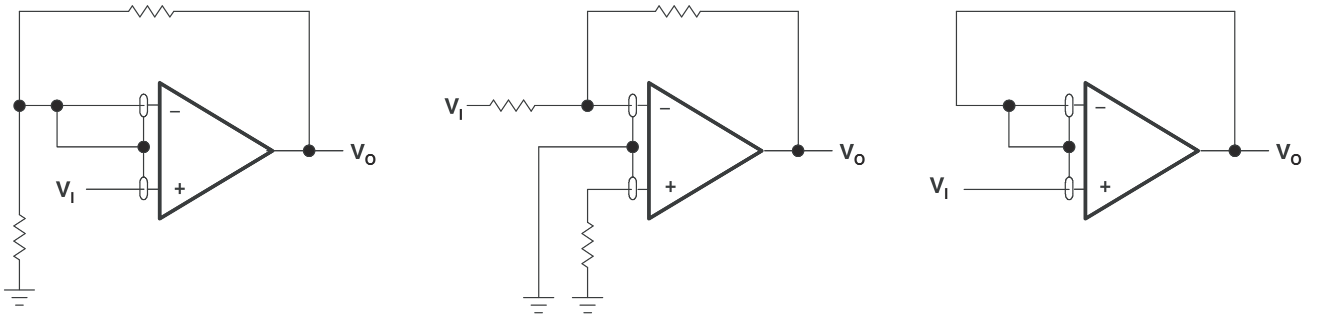


Figure 7-4. Offset Voltage vs Input Common-mode Voltage

Because of the extremely high input impedance and resulting low bias-current requirements, the TLC27L1 is an excellent choice for low-level signal processing. However, leakage currents on printed-circuit boards and sockets sometimes easily exceed bias-current requirements and cause a degradation in device performance. As best practice, include guard rings around inputs (similar to those of Figure 6-4 in the *Parameter Measurement Information* section). Drive these guards from a low-impedance source at the same voltage level as the common-mode input (see Figure 7-5).

7.1.3 Noise Performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias-current requirements of the TLC27L1 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50kΩ because bipolar devices exhibit greater noise currents.



(a) NONINVERTING AMPLIFIER
(b) INVERTING AMPLIFIER
(c) UNITY-GAIN AMPLIFIER

Figure 7-5. Guard-Ring Schemes

7.1.4 Feedback

Operational amplifier circuits almost always employ feedback, and because feedback is the first prerequisite for oscillation, caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 7-6). The value of this capacitor is optimized empirically.

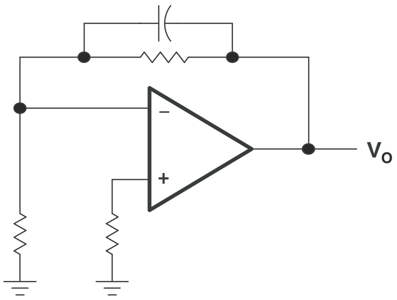


Figure 7-6. Compensation for Input Capacitance

7.1.5 Electrostatic Discharge Protection

The TLC27L1 incorporates an internal electrostatic-discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000V as tested under MIL-STD-883C, Method 3015.2. However, exercise care when handling these devices as exposure to ESD potentially results in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

7.1.6 Latch-Up

CMOS devices are susceptible to latch-up due to inherent parasitic thyristors. With this in mind, the TLC27L1 inputs and output are designed to withstand −100mA surge currents without sustaining latch-up. However, use best practices to reduce the chance of latch-up whenever possible. Do not forward bias internal-protection diodes. Do not exceed the supply voltage by more than 300mV for applied input and output voltages. Exercise care when using capacitive coupling on pulse generators. Shunt supply transients by using decoupling capacitors (0.1μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is typically between the positive supply rail and ground, and is triggered by surges on the supply lines, voltages on either the output or inputs that exceed the supply voltage, or both. After latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and typically results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.

7.1.7 Output Characteristics

The output stage of the TLC27L1 is designed to sink and source relatively high amounts of current (see also Section 5.10). If the output is subjected to a short-circuit condition, the high-current capability is able to cause device damage under certain conditions. Output current capability increases with supply voltage (see Figure 7-7).

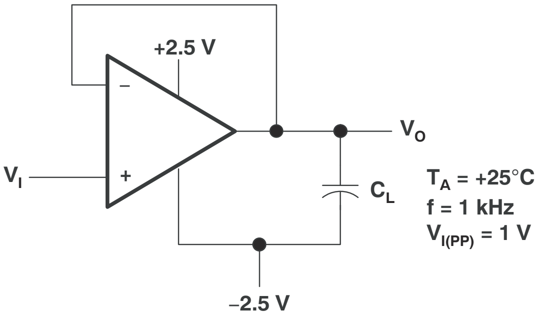
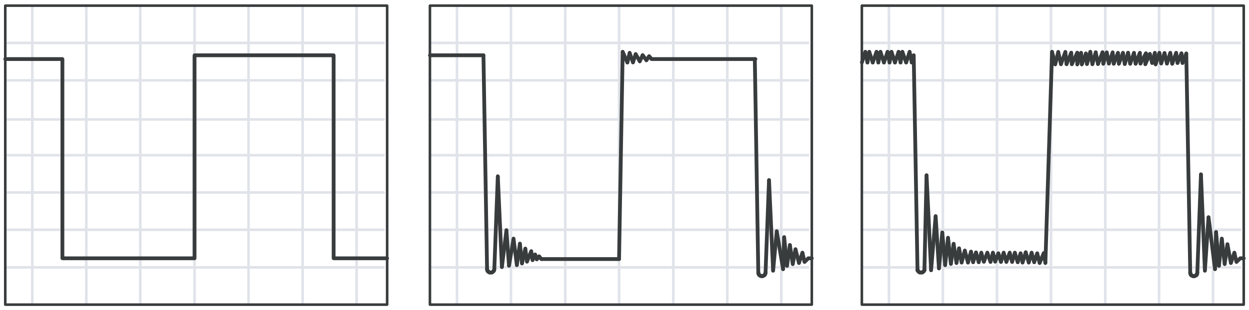


Figure 7-7. Test Circuit for Output Characteristics

All operating characteristics of the TLC27L1 were measured using a 20pF load. The devices drive higher capacitive loads. However, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 7-8). In many cases, adding some compensation in the form of a series resistor in the feedback loop alleviates the problem.



(a) C_L = 20 pF, R_L = NO LOAD　(b) C_L = 260 pF, R_L = NO LOAD　(c) C_L = 310 pF, R_L = NO LOAD

Figure 7-8. Effect of Capacitive Loads in Low-Bias Mode

Although the TLC27L1 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 7-9). There are two disadvantages to using this circuit. First, the NMOS pulldown transistor must sink a comparatively large amount of current. In this circuit, the pulldown transistor behaves like a linear resistor with an on-resistance between approximately 60Ω and 180Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0V at the output occurs. Secondly, pullup resistor R_P acts as a drain load to the pulldown resistor, and the gain of the operational amplifier is reduced at output voltage levels where the corresponding pullup resistor is not supplying the output current.

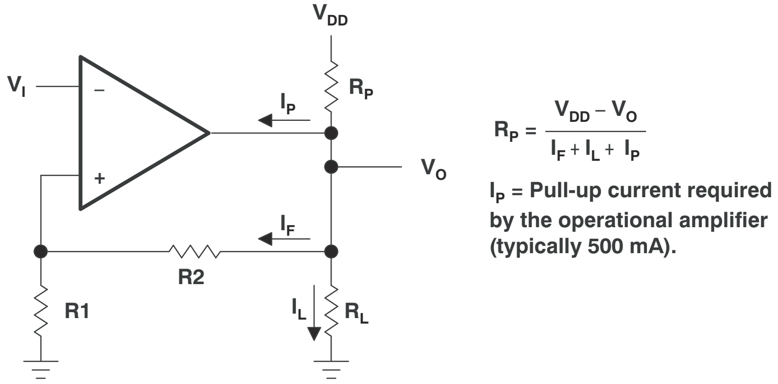


Figure 7-9. Resistive Pullup Resistor to Increase V_{OH}

7.1.8 Typical Applications

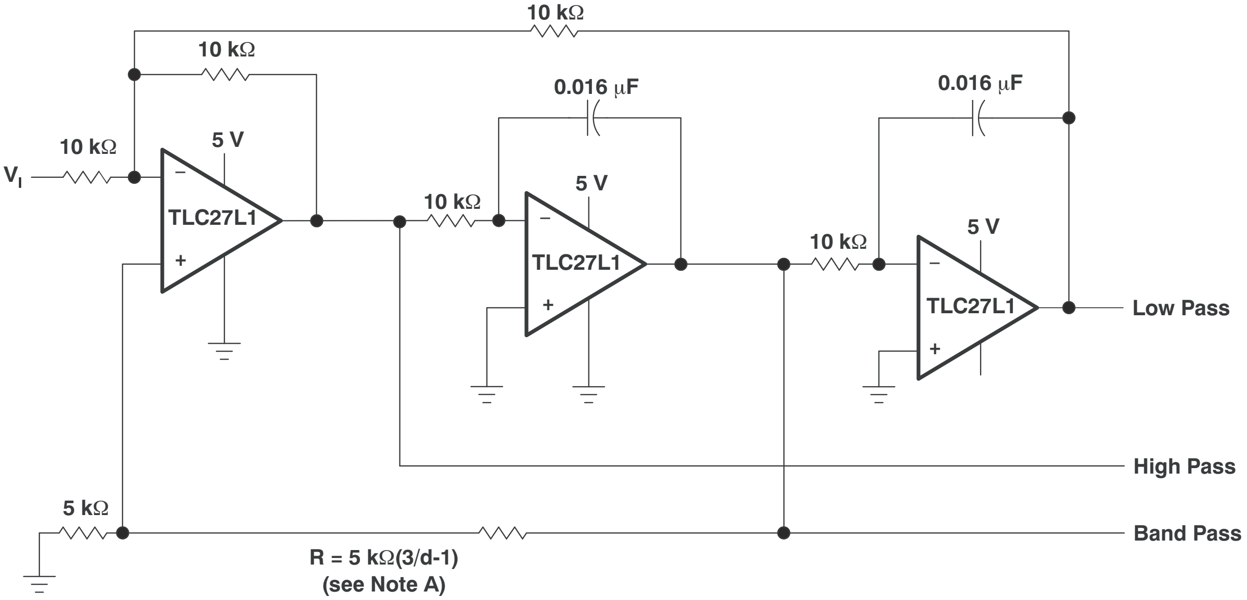


Figure 7-10. State-Variable Filter

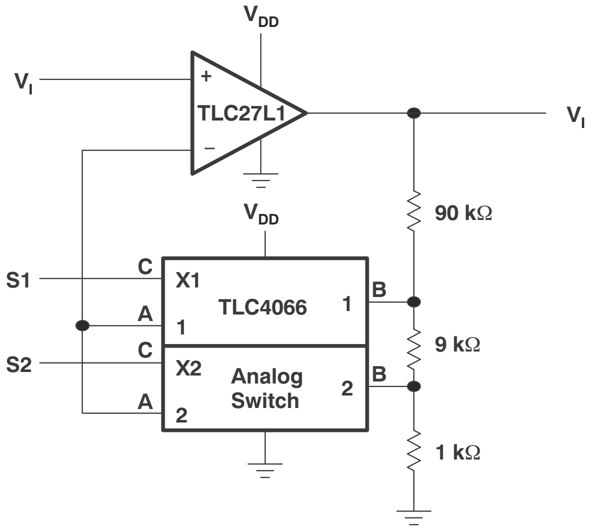


Figure 7-11. Amplifier With Digital-Gain Selection

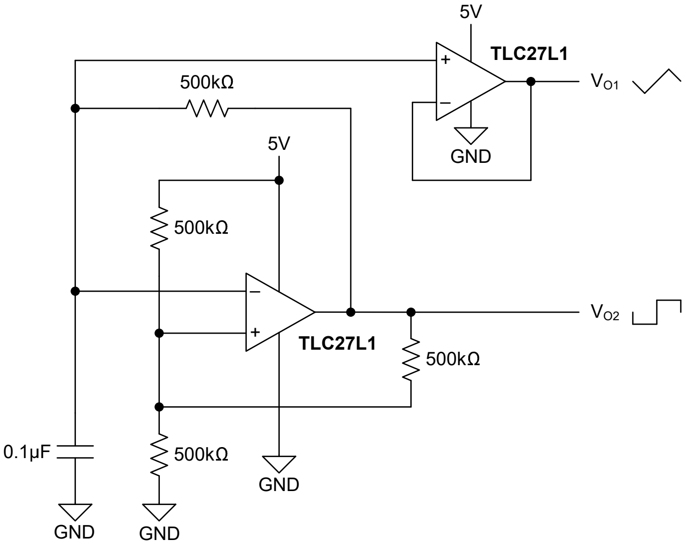


Figure 7-12. Multivibrator

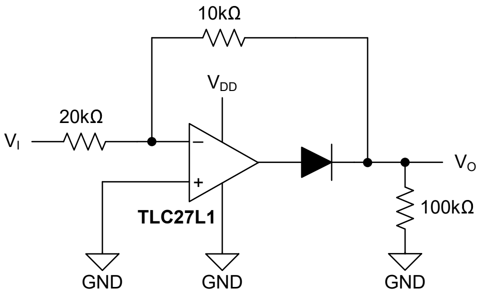


Figure 7-13. Full-Wave Rectifier

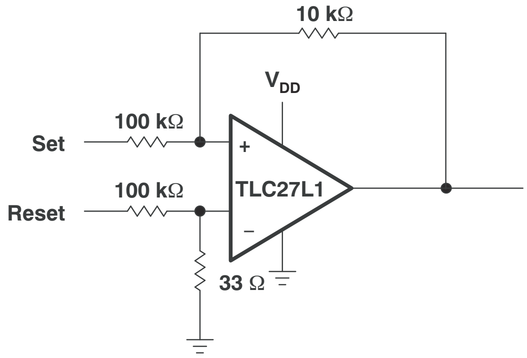


Figure 7-14. Set/Reset Flip-Flop

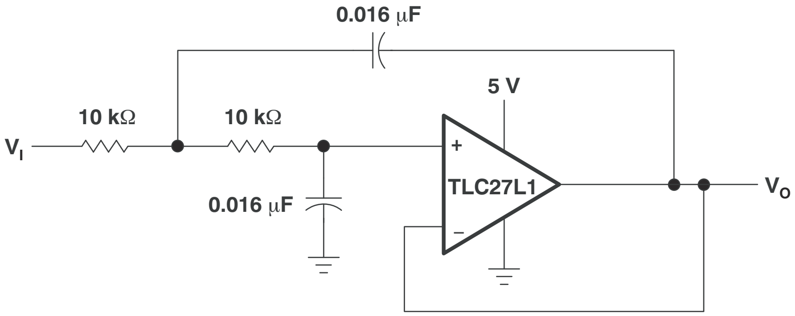


Figure 7-15. Two-Pole Low-Pass Butterworth Filter

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2005) to Revision C (July 2025) **Page**

- Deleted obsolete TLC27L1AI, TLC27L1BI, TLC27L1BC, and TLC27L1M devices and associated content from document........ 1
- Updated the numbering format for tables, figures, and cross-references throughout the document........ 1
- Added *Applications*, *Pin Configuration and Functions*, *Application and Implementation*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections........ 1
- Added *Applications* section........ 1
- Deleted *Equivalent Schematic* section........ 2
- Added *Pin Configuration and Functions* section with pin descriptions........ 2
- Added table note that input bias current and input offset current are specified by characterization........ 4
- Changed typical input offset current from 0.1pA to 0.5pA........ 4
- Changed typical minimum input common-mode voltage for T_A = 25°C from −0.3V to −0.2V........ 4
- Changed typical low-level output voltage from 0mV to 1mV for V_{DD} = 5V, and from 0mV to 5mV for V_{DD} = 10V........ 4
- Changed typical CMRR for V_{DD} = 5V at T_A = 25°C from 94dB to 87dB........ 4
- Changed typical CMRR for V_{DD} = 5V at T_A = 70°C and T_A = 0°C from 95dB to 85dB........ 4
- Changed typical CMRR for V_{DD} = 10V at T_A = 25°C from 97dB to 94dB........ 4
- Changed typical CMRR for V_{DD} =10V at T_A = 0°C and T_A = 70°C from 97dB to 93dB........ 4
- Changed parameter name from Input current (BIAS SELECT) to Offset adjustment pin input current (BIAS SELECT), and added "legacy silicon" to test conditions........ 4

- Changed typical unity-gain bandwidth at T_A = 0°C from 125kHz to 110kHz in *Operating Characteristics for V_{DD} = 10V, C Suffix* 5
- Added table note that input bias current and input offset current are specified by characterization........ 6
- Changed typical input offset current from 0.1pA to 0.5pA........ 6
- Changed typical minimum input common-mode voltage for T_A = 25°C from −0.3V to −0.2V........ 6
- Changed typical low-level output voltage from 0mV to 1mV for V_{DD} = 5V, and from 0mV to 5mV for V_{DD} = 10V........ 6
- Changed typical CMRR for V_{DD} = 5V at T_A = 25°C from 94dB to 87dB........ 6
- Changed typical CMRR for V_{DD} = 5V at T_A = 85°C and T_A = −40°C from 95dB to 85dB........ 6
- Changed typical CMRR for V_{DD} = 10V at T_A = 25°C from 97dB to 94dB........ 6
- Changed typical CMRR for V_{DD} =10V at T_A = 85°C from 97dB to 93dB........ 6
- Changed typical CMRR for V_{DD} = 10V at T_A = −40°C from 98dB to 93dB........ 6
- Changed parameter name from Input current (BIAS SELECT) to Offset adjustment pin input current (BIAS SELECT), and added "legacy silicon" to test conditions........ 6
- Changed typical unity-gain bandwidth at T_A = −40°C from 130kHz to 110kHz in *Operating Characteristics for V_{DD} = 5V, I Suffix* 7
- Changed typical unity-gain bandwidth at T_A = −40°C from 155kHz to 110kHz in *Operating Characteristics for V_{DD} = 10V, I Suffix* 7
- Deleted Figures 25 and 26........ 8
- Updated Figure 5-30........ 8
- Updated description of full-linear and full-peak responses in *Full-Power Response* 16
- Deleted *Input Offset Voltage Nulling* section........ 18
- Added guidance concerning removal of bias-select pin function and changes to input crossover region to *Input Characteristics* 18
- Deleted Figure 47 in *Output Characteristics* 20
- Updated Figures 7-12 and 7-13 in *Output Characteristics* to correct amplifier feedback connections........ 20

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC27L1ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L1AC
TLC27L1ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L1AC
TLC27L1AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	27L1AI
TLC27L1BCD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	27L1BC
TLC27L1CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L1C
TLC27L1CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L1C
TLC27L1CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L1C
TLC27L1CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	27L1C
TLC27L1CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L1CP
TLC27L1CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC27L1CP
TLC27L1ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	27L1I
TLC27L1IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L1I
TLC27L1IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27L1I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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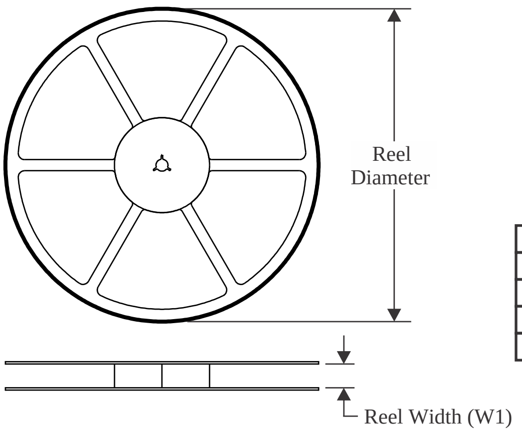
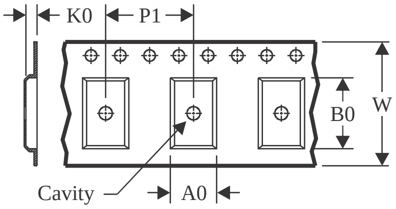
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

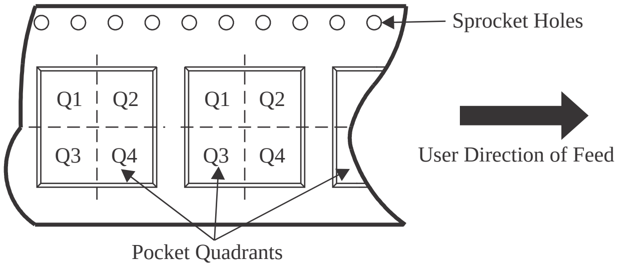


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

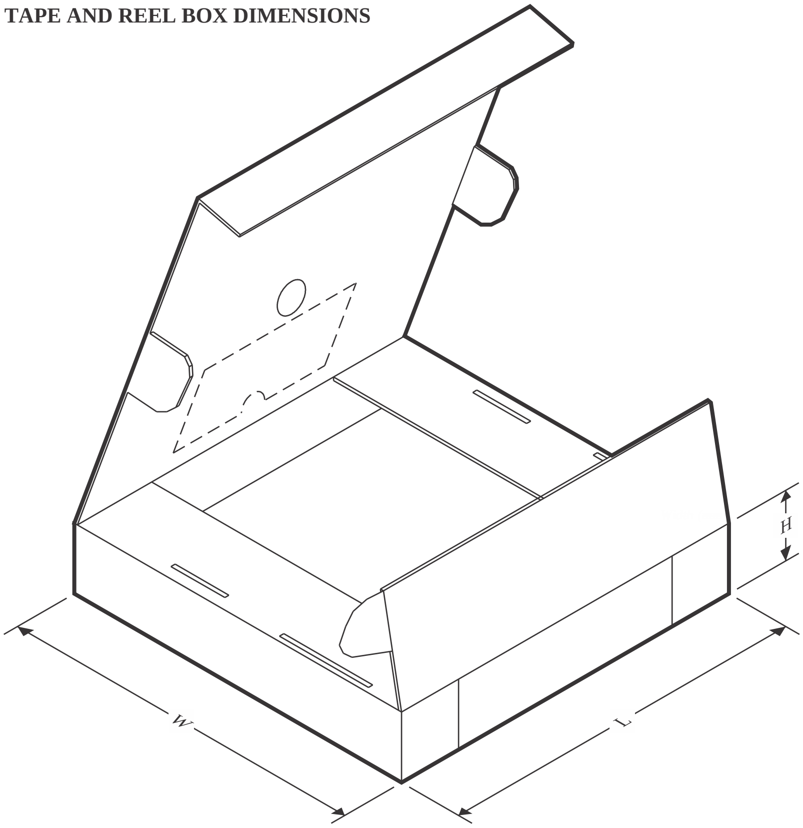
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC27L1CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC27L1IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

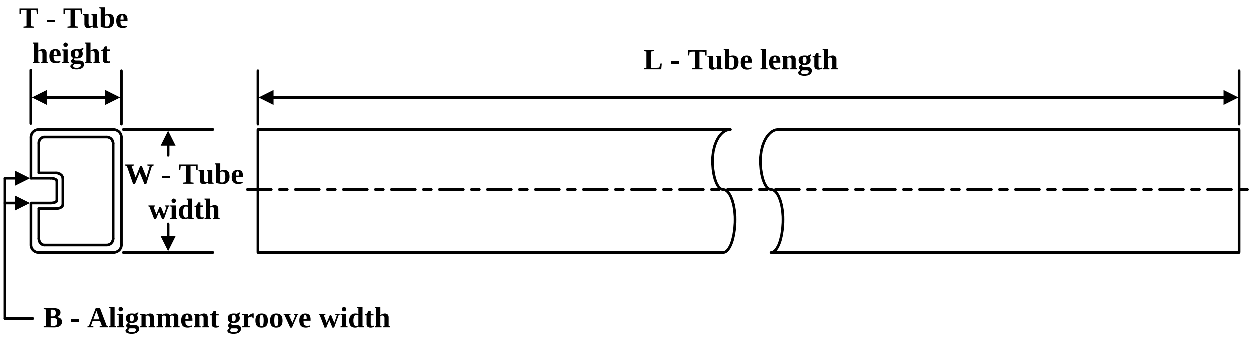
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC27L1CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC27L1IDR	SOIC	D	8	2500	353.0	353.0	32.0

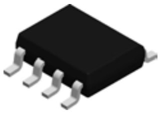
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC27L1ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L1ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L1CD	D	SOIC	8	75	507	8	3940	4.32
TLC27L1CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L1CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC27L1CD.A	D	SOIC	8	75	507	8	3940	4.32
TLC27L1CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC27L1CP.A	P	PDIP	8	50	506	13.97	11230	4.32

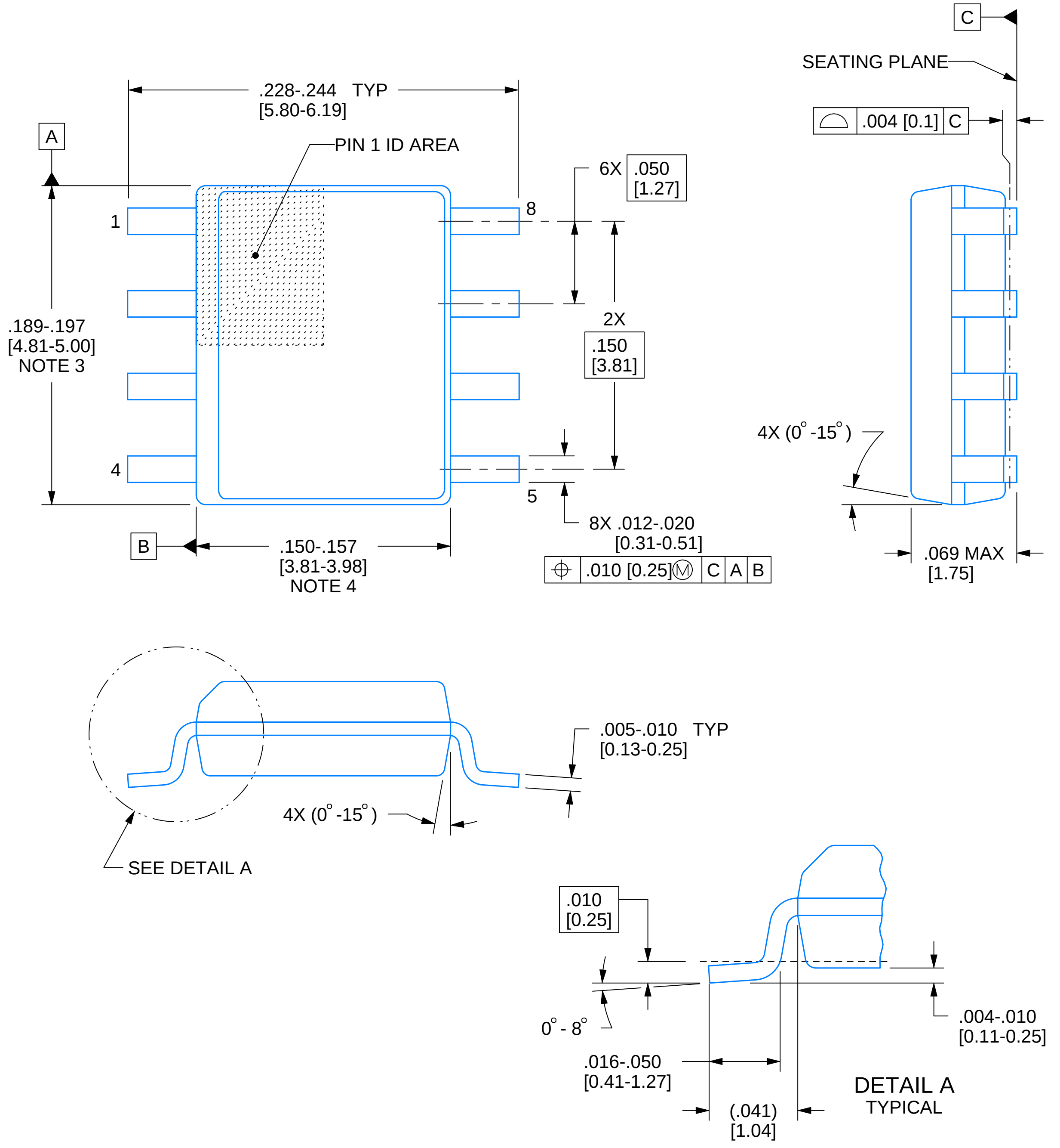
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

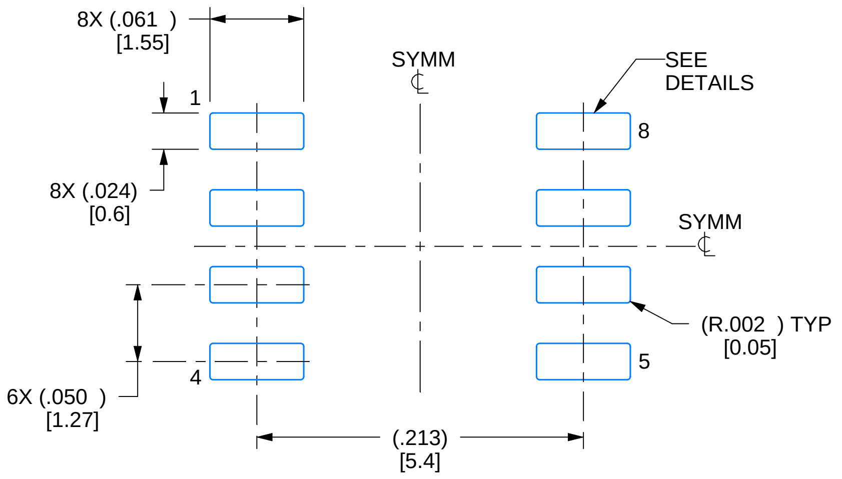
SMALL OUTLINE INTEGRATED CIRCUIT



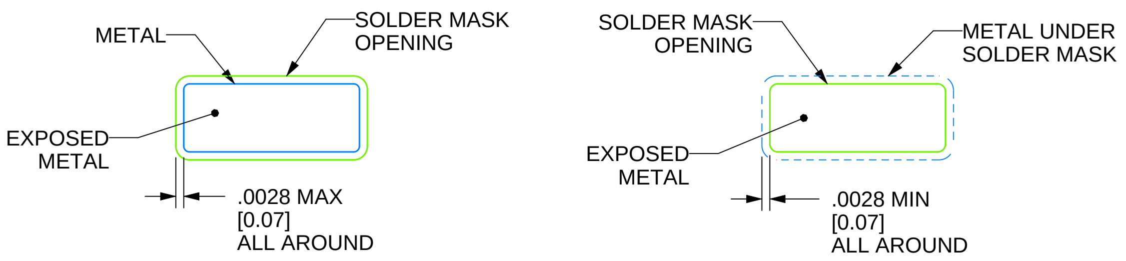
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



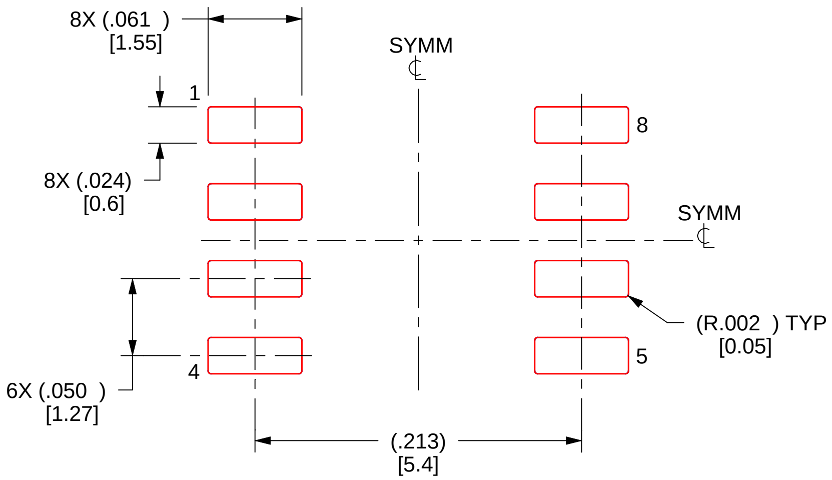
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



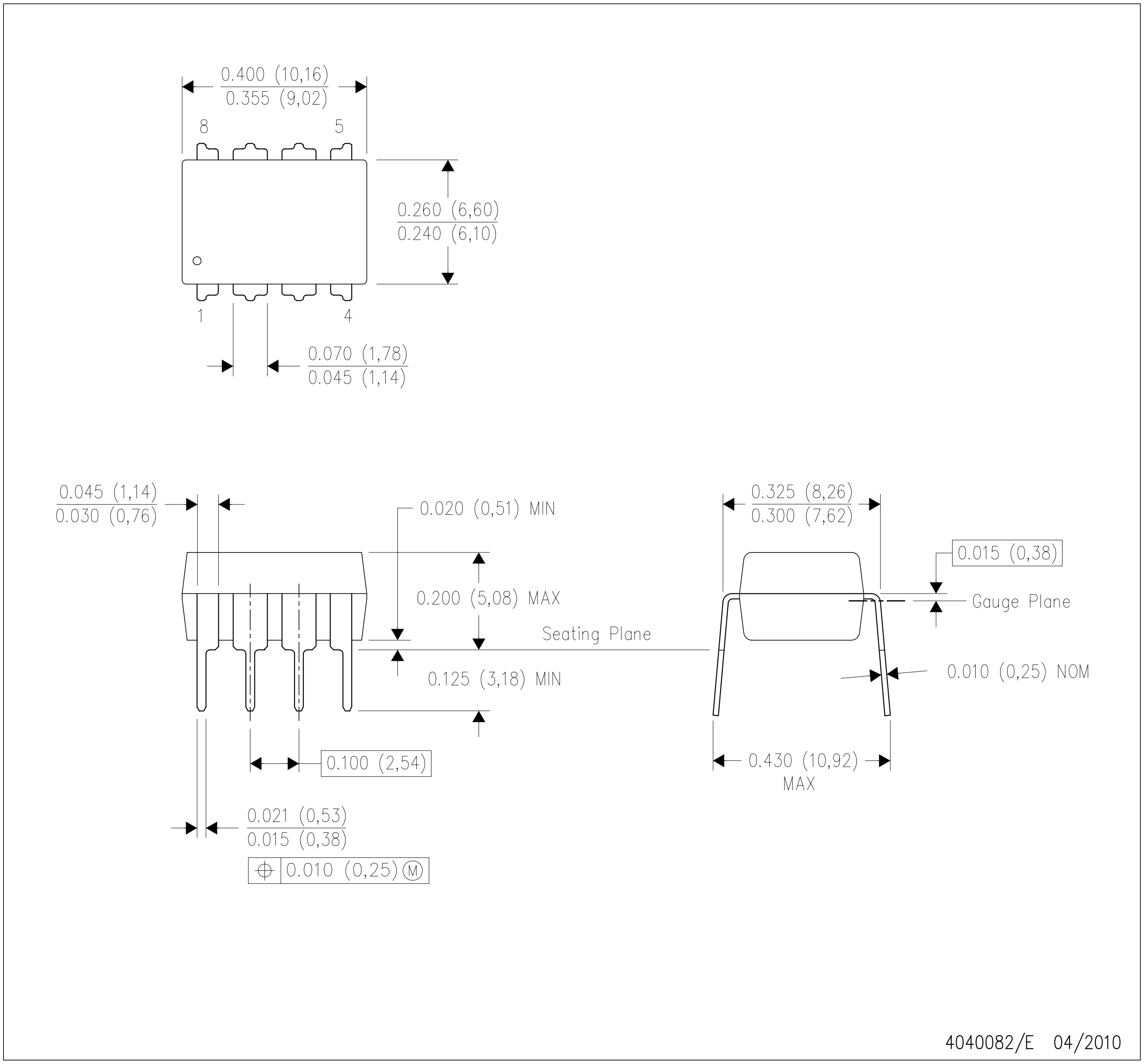
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

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