10UT

1IN-

GND

1IN+ [

8 DVDD

7 1 20UT

6 ☐ 2IN-

5 ¶ 2IN+

NC

D, JG, P, OR PW PACKAGE (TOP VIEW)

2

3

• Trimmed Offset Voltage:

TLC277 . . . 500 μ V Max at 25°C, V_{DD} = 5 V

- Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days
- Wide Range of Supply Voltages Over Specified Temperature Range:

0°C to 70°C . . . 3 V to 16 V -40°C to 85°C . . . 4 V to 16 V -55°C to 125°C . . . 4 V to 16 V

- Single-Supply Operation
- Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)
- Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz
- Output Voltage Range Includes Negative Rail
- High Input impedance . . . 10¹² Ω Typ
- ESD-Protection Circuitry
- Small-Outline Package Option Also Available in Tape and Reel
- Designed-In Latch-Up Immunity

FK PACKAGE (TOP VIEW) 2 20 19 1 ″₁₈∏ NC NC **20UT** 1IN-5 NC NC 16 6 1IN+ 2IN-15

NC - No internal connection

NC ∏8

description

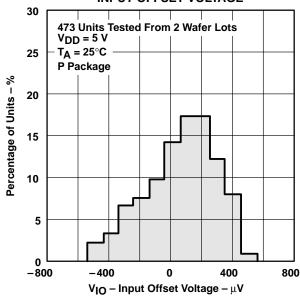
The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching those of general-purpose BiFET devices.

These devices use Texas Instruments silicongate LinCMOS $^{\text{TM}}$ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications previously reserved for BiFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

DISTRIBUTION OF TLC277 INPUT OFFSET VOLTAGE

10 11 12 13



LinCMOS is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

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description (continued)

AVAILABLE OPTIONS

			PAC	KAGED DEVI	CES		CUID
T _A	V _{IO} max AT 25°C	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CHIP FORM (Y)
0°C to 70°c	500 μV 2 mV 5 mV 10mV	TLC277CD TLC272BCD TLC272ACD TLC272CD	1111	 - -	TLC277CP TLC272BCP TLC272ACP TLC272CP	 TLC272CPW	— — — TLC272Y
-40°C to 85°C	500 μV 2 mV 5 mV 10 mV	TLC277ID TLC272BID TLC272AID TLC272ID	_ _ _ _	_ _ _ _	TLC277IP TLC272BIP TLC272AIP TLC272IP	_ _ _ _	

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

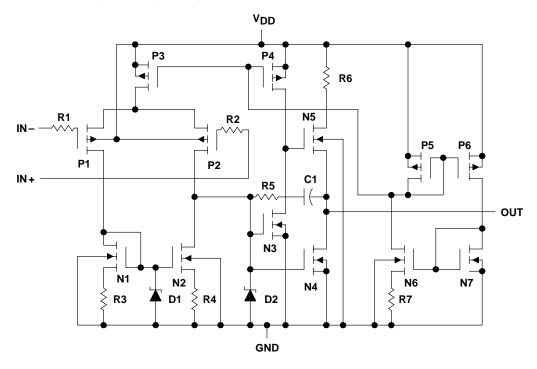
The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0° C to 70° C. The I-suffix devices are characterized for operation from -40° C to 85° C. The M-suffix devices are characterized for operation over the full military temperature range of -55° C to 125° C.

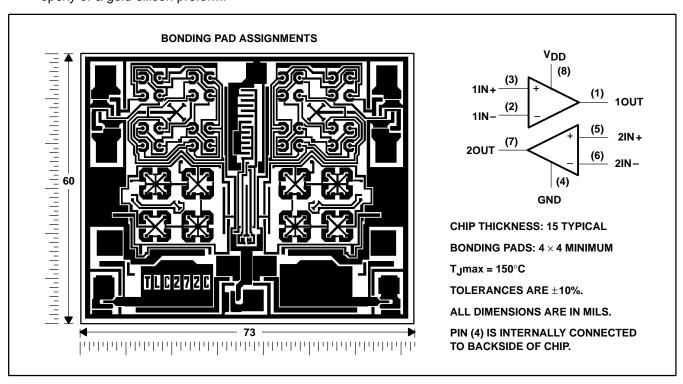


equivalent schematic (each amplifier)



TLC272Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

±V _{DD}
0.3 V to V _{DD}
±5 mA
±30 mA
45 mA
45 mA
unlimited
See Dissipation Rating Table
0°C to 70°C
–40°C to 85°C
–55°C to 125°C
–65°C to 150°C
260°C
ackage 260°C
300°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 - 2. Differential voltages are at IN+ with respect to IN-.
 - 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
Р	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
PW	525 mW	4.2 mW/°C	336 mW	N/A	N/A

recommended operating conditions

		C SU	FFIX	I SUFFIX		M SUFFIX		
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Supply voltage, V _{DD}		3	16	4	16	4	16	V
O a martin de la m	V _{DD} = 5 V	-0.2	3.5	-0.2	3.5	0	3.5	.,
Common-mode input voltage, V _{IC}	V _{DD} = 10 V	-0.2	8.5	-0.2	8.5	0	8.5	٧
Operating free-air temperature, TA		0	70	-40	85	-55	125	°C



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electrical characteristics at specified free-air temperature, $V_{\mbox{\scriptsize DD}}$ = 5 V (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T _A †	TLC272 TLC272			UNIT
						MIN	TYP	MAX	
		TI 00700	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		TLC272C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	.,
		T I 00 T 010	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	mV
l.,		TLC272AC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			6.5	
VIO	Input offset voltage	TI 00-00	V _O = 1.4 V,	V _{IC} = 0,	25°C		230	2000	
		TLC272BC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3000	
			V _O = 1.4 V,	V _{IC} = 0,	25°C		200	500	μV
		TLC277C	$R_S = 50 \Omega$	$R_L = 10 \text{ k}\Omega$	Full range			1500	
α_{VIO}	Temperature coefficient of input	offset voltage			25°C to 70°C		1.8		μV/°C
					25°C		0.1	60	
liO	Input offset current (see Note 4)		l		70°C		7	300	рA
			$V_{O} = 2.5 \text{ V},$	$V_{IC} = 2.5 V$	25°C		0.6	60	
ΙΒ	Input bias current (see Note 4)				70°C		40	600	рA
						-0.2	-0.3		
					25°C	to	to		V
V _{ICR}	Common-mode input voltage rar	nge				4	4.2		
1010	(see Note 5)				Full range	-0.2 to			V
					I un range	3.5			V
					25°C	3.2	3.8		
Vон	High-level output voltage		V _{ID} = 100 mV,	R _L = 10 kΩ	0°C	3	3.8		V
011	0			L	70°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	IOL = 0	0°C		0	50	mV
"-	, 3		,	OL.	70°C		0	50	
					25°C	5	23		
AVD	Large-signal differential voltage	amplification	V _O = 0.25 V to 2 V,	$R_I = 10 \text{ k}\Omega$	0°C	4	27		V/mV
"	3 0	•		-	70°C	4	20		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		0°C	60	84		dB
	,				70°C	60	85		
					25°C	65	95		
ksvr	Supply-voltage rejection ratio		V _{DD} = 5 V to 10 V,	VO = 1.4 V	0°C	60	94		dB
	$(\Delta V_{DD}/\Delta V_{IO})$			Ŭ	70°C	60	96		
					25°C		1.4	3.2	
I _{DD}	Supply current (two amplifiers)		V _O = 2.5 V,	$V_{IC} = 2.5 V$,	0°C		1.6	3.6	mA
	, , ,		No load		70°C	1	1.2	2.6	
Ļ								-	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T _A †	TLC272 TLC272			UNIT
						MIN	TYP	MAX	
		TI 00700	$V_0 = 1.4 V$,	V _{IC} = 0,	25°C		1.1	10	
		TLC272C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	\/
		TI 007040	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	mV
.,	Input offset voltage	TLC272AC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			6.5	
V _{IO}	input offset voltage	TI 0070D0	V _O = 1.4 V,	V _{IC} = 0,	25°C		290	2000	
		TLC272BC	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3000	.,
		TI 00770	$V_{O} = 1.4 \text{ V},$	V _{IC} = 0,	25°C		250	800	μV
		TLC277C	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			1900	
CV/IC	Temperature coefficient of input of	offset voltage			25°C to		2		μV/°C
α_{VIO}	remperature coemicient of input of	mset voltage			70°C				μν/ Ο
I _{IO}	Input offset current (see Note 4)				25°C		0.1	60	pА
טוי	input onset current (see Note 4)		V _O = 5 V,	V _{IC} = 5 V	70°C		7	300	рΑ
lin	Input bias current (see Note 4)		V() = 5 V,	AIC = 2 A	25°C		0.7	60	pА
IB	input bias current (see Note 4)				70°C		50	600	PΑ
					_	-0.2	-0.3		
	On the second of the second of the second of				25°C	to 9	to 9.2		V
VICR	Common-mode input voltage range (see Note 5)	ge				-0.2	3.2		
	(000 11010 0)				Full range	to			V
						8.5			
					25°C	8	8.5		
Voн	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	0°C	7.8	8.5		V
					70°C	7.8	8.4		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	0°C		0	50	mV
					70°C		0	50	
					25°C	10	36		
AVD	Large-signal differential voltage a	mplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	0°C	7.5	42		V/mV
					70°C	7.5	32		
					25°C	65	85		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		0°C	60	88		dB
	·				70°C	60	88		
					25°C	65	95		
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	0°C	60	94		dB
				•	70°C	60	96		
					25°C		1.9	4	
I _{DD}	Supply current (two amplifiers)		V _O = 5 V, No load	$V_{IC} = 5 V$	0°C		2.3	4.4	mA

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER		TEST COND	ITIONS	T _A †		2I, TLC2 2BI, TL0		UNIT
						MIN	TYP	MAX	
		TI 00701	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		TLC272I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			13	\/
		TI 007041	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	mV
l.,	least effect college	TLC272AI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			7	
V _{IO}	Input offset voltage	TI 0070DI	V _O = 1.4 V,	V _{IC} = 0,	25°C		230	2000	
		TLC272BI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3500	.,
		TI 00771	V _O = 1.4 V,	$V_{IC} = 0$,	25°C		200	500	μV
		TLC277I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			2000	
(V) // O	Temperature coefficient of input	offset voltage			25°C to		1.8		μV/°C
ανιο	remperature coemcient of input	Uliset voltage			85°C		1.0		μν/ Ο
lio	Input offset current (see Note 4)				25°C		0.1	60	pА
יוט	input onset current (see Note 4)		V _O = 2.5 V,	V _{IC} = 2.5 V	85°C		24	15	РΛ
lin	Input bias current (see Note 4)		V() = 2.5 V,	VIC = 2.5 V	25°C		0.6	60	pА
IB	input bias current (see Note 4)				85°C		200	35	pΑ
						-0.2	-0.3		
					25°C	to 4	to 4.2		V
VICR	Common-mode input voltage range (see Note 5)						4.2		
					Full range	-0.2 to			V
						3.5			-
					25°C	3.2	3.8		
∨он	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	−40°C	3	3.8		V
				_	85°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−40°C		0	50	mV
-	· · · · · ·			-	85°C		0	50	
					25°C	5	23		
AVD	Large-signal differential voltage	amplification	$V_{O} = 1 \text{ V to 6 V},$	R _L = 10 kΩ	−40°C	3.5	32		V/mV
'				_	85°C	3.5	19		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		−40°C	60	81		dB
	-,				85°C	60	86		
					25°C	65	95		
ksvr	Supply-voltage rejection ratio		V _{DD} = 5 V to 10 V,	VO = 1.4 V	-40°C	60	92		dB
	$(\Delta V_{DD}/\Delta V_{IO})$	V		J	85°C	60	96		
					25°C		1.4	3.2	
I _{DD}	Supply current (two amplifiers)		$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$,	-40°C		1.9	4.4	mA
	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		No load		85°C		1.1	2.4	
			1				•••		

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	PARAMETER		TEST CONDI	TIONS	T _A †	TLC27	2I, TLC2 2BI, TLC		UNIT
						MIN	TYP	MAX	
		TI 00701	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	
		TLC272I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			13	
		TI 007041	V _O = 1.4 V,	V _{IC} = 0,	25°C		0.9	5	mV
l.,	Input offset voltage	TLC272AI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			7	
V _{IO}	input offset voltage	TI 0070DI	V _O = 1.4 V,	V _{IC} = 0,	25°C		290	2000	
		TLC272BI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3500	.,
		TI 00771	V _O = 1.4 V,	V _{IC} = 0,	25°C		250	800	μV
		TLC277I	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			2900	
α_{VIO}	Temperature coefficient of input of	offset voltage			25°C to 85°C		2		μV/°C
	Innut affect comment (and Nate 4)				25°C		0.1	60	A
lio	Input offset current (see Note 4)				85°C		26	1000	рA
	January Indian Aller Aller Aller Aller		$V_0 = 5 V$,	$V_{IC} = 5 V$	25°C		0.7	60	A
lΒ	Input bias current (see Note 4)				85°C		220	2000	рA
						-0.2	-0.3		
					25°C	to	to		V
VICR	Common-mode input voltage range (see Note 5)				9	9.2			
	(see Note 5)				Full range	-0.2 to			V
					i un rungo	8.5			·
					25°C	8	8.5		
∨он	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	-40°C	7.8	8.5		V
	-			_	85°C	7.8	8.5		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−40°C		0	50	mV
				-	85°C		0	50	
					25°C	10	36		
AVD	Large-signal differential voltage a	mplification	$V_0 = 1 \text{ V to 6 V},$	$R_L = 10 \text{ k}\Omega$	−40°C	7	46		V/mV
					85°C	7	31		
					25°C	65	85		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		-40°C	60	87		dB
					85°C	60	88		
					25°C	65	95		
ksvr	SVR (AV = (AV =)		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	-40°C	60	92		dB
	$(\Delta V_{DD}/\Delta V_{IO})$				85°C	60	96		
				.,	25°C		1.4	4	
I_{DD}	Supply current (two amplifiers)		V _O = 5 V, No load	$V_{IC} = 5 V$	-40°C		2.8	5	mA
			140 1000		85°C		1.5	3.2	

[†] Full range is –40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, $V_{\mbox{\scriptsize DD}}$ = 5 V (unless otherwise noted)

	DADAMETED		TEST COND	ITIONS	T. †	TLC27	2M, TLC	277M	UNIT
	PARAMETER		TEST COND	IIIONS	T _A †	MIN	TYP	MAX	UNII
		TLC272M	V _O = 1.4 V,	V _{IC} = 0,	25°C		1.1	10	\/
V	lanut offeet veltege	TLC272IVI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	mV
V _{IO}	Input offset voltage	TLC277M	$V_0 = 1.4 V$,	$V_{IC} = 0$,	25°C		200	500	
		TLC2//IVI	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			3750	μV
αΛΙΟ	Temperature coefficient of input or voltage	offset			25°C to 125°C		2.1		μV/°C
L	Input offeet ourrent (e.e. Note 4)				25°C		0.1	60	pА
lio	Input offset current (see Note 4)		V- 05V	V 05V	125°C		1.4	15	nA
1	lament him accomment (and Nate 4)		V _O = 2.5 V	$V_{IC} = 2.5 V$	25°C		0.6	60	pА
lΒ	Input bias current (see Note 4)				125°C		9	35	nA
.,	Common-mode input voltage ran	ge			25°C	0 to 4	-0.3 to 4.2		V
VICR	(see Note 5)	-			Full range	0 to 3.5			V
					25°C	3.2	3.8		
Vон	High-level output voltage		V _{ID} = 100 mV,	$R_L = 10 \text{ k}\Omega$	−55°C	3	3.8		V
					125°C	3	3.8		
					25°C		0	50	
VOL	Low-level output voltage		$V_{ID} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C		0	50	mV
					125°C		0	50	
					25°C	5	23		
A_{VD}	Large-signal differential voltage a	mplification	$V_0 = 0.25 \text{ V to 2 V}$	$R_L = 10 \text{ k}\Omega$	−55°C	3.5	35		V/mV
					125°C	3.5	16		
					25°C	65	80		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		−55°C	60	81		dB
					125°C	60	84		
	Cumply voltage releasing and				25°C	65	95		
ksvr	Supply-voltage rejection ratio (ΔVDD/ΔVIO)		$V_{DD} = 5 \text{ V to } 10 \text{ V},$	$V_0 = 1.4 \text{ V}$	−55°C	60	90		dB
	(= · UU/ = · U/				125°C	60	97		
			V- 0.5.V	V 0.5.V	25°C		1.4	3.2	
I_{DD}	Supply current (two amplifiers)		V _O = 2.5 V, No load	$V_{IC} = 2.5 V,$	−55°C		2	5	mA
					125°C		1	2.2	

[†] Full range is –55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

	DADAMETED		TEOT 0011D	ITIONS	- +	TLC27	2M, TLC	277M	
	PARAMETER		TEST COND	ITIONS	T _A †	MIN	TYP	MAX	UNIT
		TI 0070M	$V_0 = 1.4 V$,	$V_{IC} = 0$,	25°C		1.1	10	\
,	Innut offeet voltage	TLC272M	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			12	mV
V _{IO}	Input offset voltage	TLC277M	V _O = 1.4 V,	V _{IC} = 0,	25°C		250	800	
		TLC2//W	$R_S = 50 \Omega$,	$R_L = 10 \text{ k}\Omega$	Full range			4300	μV
ανιο	Temperature coefficient of input voltage	offset			25°C to 125°C		2.2		μV/°C
	Innut offeet current (e.e. Note 4)				25°C		0.1	60	pА
lio	Input offset current (see Note 4)			V E.V	125°C		1.8	15	nA
1	lanut bing gumant (one Note 4)		$V_{O} = 5 V$,	AIC = 2 A	25°C		0.7	60	pА
IВ	Input bias current (see Note 4)				125°C		10	35	nA
	Common-mode input voltage ra	nge			25°C	0 to 9	-0.3 to 9.2		V
VICR	(see Note 5)	3			Full range	0 to 8.5			V
					25°C	8	8.5		
Vон	High-level output voltage		$V_{ID} = 100 \text{ mV},$	$R_L = 10 \text{ k}\Omega$	−55°C	7.8	8.5		V
					125°C	7.8	8.4		
					25°C		0	50	
V_{OL}	Low-level output voltage		$V_{1D} = -100 \text{ mV},$	$I_{OL} = 0$	−55°C		0	50	mV
					125°C		0	50	
	Lorgo signal differential voltage				25°C	10	36		
AVD	Large-signal differential voltage amplification		$V_0 = 1 V to 6 V$,	$R_L = 10 \text{ k}\Omega$	−55°C	7	50		V/mV
	' 				125°C	7	27		
					25°C	65	85		
CMRR	Common-mode rejection ratio		V _{IC} = V _{ICR} min		−55°C	60	87		dB
					125°C	60	86		
	Cupply voltage rejection ratio				25°C	65	95		
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})		$V_{DD} = 5 V \text{ to } 10 V,$	$V_O = 1.4 V$	−55°C	60	90		dB
	. 55 10/				125°C	60	97		
			V _O = 5 V,	V F V	25°C		1.9	4	
lDD	Supply current (two amplifiers)		VO = 5 V, No load	$V_{IC} = 5 V$	−55°C		3	6	mA
					125°C		1.3	2.8	

[†] Full range is –55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

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electrical characteristics, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

	DADAMETED	TEST COM	DITIONS	Т	LC272Y		LINIT
	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	$V_{O} = 1.4 \text{ V},$ R _S = 50 Ω ,	V _{IC} = 0, R _L = 10 kΩ		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		μV/°C
IIO	Input offset current (see Note 4)	V 0.5.V	V 0.5.V		0.1		pA
I _{IB}	Input bias current (see Note 4)	$V_0 = 2.5 \text{ V},$	$V_{IC} = 2.5 V$		0.6		pA
VICR	Common-mode input voltage range (see Note 5)			-0.2 to 4	-0.3 to 4.2		٧
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$	R _L = 10 kΩ	3.2	3.8		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I _{OL} = 0		0	50	mV
AVD	Large-signal differential voltage amplification	V _O = 0.25 V to 2 V	R _L = 10 kΩ	5	23		V/mV
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}min$		65	80		dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95		dB
I _{DD}	Supply current (two amplifiers)	V _O = 2.5 V, No load	V _{IC} = 2.5 V,		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics, V_{DD} = 10 V, T_A = 25°C (unless otherwise noted)

	DADAMETED	TEST COM	DITIONS	Т	LC272Y		UNIT
	PARAMETER	TEST CONI	DITIONS	MIN	TYP	MAX	UNII
V _{IO}	Input offset voltage	$V_{O} = 1.4 \text{ V},$ $R_{S} = 50 \Omega,$	$V_{IC} = 0$, $R_L = 10 \text{ k}\Omega$		1.1	10	mV
α_{VIO}	Temperature coefficient of input offset voltage				1.8		μV/°C
lο	Input offset current (see Note 4)	V 5V			0.1		pА
I _{IB}	Input bias current (see Note 4)	$V_O = 5 V$	$V_{IC} = 5 V$		0.7		pА
VICR	Common-mode input voltage range (see Note 5)			-0.2 to 9	-0.3 to 9.2		V
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$	R _L = 10 kΩ	8	8.5		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I _{OL} = 0		0	50	mV
AVD	Large-signal differential voltage amplification	$V_0 = 1 \text{ V to 6 V},$	R _L = 10 kΩ	10	36		V/mV
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICR} min		65	85		dB
ksvr	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	$V_{DD} = 5 \text{ V to } 10 \text{ V},$	V _O = 1.4 V	65	95		dB
I _{DD}	Supply current (two amplifiers)	V _O = 5 V, No load	V _{IC} = 5 V,		1.9	4	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.



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operating characteristics at specified free-air temperature, $V_{DD} = 5 V$

PARAMETER		TEST CO	NDITIONS	TA	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
				ť	MIN	TYP	MAX	
				25°C		3.6		
			V _{IPP} = 1 V	0°C		4		
	Class rate at scales	$R_L = 10 \text{ k}\Omega$		70°C		3		\//a
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1		25°C		2.9		V/μs
			V _{IPP} = 2.5 V	0°C		3.1		
				70°C		2.5		
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz
		$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,		25°C		320		kHz
ВОМ	Maximum output-swing bandwidth			0°C		340		
			See rigure r	70°C		260		
				25°C		1.7		
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	0°C		2		MHz
		See Figure 3		70°C		1.3		
		.,,	, _	25°C		46°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	0°C		47°		
		OL = 20 pr ,	occ rigule 3	70°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST CO	NDITIONS	TA	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
					MIN	TYP	MAX	
				25°C		5.3		
			V _{IPP} = 1 V	0°C		5.9		
	Olever made and condition made	$R_L = 10 \text{ k}\Omega$		70°C		4.3		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1		25°C		4.6		V/μs
			V _{IPP} = 5.5 V	0°C		5.1		
				70°C		3.8		
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz
			C _L = 20 pF, See Figure 1	25°C		200)	
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_I = 10 \text{ k}\Omega$,		0°C		220		kHz
		$R_{\perp} = 10 \text{ Ks2},$		70°C		140		
				25°C		2.2		
В ₁	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	0°C		2.5		MHz
		See Figure 3		70°C		1.8		
				25°C		49°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	0°C		50°		
		OL − 20 pi²,	oce i iguie 3	70°C		46°		

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operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

	PARAMETER		NDITIONS	TA	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
					MIN	TYP	MAX	
				25°C		3.6		
			V _{IPP} = 1 V	−40°C		4.5		
0.0		$R_L = 10 \text{ k}\Omega$		85°C		2.8		V/μs
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1		25°C		2.9		
		ga.e .	V _{IPP} = 2.5 V	−40°C		3.5		
				85°C		2.3		
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz
		$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF, See Figure 1	25°C		320		
ВОМ	Maximum output-swing bandwidth			−40°C		380		kHz
				85°C		250		
				25°C		1.7		
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 \text{ pF},$	−40°C		2.6		MHz
		See rigure 3		85°C		1.2		
				25°C		46°		
φm	Phase margin	$V_{l} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	−40°C		49°		
		OL = 20 pr ,	occ riguic o	85°C		43°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	PARAMETER	TEST CO	NDITIONS	TA	TLC272I, TLC272AI, TLC272BI, TLC277I			UNIT
				,,	MIN	TYP	MAX	
				25°C		5.3		
			V _{IPP} = 1 V	−40°C		6.8		
0.0	Olevanote at well-	$R_L = 10 \text{ k}\Omega$		85°C		4		V/μs
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1		25°C		4.6		
		gara r	V _{IPP} = 5.5 V	−40°C		5.8		
				85°C		3.5		
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz
			C _L = 20 pF,	25°C		200		
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_I = 10 \text{ k}\Omega$,		−40°C	; 20	260		kHz
			See rigure r	85°C		130		
				25°C		2.2		
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	−40°C		3.1		MHz
		Gee rigure 3		85°C		1.7		
			, _	25°C		49°		_
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	−40°C		52°		
			occ riguic o	85°C		46°		

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operating characteristics at specified free-air temperature, $V_{DD} = 5 \text{ V}$

	DADAMETED	TEOT 00	NDITIONS	-	TLC272	2M, TLC	277M	
	PARAMETER	TEST CO	NDITIONS	TA	MIN	TYP	MAX	UNIT
				25°C		3.6		
			V _{IPP} = 1 V	−55°C		4.7		
	Class note at smits main	$R_L = 10 \text{ k}\Omega$		125°C		2.3		\//
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1		25°C		2.9		V/μs
			V _{IPP} = 2.5 V	−55°C		3.7		
				125°C		2		
Vn	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz
				25°C		320		kHz
ВОМ	Maximum output-swing bandwidth	$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,	C _L = 20 pF,	−55°C		400		
		N_ = 10 KS2,	Occ rigure r	125°C		230		
		.,		25°C		1.7		
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	−55°C		2.9		MHz
		occ rigure o		125°C		1.1		
			, _	25°C		46°		
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	−55°C		49°		
		ο _L = 20 μ,	CCC i iguic 3	125°C		41°		

operating characteristics at specified free-air temperature, V_{DD} = 10 V

	DADAMETED	TEST CO	NDITIONS	-	TLC272	M, TLC	277M							
	PARAMETER	TEST CO	NDITIONS	TA	MIN	TYP	MAX	UNIT						
				25°C		5.3								
			V _{IPP} = 1 V	−55°C		7.1								
CD.	Class rate at smits main	$R_L = 10 \text{ k}\Omega$		125°C		3.1		Miss						
SR	Slew rate at unity gain	C _L = 20 pF, See Figure 1		25°C		4.6		V/μs						
			V _{IPP} = 5.5 V	−55°C		6.1								
				125°C		2.7								
٧n	Equivalent input noise voltage	f = 1 kHz, See Figure 2	$R_S = 20 \Omega$,	25°C		25		nV/√ Hz						
		$V_O = V_{OH}$, $R_L = 10 \text{ k}\Omega$,		25°C		200								
ВОМ	Maximum output-swing bandwidth									−55°C		280		kHz
			See rigure r	125°C		110								
				25°C		2.2								
В1	Unity-gain bandwidth	V _I = 10 mV, See Figure 3	$C_L = 20 pF$,	−55°C		3.4		MHz						
		Gee rigure 3		125°C		1.6								
				25°C		49°		_						
φm	Phase margin	$V_{I} = 10 \text{ mV},$ $C_{L} = 20 \text{ pF},$	f = B ₁ , See Figure 3	−55°C		52°								
			See rigule 3	125°C		44°								

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operating characteristics, $V_{DD} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	_	EST CONDITIO	Ne	TLC272Y			UNIT
	FARAMETER	1	TEST CONDITIONS				MAX	UNII
CD	Slew rate at unity gain	$R_L = 10 \text{ k}\Omega$,	C _L = 20 pF,	V _{IPP} = 1 V		3.6		Mar
SR		See Figure 1		V _{IPP} = 2.5 V		2.9		V/μs
Vn	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$,	See Figure 2		25		nV/√ Hz
ВОМ	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	$C_L = 20 pF,$	$R_L = 10 \text{ k}\Omega$,		320		kHz
B ₁	Unity-gain bandwidth	$V_I = 10 \text{ mV},$	$C_L = 20 pF$,	See Figure 3		1.7		MHz
φm	Phase margin	V _I = 10 mV, See Figure 3	$f = B_1$,	$C_L = 20 pF,$		46°		

operating characteristics, V_{DD} = 10 V, T_A = 25°C

	PARAMETER	-	EST CONDITIO	Ne	TLC272Y			UNIT
	FARAMETER	11	TEST SCRETTIONS				MAX	UNII
CD	Clausesta at units anim	$R_L = 10 \text{ k}\Omega$,	C _L = 20 pF,	V _{IPP} = 1 V	5.3		Miss	
SR	Slew rate at unity gain	See Figure 1		V _{IPP} = 5.5 V		4.6		V/μs
Vn	Equivalent input noise voltage	f = 1 kHz,	$R_S = 20 \Omega$,	See Figure 2		25		nV/√ Hz
ВОМ	Maximum output-swing bandwidth	V _O = V _{OH} , See Figure 1	$C_L = 20 pF,$	$R_L = 10 \text{ k}\Omega$,		200		kHz
B ₁	Unity-gain bandwidth	$V_I = 10 \text{ mV},$	$C_L = 20 pF$,	See Figure 3		2.2		MHz
φm	Phase margin	V _I = 10 mV, See Figure 3	f = B ₁ ,	C _L = 20 pF,		49°		

PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLC272 and TLC277 are optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit gives the same result.

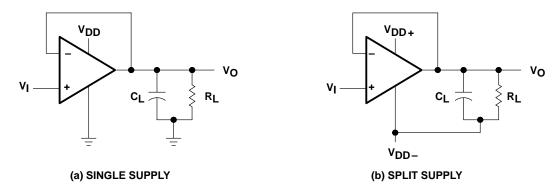


Figure 1. Unity-Gain Amplifier

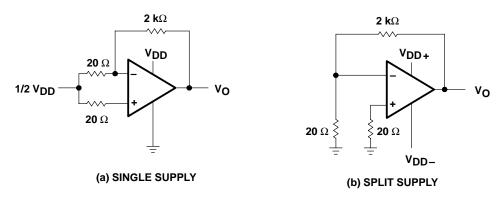


Figure 2. Noise-Test Circuit

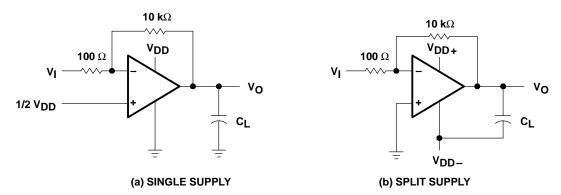


Figure 3. Gain-of-100 Inverting Amplifier



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PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLC272 and TLC277 operational amplifiers, attempts to measure the input bias current can result in erroneous readings. The bias current at normal room ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

- 1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 4). Leakages that would otherwise flow to the inputs are shunted away.
- 2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution: many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

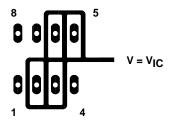


Figure 4. Isolation Metal Around Device Inputs (JG and P packages)

low-level output voltage

To obtain low-supply-voltage operation, some compromise was necessary in the input stage. This compromise results in the device low-level output being dependent on the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to Figures 14 through 19 in the Typical Characteristics of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture results in leakage and contact resistance, which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

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PARAMETER MEASUREMENT INFORMATION

full-power response

Full-power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 1. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 5). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

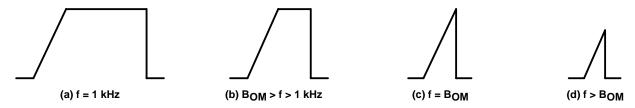


Figure 5. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.



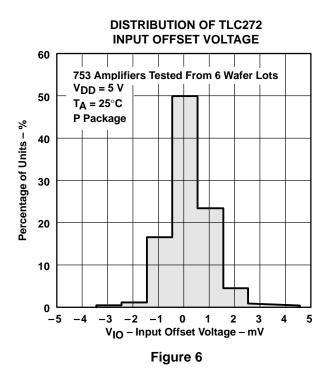
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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
VIO	Input offset voltage	Distribution	6, 7
αVIO	Temperature coefficient of input offset voltage	Distribution	8, 9
Vон	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	10, 11 12 13
V _{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	14, 15 16 17 18, 19
A _{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	20 21 32, 33
I _{IB}	Input bias current	vs Free-air temperature	22
IIO	Input offset current	vs Free-air temperature	22
VIC	Common-mode input voltage	vs Supply voltage	23
I _{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
VO(PP)	Maximum peak-to-peak output voltage	vs Frequency	29
B ₁	Unity-gain bandwidth	vs Free-air temperature vs Supply voltage	30 31
φm	Phase margin	vs Supply voltage vs Free-air temperature vs Load capacitance	34 35 36
Vn	Equivalent input noise voltage	vs Frequency	37
	Phase shift	vs Frequency	32, 33

TYPICAL CHARACTERISTICS



DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

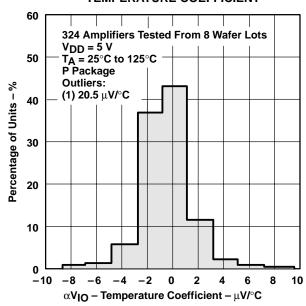


Figure 8

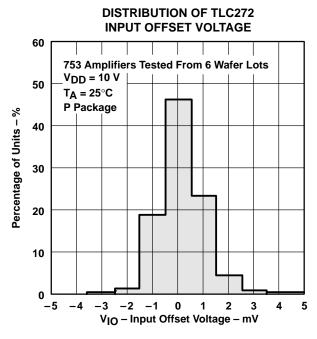


Figure 7

DISTRIBUTION OF TLC272 AND TLC277 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

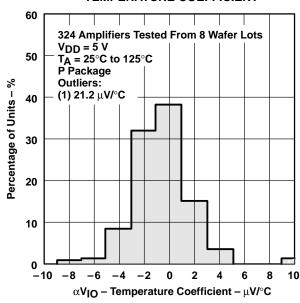
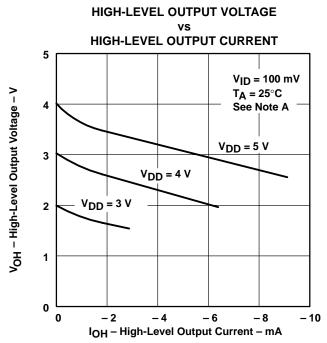
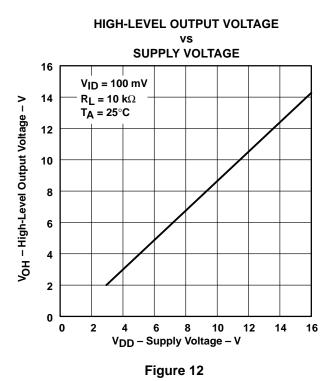


Figure 9



NOTE A: The 3-V curve only applies to the C version.

Figure 10



HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

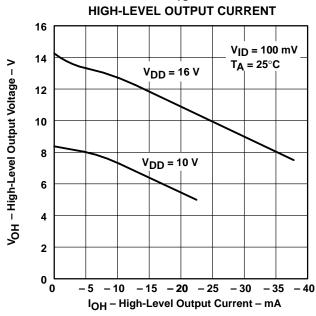


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE

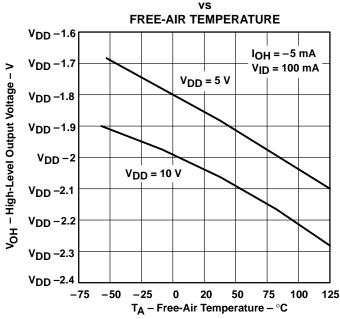
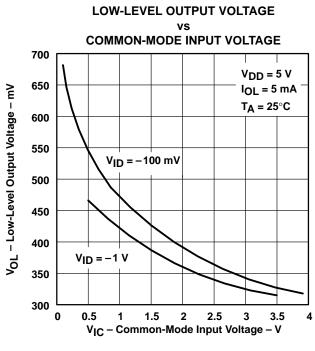


Figure 13

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.







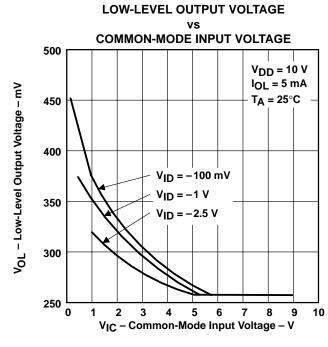


Figure 15

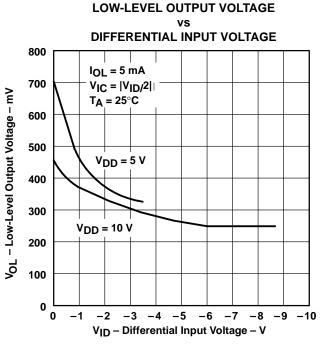
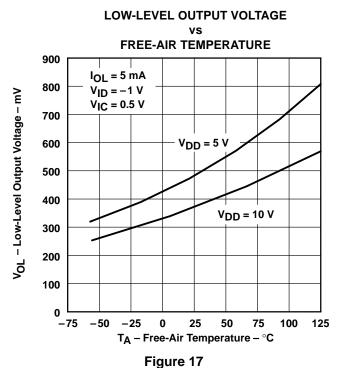
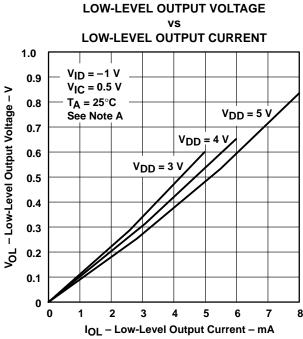


Figure 16



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





NOTE A: The 3-V curve only applies to the C version. **Figure 18**

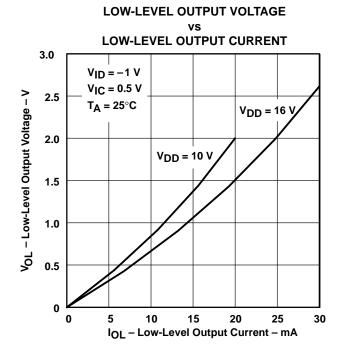
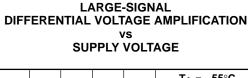
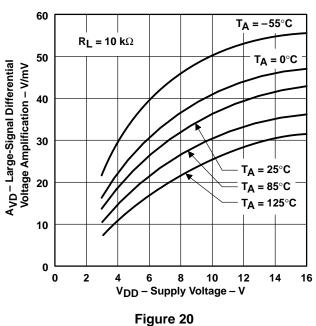


Figure 19





LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

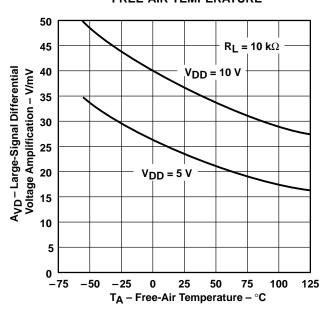


Figure 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



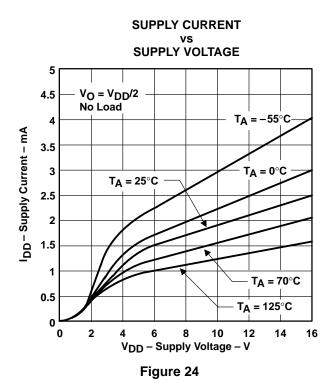
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT

FREE-AIR TEMPERATURE 10000 IIB and IIO - Input Bias and Offset Currents - pA V_{DD} = 10 V V_{IC} = 5 V See Note A 1000 lιΒ 100 llo 10 1 0.1 - 25 65 75 85 95 105

NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 22

T_A - Free-Air Temperature - °C



COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT VS SUPPLY VOLTAGE

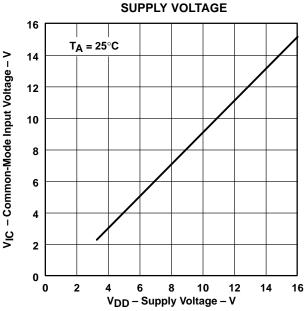


Figure 23

SUPPLY CURRENT vs

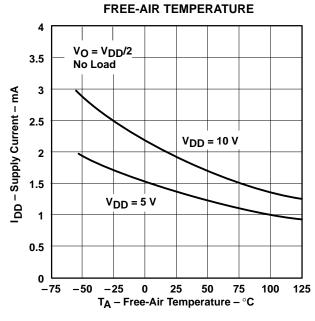


Figure 25

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



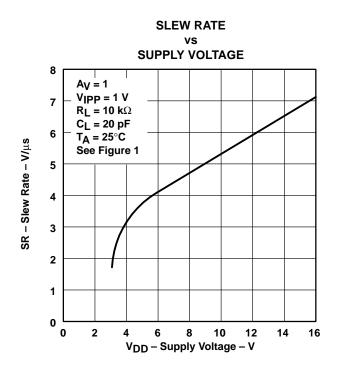


Figure 26

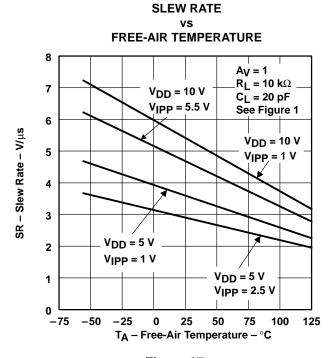
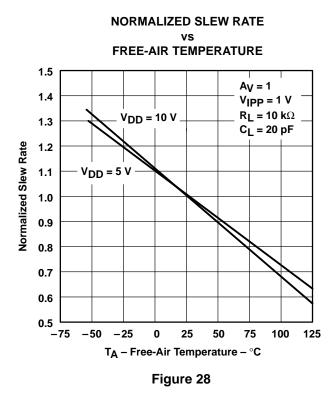
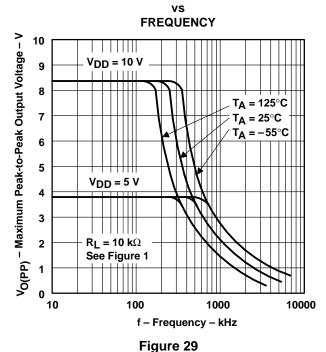


Figure 27

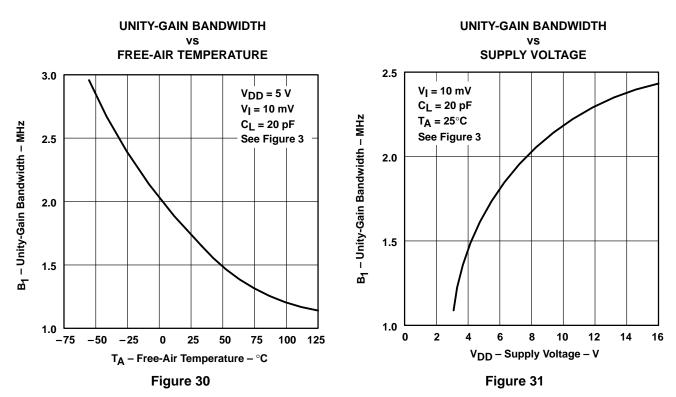


MAXIMUM PEAK OUTPUT VOLTAGE



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.





LARGE-SIGNAL DIFFERENTIAL VOLTAGE **AMPLIFICATION AND PHASE SHIFT**

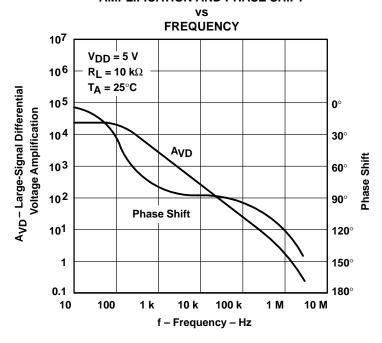


Figure 32

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT

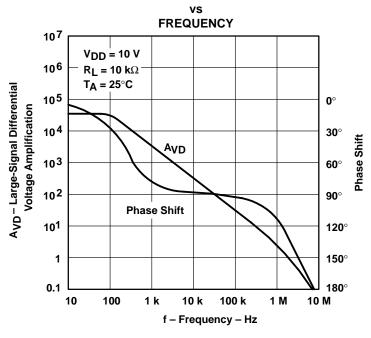
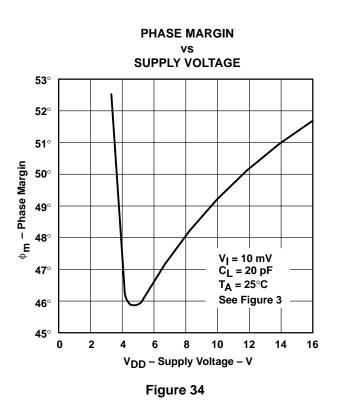
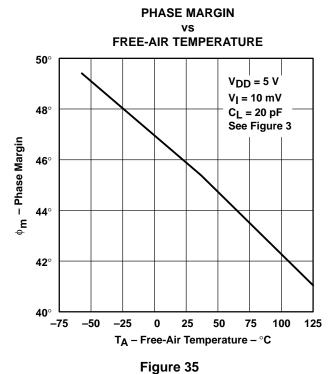


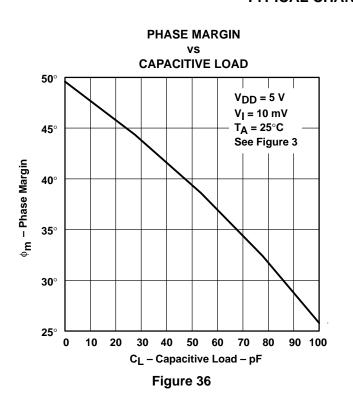
Figure 33

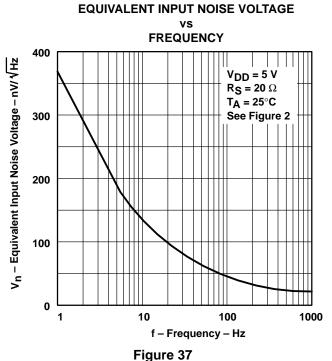




† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS





single-supply operation

While the TLC272 and TLC277 perform well using dual power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This design includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 3 V (C-suffix types), thus allowing operation with supply levels commonly available for TTL and HCMOS; however, for maximum dynamic range, 16-V single-supply operation is recommended.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. A resistive voltage divider is usually sufficient to establish this reference level (see Figure 38). The low input bias current of the TLC272 and TLC277 permits the use of very large resistive values to implement the voltage divider, thus minimizing power consumption.

The TLC272 and TLC277 work well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

- 1. Power the linear devices from separate bypassed supply lines (see Figure 39); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
- 2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, high-frequency applications may require RC decoupling.

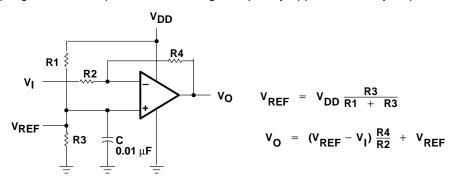


Figure 38. Inverting Amplifier With Voltage Reference

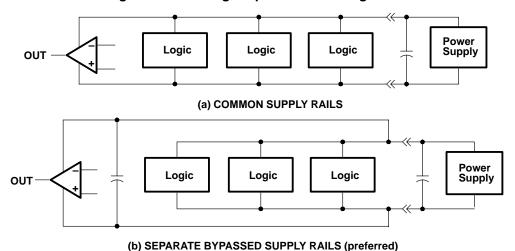


Figure 39. Common vs Separate Supply Rails

TEXAS INSTRUMENTS

input characteristics

The TLC272 and TLC277 are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD}-1$ V at $T_A=25^{\circ}$ C and at $V_{DD}-1.5$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLC272 and TLC277 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μ V/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLC272 and TLC277 are well suited for low-level signal processing; however, leakage currents on printed-circuit boards and sockets can easily exceed bias current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 4 in the Parameter Measurement Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 40).

Unused amplifiers should be connected as grounded unity-gain followers to avoid possible oscillation.

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLC272 and TLC277 result in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 k Ω , since bipolar devices exhibit greater noise currents.

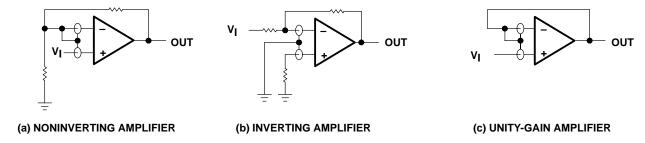


Figure 40. Guard-Ring Schemes

output characteristics

The output stage of the TLC272 and TLC277 is designed to sink and source relatively high amounts of current (see typical characteristics). If the output is subjected to a short-circuit condition, this high current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

All operating characteristics of the TLC272 and TLC277 are measured using a 20-pF load. The devices can drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figure 41). In many cases, adding a small amount of resistance in series with the load capacitance alleviates the problem.



output characteristics (continued)

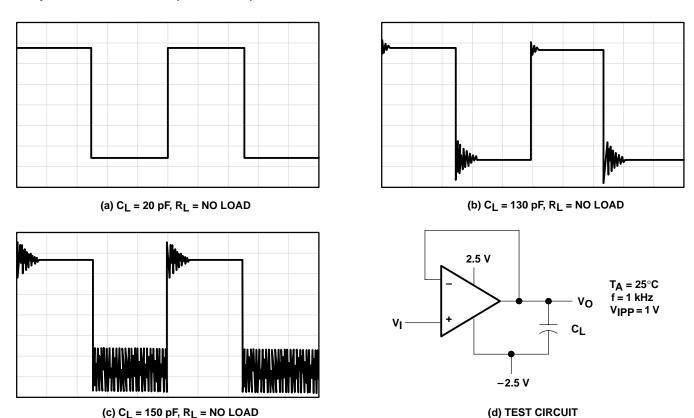
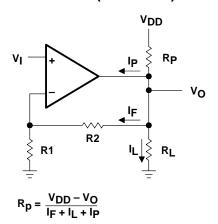


Figure 41. Effect of Capacitive Loads and Test Circuit

Although the TLC272 and TLC277 possess excellent high-level output voltage and current capability, methods for boosting this capability are available, if needed. The simplest method involves the use of a pullup resistor (Rp) connected from the output to the positive supply rail (see Figure 42). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on resistance between approximately 60 Ω and 180 Ω , depending on how hard the operational amplifier input is driven. With very low values of Rp, a voltage offset from 0 V at the output occurs. Second, pullup resistor Rp acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

output characteristics (continued)



 I_p = Pullup current required by the operational amplifier (typically 500 μ A)

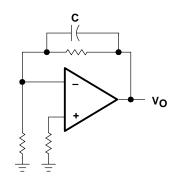


Figure 42. Resistive Pullup to Increase VOH

Figure 43. Compensation for Input Capacitance

feedback

Operational amplifier circuits almost always employ feedback, and since feedback is the first prerequisite for oscillation, some caution is appropriate. Most oscillation problems result from driving capacitive loads (discussed previously) and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 43). The value of this capacitor is optimized empirically.

electrostatic discharge protection

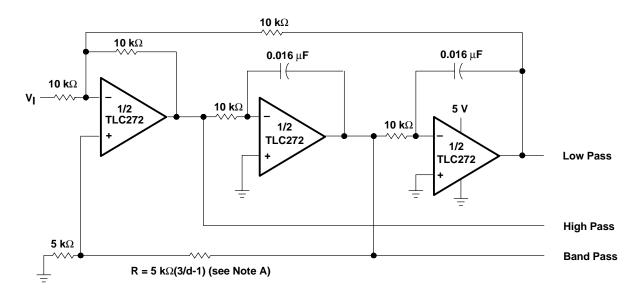
The TLC272 and TLC277 incorporate an internal electrostatic discharge (ESD) protection circuit that prevents functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC272 and TLC277 inputs and outputs were designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μ F typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occurring increases with increasing temperature and supply voltages.





NOTE A: d = damping factor, 1/Q

Figure 44. State-Variable Filter

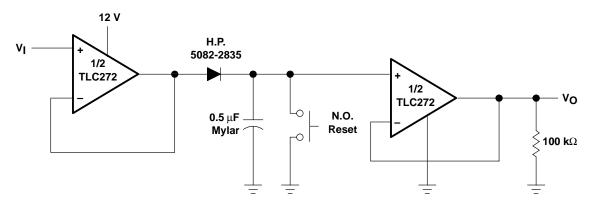
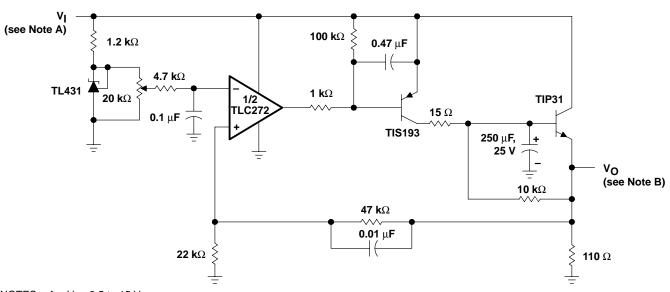
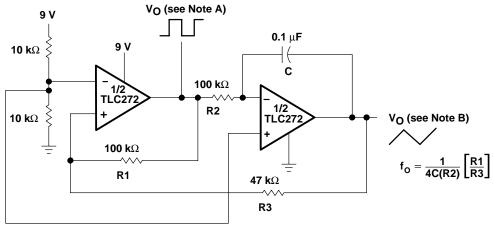


Figure 45. Positive-Peak Detector



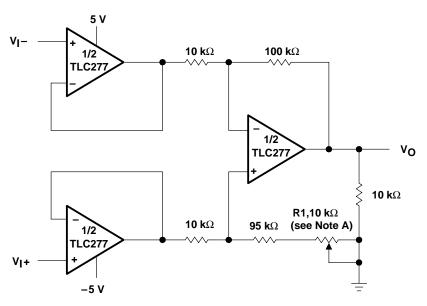
NOTES: A. $V_I = 3.5$ to 15 V B. $V_O = 2$ V, 0 to 1 A

Figure 46. Logic-Array Power Supply



NOTES: A. $V_{O(PP)} = 8 \text{ V}$ B. $V_{O(PP)} = 4 \text{ V}$

Figure 47. Single-Supply Function Generator



NOTE B: CMRR adjustment must be noninductive.

Figure 48. Low-Power Instrumentation Amplifier

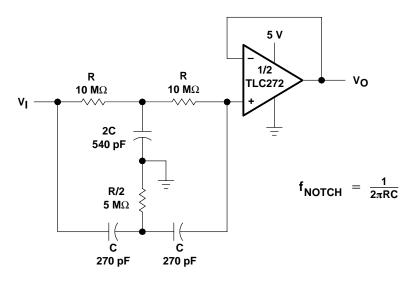


Figure 49. Single-Supply Twin-T Notch Filter

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TLC272ACD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	272AC
TLC272ACDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC
TLC272ACDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272AC
TLC272ACP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272ACP
TLC272ACP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272ACP
TLC272ACPE4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	Call TI	0 to 70	
TLC272AID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	272AI
TLC272AIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272AI
TLC272AIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272AIP
TLC272AIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272AIP
TLC272BCD	Obsolete	Production	SOIC (D) 8	-	=	Call TI	Call TI	0 to 70	272BC
TLC272BCDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC
TLC272BCDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272BC
TLC272BCP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272BCP
TLC272BCP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272BCP
TLC272BCPE4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	Call TI	0 to 70	
TLC272BCPS	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272B
TLC272BCPS.A	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272B
TLC272BID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	272BI
TLC272BIDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272BI
TLC272BIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272BIP
TLC272BIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272BIP
TLC272CD	Obsolete	Production	SOIC (D) 8	-	=	Call TI	Call TI	0 to 70	272C





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Orderable part number	, , , , , , , , , , , , , , , , , , , ,		Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)			
TLC272CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272C
TLC272CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	272C
TLC272CDR1G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272C
TLC272CDR1G4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	272C
TLC272CDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	0 to 70	
TLC272CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272CP
TLC272CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC272CP
TLC272CPE4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	Call TI	0 to 70	
TLC272CPS	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPS.A	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272
TLC272CPWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C
TLC272CPWR.A	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P272C
TLC272ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	2721
TLC272IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721
TLC272IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721
TLC272IDR1G4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721
TLC272IDR1G4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2721
TLC272IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC272IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272IP
TLC272IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC272IP
TLC272IPE4	Active	Production	PDIP (P) 8	50 TUBE	-	Call TI	Call TI	-40 to 85	
TLC277CD	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	0 to 70	277C
TLC277CDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	277C
TLC277CDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	277C
TLC277CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC277CP
TLC277CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC277CP
TLC277CPS	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277
TLC277CPS.A	Active	Production	SO (PS) 8	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277
TLC277CPSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277

-40 to 85

N/A for Pkg Type

11-Nov-2025

TLC277IP



TLC277IP.A

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Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
TLC277CPSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P277
TLC277ID	Obsolete	Production	SOIC (D) 8	-	-	Call TI	Call TI	-40 to 85	2771
TLC277IDR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2771
TLC277IDR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2771
TLC277IDRG4	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2771
TLC277IDRG4.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2771
TLC277IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC277IP

⁽¹⁾ Status: For more details on status, see our product life cycle.

Yes

NIPDAU

50 | TUBE

Production

PDIP (P) | 8

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



PACKAGE OPTION ADDENDUM

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC272ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272BIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272CPSR	so	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC272CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC272IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC272IDR1G4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC277IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC277IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



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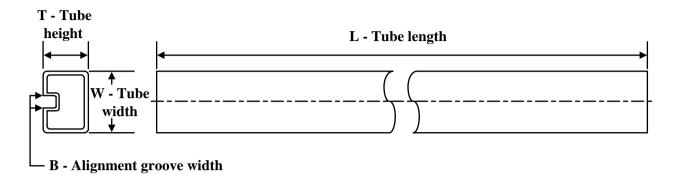
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC272ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLC272BCDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC272BIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272BIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TLC272CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272CDR1G4	SOIC	D	8	2500	353.0	353.0	32.0
TLC272CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC272CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC272IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC272IDR1G4	SOIC	D	8	2500	353.0	353.0	32.0
TLC277CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC277CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC277IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC277IDRG4	SOIC	D	8	2500	353.0	353.0	32.0



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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC272ACP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272ACP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272AIP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272AIP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272BCP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272BCP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272BCPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC272BCPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC272BIP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272BIP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272CP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272CP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC272CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC272IP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC272IP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TLC277CP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC277CP.A	Р	PDIP	8	50	506	13.97	11230	4.32
TLC277CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC277CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC277IP	Р	PDIP	8	50	506	13.97	11230	4.32
TLC277IP.A	Р	PDIP	8	50	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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