

TLC2654, TLC2654A

Advanced LinCMOS™ LOW-NOISE CHOPPER-STABILIZED OPERATIONAL AMPLIFIERS

SLOS020G – NOVEMBER 1988 – REVISED APRIL 2001

- **Input Noise Voltage**
 $0.5 \mu\text{V}$ (Peak-to-Peak) Typ, $f = 0$ to 1 Hz
 $1.5 \mu\text{V}$ (Peak-to-Peak) Typ, $f = 0$ to 10 Hz
 $47 \text{ nV}/\sqrt{\text{Hz}}$ Typ, $f = 10 \text{ Hz}$
 $13 \text{ nV}/\sqrt{\text{Hz}}$ Typ, $f = 1 \text{ kHz}$
- **High Chopping Frequency . . . 10 kHz Typ**
- **No Clock Noise Below 10 kHz**
- **No Intermodulation Error Below 5 kHz**
- **Low Input Offset Voltage**
 $10 \mu\text{V}$ Max (TLC2654A)
- **Excellent Offset Voltage Stability**
 With Temperature . . . $0.05 \mu\text{V}/^\circ\text{C}$ Max
- **A_{VD} . . . 135 dB Min (TLC2654A)**
- **CMRR . . . 110 dB Min (TLC2654A)**
- **k_{SVR} . . . 110 dB Min**
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range**
 Includes the Negative Rail
- **No Noise Degradation With External Capacitors Connected to $V_{\text{DD-}}$**
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control/Print Support Qualification to Automotive Standards**

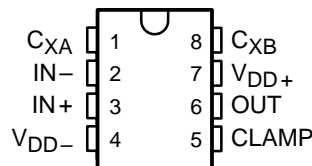
description

The TLC2654 and TLC2654A are low-noise chopper-stabilized operational amplifiers using the Advanced LinCMOS™ process. Combining this process with chopper-stabilization circuitry makes excellent dc precision possible. In addition, circuit techniques are added that give the TLC2654 and TLC2654A superior noise performance.

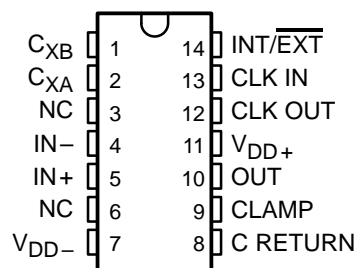
Chopper-stabilization techniques provide for extremely high dc precision by continuously nulling input offset voltage even during variations in temperature, time, common-mode voltage, and power-supply voltage. The high chopping frequency of the TLC2654 and TLC2654A (see Figure 1) provides excellent noise performance in a frequency spectrum from near dc to 10 kHz. In addition, intermodulation or aliasing error is eliminated from frequencies up to 5 kHz.

This high dc precision and low noise, coupled with the extremely high input impedance of the CMOS input stage, makes the TLC2654 and TLC2654A ideal choices for a broad range of applications such as low-level, low-frequency thermocouple amplifiers and strain gauges and wide-bandwidth and subsonic circuits. For applications requiring even greater dc precision, use the TLC2652 or TLC2652A devices, which have a chopping frequency of 450 Hz.

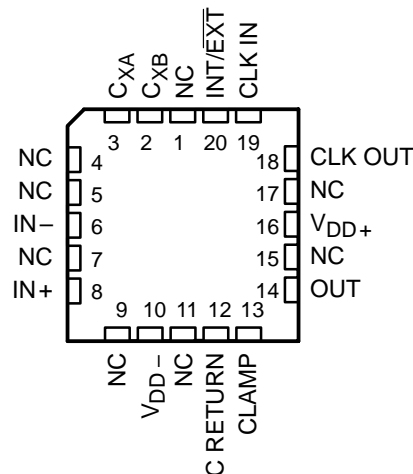
**D, JG, OR P PACKAGE
(TOP VIEW)**



**D, J, OR N PACKAGE
(TOP VIEW)**



**FK PACKAGE
(TOP VIEW)**



NC – No internal connection



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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description (continued)

The TLC2654 and TLC2654A common-mode input voltage range includes the negative rail, thereby providing superior performance in either single-supply or split-supply applications, even at power supply voltage levels as low as ± 2.3 V.

Two external capacitors are required to operate the device; however, the on-chip chopper-control circuitry is transparent to the user. On devices in the 14-pin and 20-pin packages, the control circuitry is accessible, allowing the user the option of controlling the clock frequency with an external frequency source. In addition, the clock threshold of the TLC2554 and TLC2654A requires no level shifting when used in the single-supply configuration with a normal CMOS or TTL clock input.

Innovative circuit techniques used on the TLC2654 and TLC2654A allow exceptionally fast overload recovery time. An output clamp pin is available to reduce the recovery time even further.

The device inputs and outputs are designed to withstand -100 -mA surge currents without sustaining latch-up. In addition, the TLC2654 and TLC2654A incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015; however, exercise care in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C . The I-suffix devices are characterized for operation from -40°C to 85°C . The Q-suffix devices are characterized for operation from -40°C to 125°C . The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C .

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

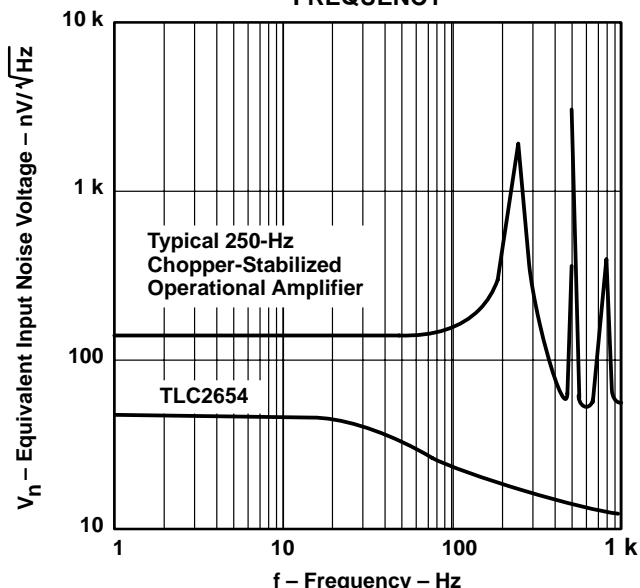


Figure 1

AVAILABLE OPTIONS

T_A	V_{IOmax} AT 25°C	PACKAGED DEVICES							
		8 PIN			14 PIN			20 PIN	
		SMALL OUTLINE (D)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SMALL OUTLINE (D)	CERAMIC DIP (J)	PLASTIC DIP (N)	CERAMIC DIP (FK)	
0°C to 70°C	10 μV 20 mV	TLC2654AC-8D	—	TLC2654ACP	TLC2654AC-14D	—	TLC2654ACN	—	
		TLC2654C-8D	—	TLC2654CP	TLC2654C-14D	—	TLC2654CN	—	
-40°C to 85°C	10 μV 20 μV	TLC2654AI-8D	—	TLC2654AIP	TLC2654AI-14D	—	TLC2654AIN	—	
		TLC2654I-8D	—	TLC2654IP	TLC2654I-14D	—	TLC2654IN	—	
-40°C to 125°C	10 μV 20 μV	TLC2654AQ-8D	—	—	—	—	—	—	
		TLC2654Q-8D	—	—	—	—	—	—	
-55°C to 125°C	10 μV 20 μV	TLC2654AM-8D	TLC2654AMJG	TLC2654AMP	TLC2654AM-14D	TLC2654AMJ	TLC2654AMN	TLC2654AMFK	
		TLC2654M-8D	TLC2654MJG	TLC2654MP	TLC2654M-14D	TLC2654MJ	TLC2654MN	TLC2654MFK	

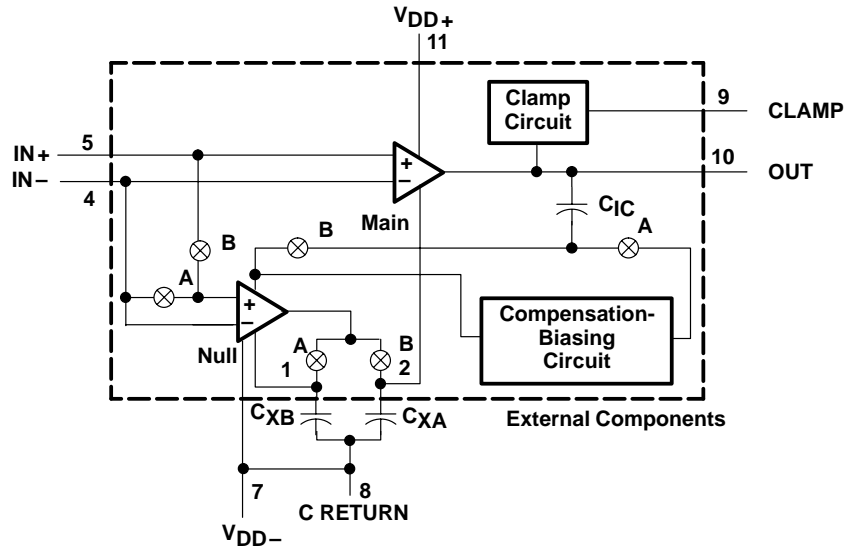
The 8-pin and 14-pin D packages are available taped and reeled. Add R suffix to device type (e.g., TLC2654AC-8DR).

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functional block diagram



Pin numbers shown are for the D (14 pin), J, and N packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	± 16 V
Input voltage, V_I (any input, see Note 1)	± 8 V
Voltage range on CLK IN and INT/EXT	V_{DD-} to $V_{DD-} + 5.2$ V
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Current into CLK IN and INT/EXT	± 5 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 85°C
Q suffix	–40°C to 125°C
M suffix	–55°C to 125°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or P package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or JG package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
2. Differential voltages are at $IN+$ with respect to $IN-$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8 pin)	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D (14 pin)	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	± 2.3	± 8	± 2.3	± 8	± 2.3	± 8	± 2.3	± 8	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V_{DD-}	$V_{DD+} - 2.3$	V
Clock input voltage	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V_{DD-}	$V_{DD-} + 5$	V
Operating free-air temperature, T_A	0	70	–40	85	–40	125	–55	125	°C



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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A †	TLC2654C			TLC2654AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage (see Note 4)	V _{IC} = 0, R _S = 50 Ω	25°C	5 20		4 10		μV		
			Full range	34		24				
αV _{IO}	Temperature coefficient of input offset voltage		Full range	0.01 0.05		0.01 0.05		μV/°C		
	Input offset voltage long-term drift (see Note 5)		25°C	0.003 0.06		0.003 0.02		μV/mo		
I _{IO}	Input offset current		25°C	30 60		30 60		pA		
			Full range	150		150				
I _{IB}	Input bias current		25°C	50 60		50 60		pA		
			Full range	150		150				
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	Full range	–5 to 2.7		–5 to 2.7		V		
V _{OM+}	Maximum positive peak output voltage swing	R _L = 10 kΩ, See Note 6	25°C	4.7	4.8	4.7	4.8	V		
			Full range	4.7		4.7				
V _{OM–}	Maximum negative peak output voltage swing	R _L = 10 kΩ, See Note 6	25°C	–4.7	–4.9	–4.7	–4.9	V		
			Full range	–4.7		–4.7				
A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V, R _L = 10 kΩ	25°C	120	155	135	155	dB		
			Full range	120		130				
	Internal chopping frequency		25°C	10		10		kHz		
	Clamp on-state current	R _L = 100 kΩ	25°C	25		25		μA		
			Full range	25		25				
	Clamp off-state current	V _O = –4 V to 4 V	25°C	100		100		pA		
			Full range	100		100				
CMRR	Common-mode rejection ratio	V _O = 0, V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	105	125	110	125	dB		
			Full range	105		110				
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ±2.3 V to ±8 V, V _O = 0, R _S = 50 Ω	25°C	110	125	110	125	dB		
			Full range	110		110				
I _{DD}	Supply current	V _O = 0, No load	25°C	1.5	2.4	1.5	2.4	mA		
			Full range	2.5		2.5				

† Full range is 0°C to 70°C.

- NOTES: 4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.
5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^{\circ}C$ extrapolated to $T_A = 25^{\circ}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
6. Output clamp is not connected.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS	T _A †	TLC2654C			TLC2654AC			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR +	Positive slew rate at unity gain	V _O = ±2.3 V, R _L = 10 kΩ, C _L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.3			1.3			
SR –	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.7			1.7			
V _n	Equivalent input noise voltage (see Note 7)	f = 10 Hz	25°C	47			47 75			nV/√Hz
		f = 1 kHz		13			13 20			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C	0.5			0.5			μV
		f = 0 to 10 Hz		1.5			1.5			
I _n	Equivalent input noise current	f = 10 kHz	25°C	0.004			0.004			pA/√Hz
Gain-bandwidth product		f = 10 kHz, R _L = 10 kΩ, C _L = 100 pF	25°C	1.9			1.9			MHz
φ _m	Phase margin at unity gain	R _L = 10 kΩ, C _L = 100 pF	25°C	48°			48°			

† Full range is 0°C to 70°C.

NOTE 7: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.



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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A †	TLC2654I			TLC2654AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage (see Note 4)	V _{IC} = 0, R _S = 50 Ω	25°C	5 20		4 10		μV			
			Full range	40		30					
α _{VIO}	Temperature coefficient of input offset voltage		Full range	0.01 0.05		0.01 0.05		μV/°C			
	Input offset voltage long-term drift (see Note 5)		25°C	0.003 0.06		0.003 0.02		μV/mo			
I _{IO}	Input offset current		25°C	30 60		30 60		pA			
			Full range	200		200					
I _{IB}	Input bias current		25°C	50 60		50 60		pA			
			Full range	200		200					
V _{ICR}	Common-mode input voltage range	R _S = 50 Ω	Full range	–5 to 2.7		–5 to 2.7		V			
V _{OM+}	Maximum positive peak output voltage swing	R _L = 10 kΩ, See Note 6	25°C	4.7	4.8	4.7	4.8	V			
			Full range	4.7		4.7					
V _{OM–}	Maximum negative peak output voltage swing	R _L = 10 kΩ, See Note 6	25°C	–4.7	–4.9	–4.7	–4.9	V			
			Full range	–4.7		–4.7					
A _{VD}	Large-signal differential voltage amplification	V _O = ±4 V, R _L = 10 kΩ	25°C	120	155	135	155	dB			
			Full range	120		125					
	Internal chopping frequency		25°C	10		10		kHz			
	Clamp on-state current	R _L = 100 kΩ	25°C	25		25		μA			
			Full range	25		25					
	Clamp off-state current	V _O = –4 V to 4 V	25°C	100		100		pA			
			Full range	100		100					
CMRR	Common-mode rejection ratio	V _O = 0, V _{IC} = V _{ICRmin} , R _S = 50 Ω	25°C	105	125	110	125	dB			
			Full range	105		110					
k _{SVR}	Supply voltage rejection ratio (ΔV _{DD±} /ΔV _{IO})	V _{DD±} = ± 2.3 V to ± 8 V, V _O = 0, R _S = 50 Ω	25°C	110	125	110	125	dB			
			Full range	110		110					
I _{DD}	Supply current	V _O = 0, No load	25°C	1.5	2.4	1.5	2.4	mA			
			Full range	2.5		2.5					

† Full range is $-40^\circ C$ to $85^\circ C$

- NOTES: 4. This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.
5. Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
6. Output clamp is not connected.

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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS	T _A [†]	TLC2654I			TLC2654AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain	V _O = ±2.3 V, R _L = 10 kΩ, C _L = 100 pF	25°C	1.5	2		1.5	2		V/μs
			Full range	1.2			1.2			
SR–	Negative slew rate at unity gain		25°C	2.3	3.7		2.3	3.7		V/μs
			Full range	1.5			1.5			
V _n	Equivalent input noise voltage (see Note 7)	f = 10 Hz	25°C	47			47 75			nV/√Hz
		f = 1 kHz		13			13 20			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0 to 1 Hz	25°C	0.5			0.5			μV
		f = 0 to 10 Hz		1.5			1.5			
I _n	Equivalent input noise current	f = 10 kHz	25°C	0.004			0.004			pA/√Hz
Gain-bandwidth product		f = 10 kHz, R _L = 10 kΩ, C _L = 100 pF	25°C	1.9			1.9			MHz
φ _m	Phase margin at unity gain	R _L = 10 kΩ, C _L = 100 pF	25°C	48°			48°			

† Full range is -40°C to 85°C .

NOTE 7: This parameter is tested on a sample basis for the TLC2654A. For other test requirements, please contact the factory. This statement has no bearing on testing or nontesting of other parameters.



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electrical characteristics at specified free-air temperature, $V_{DD} \pm = \pm 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2654Q TLC2654M			TLC2654AQ TLC2654AM			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage (see Note 4)	$V_{IC} = 0, \quad R_S = 50 \, \Omega$	25°C		5	20		4	10	μV
		Full range			50			40	
α_{VIO} Temperature coefficient of input offset voltage		Full range		0.01	0.05*		0.01	0.05*	$\mu V/^{\circ}C$
Input offset voltage long-term drift (see Note 5)		25°C		0.003	0.06*		0.003	0.02*	$\mu V/mo$
I_{IO} Input offset current		25°C		30	60		30	60	pA
		Full range			500			500	
I_{IB} Input bias current		25°C		50	60		50	60	pA
		Full range			500			500	
V_{ICR} Common-mode input voltage range	$R_S = 50 \, \Omega$	Full range		–5 to 2.7			–5 to 2.7		V
V_{OM+} Maximum positive peak output voltage swing	$R_L = 10 \, k\Omega, \quad$ See Note 6	25°C		4.7	4.8		4.7	4.8	V
		Full range		4.7			4.7		
V_{OM-} Maximum negative peak output voltage swing	$R_L = 10 \, k\Omega, \quad$ See Note 6	25°C		–4.7	–4.9		–4.7	–4.9	V
		Full range		–4.7			–4.7		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4 \, V, \quad R_L = 10 \, k\Omega$	25°C		120	155		135	155	dB
		Full range		120			120		
Internal chopping frequency		25°C		10			10		kHz
Clamp on-state current	$R_L = 100 \, k\Omega$	25°C		25			25		μA
		Full range		25			25		
Clamp off-state current	$V_O = -4 \, V \text{ to } 4 \, V$	25°C			100			100	pA
		Full range			500			500	
CMRR Common-mode rejection ratio	$V_O = 0, \quad V_{IC} = V_{ICRmin}, \quad R_S = 50 \, \Omega$	25°C		105	125		110	125	dB
		Full range		105			110		
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD} \pm / \Delta V_{IO}$)	$V_{DD} \pm = \pm 2.3 \, V \text{ to } \pm 8 \, V, \quad V_O = 0, \quad R_S = 50 \, \Omega$	25°C		110	125		110	125	dB
		Full range		105			110		
I_{DD} Supply current	$V_O = 0, \quad$ No load	25°C		1.5	2.4		1.5	2.4	mA
		Full range			2.5			2.5	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.

† Full range is -40° to $125^{\circ}C$ for Q suffix, -55° to $125^{\circ}C$ for M suffix.

- NOTES:
- This parameter is not production tested full range. Thermocouple effects preclude measurement of the actual V_{IO} of these devices in high-speed automated testing. V_{IO} is measured to a limit determined by the test equipment capability at the temperature extremes. The test ensures that the stabilization circuitry is performing properly.
 - Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^{\circ}C$ extrapolated to $T_A = 25^{\circ}C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
 - Output clamp is not connected.



TLC2654, TLC2654A

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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A^\dagger	TLC2654Q TLC2654M TLC2654AQ TLC2654AM			UNIT
			MIN	TYP	MAX	
SR+ Positive slew rate at unity gain	$V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	1.5	2		V/ μs
		Full range	1.1			
SR– Negative slew rate at unity gain		25°C	2.3	3.7		V/ μs
		Full range	1.3			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		47		nV/ $\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$	25°C		13		
$V_{N(PP)}$ Peak-to-peak equivalent input noise voltage	$f = 0\text{ to }1\text{ Hz}$	25°C		0.5		μV
	$f = 0\text{ to }10\text{ Hz}$	25°C		1.5		
I_n Equivalent input noise current	$f = 1\text{ kHz}$	25°C		0.004		pA/ $\sqrt{\text{Hz}}$
Gain-bandwidth product	$f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		1.9		MHz
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		48°		

† Full range is -40° to 125°C for Q suffix, -55° to 125°C for M suffix.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2
	Normalized input offset voltage	vs Chopping frequency	3
I_{IO}	Input offset current	vs Chopping frequency vs Free-air temperature	4 5
I_{IB}	Input bias current	vs Common-mode input voltage vs Chopping frequency vs Free-air temperature	6 7 8
	Clamp current	vs Output voltage	9
V_{OM}	Maximum peak output voltage swing	vs Output current vs Free-air temperature	10 11
$V_{O(PP)}$	Maximum peak-to-peak output voltage swing	vs Frequency	12
CMRR	Common-mode rejection ratio	vs Frequency	13
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	14 15
	Chopping frequency	vs Supply voltage vs Free-air temperature	16 17
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	18 19
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	20 21
SR	Slew rate	vs Supply voltage vs Free-air temperature	22 23
	Voltage-follower pulse response	Small signal Large signal	24 25
$V_{N(PP)}$	Peak-to-peak input noise voltage	vs Chopping frequency	26, 27
V_n	Equivalent input noise voltage	vs Frequency	28
kSVR	Supply voltage rejection ratio	vs Frequency	29
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	30 31
ϕ_m	Phase margin	vs Supply voltage vs Load capacitance	32 33
	Phase shift	vs Frequency	14

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TYPICAL CHARACTERISTICS†

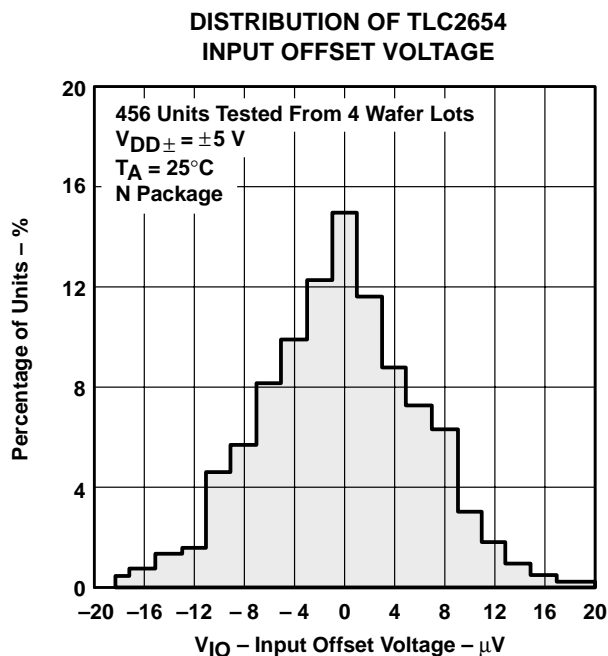


Figure 2

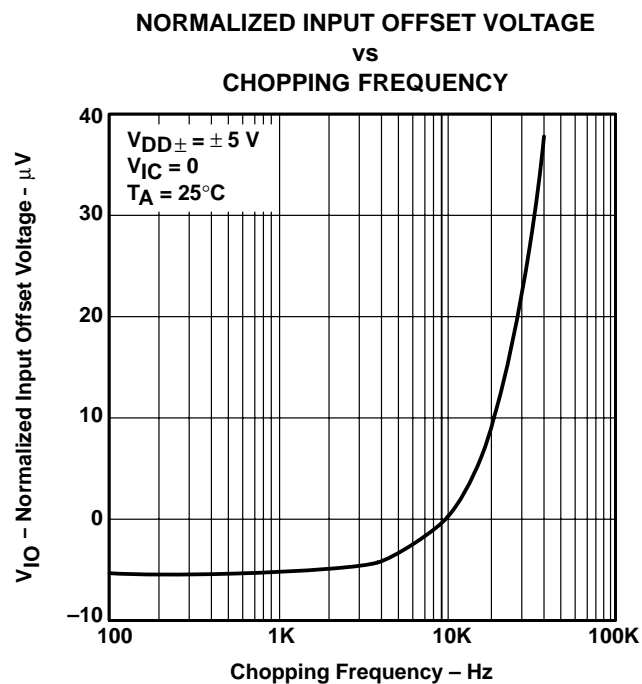


Figure 3

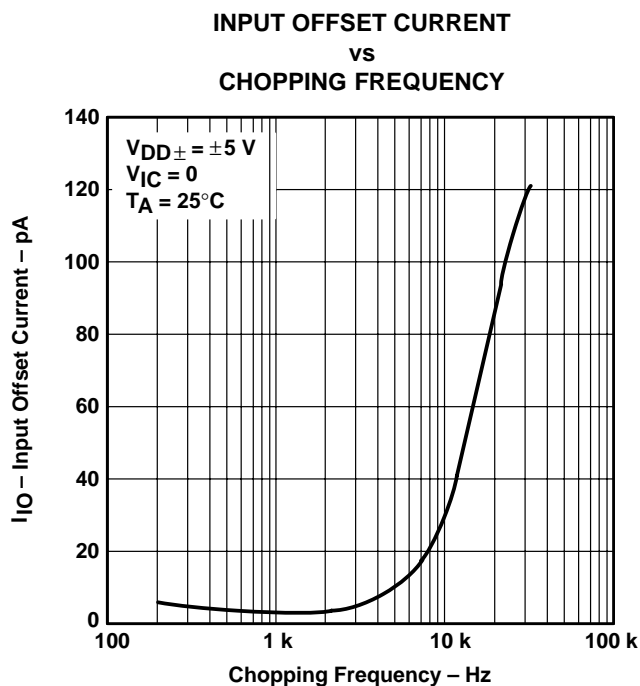


Figure 4

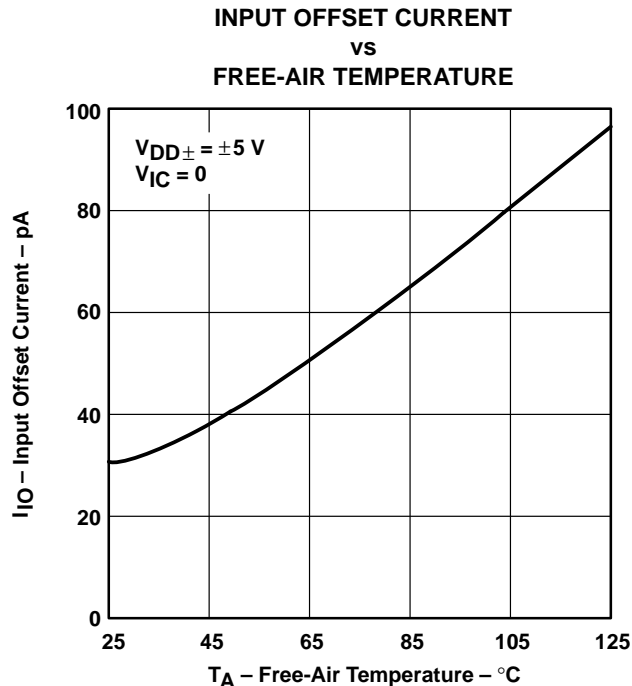


Figure 5

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

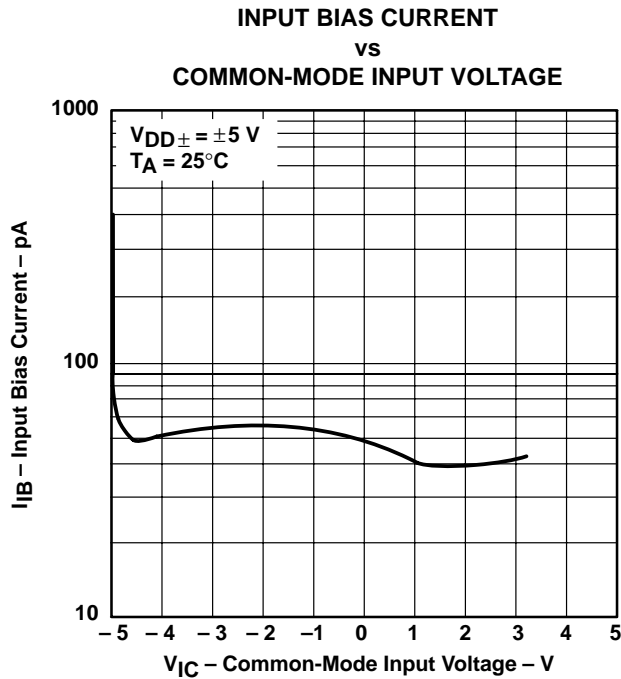


Figure 6

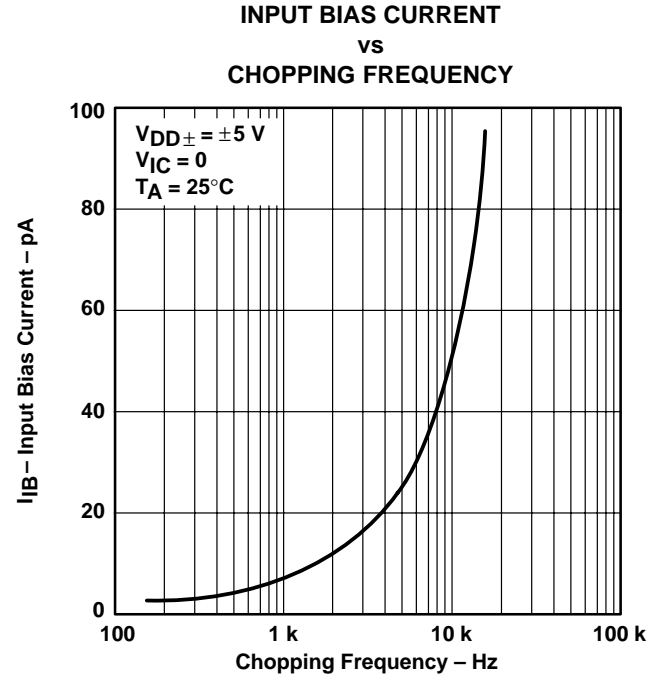


Figure 7

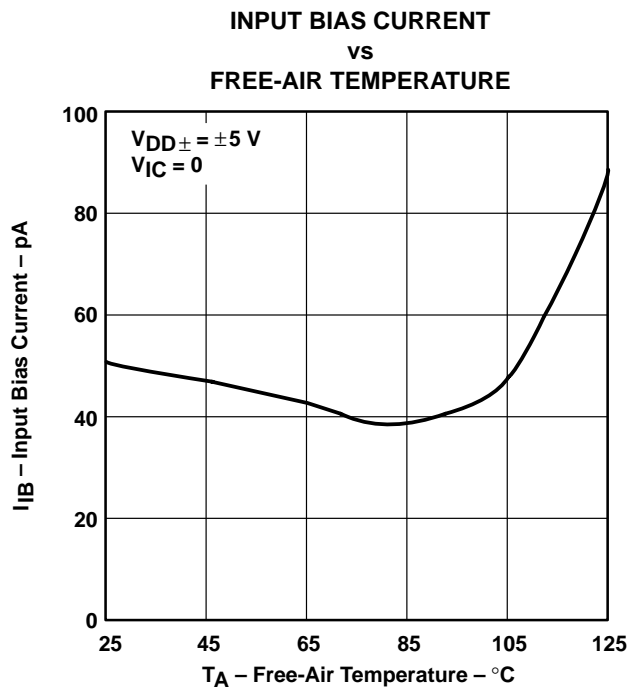


Figure 8

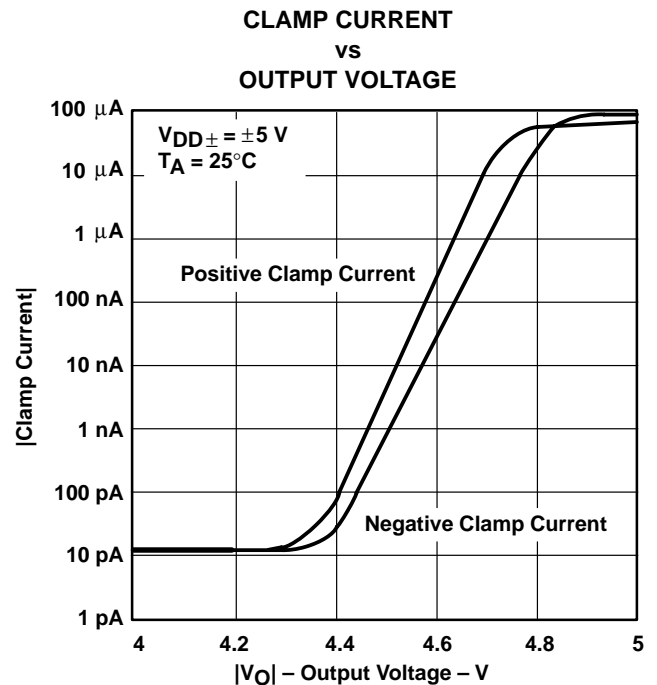


Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

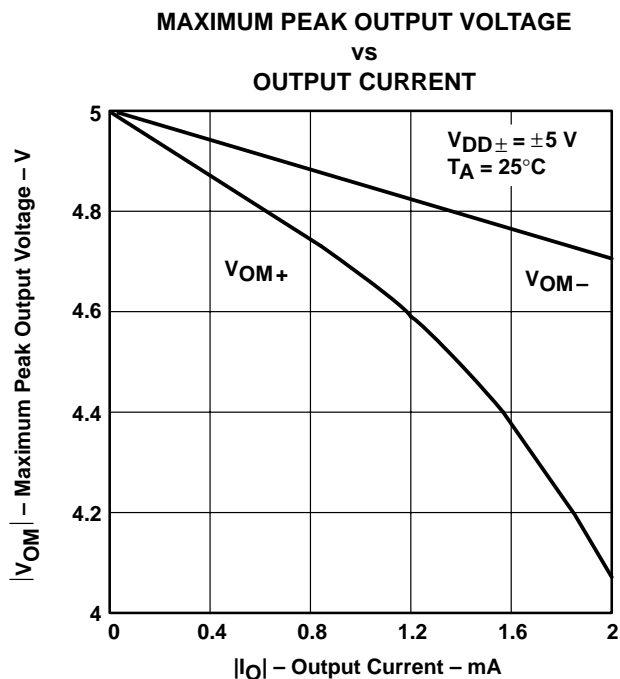


Figure 10

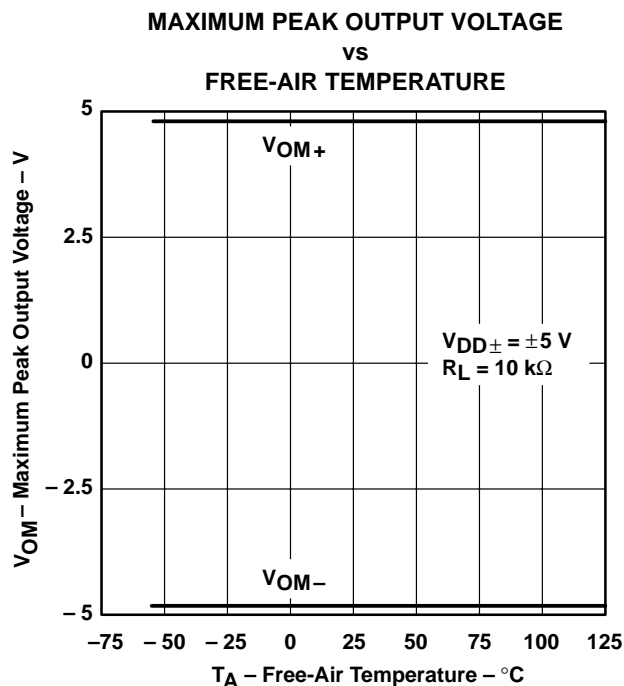


Figure 11

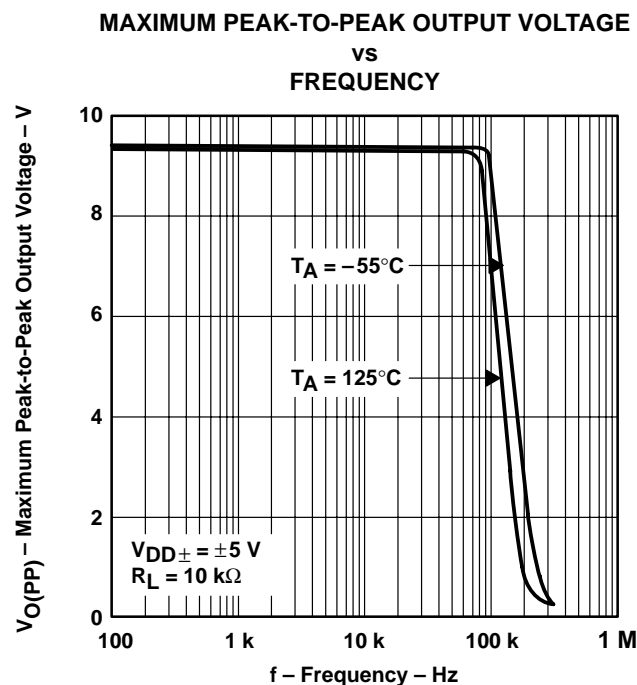


Figure 12

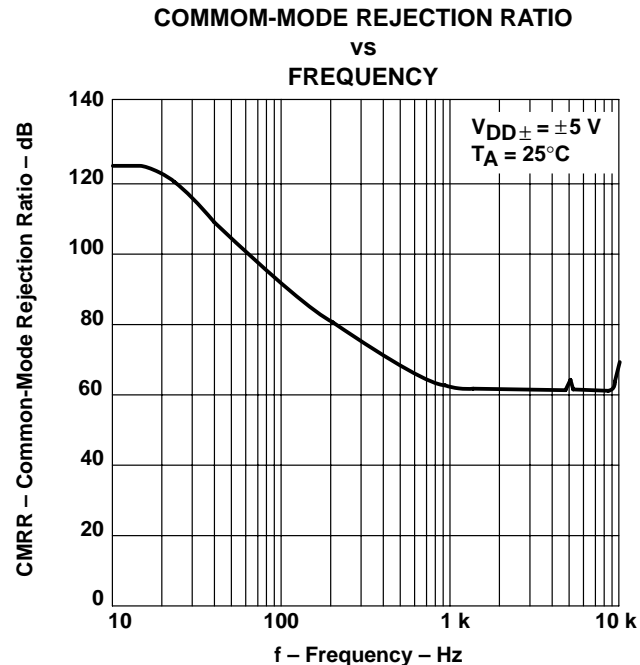


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

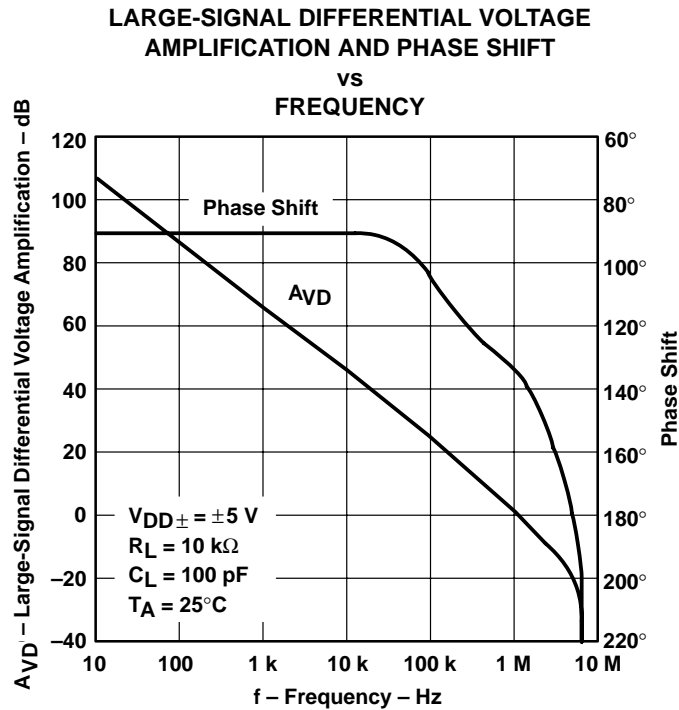


Figure 14

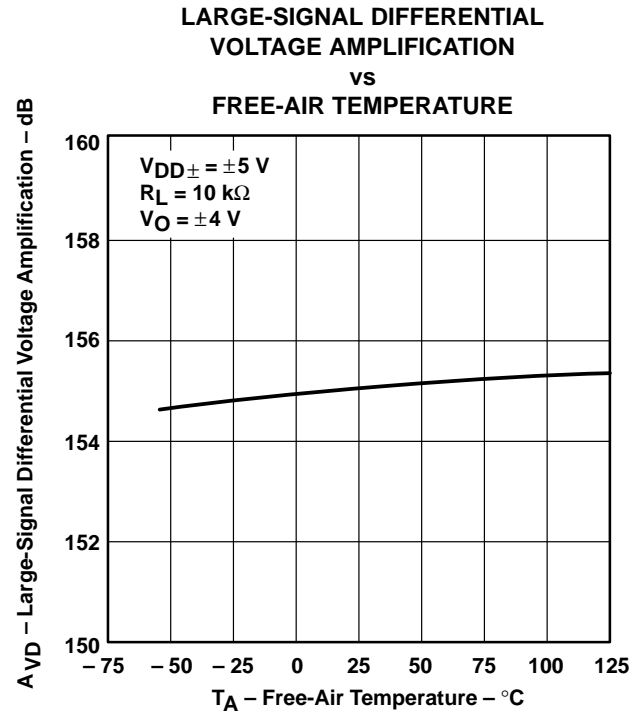


Figure 15

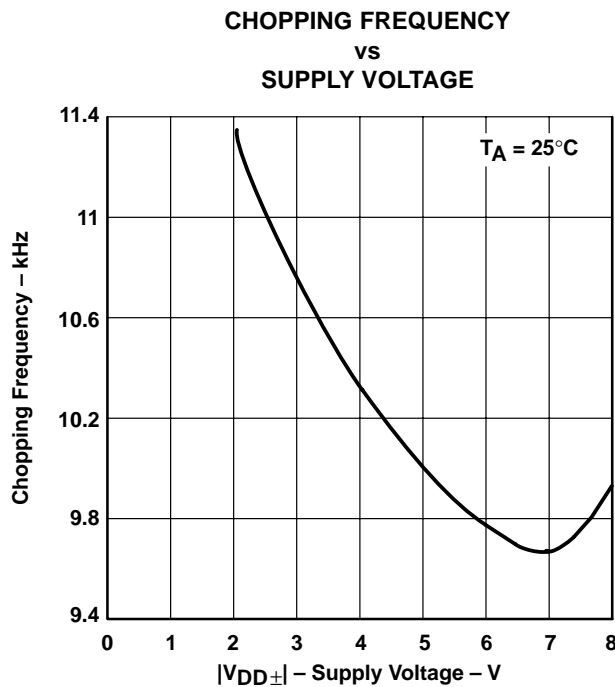


Figure 16

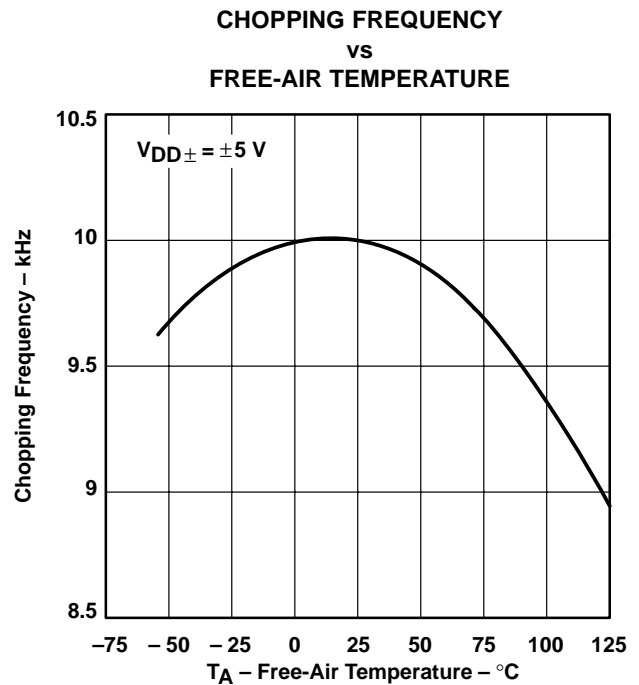


Figure 17

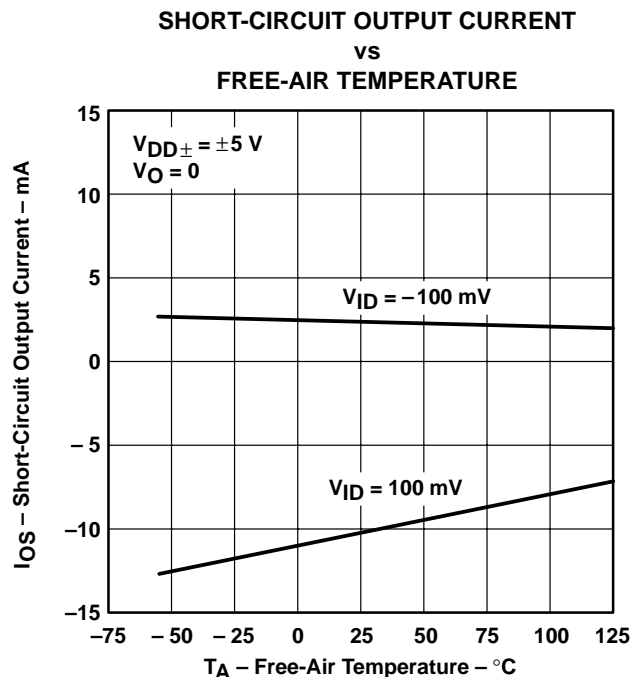
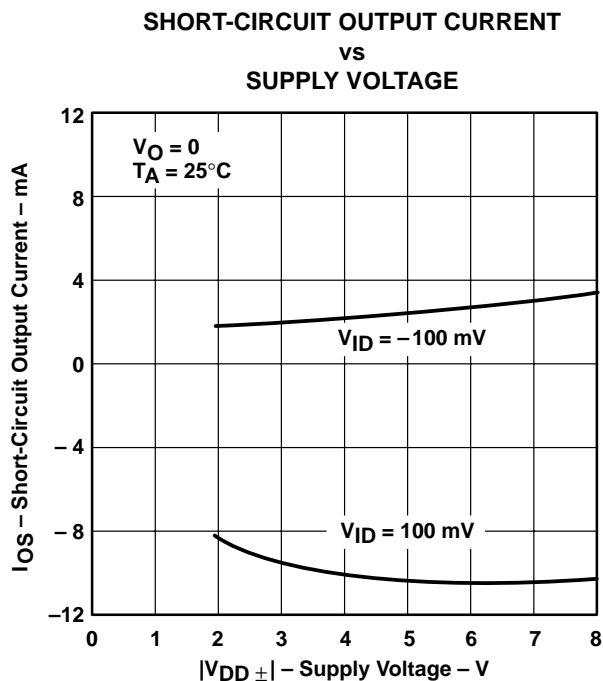
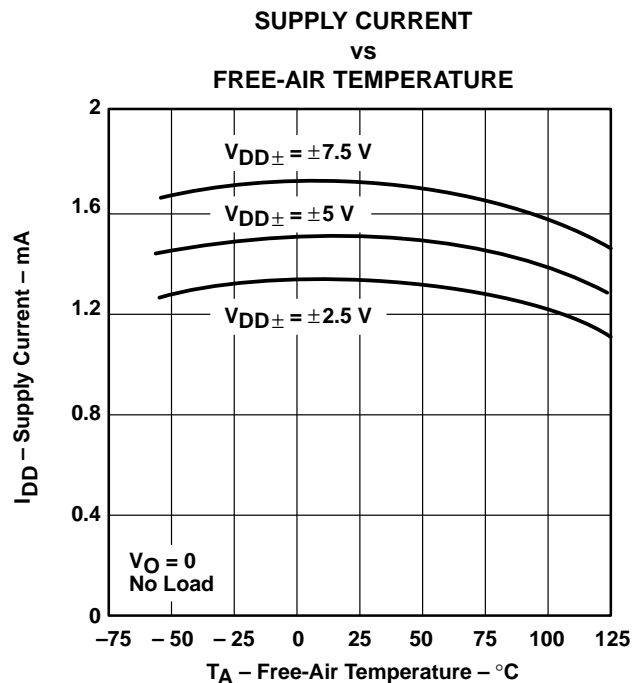
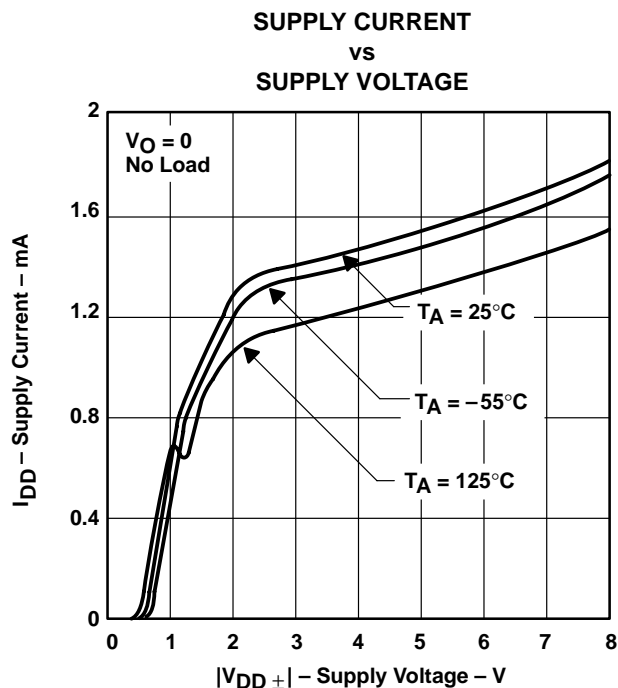
† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS†

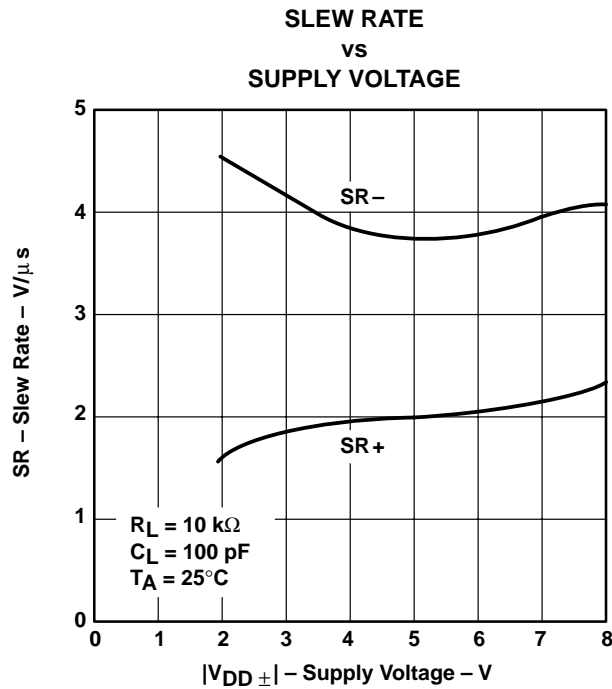


Figure 22

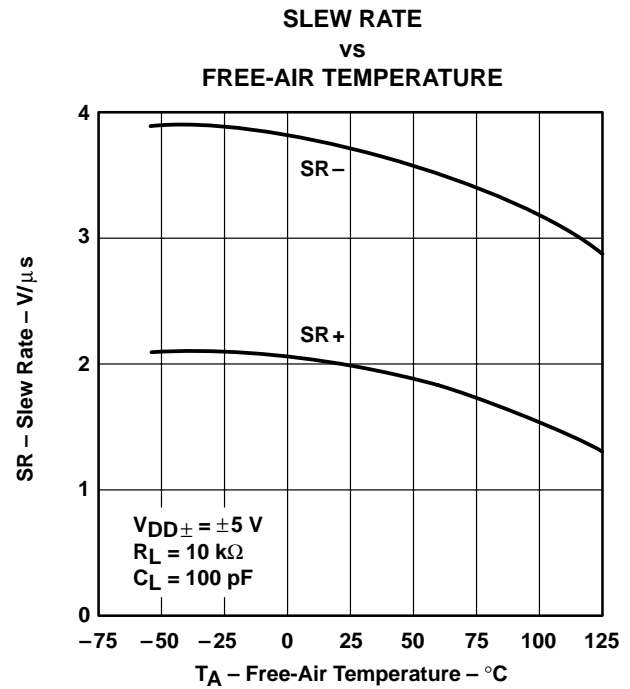


Figure 23

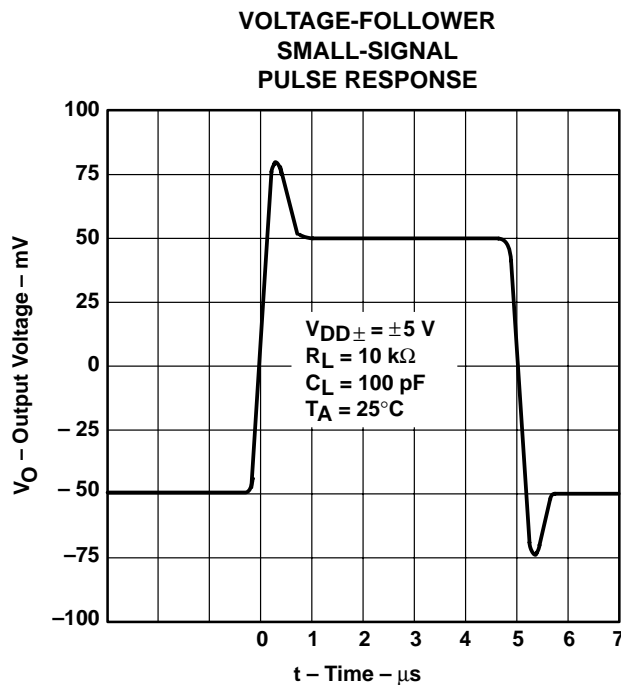


Figure 24

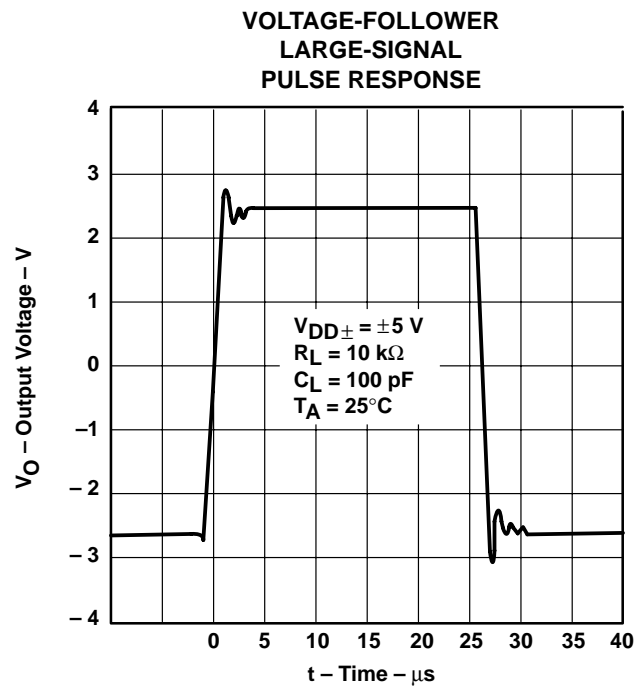


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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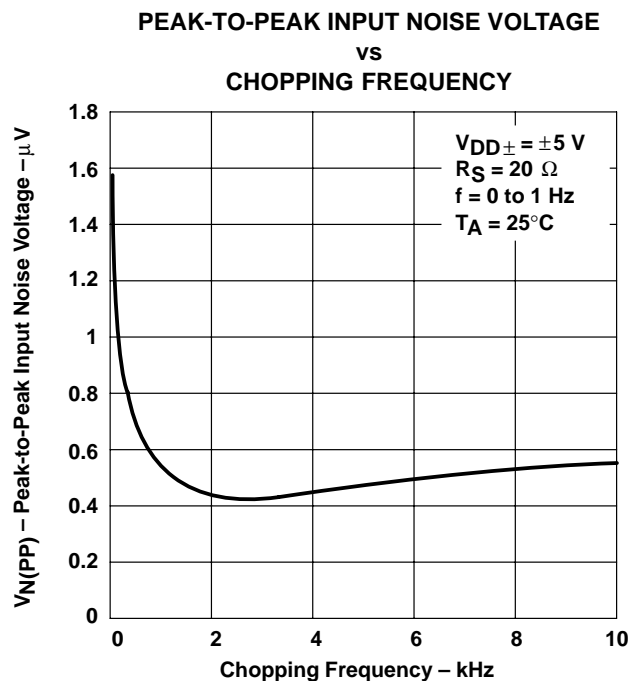


Figure 26

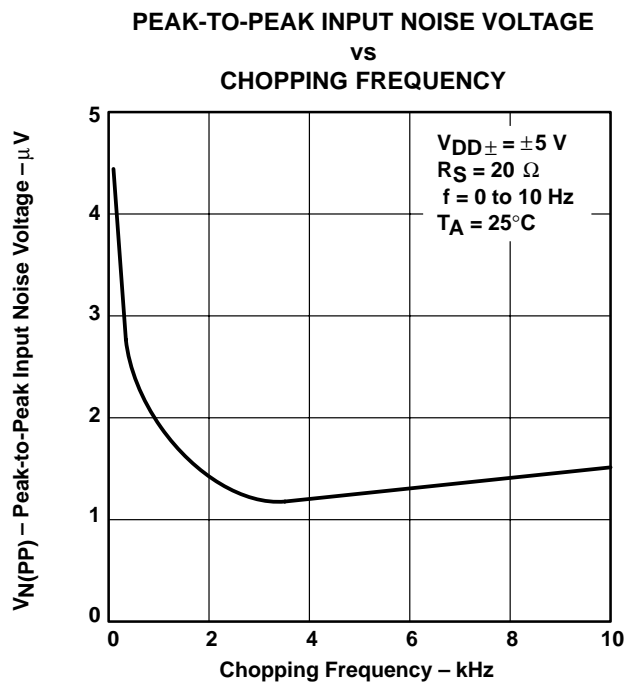


Figure 27

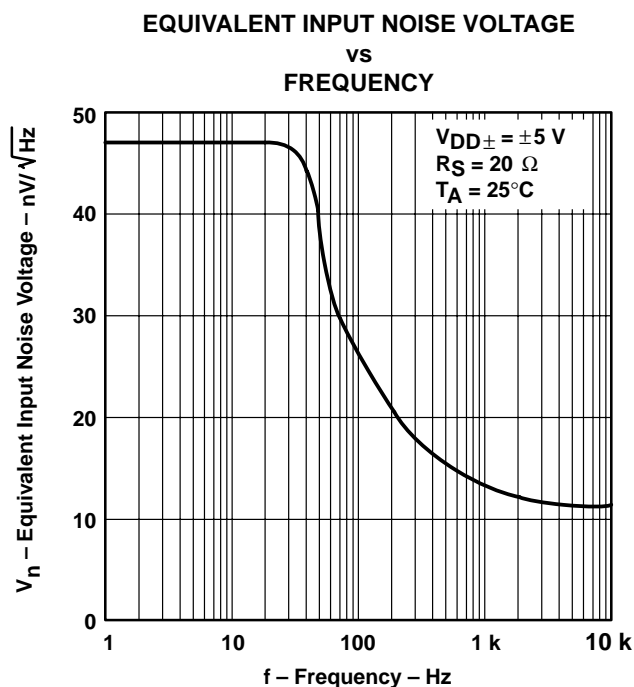


Figure 28

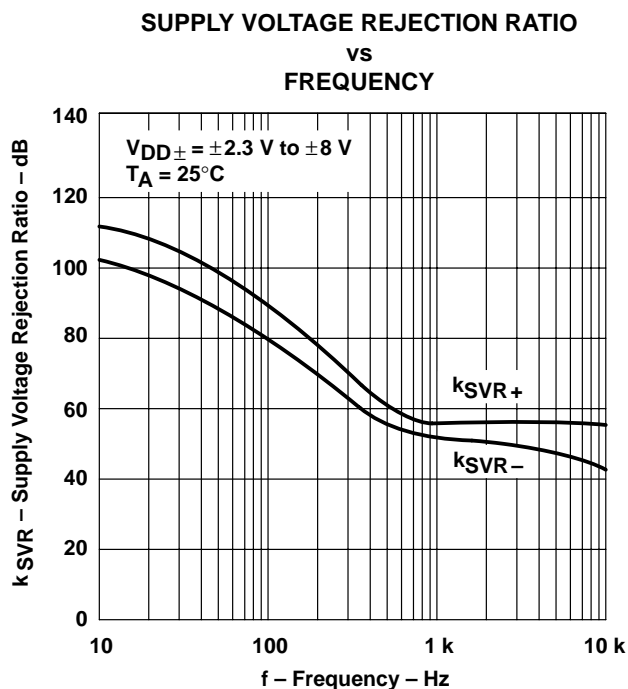


Figure 29

TYPICAL CHARACTERISTICS†

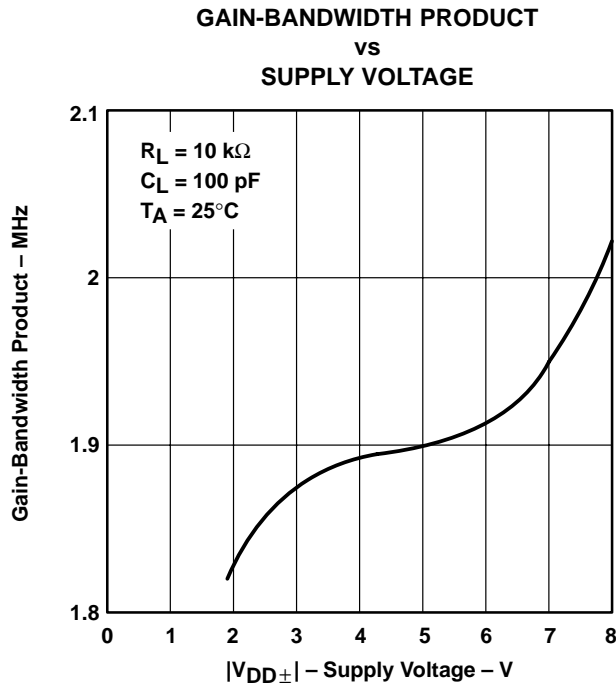


Figure 30

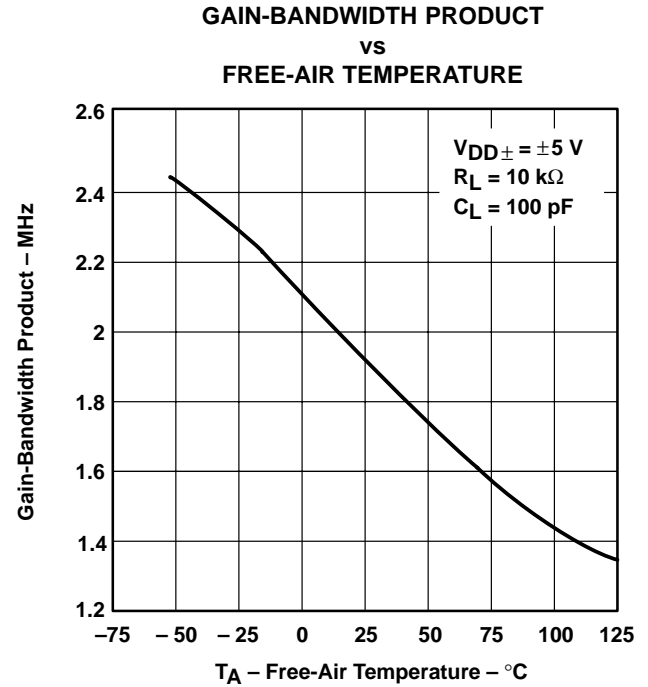


Figure 31

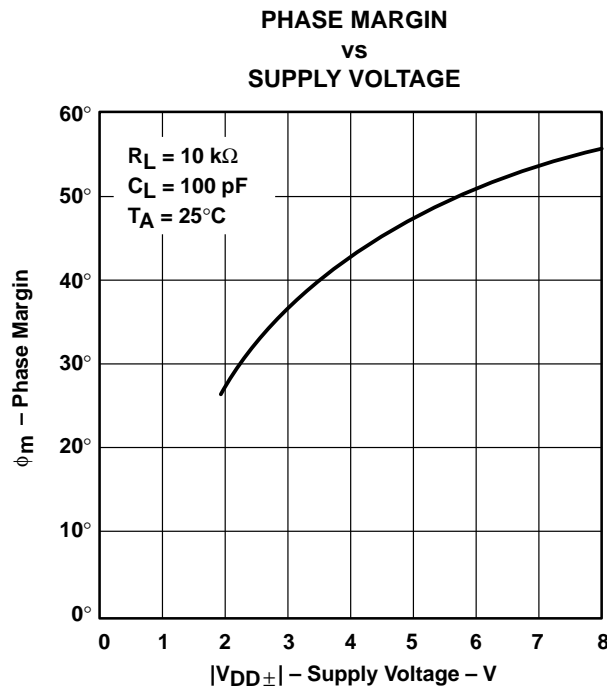


Figure 32

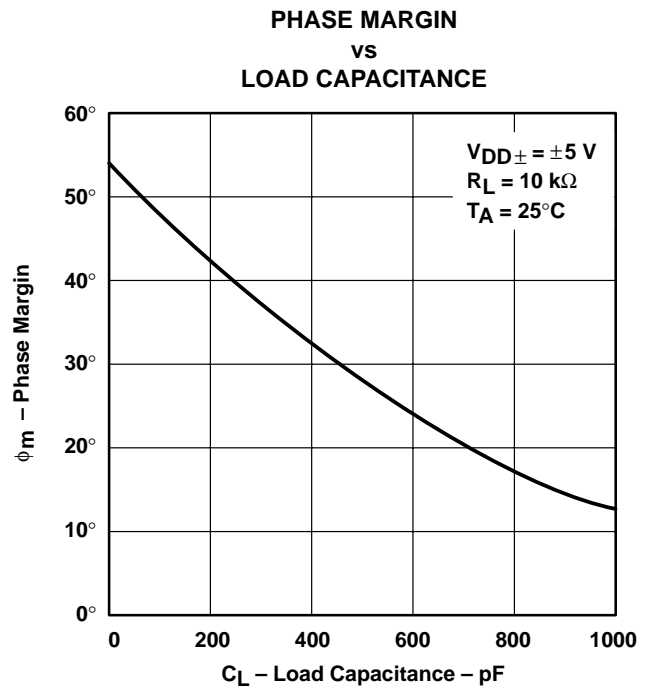


Figure 33

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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APPLICATION INFORMATION

capacitor selection and placement

Leakage and dielectric absorption are the two important factors to consider when selecting external capacitors C_{XA} and C_{XB} . Both factors can cause system degradation, negating the performance advantages realized by using the TLC2654.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at $T_A = 125^\circ\text{C}$. In addition, guard bands are recommended around the capacitor connections on both sides of the printed-circuit board to alleviate problems caused by surface leakage on circuit boards.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications needing fast settling of input voltage, high-quality film capacitors such as mylar, polystyrene, or polypropylene should be used. In other applications, a ceramic or other low-grade capacitor can suffice.

Unlike many choppers available today, the TLC2654 is designed to function with values of C_{XA} and C_{XB} in the range of $0.1\ \mu\text{F}$ to $1\ \mu\text{F}$ without degradation to input offset voltage or input noise voltage. These capacitors should be located as close as possible to C_{XA} and C_{XB} and return to either V_{DD-} or C RETURN. On many choppers, connecting these capacitors to V_{DD-} causes degradation in noise performance; this problem is eliminated on the TLC2654.

internal/external clock

The TLC2654 has an internal clock that sets the chopping frequency to a nominal value of 10 kHz. On 8-pin packages, the chopping frequency can only be controlled by the internal clock; however, on all 14-pin packages and the 20-pin FK package the device chopping frequency can be set by the internal clock or controlled externally by use of the $\text{INT}/\overline{\text{EXT}}$ and CLK IN. To use the internal 10-kHz clock, no connection is necessary. If external clocking is desired, connect $\text{INT}/\overline{\text{EXT}}$ to V_{DD-} and the external clock to CLK IN. The external clock trip point is 2.5 V above the negative rail; however, CLK IN can be driven from the negative rail to 5 V above the negative rail. This allows the TLC2654 to be driven directly by 5-V TTL and CMOS logic when operating in the single-supply configuration. If this 5-V level is exceeded, damage could occur to the device unless the current into CLK IN is limited to $\pm 5\ \text{mA}$. A divide-by-two frequency divider interfaces with CLK IN and sets the chopping frequency. The chopping frequency appears on CLK OUT.

overload recovery/output clamp

When large differential-input-voltage conditions are applied to the TLC2654, the nulling loop attempts to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time (see Figure 34). Typical overload recovery time for the TLC2654 is significantly faster than competitive products; however, this time can be reduced further by use of internal clamp circuitry accessible through CLAMP if required.

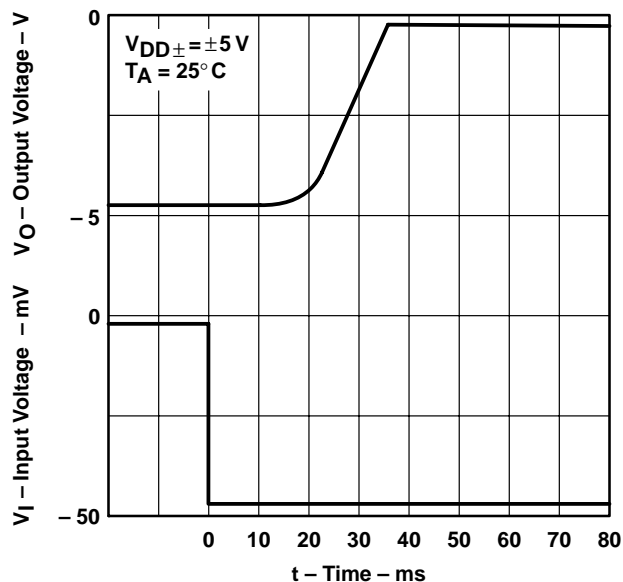


Figure 34. Overload Recovery

APPLICATION INFORMATION

overload recovery/output clamp (continued)

The clamp is a switch that is automatically activated when the output is approximately 1 V from either supply rail. When connected to the inverting input (in parallel with the closed-loop feedback resistor), the closed-loop gain is reduced and the TLC2654 output is prevented from going into saturation. Since the output must source or sink current through the switch (see Figure 9), the maximum output voltage swing is slightly reduced.

thermoelectric effects

To take advantage of the extremely low offset voltage temperature coefficient of the TLC2654, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed-circuit board). It is not uncommon for dissimilar metal junctions to produce thermoelectric voltages in the range of several microvolts per degree Celsius (orders of magnitude greater than the 0.01 $\mu\text{V}/^\circ\text{C}$ typical of the TLC2654).

To help minimize thermoelectric effects, pay careful attention to component selection and circuit-board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches, etc.) in the input signal path. Cancel thermoelectric effects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire-wound resistors, is also beneficial.

latch-up avoidance

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2654 inputs and outputs are designed to withstand -100-mA surge currents without sustaining latch-up; however, techniques to reduce the chance of latch-up should be used whenever possible. Internal protection diodes should not, by design, be forward biased. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be stunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the supply rails and is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor. The chance of latch-up occurring increases with increasing temperature and supply voltage.

electrostatic-discharge protection

The TLC2654 incorporates internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices, as exposure to ESD may result in degradation of the device parametric performance.

theory of operation

Chopper-stabilized operational amplifiers offer the best dc performance of any monolithic operational amplifier. This superior performance is the result of using two operational amplifiers — a main amplifier and a nulling amplifier — plus oscillator-controlled logic and two external capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2654 achieves submicrovolt input offset voltage, submicrovolt noise voltage, and offset voltage variations with temperature in the $\text{nV}/^\circ\text{C}$ range.

The TLC2654 on-chip control logic produces two dominant clock phases: a nulling phase and an amplifying phase. The term chopper-stabilized derives from the process of switching between these two clock phases. Figure 35 shows a simplified block diagram of the TLC2654. Switches A and B are make-before-break types.

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APPLICATION INFORMATION

theory of operation (continued)

The TLC2654 removes this restriction on ac performance by using a 10-kHz internal clock frequency. This high chopping frequency allows amplification of input signals up to 5 kHz without errors due to intermodulation and greatly reduces low-frequency noise.

THERMAL INFORMATION

temperature coefficient of input offset voltage

Figure 36 shows the effects of package-included thermal EMF. The TLC2654 can null only the offset voltage within its nulling loop. There are metal-to-metal junctions outside the nulling loop (bonding wires, solder joints, etc.) that produce EMF. In Figure 36, a TLC2654 packaged in a 14-pin plastic package (N package) was placed in an oven at 25°C at $t = 0$, biased up, and allowed to stabilize. At $t = 3$ min, the oven was turned on and allowed to rise in temperature to 125°C. As evidenced by the curve, the overall change in input offset voltage with temperature is less than the specified maximum limit of 0.05 $\mu\text{V}/^\circ\text{C}$.

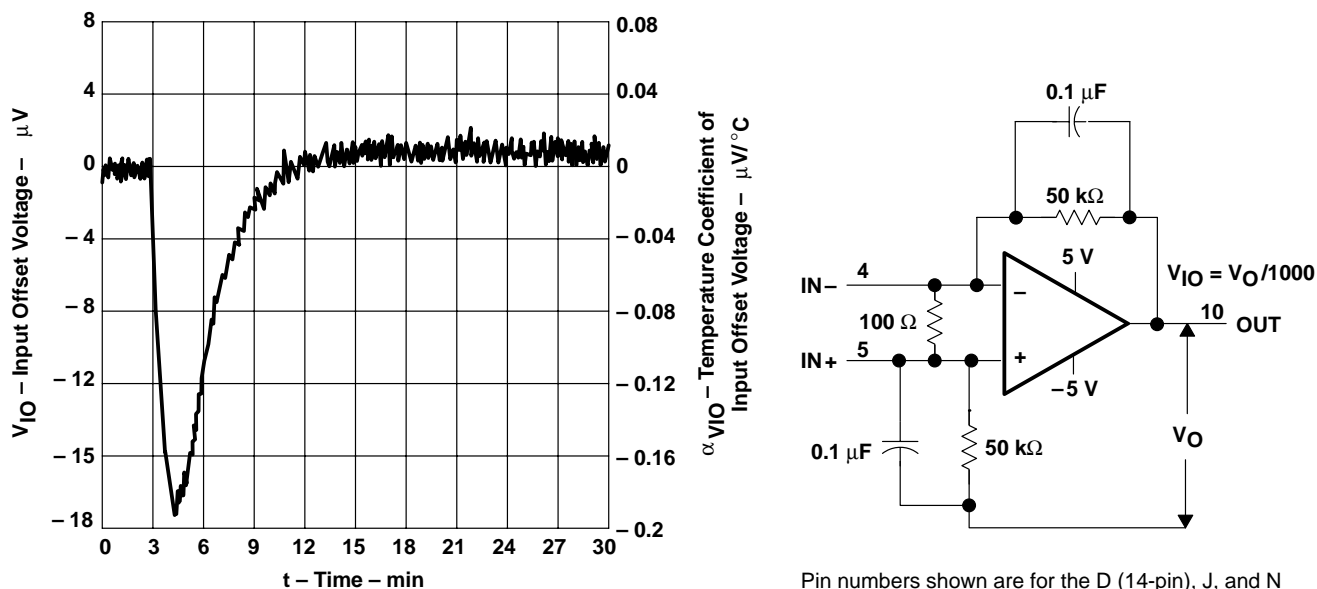


Figure 36. Effects of Package-Induced Thermal EMF

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9089504QPA	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089504QPA TLC2654AM
TLC2654AC-8D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2654AC
TLC2654AC-8D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2654AC
TLC2654ACP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2654AC
TLC2654ACP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2654AC
TLC2654AI-8D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2654AI
TLC2654AI-8D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2654AI
TLC2654AIP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2654AI
TLC2654AIP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2654AI
TLC2654AMJGB	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089504QPA TLC2654AM
TLC2654AMJGB.A	Active	Production	CDIP (JG) 8	50 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9089504QPA TLC2654AM
TLC2654C-14DR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2654C
TLC2654C-14DR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC2654C
TLC2654C-8D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2654C
TLC2654C-8D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2654C
TLC2654C-8DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	2654C
TLC2654C-8DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2654C
TLC2654CN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2654CN
TLC2654CN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC2654CN
TLC2654CP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2654CP
TLC2654CP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC2654CP
TLC2654I-8D	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	2654I
TLC2654I-8D.A	Active	Production	SOIC (D) 8	75 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2654I
TLC2654I-8DR	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2654I
TLC2654I-8DR.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2654I
TLC2654IP	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC2654IP
TLC2654IP.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC2654IP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLC2654A, TLC2654AM :

- Catalog : [TLC2654A](#)
- Military : [TLC2654AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

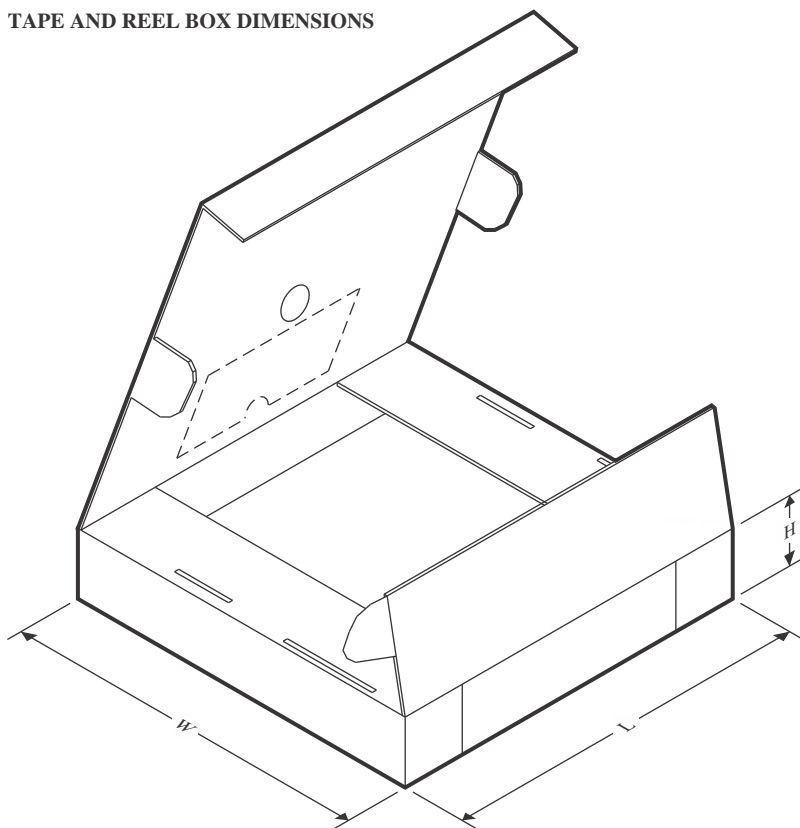
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2654C-14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2654C-8DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2654I-8DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

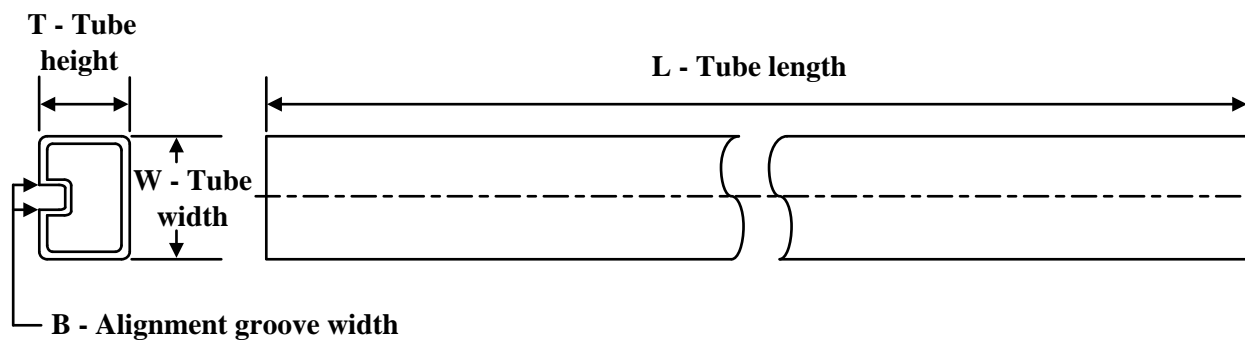
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

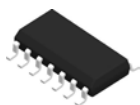
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2654C-14DR	SOIC	D	14	2500	350.0	350.0	43.0
TLC2654C-8DR	SOIC	D	8	2500	353.0	353.0	32.0
TLC2654I-8DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE

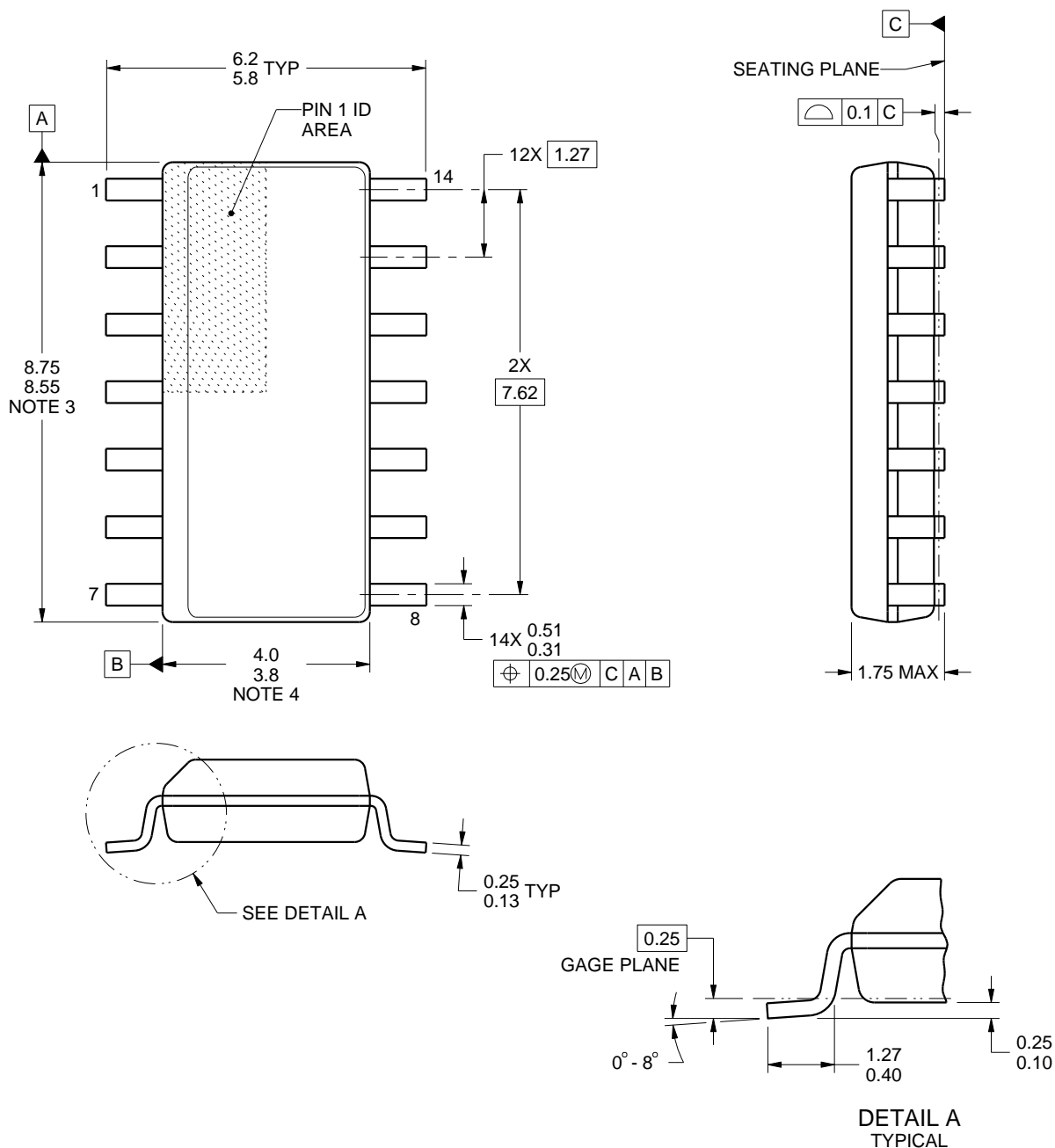


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC2654AC-8D	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654AC-8D	D	SOIC	8	75	507	8	3940	4.32
TLC2654AC-8D.A	D	SOIC	8	75	507	8	3940	4.32
TLC2654AC-8D.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2654ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2654AI-8D	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654AI-8D	D	SOIC	8	75	507	8	3940	4.32
TLC2654AI-8D.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654AI-8D.A	D	SOIC	8	75	507	8	3940	4.32
TLC2654AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2654AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2654C-8D	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654C-8D	D	SOIC	8	75	507	8	3940	4.32
TLC2654C-8D.A	D	SOIC	8	75	507	8	3940	4.32
TLC2654C-8D.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC2654CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC2654CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2654CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC2654I-8D	D	SOIC	8	75	507	8	3940	4.32
TLC2654I-8D	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654I-8D.A	D	SOIC	8	75	507	8	3940	4.32
TLC2654I-8D.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC2654IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC2654IP.A	P	PDIP	8	50	506	13.97	11230	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

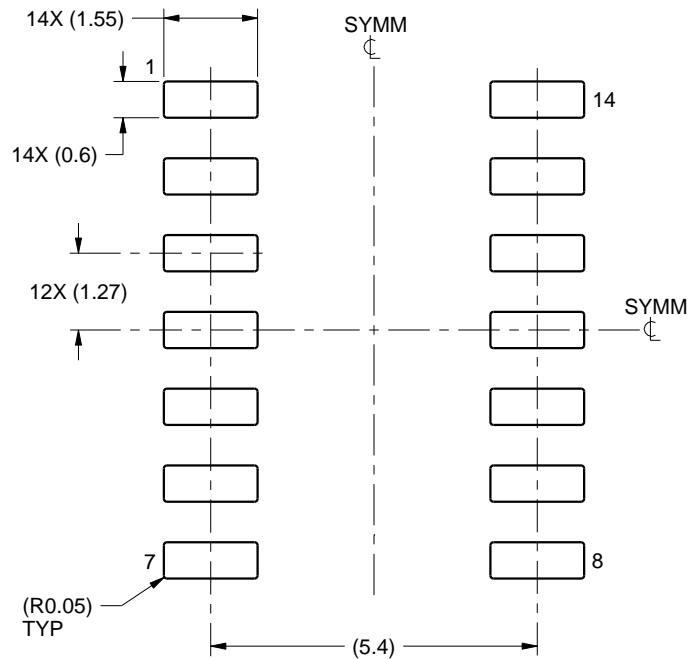
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

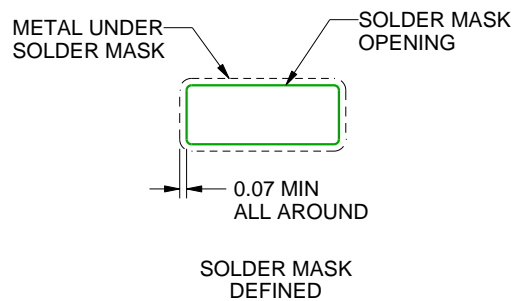
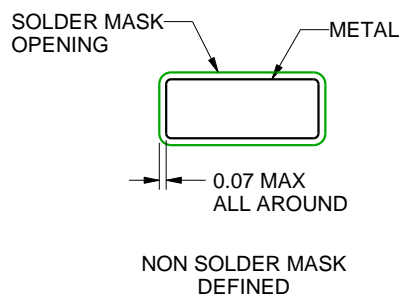
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

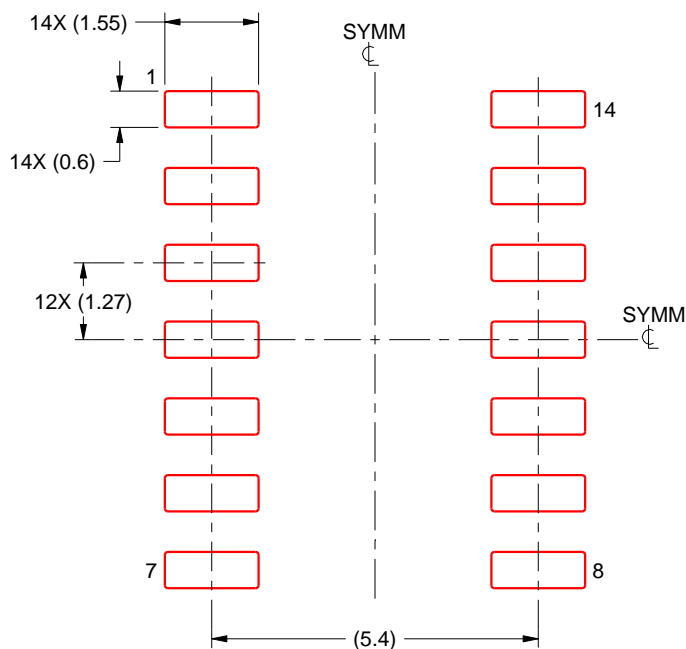
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

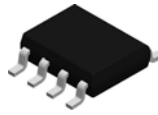


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

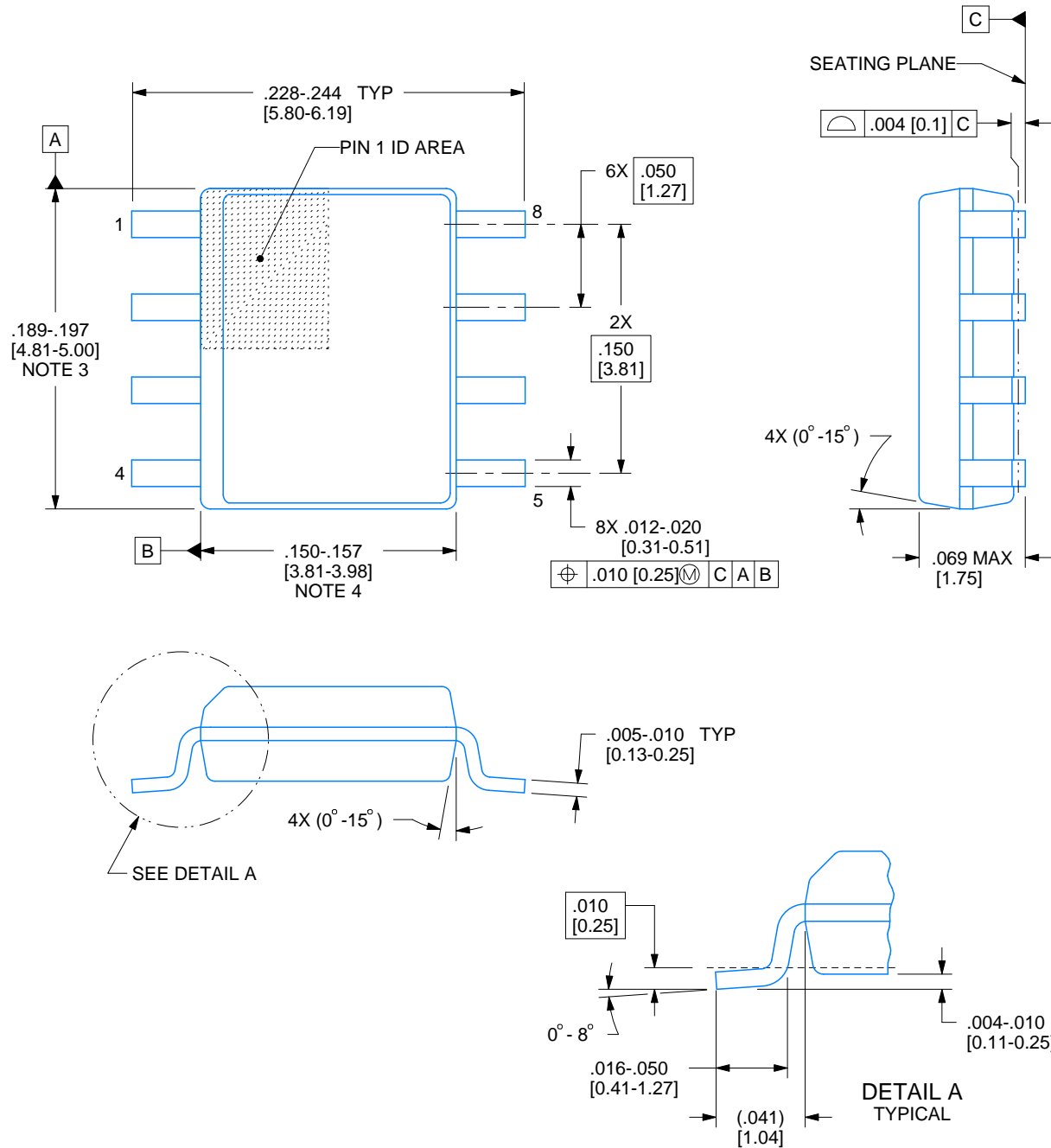
4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

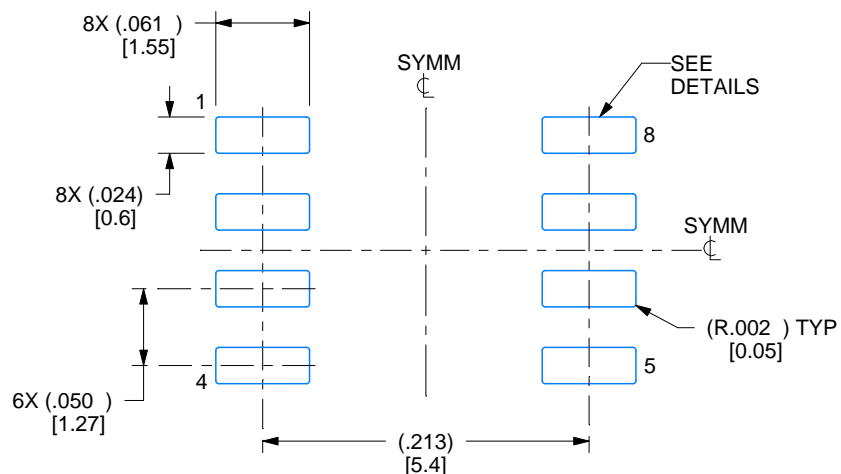
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

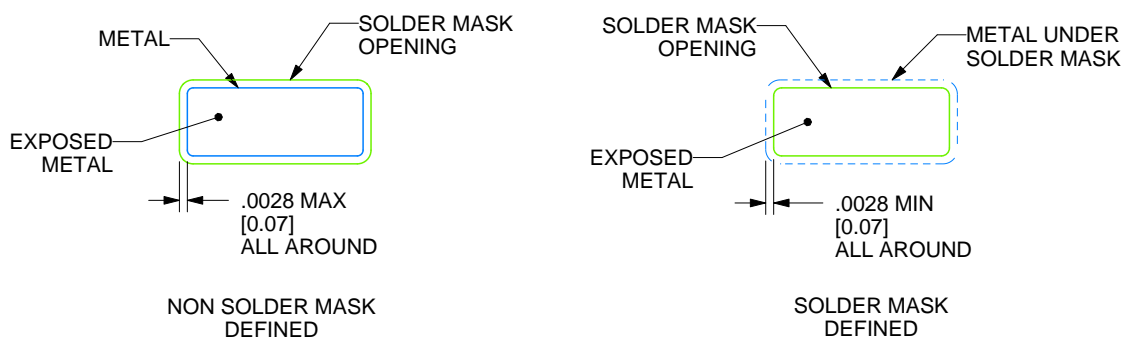
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

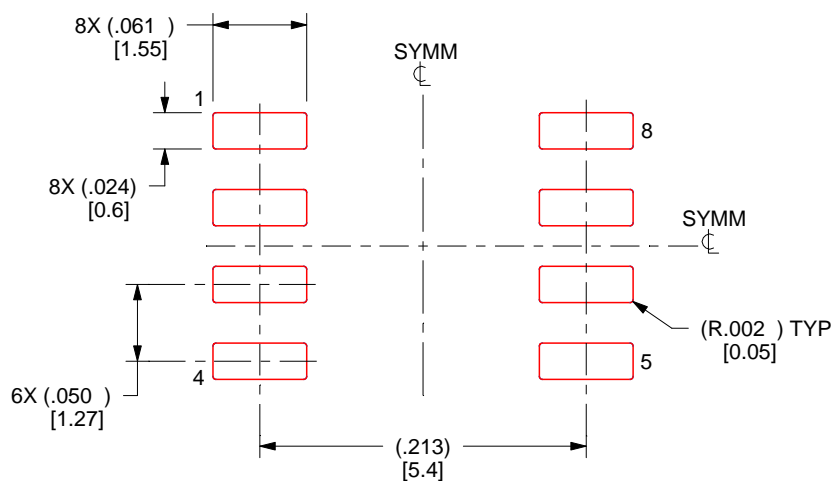
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

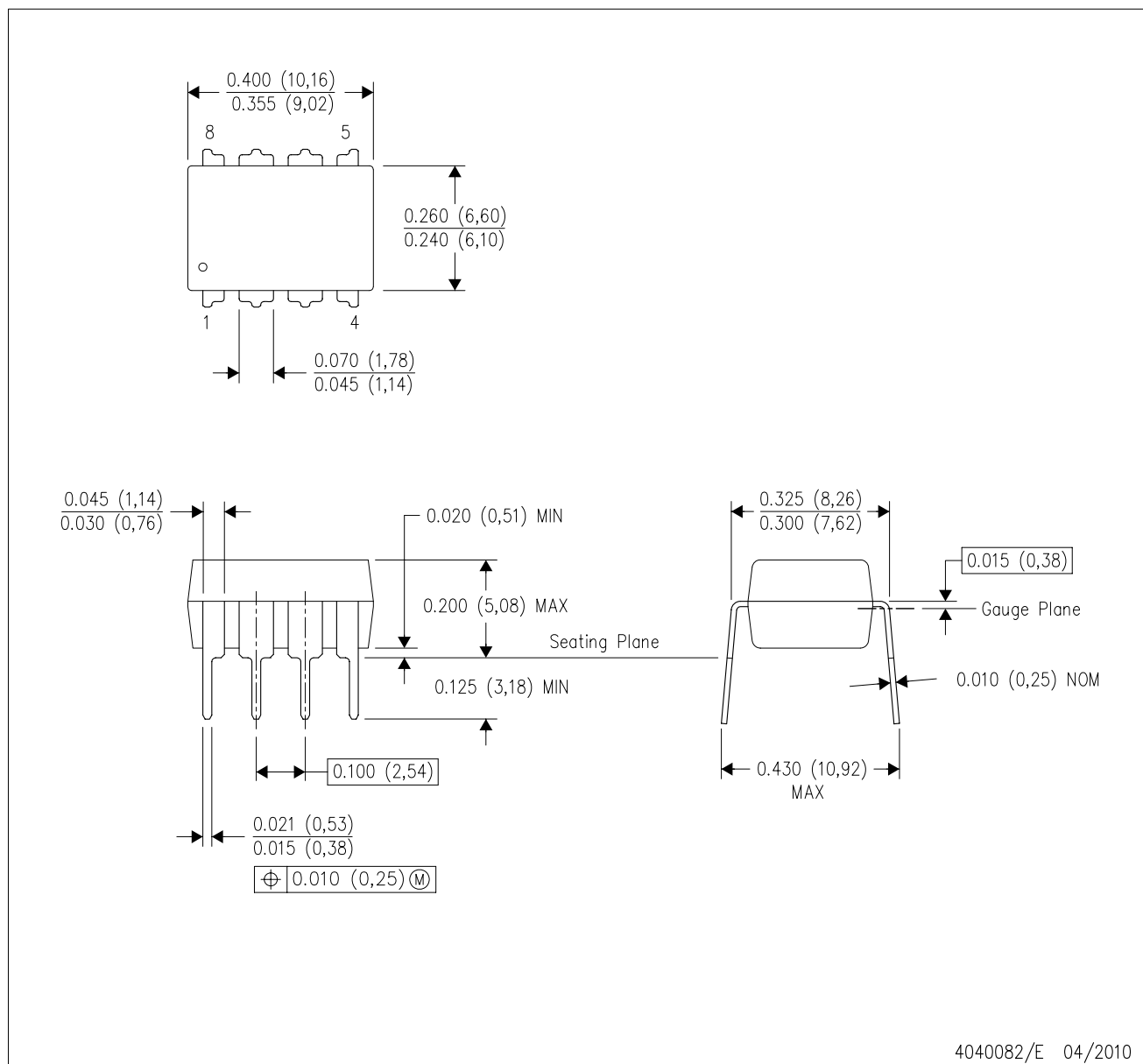
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

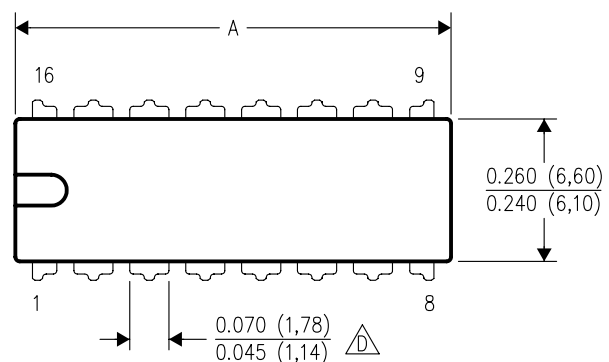


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

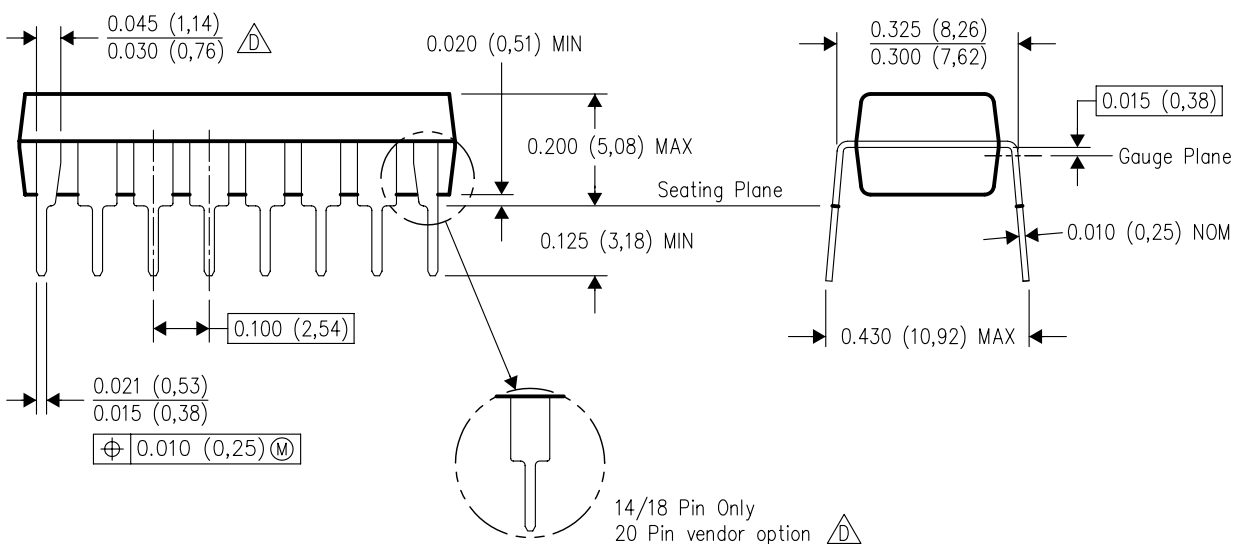
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



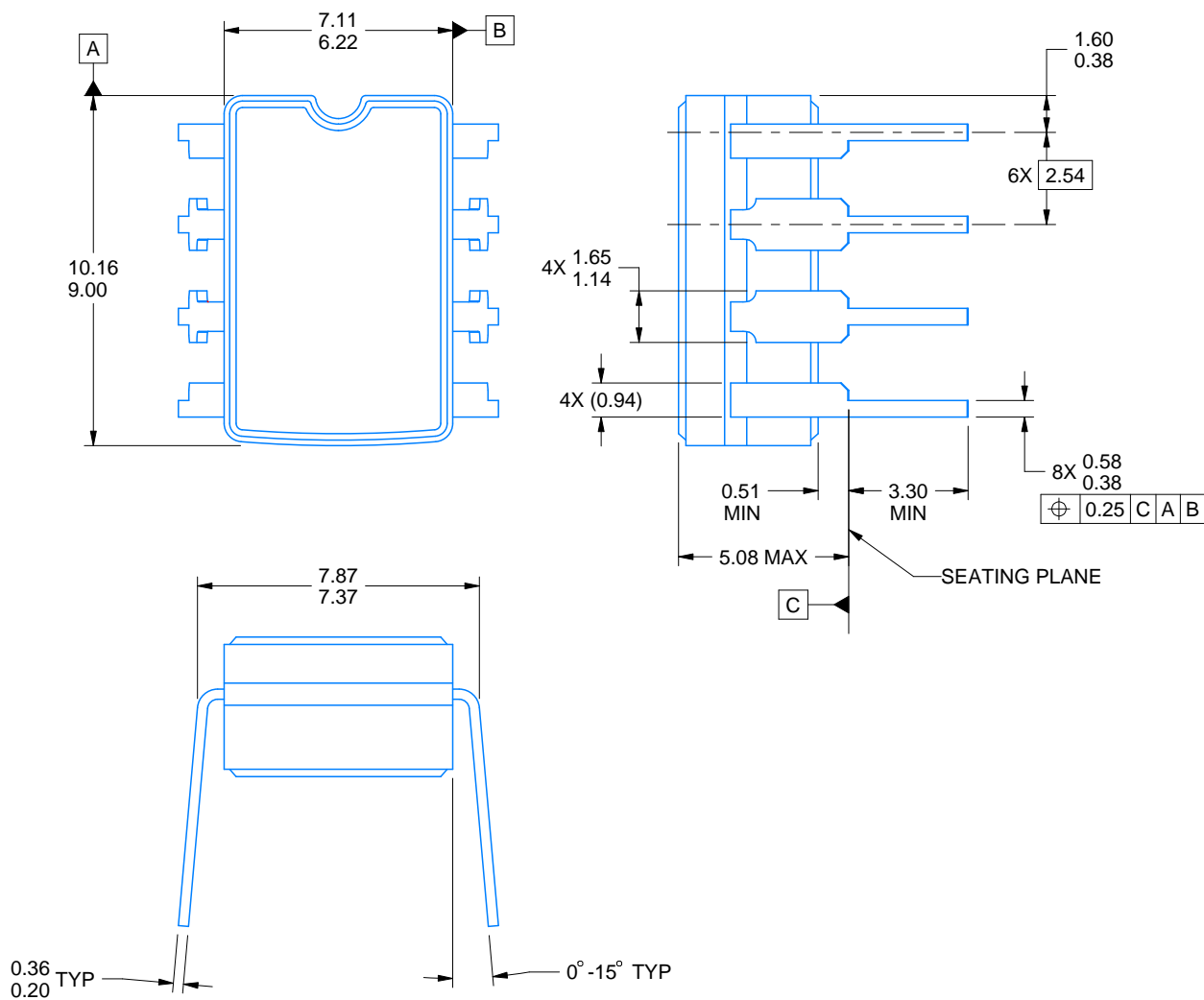
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

JG0008A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

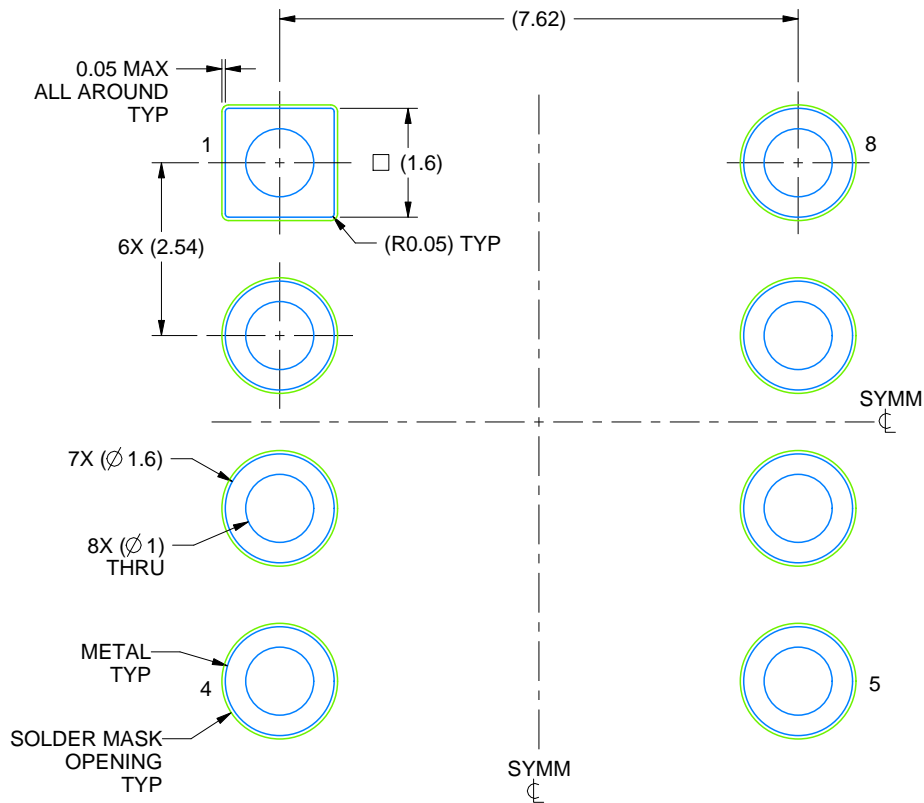
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

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