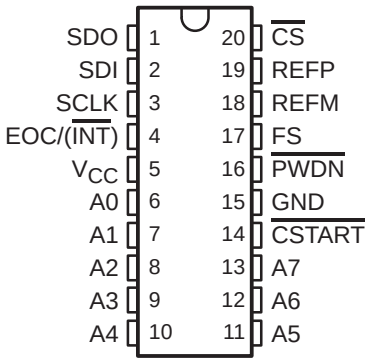
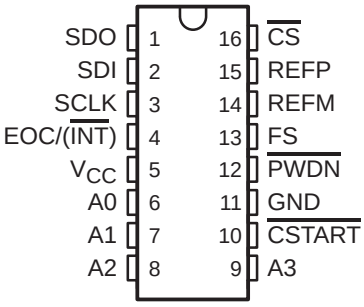
- **Maximum Throughput 400 KSPS**
- **Built-In Reference and 8× FIFO**
- **Differential/Integral Nonlinearity Error: ±1 LSB**
- **Signal-to-Noise and Distortion Ratio: 69 dB, f_i = 12 kHz**
- **Spurious Free Dynamic Range: 75 dB, f_i = 12 kHz**
- **SPI/DSP-Compatible Serial Interfaces With SCLK up to 20 MHz**
- **Single Supply 5 Vdc**
- **Analog Input Range 0 V to Supply Voltage With 500 kHz BW**
- **Hardware Controlled and Programmable Sampling Period**
- **Low Operating Current (4 mA at 5.5 V External Ref, 6 mA at 5.5 V, Internal Ref)**
- **Power Down: Software/Hardware Power-Down Mode (1 μA Max, Ext Ref), Auto Power-Down Mode (1 μA, Ext Ref)**
- **Programmable Auto-Channel Sweep**

DW OR PW PACKAGE
(TOP VIEW)



D OR PW PACKAGE
(TOP VIEW)

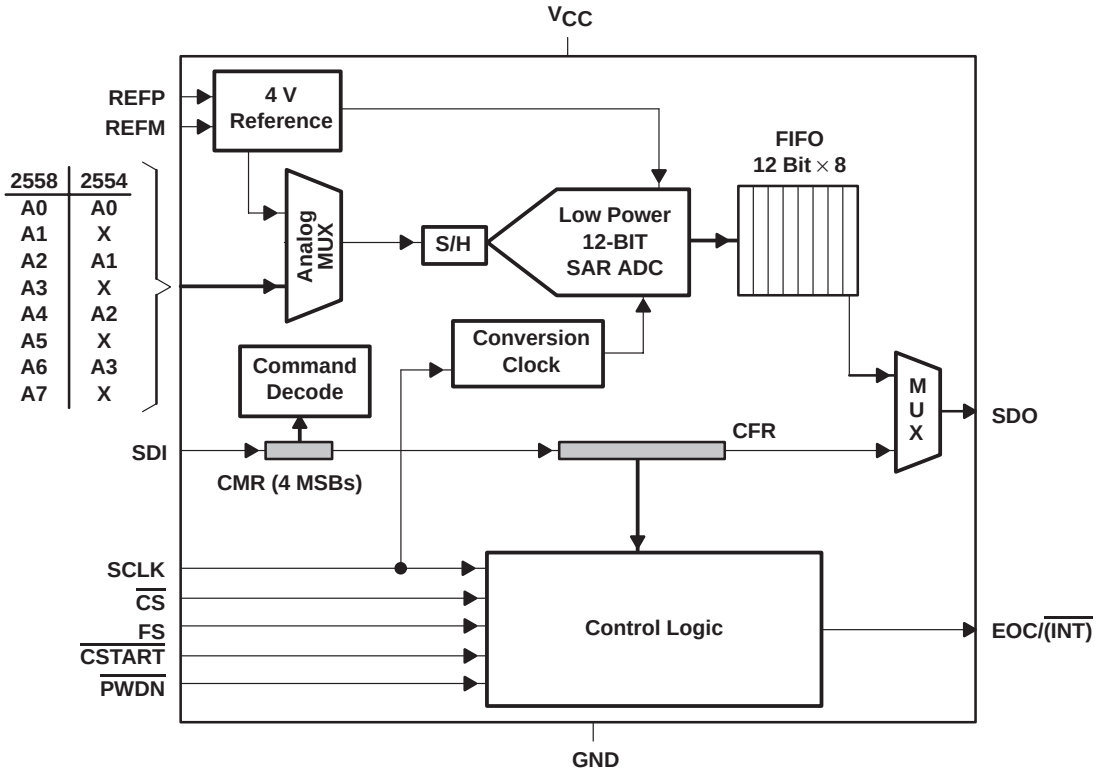


description

The TLC2558 and TLC2554 are a family of high-performance, 12-bit low power, 1.6 μs, CMOS analog-to-digital converters (ADC) which operate from a single 5 V power supply. These devices have three digital inputs and a 3-state output [chip select ($\overline{CS}$), serial input-output clock (SCLK), serial data input (SDI), and serial data output (SDO)] that provide a direct 4-wire interface to the serial port of most popular host microprocessors (SPI interface). When interfaced with a DSP, a frame sync (FS) signal is used to indicate the start of a serial data frame.

In addition to a high-speed A/D converter and versatile control capability, these devices have an on-chip analog multiplexer that can select any analog inputs or one of three internal self-test voltages. The sample-and-hold function is automatically started after the fourth SCLK edge (normal sampling) or can be controlled by a special pin, $\overline{CSTART}$, to extend the sampling period (extended sampling). The normal sampling period can also be programmed as short (12 SCLKs) or as long (24 SCLKs) to accommodate faster SCLK operation popular among high-performance signal processors. The TLC2558 and TLC2554 are designed to operate with very low power consumption. The power-saving feature is further enhanced with software/hardware/auto power down modes and programmable conversion speeds. The converter uses the external SCLK as the source of the conversion clock to achieve higher (up to 1.6 μs when a 20 MHz SCLK is used) conversion speed. There is a 4-V internal reference available. An optional external reference can also be used to achieve maximum flexibility.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	20-TSSOP (PW)	20-SOIC (DW)	16-SOIC (D)	16-TSSOP (PW)
0°C to 70°C	TLC2558CPW	TLC2558CDW	TLC2554CD	TLC2554CPW
–40°C to 85°C	TLC2558IPW	TLC2558IDW	TLC2554ID	TLC2554IPW

Terminal Functions

TERMINAL NAME	TERMINAL NO. TLC2554	TERMINAL NO. TLC2558	I/O	DESCRIPTION
A0 A0 A1 A1 A2 A2 A3 A3 A4 A5 A6 A7	6 7 8 9	6 7 8 9 10 11 12 13	I	Analog signal inputs. The analog inputs are applied to these terminals and are internally multiplexed. The driving source impedance should be less than or equal to 1 kΩ. For a source impedance greater than 1 kΩ, use the asynchronous conversion start signal $\overline{\text{CSTART}}$ ($\overline{\text{CSTART}}$ low time controls the sampling period) or program long sampling period to increase the sampling time.
$\overline{\text{CS}}$	16	20	I	Chip select. A high-to-low transition on the $\overline{\text{CS}}$ input resets the internal 4-bit counter, enables SDI, and removes SDO from 3-state within a maximum setup time. SDI is disabled within a setup time after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{\text{CS}}$ whichever happens first. SDO is 3-stated after the rising edge of $\overline{\text{CS}}$. $\overline{\text{CS}}$ can be used as the FS pin when a dedicated serial port is used.
$\overline{\text{CSTART}}$	10	14	I	This terminal controls the start of sampling of the analog input from a selected multiplex channel. A high-to-low transition starts sampling of the analog input signal. A low-to-high transition puts the S/H in hold mode and starts the conversion. This input is independent from SCLK and works when $\overline{\text{CS}}$ is high (inactive). The low time of $\overline{\text{CSTART}}$ controls the duration of the sampling period of the converter (extended sampling). Tie this terminal to V_{CC} if not used.
EOC/($\overline{\text{INT}}$)	4	4	O	End of conversion or interrupt to host processor. **[PROGRAMMED AS EOC]**: This output goes from a high-to-low logic level at the end of the sampling period and remains low until the conversion is complete and data are ready for transfer. EOC is used in conversion mode 00 only. **[PROGRAMMED AS $\overline{\text{INT}}$]**: This pin can also be programmed as an interrupt output signal to the host processor. The falling edge of $\overline{\text{INT}}$ indicates data are ready for output. The following $\overline{\text{CS}}\downarrow$ or $\overline{\text{FS}}\uparrow$ clears $\overline{\text{INT}}$. The falling edge of $\overline{\text{INT}}$ puts SDO back to 3-state even if $\overline{\text{CS}}$ is still active.
FS	13	17	I	DSP frame sync input. Indication of the start of a serial data frame in or out of the device. If FS remains low at the falling edge of $\overline{\text{CS}}$, SDI is not enabled. A high-to-low transition on the FS input resets the internal 4-bit counter and enables SDI within a maximum setup time. SDI is disabled within a setup time after the 4-bit counter counts to 16 (clock edges) or a low-to-high transition of $\overline{\text{CS}}$ whichever happens first. SDO is 3-stated after the 16th bit is presented. Tie this terminal to V_{CC} if not used.
GND	11	15	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
$\overline{\text{PWDN}}$	12	16	I	Both analog and reference circuits are powered down when this pin is at logic zero. The device can be restarted by active $\overline{\text{CS}}$ or $\overline{\text{CSTART}}$ after this pin is pulled back to logic one.
SCLK	3	3	I	Input serial clock. This terminal receives the serial SCLK from the host processor. SCLK is used to clock the input SDI to the input register. It is also used as the source of the conversion clock.
SDI	2	2	I	Serial data input. The input data is presented with the MSB (D15) first. The first 4-bit MSBs, D(15–12) are decoded as one of the 16 commands (12 only for the TLC2554). All trailing blanks are filled with zeros. The configure write commands require an additional 12 bits of data. When FS is not used (FS =1), the first MSB (D15) is expected after the falling edge of CS and is shifted in on the rising edges of SCLK (after $\overline{\text{CS}}\downarrow$). When FS is used (typical with an active FS from a DSP) the first MSB (D15) is expected after the falling edge of FS and is shifted in on the falling edges of SCLK.

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TLC2554	TLC2558		
SDO	1	1	O	The 3-state serial output for the A/D conversion result. SDO is kept in the high-impedance state when $\overline{CS}$ is high and after the $\overline{CS}$ falling edge and until the MSB (D15) is presented. The output format is MSB (D15) first. When FS is not used (FS = 1 at the falling edge of $\overline{CS}$), the MSB (D15) is presented to the SDO pin after the $\overline{CS}$ falling edge, and successive data are available at the rising edge of SCLK. When FS is used (FS = 0 at the falling edge of $\overline{CS}$), the MSB (D15) is presented to SDO after the falling edge of $\overline{CS}$ and FS = 0 is detected. Successive data are available at the falling edge of SCLK. (This is typically used with an active FS from a DSP.) For conversion and FIFO read cycles, the first 12 bits are the result from the previous conversion (data) followed by 4 trailing zeros. The first four bits from SDO for CFR read cycles should be ignored. The register content is in the last 12 bits. SDO is 3 stated after the 16th bit.
REFM	14	18	I	External reference input or internal reference decoupling.
REFP	15	19	I	External reference input or internal reference decoupling. (Shunt capacitors of 10 μF and 0.1 μF between REFP and REFM.) The maximum input voltage range is determined by the difference between the voltage applied to this terminal and the REFM terminal when an external reference is used.
V_{CC}	5	5	I	Positive supply voltage

detailed description

analog inputs and internal test voltages

The 4/8 analog inputs and three internal test inputs are selected by the analog multiplexer depending on the command entered. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching.

pseudo-differential/single-ended input

All analog inputs can be programmed as single-ended or pseudo-differential mode. Pseudo-differential mode is enabled by setting CFR.D7 – 1. Only three analog input channels (or seven channels for TLC2558) are available for TLV2554 since one input (A1 for TLC2554 or A2 for TLC2558) is used as the MINUS input when pseudo-differential mode is used. The minus input pin can have a maximum ±0.2 V ripple. This is normally used for ground noise rejection.

converter

The TLC2554/58 uses a 12-bit successive approximation ADC and 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion system determines each bit by examining the charge on a series of binary-weighted capacitors (see Figure 1). In the first phase of the conversion process, the analog input is sampled by closing the SC switch and all ST switches simultaneously. This action charges all the capacitors to the input voltage.

converter (continued)

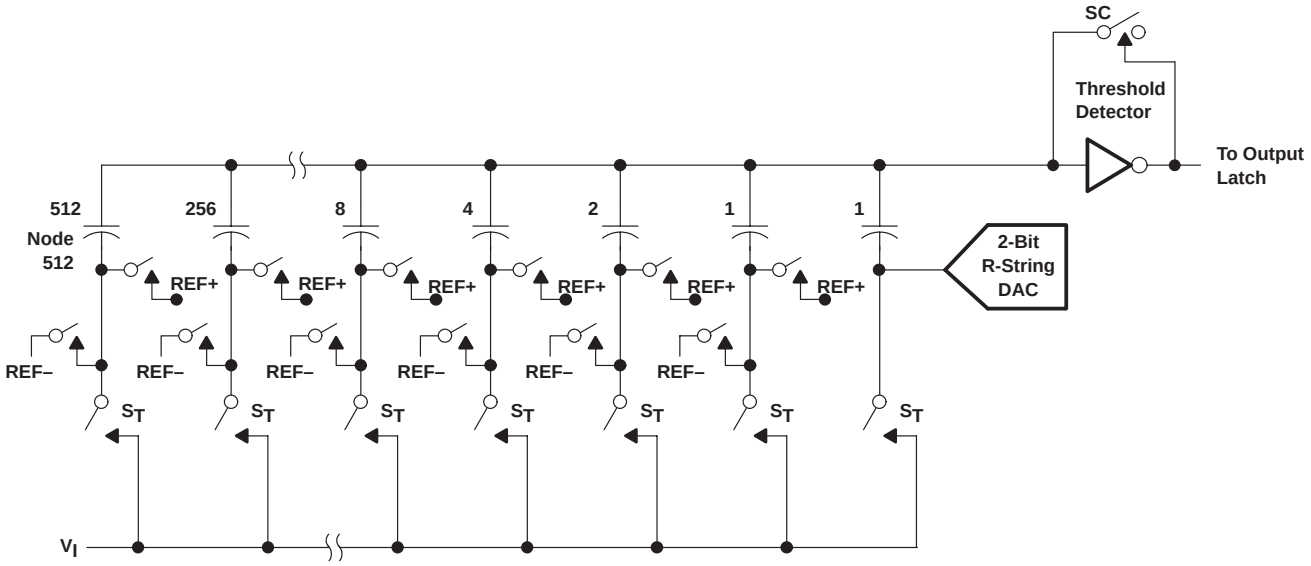


Figure 1. Simplified Model of the Successive-Approximation System

In the next phase of the conversion process the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference (REFM) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the REFP voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to REFM. If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half the V_{CC} voltage), a bit 0 is placed in the output register and the 512-weight capacitor is switched to REFM. If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register. The 512-weight capacitor remains connected to REFP through the remainder of the successive-approximation process. The process is repeated for the 1024-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted.

With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

serial interface

INPUT DATA FORMAT	
MSB	**LSB**
D15–D12	D11–D0
Command	Configuration data field

Input data is binary. All trailing blanks can be filled with zeros.

OUTPUT DATA FORMAT READ CFR	
MSB	**LSB**
D15–D12	D11–D0
Don't care	Register content

OUTPUT DATA FORMAT CONVERSION/READ FIFO	
MSB	**LSB**
D15–D4	D3–D0
Conversion result	All zeros

serial interface (continued)

The output data format is either binary (unipolar straight binary) or 2s complement.

binary

Zero scale code = 000h, Vcode = VREFM
Full scale code = FFFh, Vcode = VREFP – 1 LSB

2's complement

Minus full scale code = 800h, Vcode = VREFM
Full scale code = 7FFh, Vcode = VREFP – 1 LSB

control and timing

start of the cycle:

- When FS is not used (FS = 1 at the falling edge of $\overline{CS}$), the falling edge of $\overline{CS}$ is the start of the cycle. Input data is shifted in on the rising edge, and output data changes on the falling edge of SCLK. This is typically used for a SPI microcontroller, although it can also be used for a DSP.
- When FS is used (FS is an active signal from a DSP), the falling edge of FS is the start of the cycle. Input data is shifted in on the falling edge, and output data changes on the rising edge of SCLK. This is typically used for a TMS320 DSP.

first 4-MSBs: the command register (CMR)

The TLC2554/TLC2558 have a 4-bit command set (see Table 1) plus a 12-bit configuration data field. Most of the commands require only the first 4 MSBs, i.e. without the 12-bit data field.

NOTE:
The device requires a write CFR (configuration register) with 000h data (write A000h to the serial input) at power up to initialize host select mode.

The valid commands are listed in Table 1.

Table 1. TLC2554/TLC2558 Command Set

SDI D(15–12) BINARY, HEX		TLC2558 COMMAND	TLC2554 COMMAND
0000b	0000h	Select analog input channel 0	Select analog input channel 0
0001b	1000h	Select analog input channel 1	N/A
0010b	2000h	Select analog input channel 2	Select analog input channel 1
0011b	3000h	Select analog input channel 3	N/A
0100b	4000h	Select analog input channel 4	Select analog input channel 2
0101b	5000h	Select analog input channel 5	N/A
0110b	6000h	Select analog input channel 6	Select analog input channel 3
0111b	7000h	Select analog input channel 7	N/A
1000b	8000h	SW power down (analog + reference)	
1001b	9000h	Read CFR register data shown as SDO D(11–0)	
1010b	A000h plus data	Write CFR followed by 12-bit data	
1011b	B000h	Select test, voltage = (REFP+REFM)/2	
1100b	C000h	Select test, voltage = REFM	
1101b	D000h	Select test, voltage = REFP	
1110b	E000h	FIFO read, FIFO contents shown as SDO D(15–4), D(3–0) = 0000	
1111b	F000h plus data	Reserved	

control and timing (continued)

configuration

Configuration data is stored in one 12-bit configuration register (CFR) (see Table 2 for CFR bit definitions). Once configured after first power up, the information is retained in the H/W or S/W power-down state. When the device is being configured, a write CFR cycle is issued by the host processor. This is a 16-bit write. If the SCLK stops after the first 8 bits are entered, then the next eight bits can be taken after the SCLK is resumed. The status of the CFR can be read with a read CFR command.

Table 2. TLC2554/TLC2558 Configuration Register (CFR) Bit Definitions

BIT	DEFINITION	
D(15–12)	All zeros, nonprogrammable	
D11	Reference select 0: External 1: Internal	
D10	Output select 0: Unipolar straight binary 1: 2's complement	
D9	Sample period select 0: Short sampling 12 SCLKs (1x sampling time) 1: Long sampling 24 SCLKs (2x sampling time)	
D8	Conversion clock source select 0: Conversion clock = SCLK 1: Conversion clock = SCLK/2	
D7	Input select 0: Normal 1: Pseudo differential CH A2(2558) or CH A1 (2554) is the differential input	
D(6,5)	Conversion mode select 00: Single shot mode 01: Repeat mode 10: Sweep mode 11: Repeat sweep mode	
D(4,3)†	**TLC2558**	**TLC2554**
	Sweep auto sequence select 00: 0–1–2–3–4–5–6–7 01: 0–2–4–6–0–2–4–6 10: 0–0–2–2–4–4–6–6 11: 0–2–0–2–0–2–0–2	Sweep auto sequence select 00: N/A 01: 0–1–2–3–0–1–2–3 10: 0–0–1–1–2–2–3–3 11: 0–1–0–1–0–1–0–1
D2	EOC/$\overline{\text{INT}}$ – pin function select 0: Pin used as $\overline{\text{INT}}$ 1: Pin used as EOC	
D(1,0)	FIFO trigger level (sweep sequence length) 00: Full ($\overline{\text{INT}}$ generated after FIFO level 7 filled) 01: 3/4 ($\overline{\text{INT}}$ generated after FIFO level 5 filled) 10: 1/2 ($\overline{\text{INT}}$ generated after FIFO level 3 filled) 11: 1/4 ($\overline{\text{INT}}$ generated after FIFO level 1 filled)	

† These bits only take effect in conversion modes 10 and 11.

sampling

The sampling period starts after the first 4 input data are shifted in if they are decoded as one of the conversion commands. These are select analog input (channel 0 through 7) and select test (channel 1 through 3).

normal sampling

When the converter is using normal sampling, the sampling period is programmable. It can be 12 SCLKs (short sampling) or 24 SCLKs (long sampling). Long sampling helps the input analog signal sampled to settle to 0.5 LSB accuracy when input source resistance is high.

extended sampling

An asynchronous (to the SCLK) signal, via dedicated hardware pin $\overline{\text{CSTART}}$, can be used in order to have total control of the sampling period and the start of a conversion. This is extended sampling. The falling edge of $\overline{\text{CSTART}}$ is the start of the sampling period. The rising edge of $\overline{\text{CSTART}}$ is the end of the sampling period and the start of the conversion. This function is useful for an application that requires:

- The use of an extended sampling period to accommodate different input source impedance.
- The use of a faster I/O clock on the serial port but not enough sampling time is available due to the fixed number of SCLKs. This could be due to a high input source impedance or due to higher MUX ON resistance at lower supply voltage (refer to application information).

Once the conversion is complete, the processor can initiate a read cycle using either the read FIFO command to read the conversion result or simply select the next channel number for conversion. Since the device has a valid conversion result in the output buffer, the conversion result is simply presented at the serial data output.

TLC2554/TLC2558 conversion modes

The TLC2554 and TLC2558 have four different conversion modes (mode 00, 01, 10, 11). The operation of each mode is slightly different, depending on how the converter performs the sampling and which host interface is used. The trigger for a conversion can be an active $\overline{\text{CSTART}}$ (extended sampling), $\overline{\text{CS}}$ (normal sampling, SPI interface), or FS (normal sampling, TMS320 DSP interface). When FS is used as the trigger, $\overline{\text{CS}}$ can be held active, i.e. $\overline{\text{CS}}$ does not need to be toggled through the trigger sequence. Different types of triggers should not be mixed throughout the repeat and sweep operations. When $\overline{\text{CSTART}}$ is used as the trigger, the conversion starts on the rising edge of $\overline{\text{CSTART}}$. The minimum low time for $\overline{\text{CSTART}}$ is 800 ns. If an active $\overline{\text{CS}}$ or FS is used as the trigger, the conversion is started after the 16th or 28th SCLK edge. Enough time (for conversion) should be allowed between consecutive triggers so that no conversion is terminated prematurely.

one shot mode (mode 00)

One shot mode (mode 00) does not use the FIFO, and the EOC is generated as the conversion is in progress (or $\overline{\text{INT}}$ is generated after the conversion is done).

repeat mode (mode 01)

Repeat mode (mode 01) uses the FIFO. Once the programmed FIFO threshold is reached, the FIFO must be read, or the data is lost and the sequence starts over again. This allows the host to set up the converter and continue monitoring a fixed input and come back to get a set of samples when preferred. The first conversion must start with a select command so an analog input channel can be selected.

sweep mode (mode 10)

Sweep mode (mode 10) also uses the FIFO. Once it is programmed in this mode, all of the channels listed in the selected sweep sequence are visited in sequence. The results are converted and stored in the FIFO. This sweep sequence may not be completed if the FIFO threshold is reached before the list is completed. This allows the system designer to change the sweep sequence length. Once the FIFO has reached its programmed threshold, an interrupt ($\overline{\text{INT}}$) is generated. The host must issue a read FIFO command to read and clear the FIFO before the next sweep can start.

TLC2554/TLC2558 conversion modes (continued)

repeat sweep mode (mode 11)

Repeat sweep mode (mode 11) works the same way as mode 10 except the operation has an option to continue even if the FIFO threshold is reached. Once the FIFO has reached its programmed threshold, an interrupt ($\overline{INT}$) is generated. Then two things may happen:

1. The host may choose to act on it (read the FIFO) or ignore it. If the next cycle is a read FIFO cycle, all of the data stored in the FIFO is retained until it has been read in order.
2. If the next cycle is not a read FIFO cycle, or another $\overline{CSTART}$ is generated, all of the content stored in the FIFO is cleared before the next conversion result is stored in the FIFO, and the sweep is continued.

Table 3. TLC2554/TLC2558 Conversion Mode

CONVERSION MODE	CFR D(6,5)	SAMPLING TYPE	OPERATION
One shot	00	Normal	• Single conversion from a selected channel • $\overline{CS}$ or $\overline{FS}$ to start select/sampling/conversion/read • One $\overline{INT}$ or EOC generated after each conversion • Host must serve $\overline{INT}$ by selecting channel, and converting and reading the previous output.
		Extended	• Single conversion from a selected channel • $\overline{CS}$ to select/read • $\overline{CSTART}$ to start sampling and conversion • One $\overline{INT}$ or EOC generated after each conversion • Host must serve $\overline{INT}$ by selecting next channel and reading the previous output.
Repeat	01	Normal	• Repeated conversions from a selected channel • $\overline{CS}$ or $\overline{FS}$ to start sampling/conversion • One $\overline{INT}$ generated after FIFO is filled up to the threshold • Host must serve $\overline{INT}$ by either 1) (FIFO read) reading out all of the FIFO contents up to the threshold, then repeat conversions from the same selected channel or 2) writing another command(s) to change the conversion mode. If the FIFO is not read when $\overline{INT}$ is served, it is cleared.
		Extended	• Same as normal sampling except $\overline{CSTART}$ starts each sampling and conversion when $\overline{CS}$ is high.
Sweep	10	Normal	• One conversion per channel from a sequence of channels • $\overline{CS}$ or $\overline{FS}$ to start sampling/conversion • One $\overline{INT}$ generated after FIFO is filled up to the threshold • Host must serve $\overline{INT}$ by (FIFO read) reading out all of the FIFO contents up to the threshold, then write another command(s) to change the conversion mode.
		Extended	• Same as normal sampling except $\overline{CSTART}$ starts each sampling and conversion when $\overline{CS}$ is high.
Repeat sweep	11	Normal	• Repeated conversions from a sequence of channels • $\overline{CS}$ or $\overline{FS}$ to start sampling/conversion • One $\overline{INT}$ generated after FIFO is filled up to the threshold • Host must serve $\overline{INT}$ by either 1) (FIFO read) reading out all of the FIFO contents up to the threshold, then repeat conversions from the same selected channel or 2) writing another command(s) to change the conversion mode. If the FIFO is not read when $\overline{INT}$ is served it is cleared.
		Extended	• Same as normal sampling except $\overline{CSTART}$ starts each sampling and conversion when $\overline{CS}$ is high.

NOTE: Programming the EOC/$\overline{INT}$ pin as the EOC signal works for mode 00 only. The other three modes automatically generate an $\overline{INT}$ signal irrespective of whether EOC/INT is programmed.

timing diagrams

The timing diagrams can be categorized into two major groups: nonconversion and conversion. The nonconversion cycles are read and write (configuration). None of these cycles carry a conversion. Conversion cycles are those four modes of conversion.

read cycle (read FIFO or read CFR)

read CFR cycle:

The read command is decoded in the first 4 clocks. SDO outputs the contents of the CFR after the 4th SCLK.

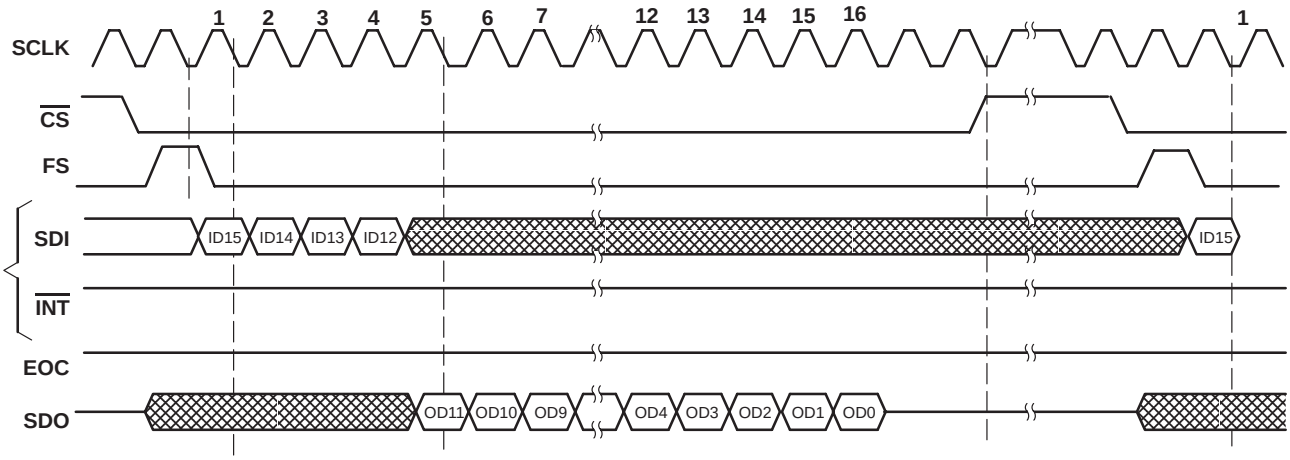


Figure 2. TLC2554/TLC2558 Read CFR Cycle (FS active)

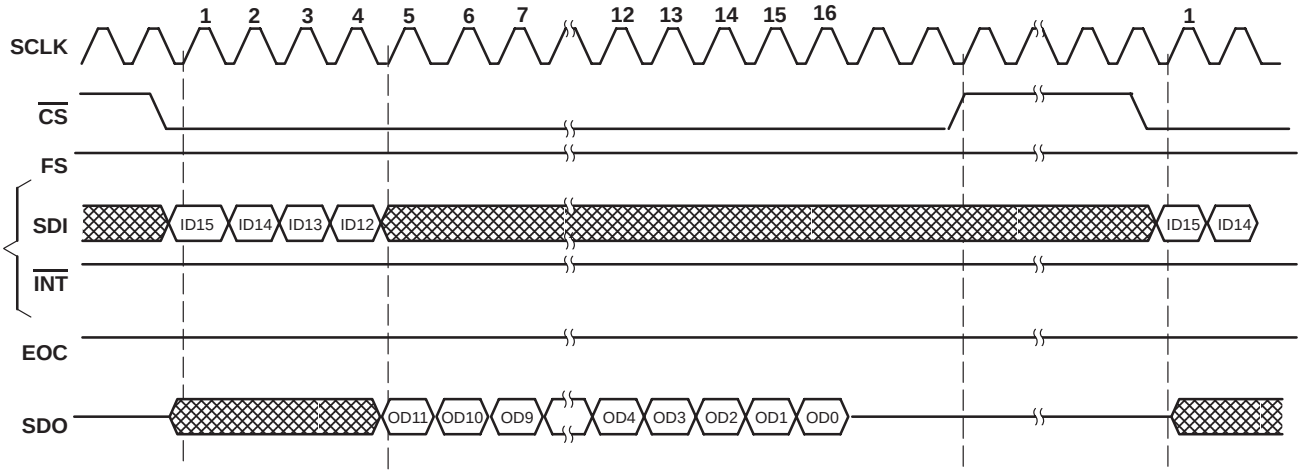


Figure 3. TLC2554/TLC2558 Read CFR Cycle (FS = 1)

read cycle (read FIFO or read CFR) (continued)

FIFO read cycle

The first command in the active cycle after INT is generated, if the FIFO is used, is assumed as the FIFO read command. The first FIFO content is output immediately before the command is decoded. If this command is not a FIFO read, then the output is terminated but the first data in the FIFO is retained until a valid FIFO read command is decoded. Use of more layers of the FIFO reduces the time taken to read multiple data. This is because the read cycle does not generate EOC or INT nor does it carry out any conversion.

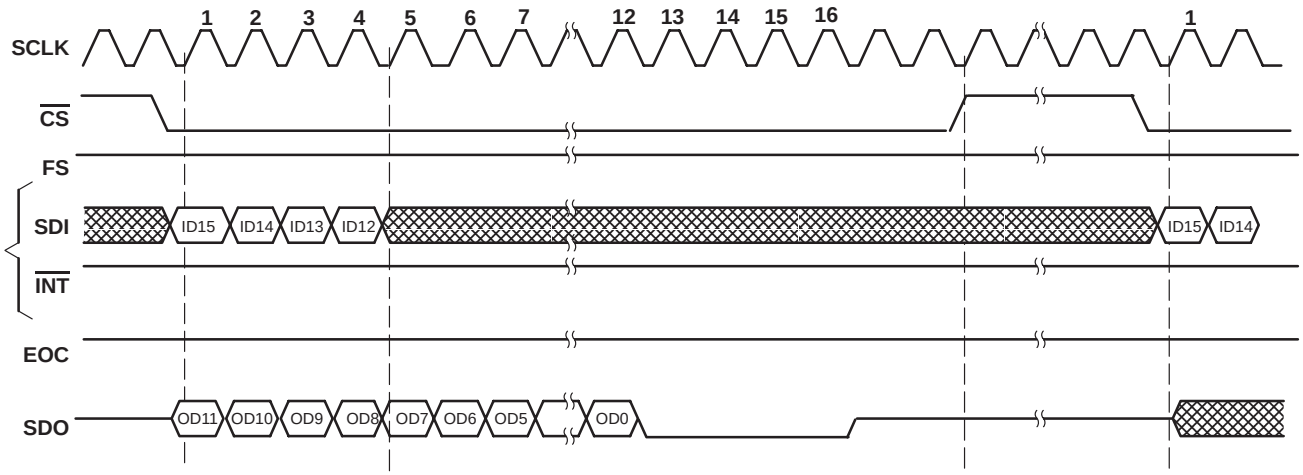


**Figure 4. TLC2554/TLC2558 Continuous FIFO Read Cycle (FS = 1)
(controlled by SCLK, SCLK can stop between each 16 SCLKs)**

write cycle (write CFR)

The write cycle is used to write to the configuration register CFR (with 12-bit register content). The write cycle does not generate an EOC or $\overline{\text{INT}}$ nor does it carry out any conversion.

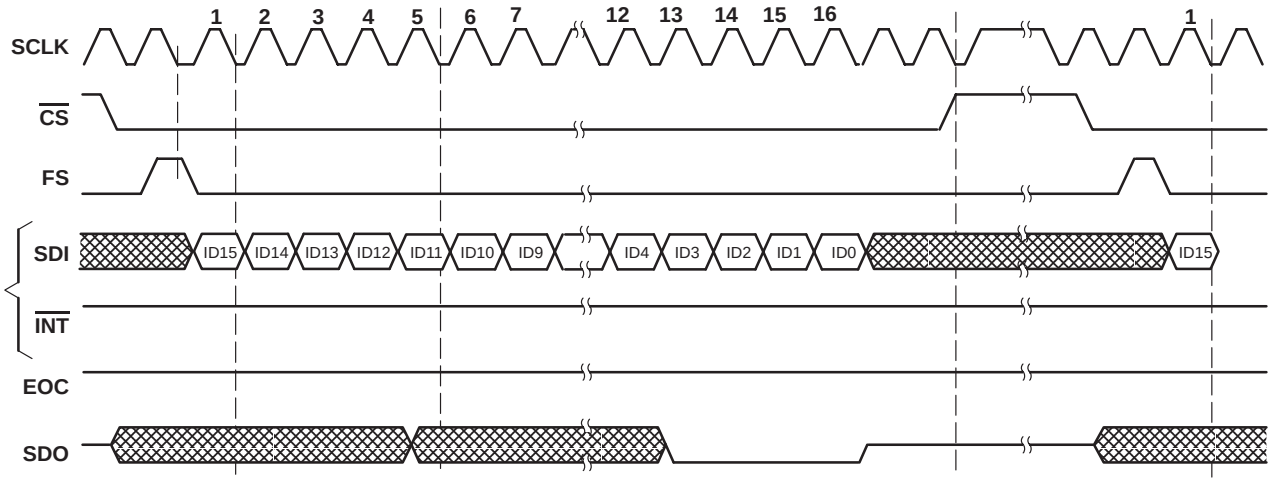


Figure 5. TLC2554/TLC2558 Write Cycle (FS active)

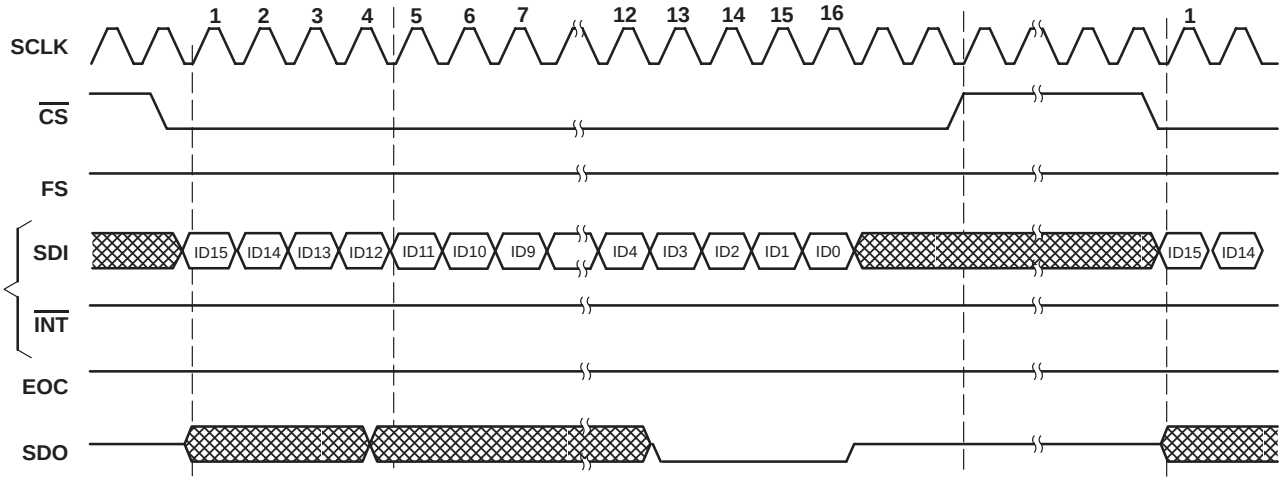


Figure 6. TLC2554/TLC2558 Write Cycle (FS = 1)

conversion cycles

DSP/normal sampling

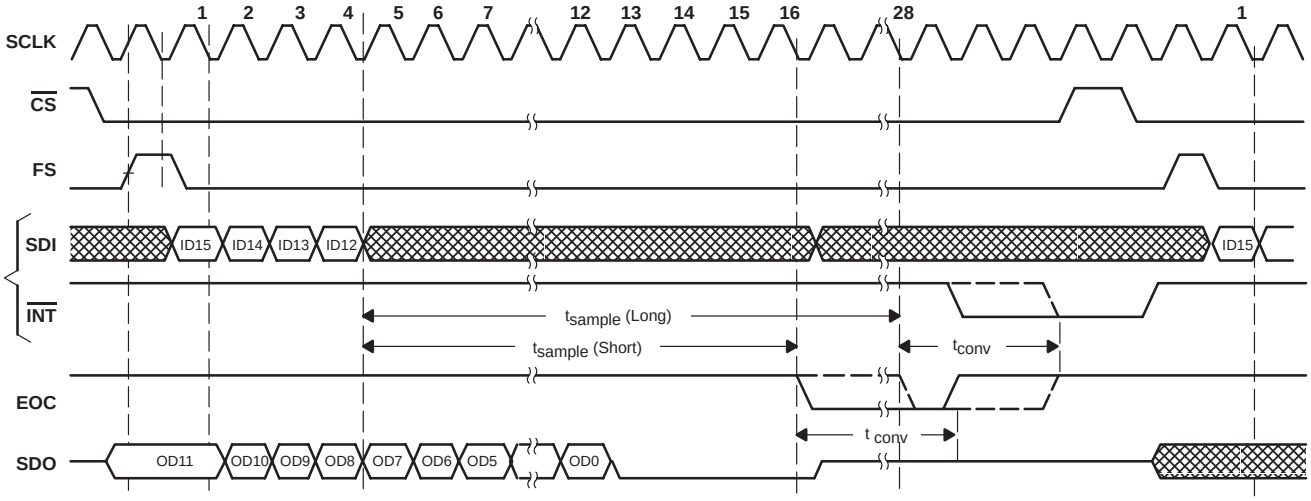


Figure 7. Mode 00 Single Shot/Normal Sampling (FS signal used)

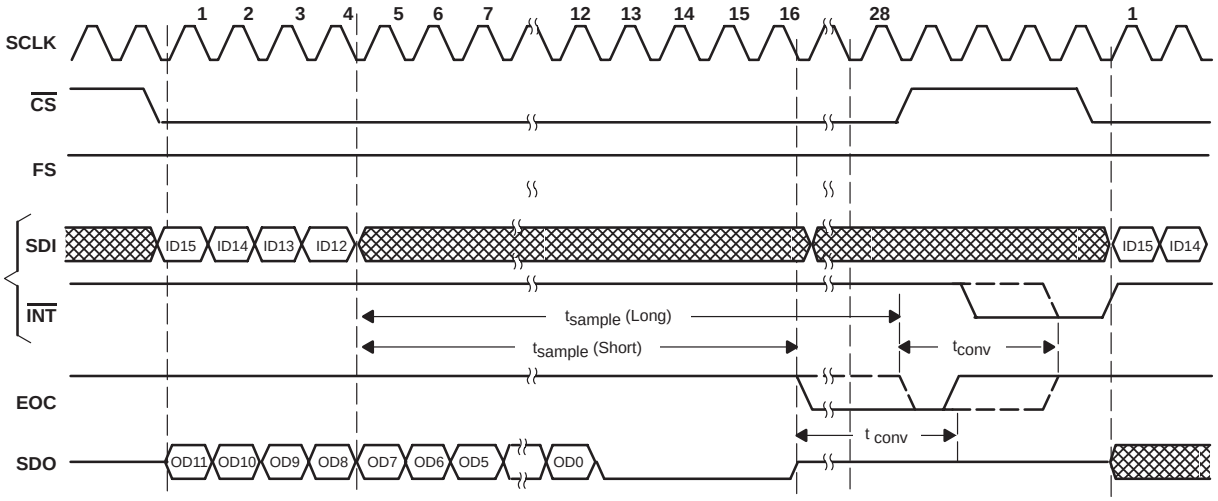
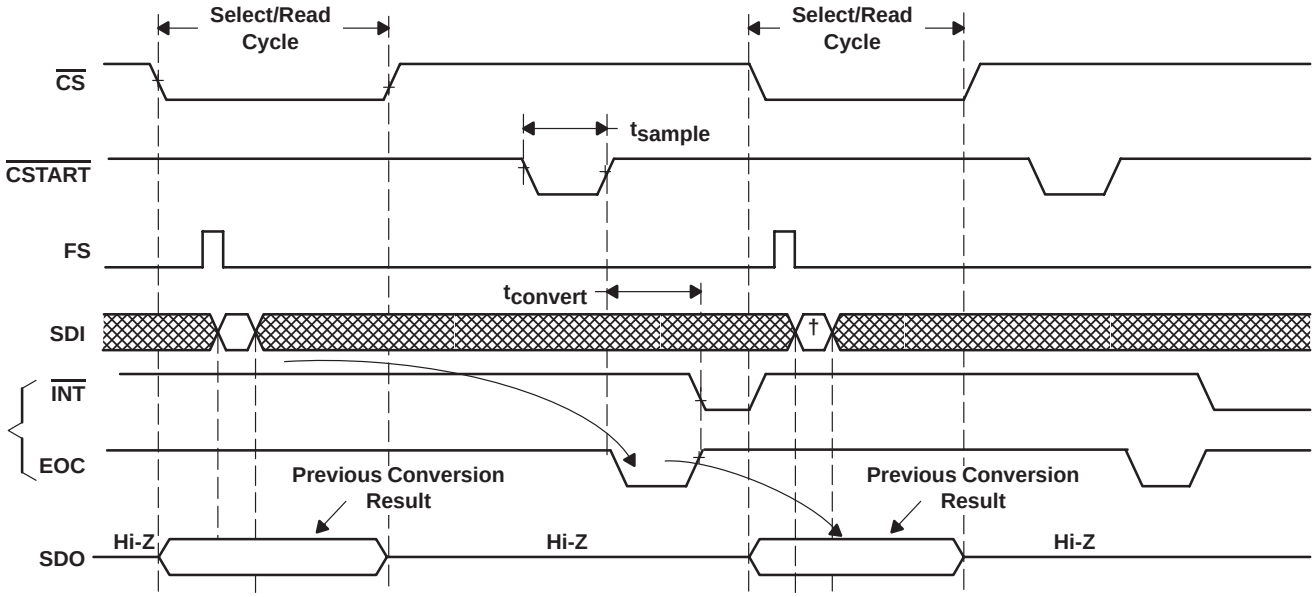


Figure 8. Mode 00 Single Shot/Normal Sampling (FS = 1, FS signal not used)

conversion cycles (continued)



† This is one of the single shot commands. Conversion starts on next rising edge of CSTART.

Figure 9. Mode 00 Single Shot/Extended Sampling (FS signal used, FS pin connected to TMS320 DSP)

CS used as FS input

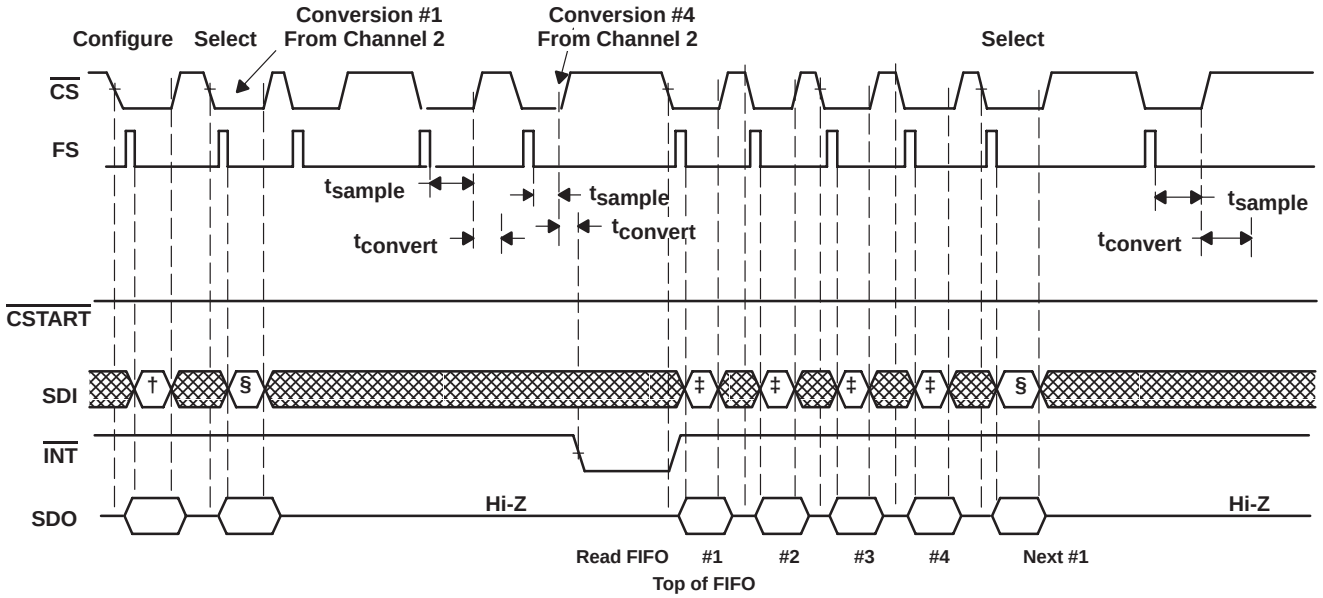
When interfacing with the TMS320 DSP using conversion mode 00, the FSR signal from the DSP may be connected to the CS input if this is the only device on the serial port. This will save one output pin from the DSP. Output data is made available on the rising edge of SCLK and input data is latched on the rising edge of SCLK in this case.

modes using the FIFO: modes 01, 10, 11 timing

Modes 01, 10, and 11 timing are very similar except for how and when the FIFO is read, how the device is configured, and how channel(s) are selected.

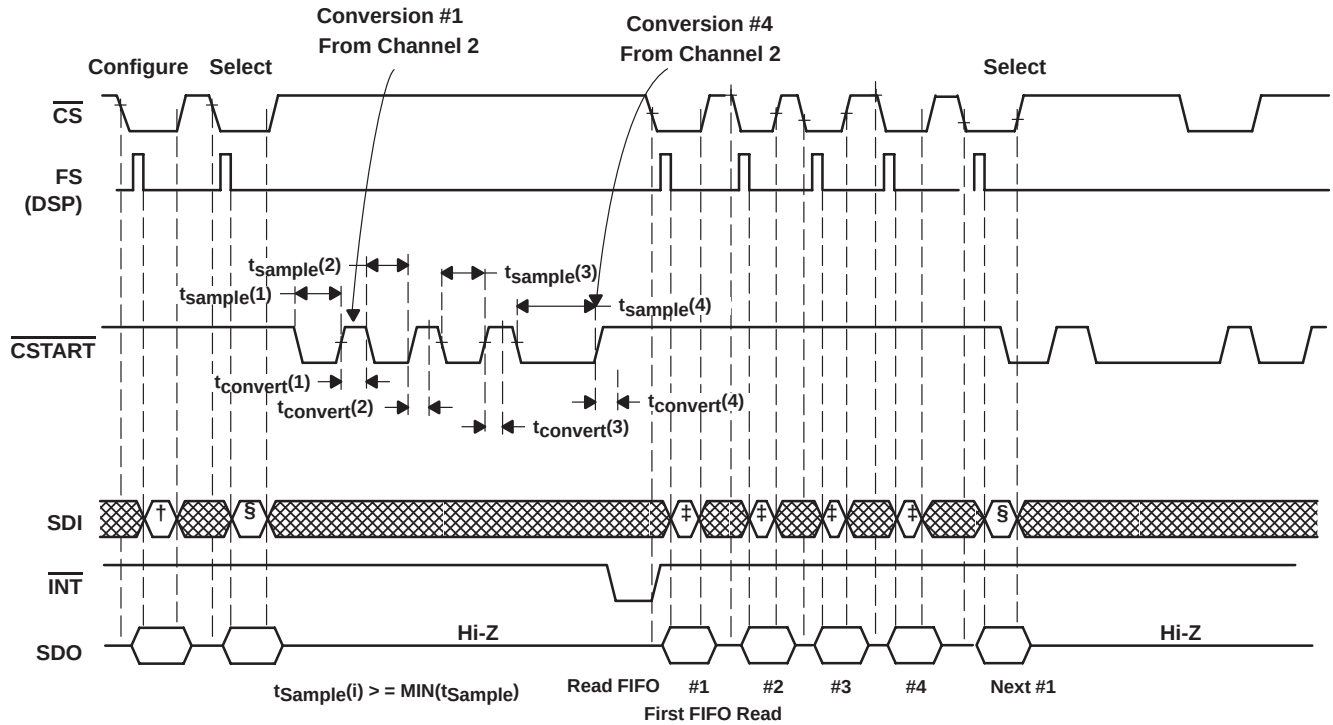
Mode 01 (repeat mode) requires a two-cycle configuration where the first one sets the mode and the second one selects the channel. Once the FIFO is filled up to the threshold programmed, it has the option to either read the FIFO or configure for other modes. Therefore, the sequence is either configure: select : triggered conversions : FIFO read : select : triggered conversions : FIFO read or configure : select : triggered conversions : configure : .... Each configure clears the FIFO and the action that follows the configure command depends on the mode setting of the device.

modes using the FIFO: modes 01, 10, 11 timing (continued)



† Command = Configure write for mode 01, FIFO threshold = 1/2
‡ Command = Read FIFO, 1st FIFO read
§ Command = Select ch2.

Figure 10. TLC2554/TLC2558 Mode 01 DSP Serial Interface (conversions triggered by FS)



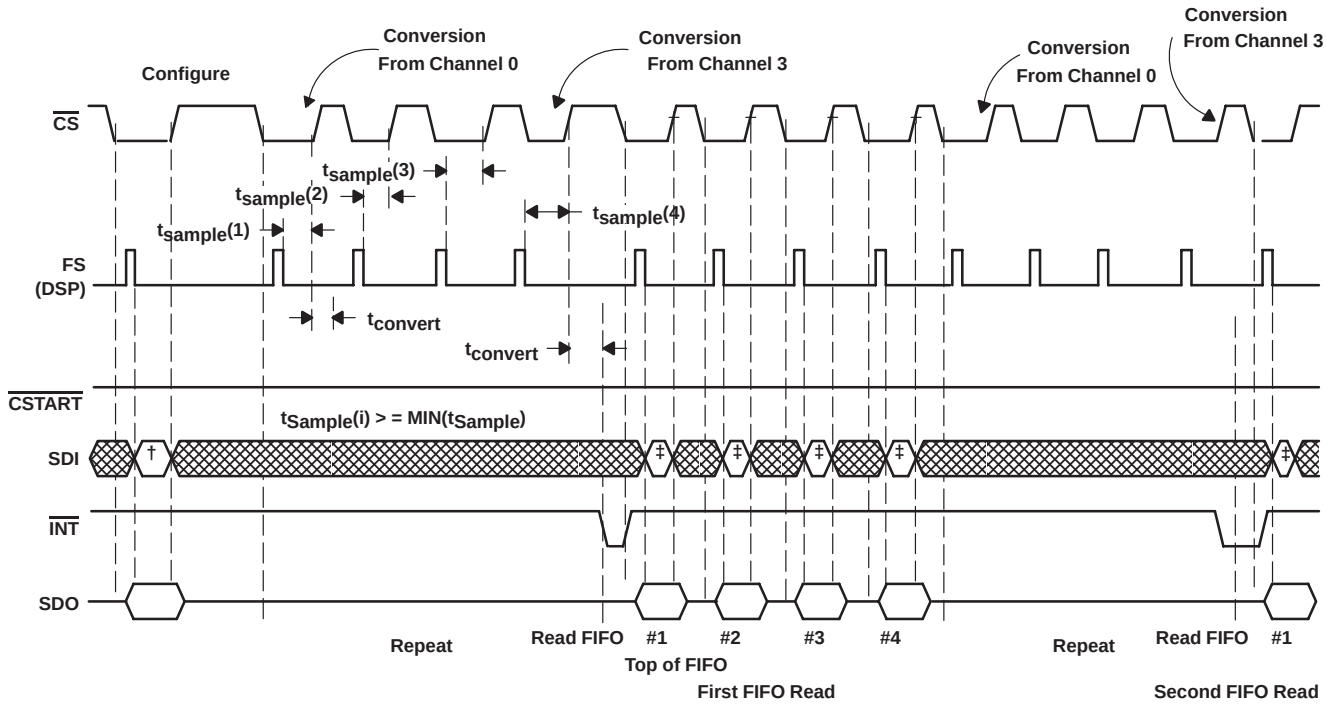
† Command = Configure write for mode 01, FIFO threshold = 1/2
‡ Command = Read FIFO, 1st FIFO read
§ Command = Select ch2.

Figure 11. TLC2554/TLC2558 Mode 01 µp/DSP Serial Interface (conversions triggered by $\overline{\text{CSTART}}$)

modes using the FIFO: modes 01, 10, 11 timing (continued)

Mode 10 (sweep mode) requires reconfiguration at the start of each new sweep sequence. Once the FIFO is filled up to the programmed threshold, the host has the option to either read the FIFO or configure for other modes. Once the FIFO is read, the host must reconfigure the device before the next sweep sequence can be started. So the sequence is either configure : triggered conversions : FIFO read : configure. or configure : triggered conversions : configure : .... Each configure clears the FIFO and the action that follows the configure command depends on the mode setting of the device.

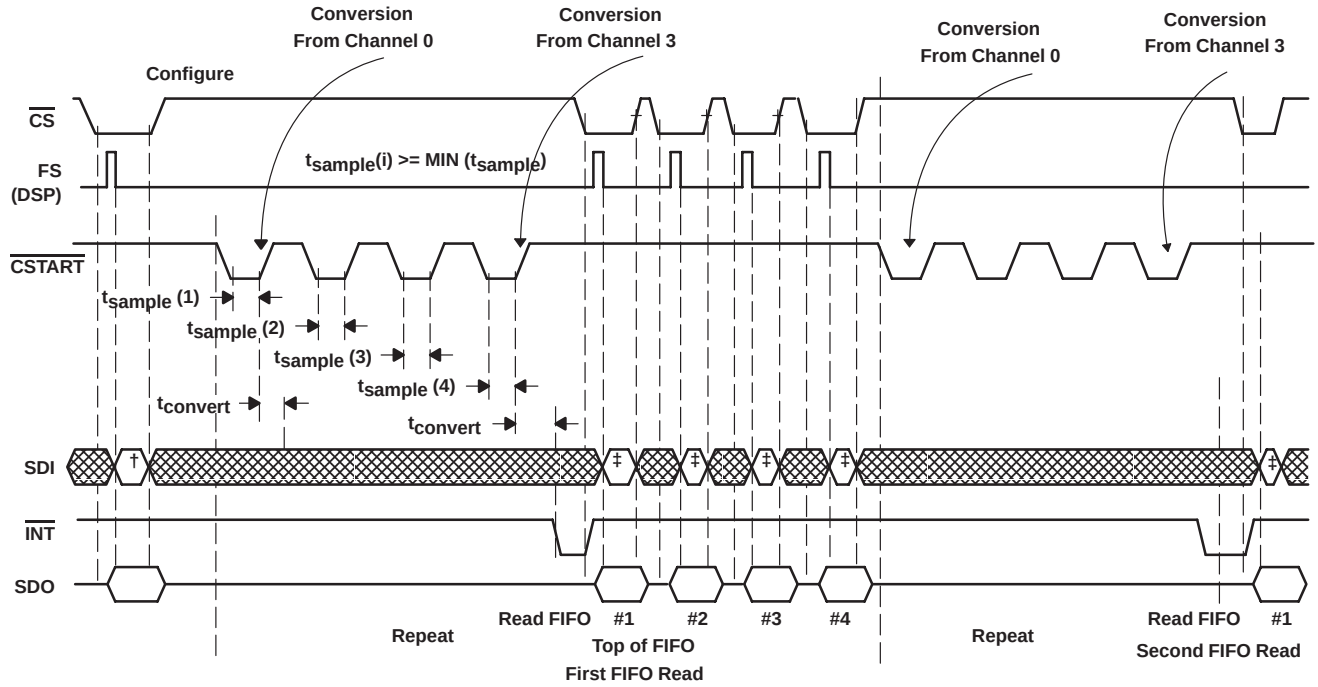
Mode 11 (repeat sweep mode) requires one cycle configuration. This sweep sequence can be repeated without reconfiguration. Once the FIFO is filled up to the programmed threshold, the host has the option to either read the FIFO or configure for other modes. So the sequence is either configure : triggered conversions : FIFO read : triggered conversions : FIFO read ... or configure : triggered conversions : configure : .... Each configure clears the FIFO and the action that follows the configure command depends on the mode setting of the device.



† Command = Configure write for mode 10 or 11, FIFO threshold = 1/2, sweep seq = 0–1–2–3.
‡ Command = Read FIFO

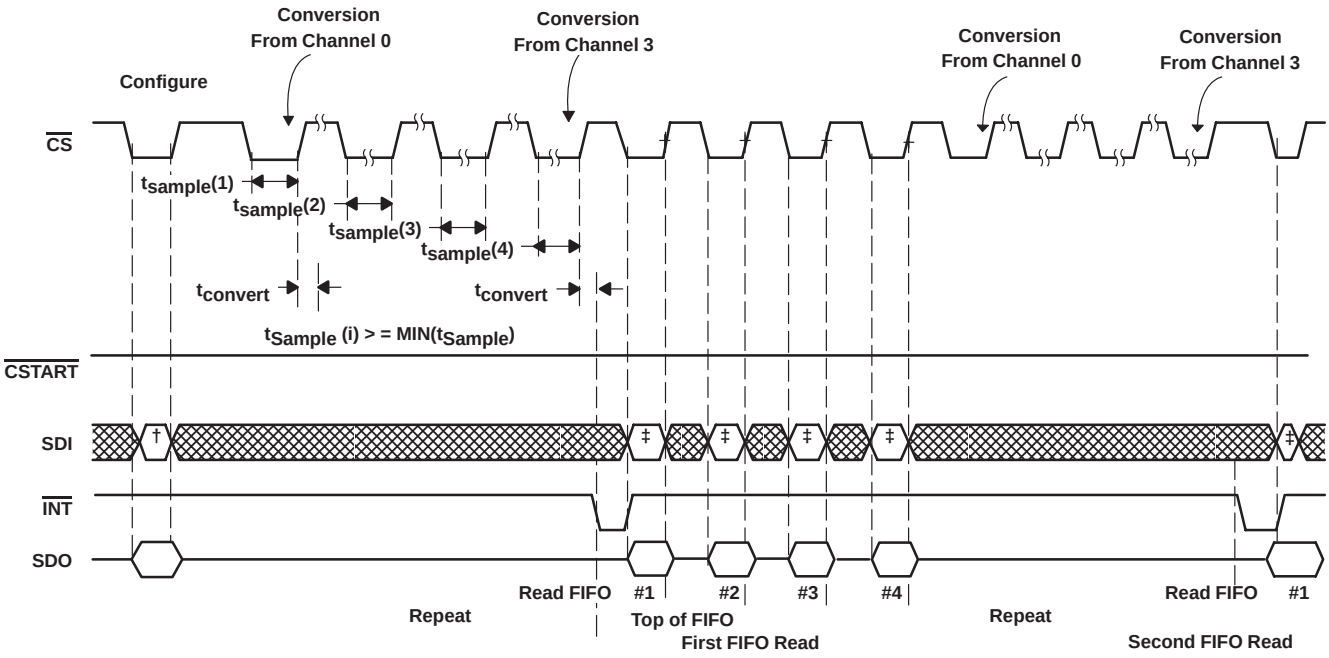
Figure 12. TLC2554/TLC2558 Mode 10/11 DSP Serial Interface (conversions triggered by FS)

modes using the FIFO: modes 01, 10, 11 timing (continued)



† Command = Configure write for mode 10 or 11, FIFO threshold = 1/2, sweep seq = 0–1–2–3.
‡ Command = Read FIFO

Figure 13. TLC2554/TLC2558 Mode 10/11 DSP Serial Interface (conversions triggered by $\overline{\text{CSTART}}$)



† Command = Configure write for mode 10 or 11, FIFO threshold = 1/2, sweep seq = 0–1–2–3.
‡ Command = Read FIFO

Figure 14. TLC2554/TLC2558 Mode 00/11 μp Serial Interface (conversions triggered by $\overline{\text{CS}}$)

FIFO operation

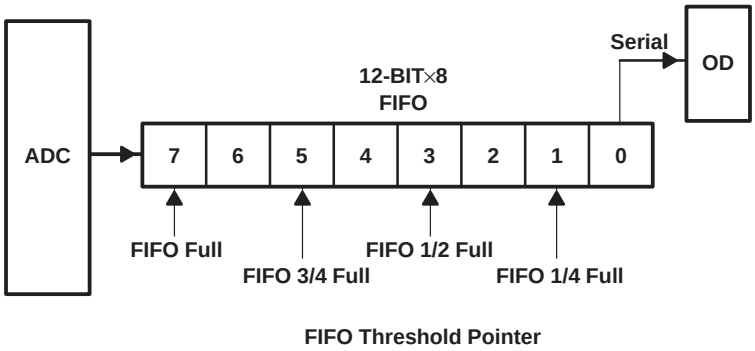


Figure 15. TLC2554/TLC2558 FIFO

The device has an 8 layer FIFO that can be programmed for different thresholds. An interrupt is sent to the host after the preprogrammed threshold is reached. The FIFO can be used to store data from either a fixed channel or a series of channels based on a preprogrammed sweep sequence. For example, an application may require eight measurements from channel 3. In this case, the FIFO is filled with 8 data sequentially taken from channel 3. Another application may require data from channel 0, channel 2, channel 4, and channel 6 in an orderly manner. Therefore, the threshold is set for 1/2 and the sweep sequence 0–2–4–6–0–2–4–6 is chosen. An interrupt is sent to the host as soon as all four data are in the FIFO.

SCLK and conversion speed

There are multiple ways to adjust the conversion speed. The maximum equivalent conversion clock (f_{SCLK}/DIV) should not exceed 10 MHz.

- The SCLK is used as the source of the conversion clock and 14 conversion clocks are required to complete a conversion plus 4 SCLKs overhead.

  The devices can operate with an SCLK up to 20 MHz for the supply voltage range specified. The clock divider provides speed options appropriate for an application where a high speed SCLK is used for faster I/O. The total conversion time is $14 \times (DIV/f_{SCLK})$ where DIV is 1 or 2. For example a 20-MHz SCLK with the divide by 2 option produces a $\{14 \times (2/20\ M) + 4 \times (1/20\ MHz)\} = 1.6\ \mu s$ conversion time.

- Auto power down can be used. This mode is always on. If the device is not accessed (by $\overline{CS}$ or $\overline{CSTART}$), the converter is powered down to save power. The built-in reference is left on in order to quickly resume operation within one half SCLK period. This provides unlimited choices to trade speed with power savings.

reference voltage

The device has a built-in reference with a level of 4 V. If the internal reference is used, REFP is set to 4 V and REFM is set to 0 V. An external reference can also be used through two reference input pins, REFP and REFM, if the reference source is programmed as external. The voltage levels applied to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REFP, REFM, and the analog input should not exceed the positive supply or be lower than GND consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than REFP and at zero when the input signal is equal to or lower than REFM.

FIFO operation (continued)

power down

Writing 8000h to the device puts the device into a software power-down state. For a hardware power down, the dedicated $\overline{\text{PWDN}}$ pin provides another way to power down the device asynchronously. These two power-down modes power down the entire device including the built-in reference to save power. It requires 20 ms to resume from either a software or hardware power down.

Auto power down mode is always enabled. This mode maintains the built-in reference if an internal reference is used, so resumption is fast enough to be used between cycles.

The configuration register is not affected by any of the power down modes but the sweep operation sequence has to be started over again. All FIFO contents are cleared by the power-down modes.

power up and initialization

Initialization requires:

1. Determine processor type by writing A000h to the TLC2554/58
2. Configure the device

The first conversion after power up or resuming from power down is not valid.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, GND to V_{CC} . . . . . –0.3 V to 6.5 V
Analog input voltage range . . . . . –0.3 V to V_{CC} + 0.3 V
Reference input voltage . . . . . V_{CC} + 0.3 V
Digital input voltage range . . . . . –0.3 V to V_{CC} + 0.3 V
Operating virtual junction temperature range, T_J . . . . . –40°C to 150°C
Operating free-air temperature range, T_A: TLC2554/58C . . . . . 0°C to 70°C
TLC2554/58I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Positive external reference voltage input, V_{REFP} (see Note 1)	2		V_{CC}	V
Negative external reference voltage input, V_{REFM} (note Note 1)	0		2	V
Differential reference voltage input, $V_{REFP} – V_{REFM}$ (see Note 1)	2	V_{CC}	V_{CC}+0.2	V
Analog input voltage (see Note 1)	0		V_{CC}	V
High level control input voltage, V_{IH}	2.1			V
Low-level control input voltage, V_{IL}			0.6	V
Rise time, for $\overline{\text{CS}}$, $\overline{\text{CSTART}}$ SDI at 0.5 pF, $t_{r(I/O)}$			4.76	ns
Fall time, for $\overline{\text{CS}}$, $\overline{\text{CSTART}}$ SDI at 0.5 pF, $t_{f(I/O)}$			2.91	ns
Rise time, for $\overline{\text{INT}}$, EOC, SDO at 30 pF, $t_{r(Output)}$			2.43	ns
Fall time, for $\overline{\text{INT}}$, EOC, SDO at 30 pF, $t_{f(Output)}$			2.3	ns

NOTE 1: When binary output format is used, analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (000000000000). The device is functional with reference down to 2 V ($V_{REFP} – V_{REFM}$ –1); however, the electrical specifications are no longer applicable.

recommended operating conditions (continued)

		MIN	NOM	MAX	UNIT
Transition time, for FS, SCLK, SDI, $t_{t(CLK)}$		0.5			SCLK
Setup time, CS falling edge before SCLK rising edge (FS=1) or before SCLK falling edge (when FS is active), $t_{su(CS-SCLK)}$		0.5			SCLK
Hold time, CS rising edge after SCLK rising edge (FS=1) or after SCLK falling edge (when FS is active), $t_{h(SCLK-CS)}$		5			ns
Delay time, delay from CS falling edge to FS rising edge, $t_{d(CSL-FSH)}$		0.5		7	SCLKs
Delay time, delay time from 16th SCLK falling edge to CS rising edge (FS is active), $t_{d(SCLK16F-CSH)}$		0.5			SCLKs
Setup time, FS rising edge before SCLK falling edge, $t_{su(FSH-SCLKF)}$				0.5	SCLKs
Hold time, FS hold high after SCLK falling edge, $t_{h(FSH-SCLKF)}$		0.5			SCLKs
Pulse width, CS high time, $t_{wH(CS)}$		100			ns
SCLK cycle time, V_{CC} = 2.7 V to 3.6V, $t_{c(SCLK)}$		67			ns
SCLK cycle time, V_{CC} = 4.5 V to 5.5V, $t_{c(SCLK)}$		50			ns
Pulse width, SCLK low time, $t_{wL(SCLK)}$		20		30	ns
Pulse width, SCLK high time, $t_{wH(SCLK)}$		20		30	ns
Setup time, SDI valid before falling edge of SCLK (FS is active) or the rising edge of SCLK (FS=1), $t_{su(DI-SCLK)}$				25	ns
Hold time, SDI hold valid after falling edge of SCLK (FS is active) or the rising edge of SCLK (FS=1), $t_{h(DI-SCLK)}$		5			ns
Delay time, delay from CS falling edge to SDO valid, $t_{d(CSL-DOV)}$		1		25	ns
Delay time, delay from FS falling edge to SDO valid, $t_{d(FSL-DOV)}$		1		25	ns
Delay time, delay from SCLK rising edge (FS is active) or SCLK falling edge (FS=1) SDO valid, $t_{d(CLK-DOV)}$		1		25	ns
Delay time, delay from CS rising edge to SDO 3-stated, $t_{d(CSH-DOZ)}$		1		25	ns
Delay time, delay from 16th SCLK falling edge (FS is active) or the 16th rising edge (FS=1) to EOC falling edge, $t_{d(CLK-EOCL)}$		1		25	ns
Delay time, delay from EOC rising edge to SDO 3-stated if CS is low, $t_{d(EOCH-DOZ)}$		1		50	ns
Delay time, delay from 16th SCLK rising edge to INT falling edge (FS =1) or from the 16th falling edge SCLK to INT falling edge (when FS active), $t_{d(SCLK-INTL)}$				3.5	µs
Delay time, delay from CS falling edge to INT rising edge, $t_{d(CSL-INTH)}$		1		50	ns
Delay time, delay from CS rising edge to CSTART falling edge, $t_{d(CSH-CSTARTL)}$		100			ns
Delay time, delay from CSTART rising edge to EOC falling edge, $t_{d(CSTARTH-EOCL)}$		1		50	ns
Pulse width, CSTART low time, t_{wL}(CSTART)		0.8			µs
Delay time, delay from CS rising edge to EOC rising edge, $t_{d(CSH-EOCH)}$		1		50	ns
Delay time, delay from CSTART rising edge to CSTART falling edge, $t_{d(CSTARTH-CSTARTL)}$		3.6			µs
Delay time, delay from CSTART rising edge to INT falling edge, $t_{d(CSTARTH-INTL)}$		3.5			µs
Operating free-air temperature, T_A	TLC2554C/TLC2558C	0		70	°C
	TLC2554I/TLC2558I	–40		85	

NOTE 2: This is the time required for the clock input signal to fall from V_{IH} max or to rise from V_{IL} max to V_{IH} min. In the vicinity of normal room temperature, the devices function with input clock transition time as slow as 1 µs for remote data-acquisition applications where the sensor and A/D converter are placed several feet away from the controlling microprocessor.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = V_{REFP} = 4.5 V to 5.5 V, SCLK frequency = 20 MHz at 5 V, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 5.5 V, I_{OH} = –20 µA at 30 pF load		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 5.5 V, I_{OL} = 20 µA at 30 pF load				0.4	V
I_{OZ}	Off-state output current (high-impedance-state)	V_O = V_{CC}	$\overline{CS}$ = V_{CC}		1	2.5	µA
		V_O = 0			–1	-2.5	
I_{IH}	High-level input current	V_I = V_{CC}			0.005	2.5	µA
I_{IL}	Low-level input current	V_I = 0 V			–0.005	2.5	µA
I_{CC}	Operating supply current, normal sampling (short)	$\overline{CS}$ at 0 V, Ext ref	V_{CC} = 4.5 V to 5.5 V			4	mA
		$\overline{CS}$ at 0 V, Int ref	V_{CC} = 4.5 V to 5.5 V			6	mA
I_{CC}	Operating supply current, extended sampling	$\overline{CS}$ at 0 V, Ext ref	V_{CC} = 4.5 V to 5.5 V		1.9		mA
		$\overline{CS}$ at 0 V, Int ref	V_{CC} = 4.5 V to 5.5 V		2		mA
	Internal reference supply current	$\overline{CS}$ at 0 V, V_{CC} = 4.5 V to 5.5 V				2	mA
$I_{CC(PD)}$	Power-down supply current	For all digital inputs, 0≤ V_I ≤ 0.3 V or V_I ≥ V_{CC}– 0.3 V, SCLK = 0, V_{CC} = 4.5 V to 5.5 V, Ext clock			0.1	1	µA
$I_{CC(AUTOPWDN)}$	Auto power-down current	For all digital inputs, 0≤ V_I ≤ 0.3 V or V_I ≥ V_{CC}– 0.3 V, SCLK = 0, V_{CC} = 4.5 V to 5.5 V, Ext clock, Ext ref				5‡	µA
	Selected channel leakage current	Selected channel at V_{CC}				1	µA
		Selected channel at 0 V				–1	
	Maximum static analog reference current into REFP (use external reference)	V_{REFP} = V_{CC} = 5.5 V, V_{REFM} = GND				1	µA
C_i	Input capacitance	Analog inputs			45	50	pF
		Control Inputs			5	25	
Z_i	Input MUX ON resistance	V_{CC} = 5.5 V				500	Ω

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ 800 µA if internal reference is used.

ac specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio +distortion	f_I = 12 kHz at 400 KSPS	69	71		dB
THD	Total harmonic distortion	f_I = 12 kHz at 400 KSPS		–82	–76	dB
ENOB	Effective number of bits	f_I = 12 kHz at 400 KSPS		11.6		Bits
SFDR	Spurious free dynamic range	f_I = 12 kHz at 400 KSPS		–84	–75	dB
Analog input						
	Full power bandwidth, –3 dB			1		MHz
	Full power bandwidth, –1 dB			500		kHz

reference specifications (0.1 μF and 10 μF between REFP and REFM pins)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Reference input voltage, REFP	V_{CC} = 4.5 V				V_{CC}	V
Input impedance	V_{CC} = 5.5 V	CS = 1, SCLK = 0, (off)	100			MΩ
		CS = 0, SCLK = 20 MHz (on)	20	25		kΩ
Input voltage difference, REFP – REFM	V_{CC} = 4.5 V		2		V_{CC}	V
Internal reference voltage,REFP – REFM	V_{CC} = 5.5 V	Reference select = internal	3.85	4	4.15	V
Internal reference start up time	V_{CC} = 5.5 V	10 μF		20		ms
Reference temperature coefficient	V_{CC} = 4.5 V			16	40	PPM/°C

operating characteristics over recommended operating free-air temperature range, $V_{CC} = V_{REFP}$ = 4.5 V, SCLK frequency = 20 MHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Integral linearity error (INL) (see Note 4)					±1	LSB
	Differential linearity error (DNL)		See Note 3			±1	LSB
E_O	Offset error (see Note 5)		See Note 3			±2.5	LSB
E_G	Gain error (see Note 5)		See Note 3		±1	±2	LSB
E_T	Total unadjusted error (see Note 6)					±2	LSB
	Self-test output code (see Table 1 and Note 7)		SDI = B000h		800h (2048D)		
			SDI = C000h		000h (0D)		
			SDI = D000h		FFFh (4095D)		
t_{conv}	Conversion time	External SCLK			(14XDIV) / f_{SCLK}		
t_{sample}	Sampling time		At 1 kΩ	600			ns
$t_{t(I/O)}$	Transition time for EOC, $\overline{INT}$					50	ns
$t_{t(CLK)}$	Transition time for SDI, SDO					25	ns

† All typical values are at T_A = 25°C.

NOTES: 3. Analog input voltages greater than that applied to REFP convert as all ones (111111111111), while input voltages less than that applied to REFM convert as all zeros (0000000000). The device is functional with reference down to 2 V (VREFP – VREFM); however, the electrical specifications are no longer applicable.
4. Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.
5. Zero error is the difference between 000000000000 and the converted output for zero input voltage: full-scale error is the difference between 111111111111 and the converted output for full-scale input voltage.
6. Total unadjusted error comprises linearity, zero, and full-scale errors.
7. Both the input data and the output codes are expressed in positive logic.

PARAMETER MEASUREMENT INFORMATION

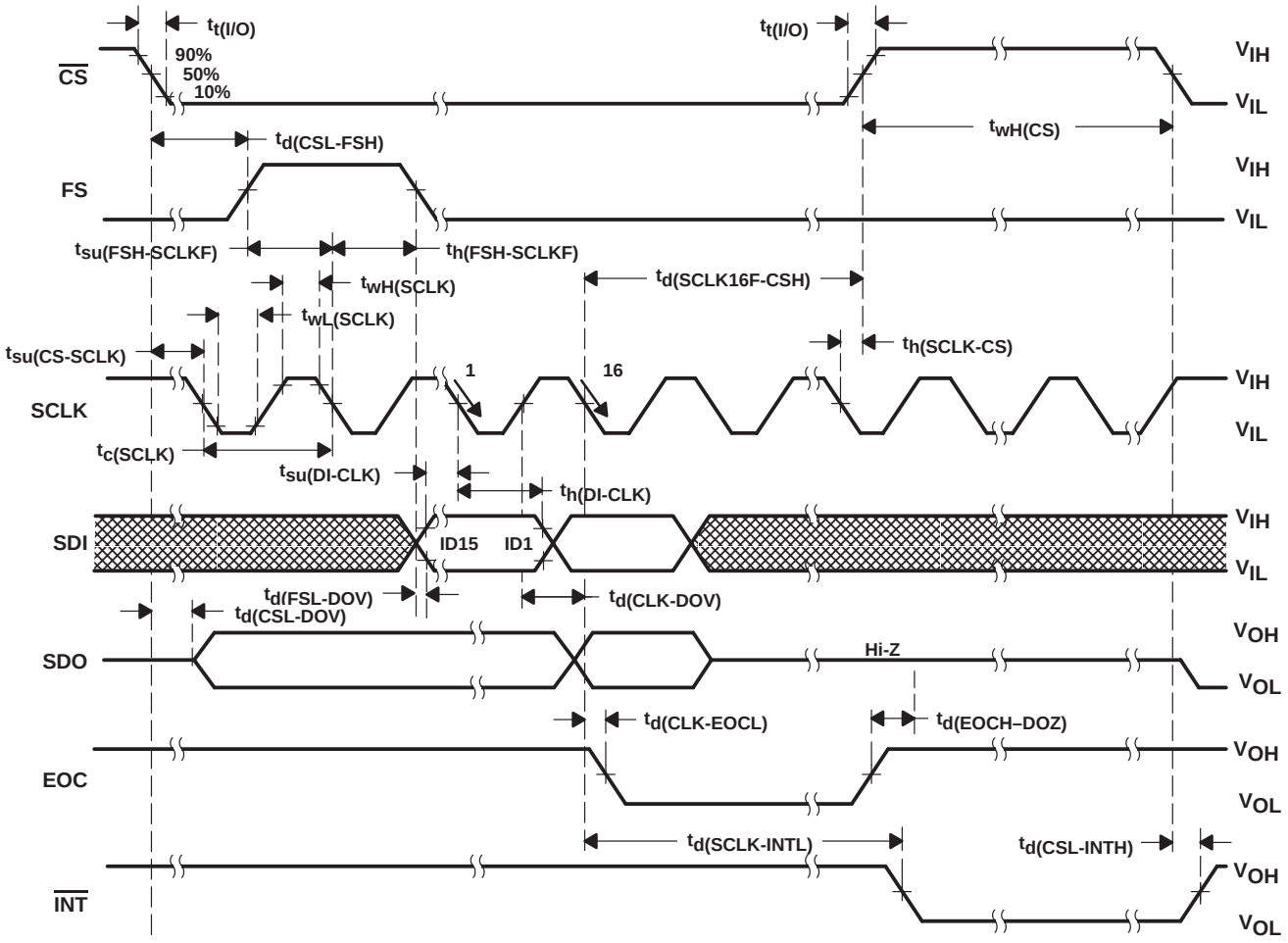


Figure 16. Critical Timing (normal sampling, FS is active)

PARAMETER MEASUREMENT INFORMATION

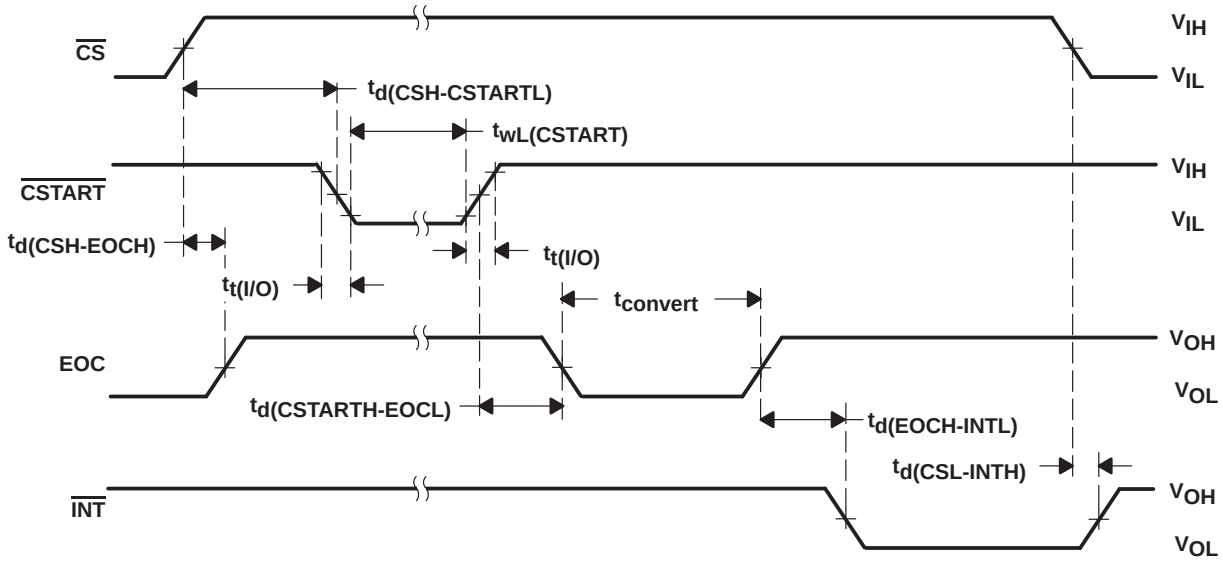


Figure 17. Critical Timing (extended sampling, single shot)

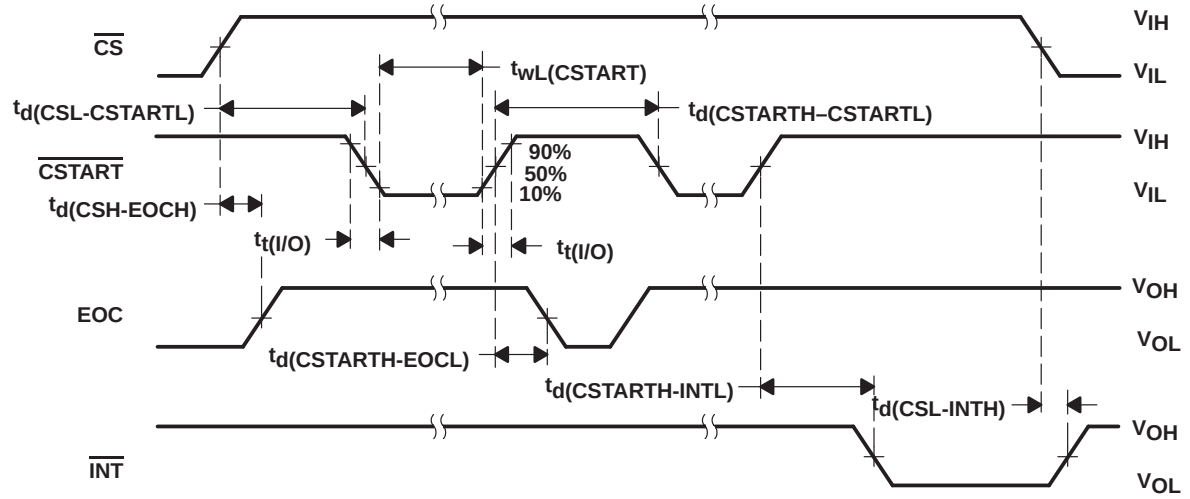


Figure 18. Critical Timing (extended sampling, repeat/sweep/repeat sweep)

PARAMETER MEASUREMENT INFORMATION

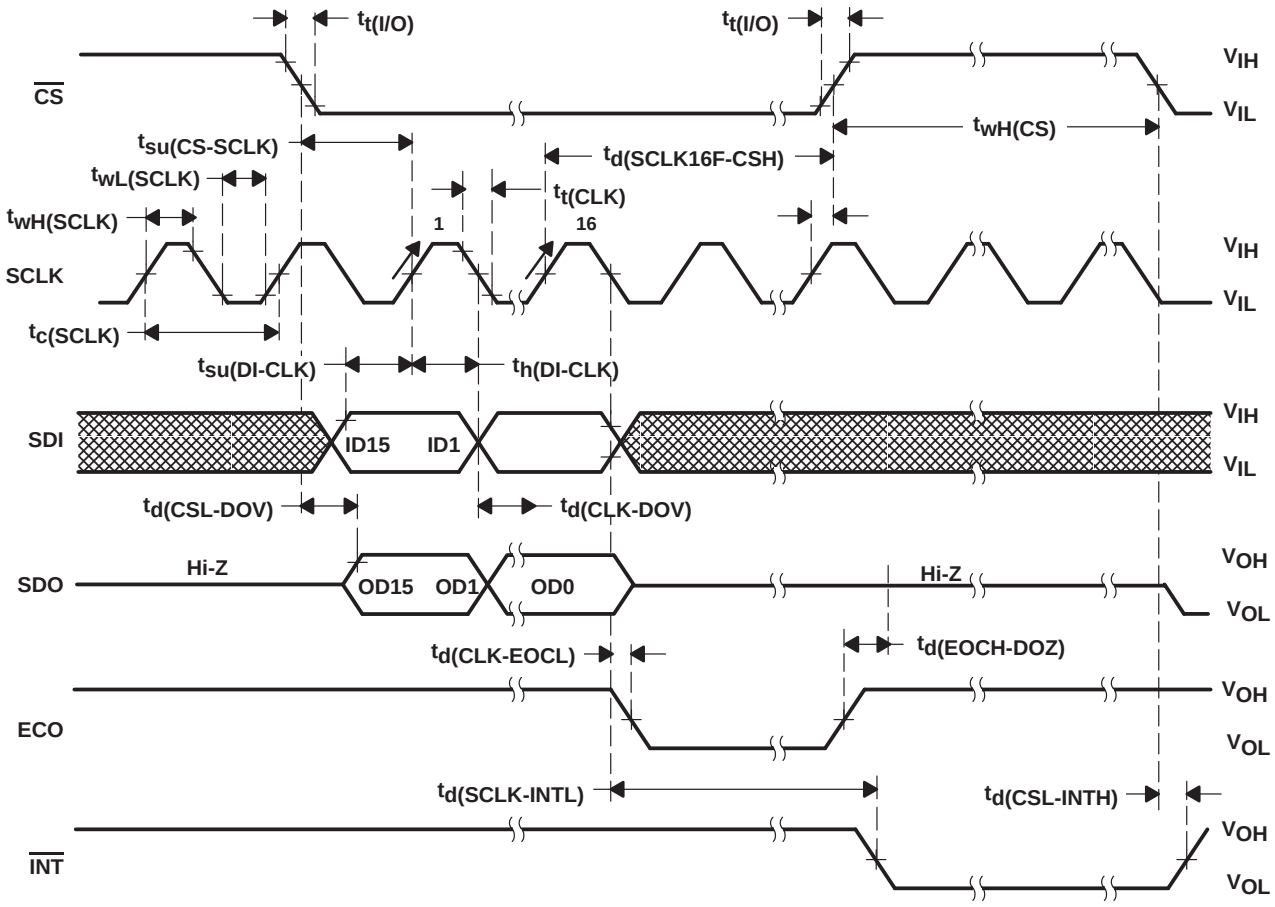


Figure 19. Critical Timing (normal sampling, FS = 1)

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY vs TEMPERATURE

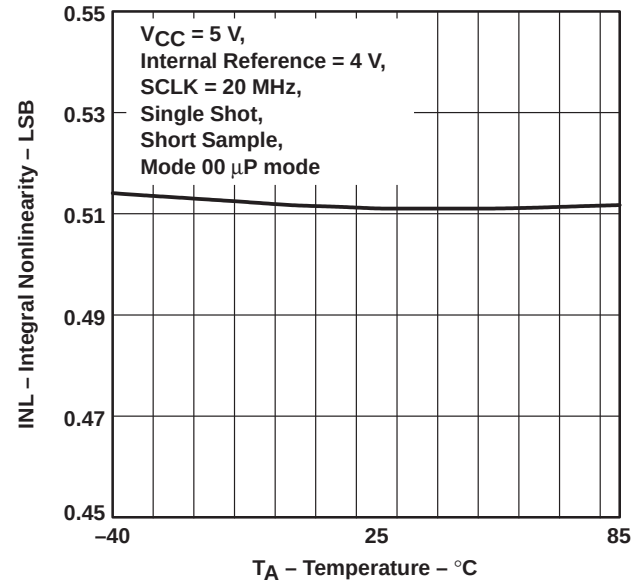


Figure 20

DIFFERENTIAL NONLINEARITY vs TEMPERATURE

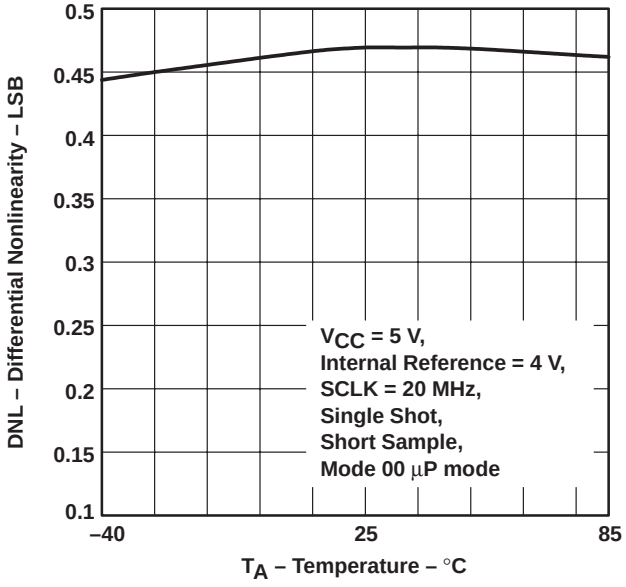


Figure 21

OFFSET ERROR vs TEMPERATURE

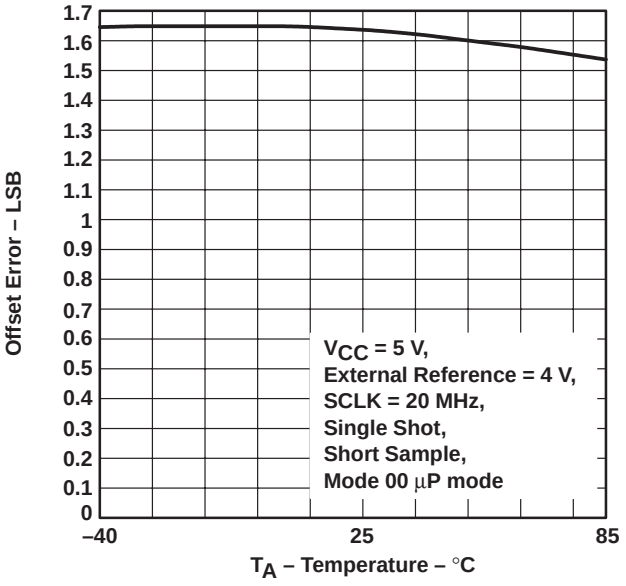


Figure 22

GAIN ERROR vs TEMPERATURE

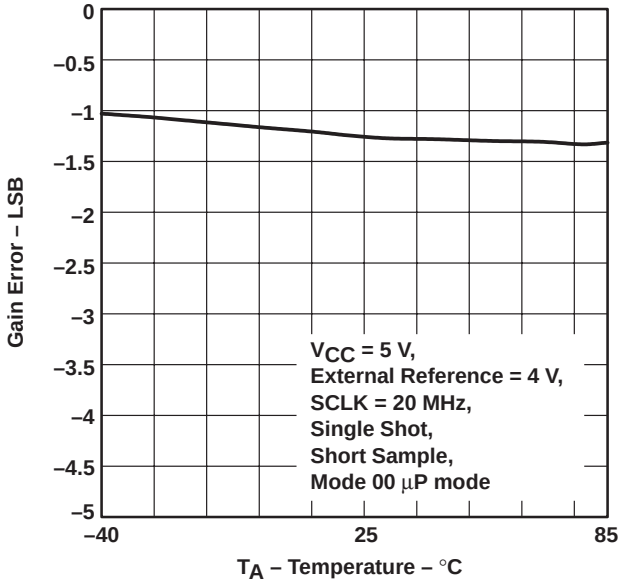


Figure 23

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs TEMPERATURE

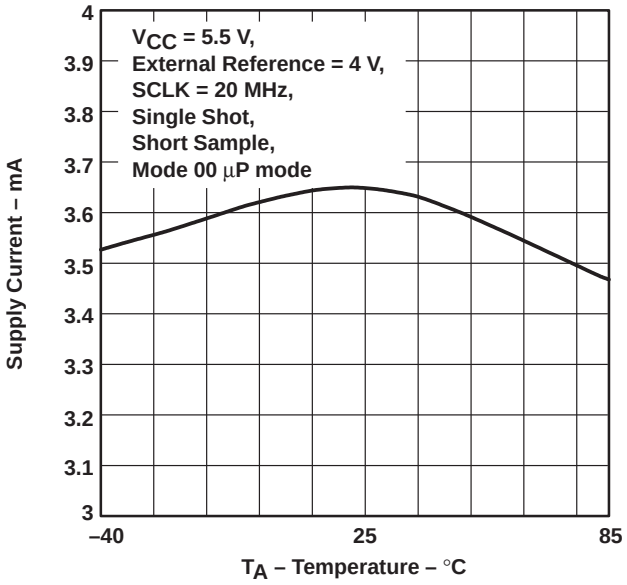


Figure 24

POWER DOWN CURRENT vs TEMPERATURE

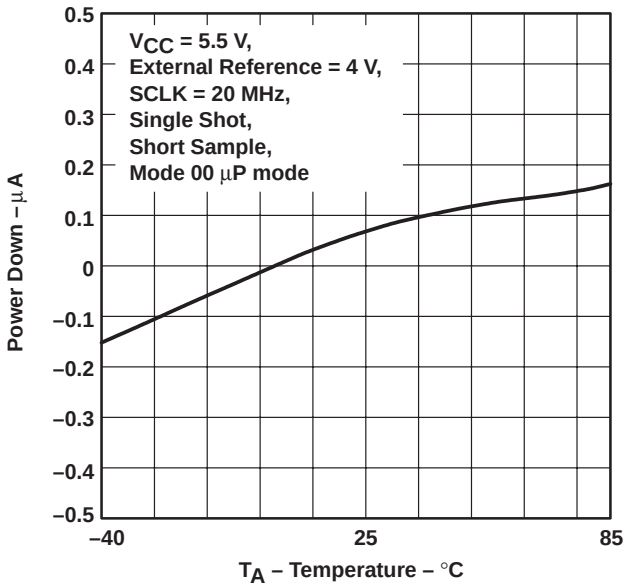


Figure 25

INTEGRAL NONLINEARITY vs SAMPLES

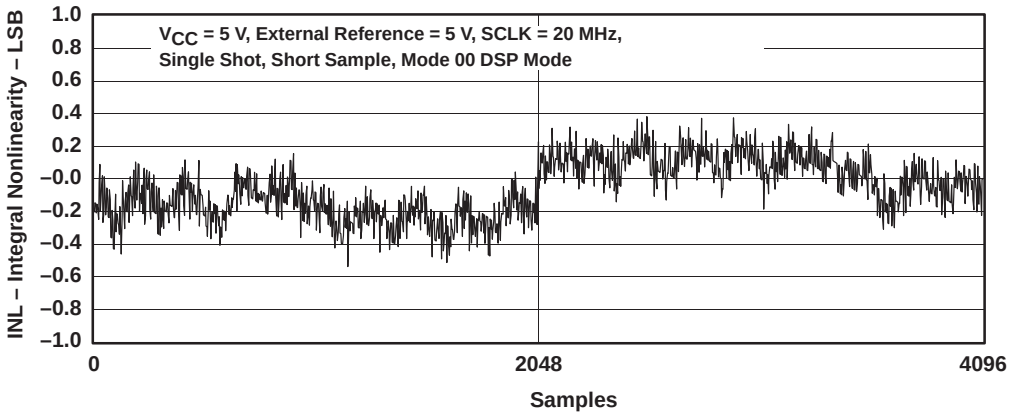


Figure 26

TYPICAL CHARACTERISTICS

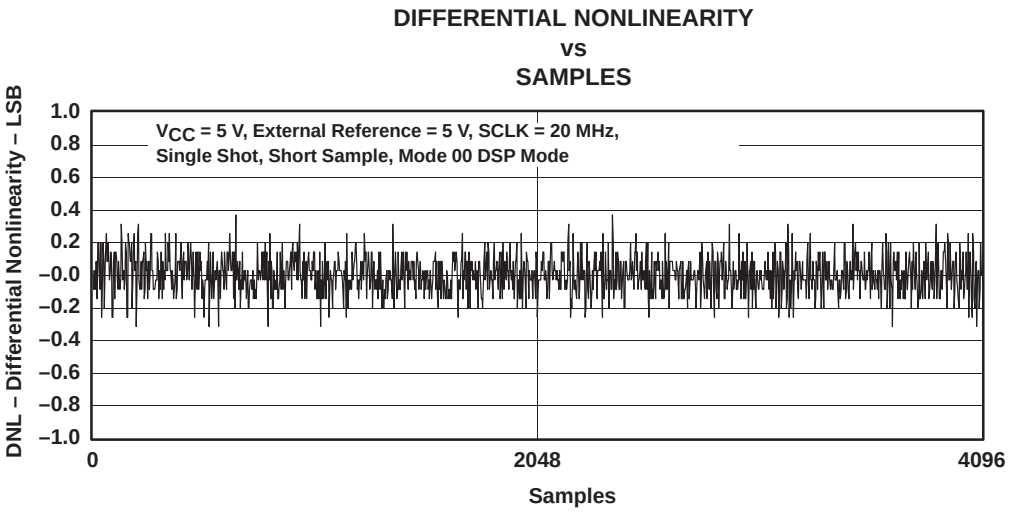


Figure 27

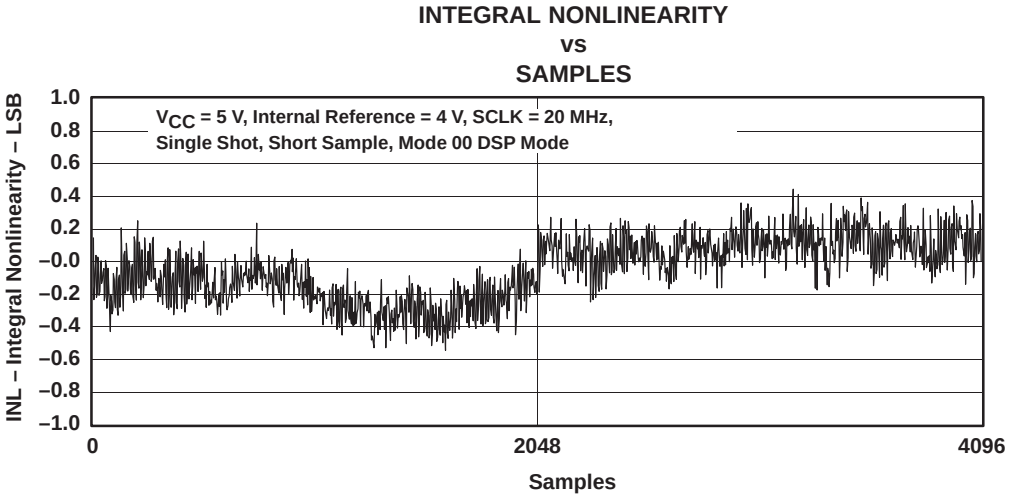


Figure 28

TYPICAL CHARACTERISTICS

DIFFERENTIAL NONLINEARITY
vs
SAMPLES

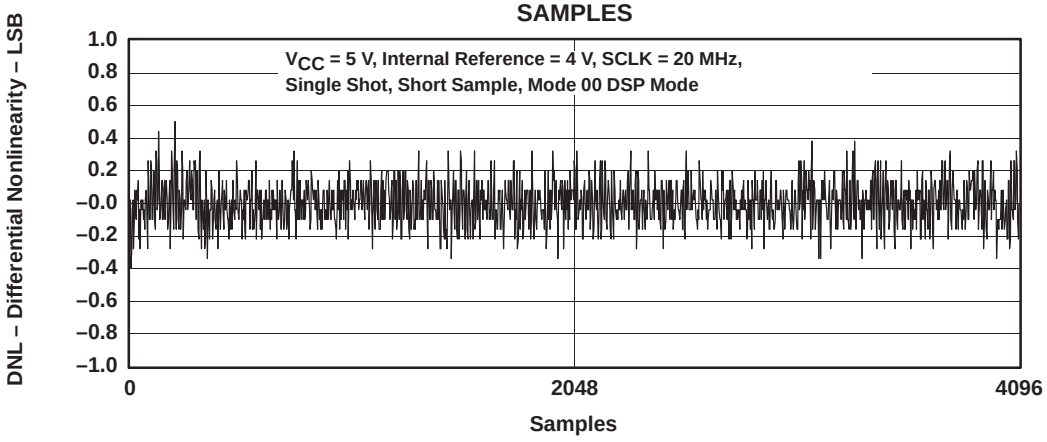


Figure 29

FAST POURIER TRANSFORM
vs
FREQUENCY

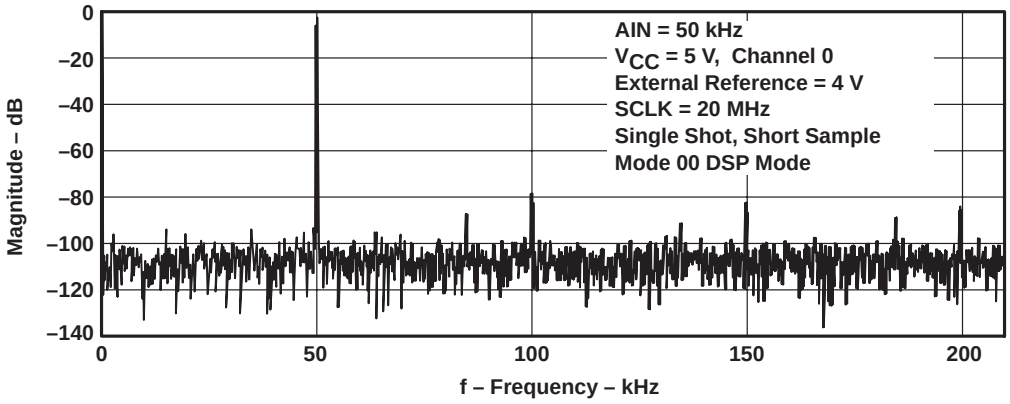


Figure 30

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE + DISTORTION
vs
INPUT FREQUENCY

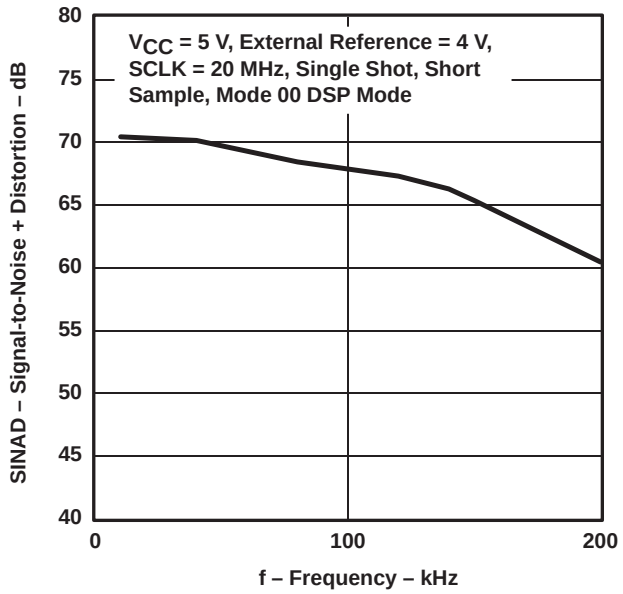


Figure 31

EFFECTIVE NUMBER OF BITS
vs
INPUT FREQUENCY

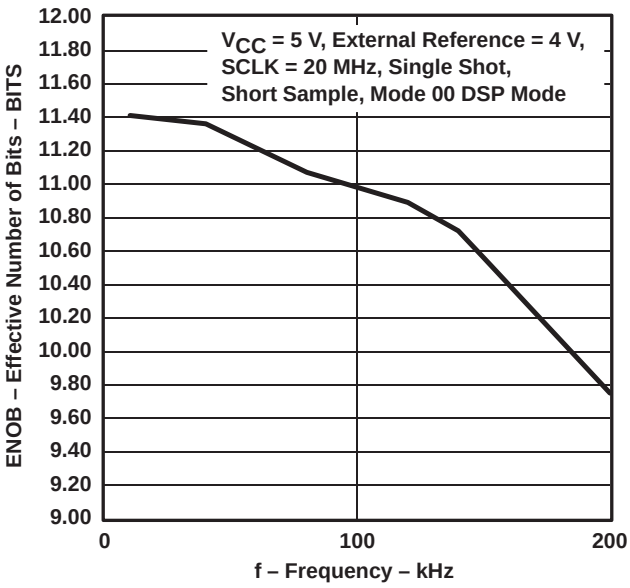


Figure 32

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

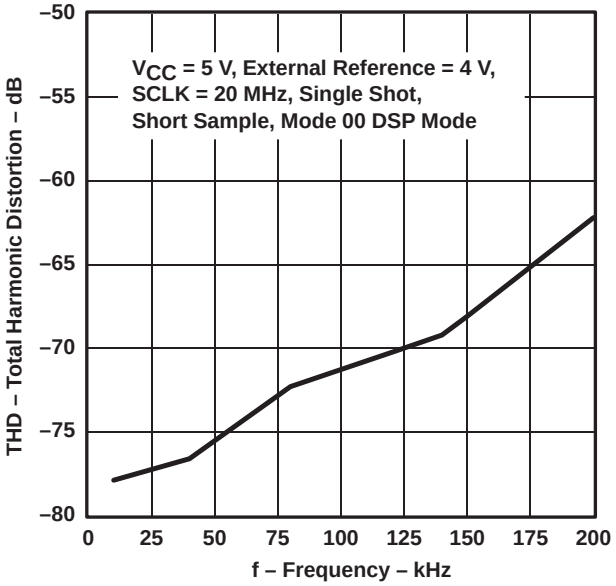


Figure 33

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY

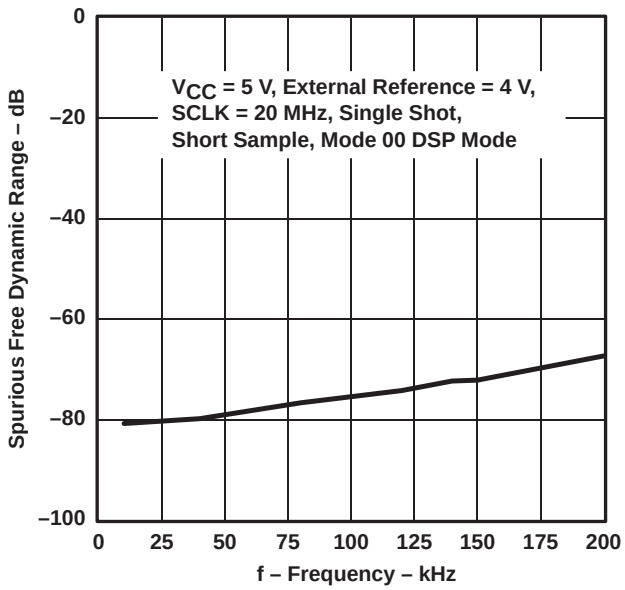
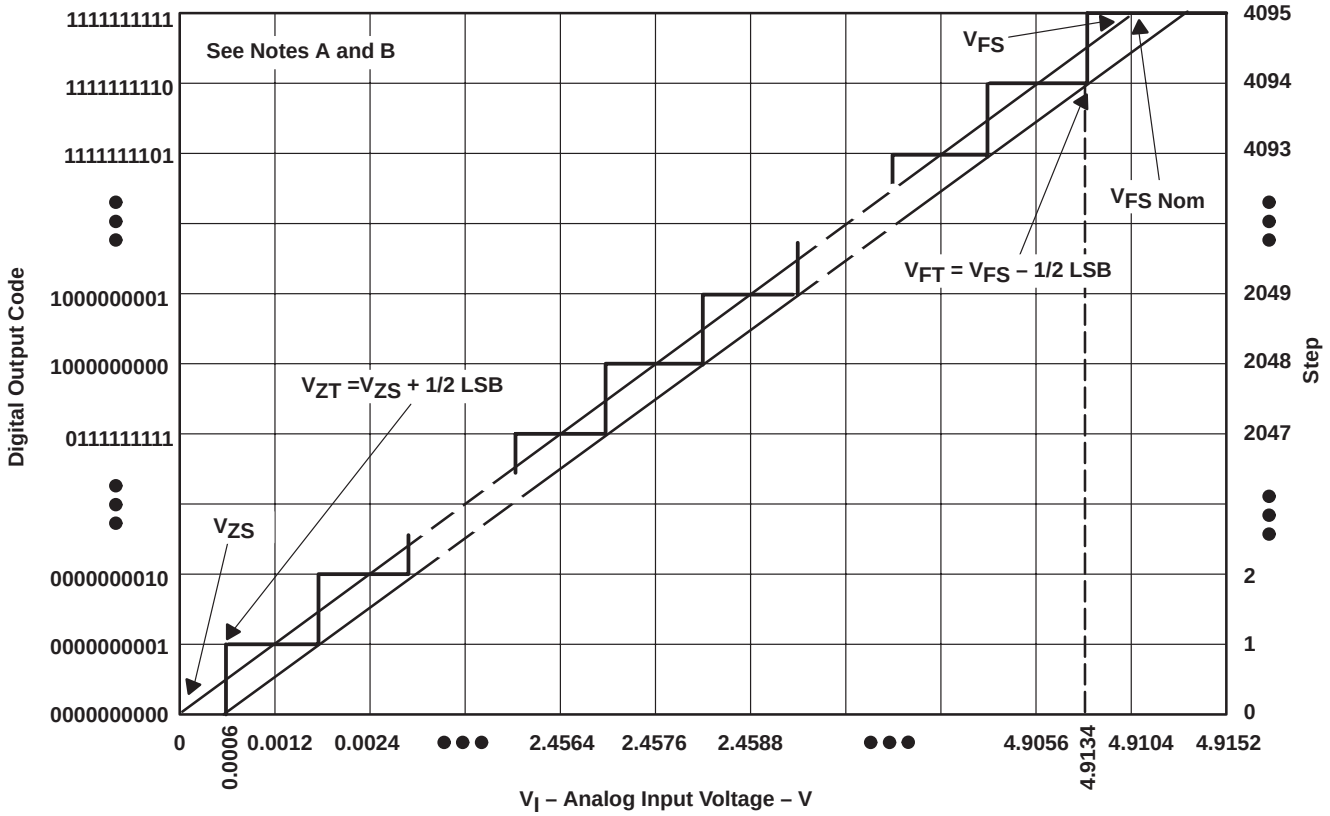


Figure 34

PRINCIPLES OF OPERATION



NOTES: A. This curve is based on the assumption that V_{ref+} and V_{ref-} have been adjusted so that the voltage at the transition from digital 0 to 1 (V_{ZT}) is 0.0006 V, and the transition to full scale (V_{FT}) is 4.9134 V, 1 LSB = 1.2 mV.

B. The full scale value (V_{FS}) is the step whose nominal midstep value has the highest absolute value. The zero-scale value (V_{ZS}) is the step whose nominal midstep value equals zero.

Figure 35. Ideal 12-Bit ADC Conversion Characteristics

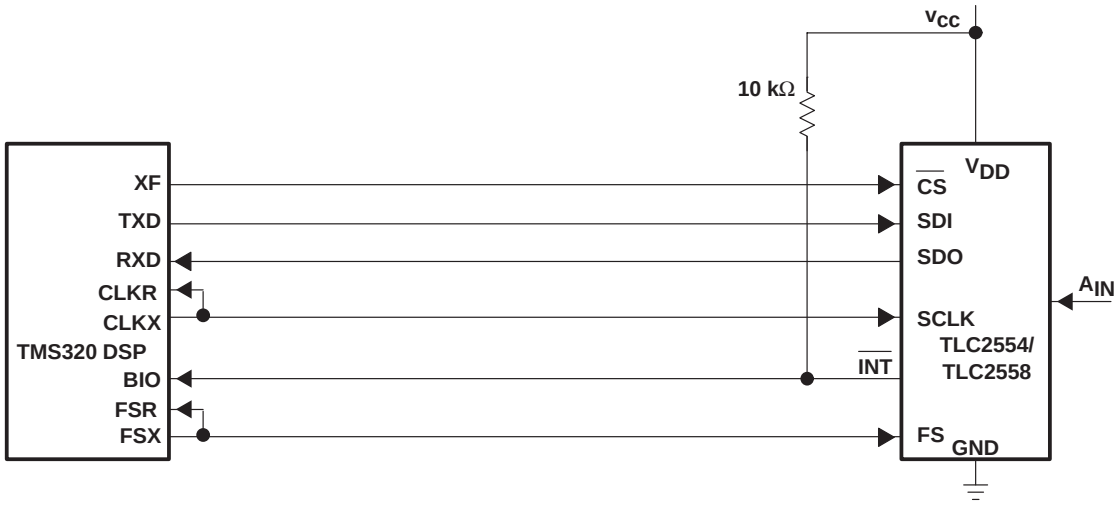


Figure 36. Typical Interface to a TMS320 DSP

PRINCIPLES OF OPERATION

simplified analog input analysis

Using the equivalent circuit in Figure 39, the time required to charge the analog input capacitance from 0 to VS within 1/2 LSB can be derived as follows.

The capacitance charging voltage is given by:

$$Vc = Vs\left(1–EXP\left(\frac{–tc}{Rt \times Ci}\right)\right) \quad (1)$$

Where

Rt = Rs + Zi
tc = Cycle time

The input impedance Zi is 0.5 kΩ at 5 V. The final voltage to 1/2 LSB is given by:

$$VC\ (1/2\ LSB) = VS–\left(\frac{VS}{8192}\right) \quad (2)$$

Equating equation 1 to equation 2 and solving for cycle time tc gives:

$$Vs–\left(\frac{VS}{8192}\right) = Vs\left(1–EXP\left(\frac{–tc}{Rt \times Ci}\right)\right) \quad (3)$$

and time to change to 1/2 LSB (minimum sampling time) is:

$$tch\ (1/2\ LSB) = Rt \times Ci \times In(8192)$$

Where

In(8192) = 9.011

Therefore, with the values given, the time for the analog input signal to settle is:

$$tch\ (1/2\ LSB) = (Rs + 0.5\ k\Omega) \times Ci \times In(8192) \quad (4)$$

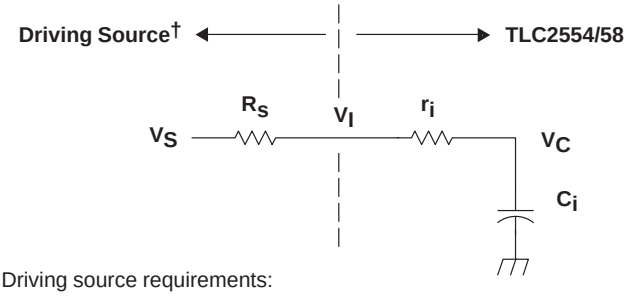
This time must be less than the converter sample time shown in the timing diagrams. This is 12× SCLKs (if the sampling mode is short normal sampling mode).

$$tch\ (1/2\ LSB) \leq 12\times \frac{1}{f(SCLK)} \quad (5)$$

Therefore the maximum SCLK frequency is:

$$max\left[f(SCLK)\right] = \frac{12}{tch\ (1/2\ LSB)} = \frac{12}{[In(8192) \times Rt \times Ci]} \quad (6)$$

PRINCIPLES OF OPERATION



V_I = Input Voltage at AIN
V_S = External Driving Source Voltage
R_S = Source Resistance
r_i = Input Resistance (MUX on Resistance)
C_i = Input Capacitance
V_C = Capacitance Charging Voltage

† Driving source requirements:

- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_S must be real at the input frequency.

Figure 37. Equivalent Input Circuit Including the Driving Source

maximum conversion throughput

For a supply voltage of 5 V, if the source impedance is less than 1 kΩ, and the ADC analog input capacitance Ci is less than 50 pF, this equates to a minimum sampling time tch(0.5 LSB) of 0.676 μs. Since the sampling time requires 12 SCLKs, the fastest SCLK frequency is 12/tch = 18 MHz.

The minimal total cycle time is given as:

$$tc = tcommand + tch + tconv + td(EOCH–CSL) = 4 \times \frac{1}{f(SCLK)} + 12 \times \frac{1}{f(SCLK)} + 1.6\ \mu s + 0.1\ \mu s$$

$$= 16 \times \frac{1}{18\ MHz} + 1.7\ \mu s = 2.59\ \mu s$$

This is equivalent to a maximum throughput of 386 KSPS. The throughput can be even higher with a smaller source impedance.

When source impedance is 100 Ω, the minimum sampling time becomes:

$$tch\ (1/2\ LSB) = Rt \times Ci \times In(8192) = 0.27\ \mu s$$

The maximum SCLK frequency possible is 12/tch = 44 MHz. Then a 20 MHz clock (maximum SCLK frequency for the TLC2554/2548) can be used. The minimal total cycle time is then reduced to:

$$tc = tcommand + tch + tconv + td(EOCH–CSL) = 4 \times \frac{1}{f(SCLK)} + 12 \times \frac{1}{f(SCLK)} + 1.6\ \mu s + 0.1\ \mu s$$

$$= 0.8\ \mu s + 1.6\ \mu s + 0.1\ \mu s = 2.5\ \mu s$$

The maximum throughput is 1/2.5 μs = 400 KSPS for this case.

PRINCIPLES OF OPERATION

power down calculations

$$i(AVERAGE) = (f_S/f_{SMAX}) \times i(ON) + (1–f_S/f_{SMAX}) \times i(OFF)$$

CASE 1: If V_{DD} = 3.3 V, auto power down, and an external reference is used:

$$f_S = 10\ kHz$$

$$f_{SMAX} = 200\ kHz$$

$$i(ON) = \sim 1\ mA \quad \textit{operating current and } i(OFF) = \sim 1\ \mu A \textit{ auto power-down current}$$

so

$$i(AVERAGE) = 0.05 \times 1000\ \mu A + 0.95 \times 1\ \mu A = 51\ \mu A$$

CASE 2: Now if software power down is used, another cycle is needed to shut it down.

$$f_S = 20\ kHz$$

$$f_{SMAX} = 200\ kHz$$

$$i(ON) = \sim 1\ mA \quad \textit{operating current and } i(OFF) = \sim 1\ \mu A \textit{ power-down current}$$

so

$$i(AVERAGE) = 0.1 \times 1000\ \mu A + 0.9 \times 1\ \mu A = 101\ \mu A$$

In reality this will be less since the second conversion never happened. It is only the additional cycle to shut down the ADC.

CASE 3: Now if the hardware power down is used.

$$f_S = 10\ kHz$$

$$f_{SMAX} = 200\ kHz$$

$$i(ON) = \sim 1\ mA \quad operating\ current\ and\ i(OFF) = \sim 1\ \mu A\ power\text{-}down\ current$$

so

$$i(AVERAGE) = 0.05 \times 1000\ \mu A + 0.95 \times 1\ \mu A = 51\ \mu A$$

difference between modes of conversion

The major difference between sweep mode (mode 10) and repeat sweep mode (mode 11) is that the sweep sequence ends after the FIFO is filled up to the programmed threshold. The repeat sweep can either dump the FIFO (by ignoring the FIFO content but simply reconfiguring the device) or read the FIFO and then repeat the conversions on the the same sequence of the channel as before.

FIFO reads are expected after the FIFO is filled up to the threshold in each case. Mode 10 – the device allows only FIFO read or CFR read or CFR write to be executed. Any conversion command is ignored. In the case of mode 11, in addition to the above commands, conversion commands are also executed , i.e. the FIFO is cleared and the sweep sequence is restarted.

Both single shot and repeat modes require selection of a channel after the device is configured for these modes. Single shot mode does not use the FIFO, but repeat mode does. When the device is operating in repeat mode, the FIFO can be dumped (by ignoring the FIFO content and simply reconfiguring the device) or the FIFO can be read and then the conversions repeated on the same channel as before. However, the channel has to be selected first before any conversion can be carried out. The devices can be programmed with the following sequences for operating in the different modes that use a FIFO:

PRINCIPLES OF OPERATION

difference between modes of conversion (continued)

REPEAT:

Configure FIFO Depth=4 /CONV Mode 01
Select Channel/
1st Conv ($\overline{CS}$ or $\overline{CSTART}$)
2nd Conv ($\overline{CS}$ or $\overline{CSTART}$)
3rd Conv ($\overline{CS}$ or $\overline{CSTART}$)
4th Conv ($\overline{CS}$ or $\overline{CSTART}$
FIFO READ 1
FIFO READ 2
FIFO READ 3
FIFO READ 4
Select Channel
1st Conv ($\overline{CS}$ or $\overline{CSTART}$)
2nd Conv ($\overline{CS}$ or $\overline{CSTART}$)
3rd Conv ($\overline{CS}$ or $\overline{CSTART}$)
4th Conv ($\overline{CS}$ or $\overline{CSTART}$

SWEEP:

Configure FIFO Depth=4 SEQ=1–2–3–4/CONV Mode 10
conv ch 1 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 2 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 3 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 4 ($\overline{CS}$/$\overline{CSTART}$
FIFO READ ch 1 result
FIFO READ ch 2 result
FIFO READ ch 3 result
FIFO READ ch 4 result
Configure (not required if same sweep sequence is to be used again)

REPEAT SWEEP:

Configure FIFO Depth=4 SWEEP SEQ=1-2-3-4/CONV Mode 11
conv ch 1 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 2 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 3 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 4 ($\overline{CS}$/$\overline{CSTART}$
FIFO READ ch 1 result
FIFO READ ch 2 result
FIFO READ ch 3 result
FIFO READ ch 4 result
conv ch 1 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 2 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 3 ($\overline{CS}$/$\overline{CSTART}$)
conv ch 4 ($\overline{CS}$/$\overline{CSTART}$

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2554ID	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC2554I
TLC2554ID.A	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC2554I
TLC2554IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y2554
TLC2554IPW.A	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y2554
TLC2558CDW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC2558C
TLC2558CDW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC2558C
TLC2558IDW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC2558I
TLC2558IDW.A	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLC2558I
TLC2558IPW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y2558
TLC2558IPW.A	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y2558
TLC2558IPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y2558
TLC2558IPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y2558

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

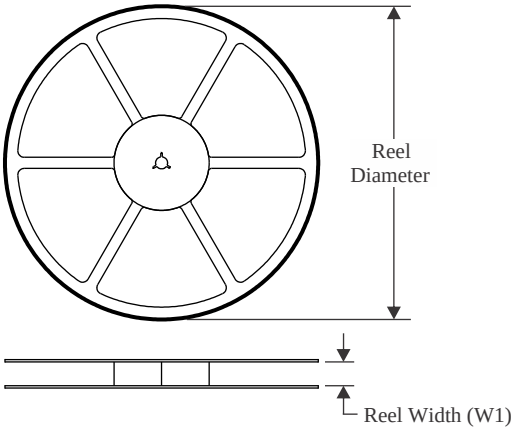
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

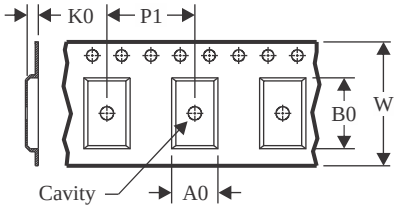
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

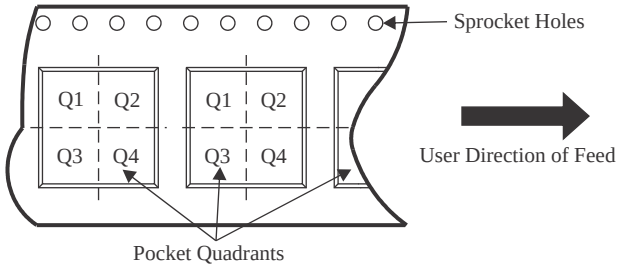


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

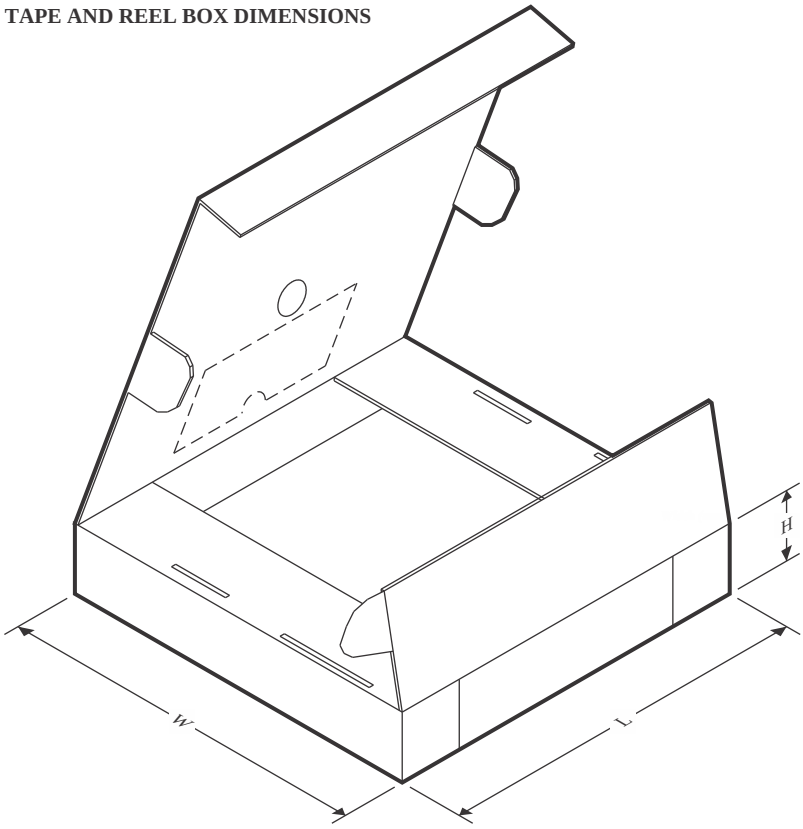
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2558IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

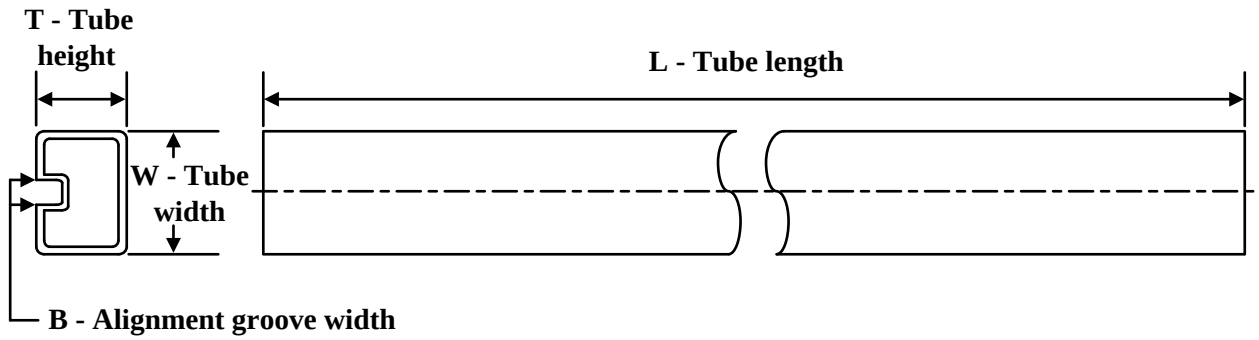
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2558IPWR	TSSOP	PW	20	2000	350.0	350.0	43.0

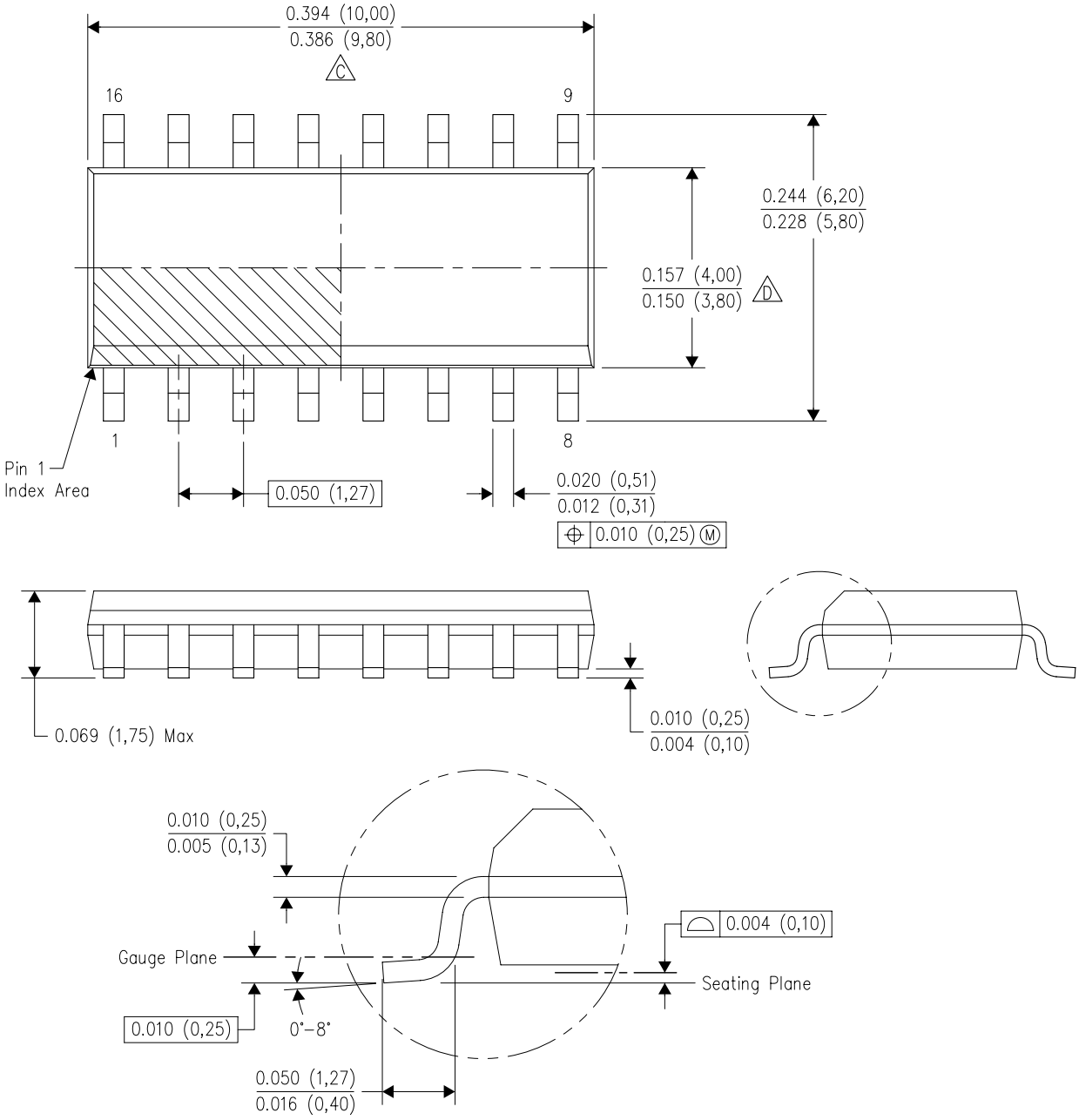
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC2554ID	D	SOIC	16	40	505.46	6.76	3810	4
TLC2554ID.A	D	SOIC	16	40	505.46	6.76	3810	4
TLC2554IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
TLC2554IPW.A	PW	TSSOP	16	90	530	10.2	3600	3.5
TLC2558CDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC2558CDW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC2558IDW	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC2558IDW.A	DW	SOIC	20	25	506.98	12.7	4826	6.6
TLC2558IPW	PW	TSSOP	20	70	530	10.2	3600	3.5
TLC2558IPW.A	PW	TSSOP	20	70	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



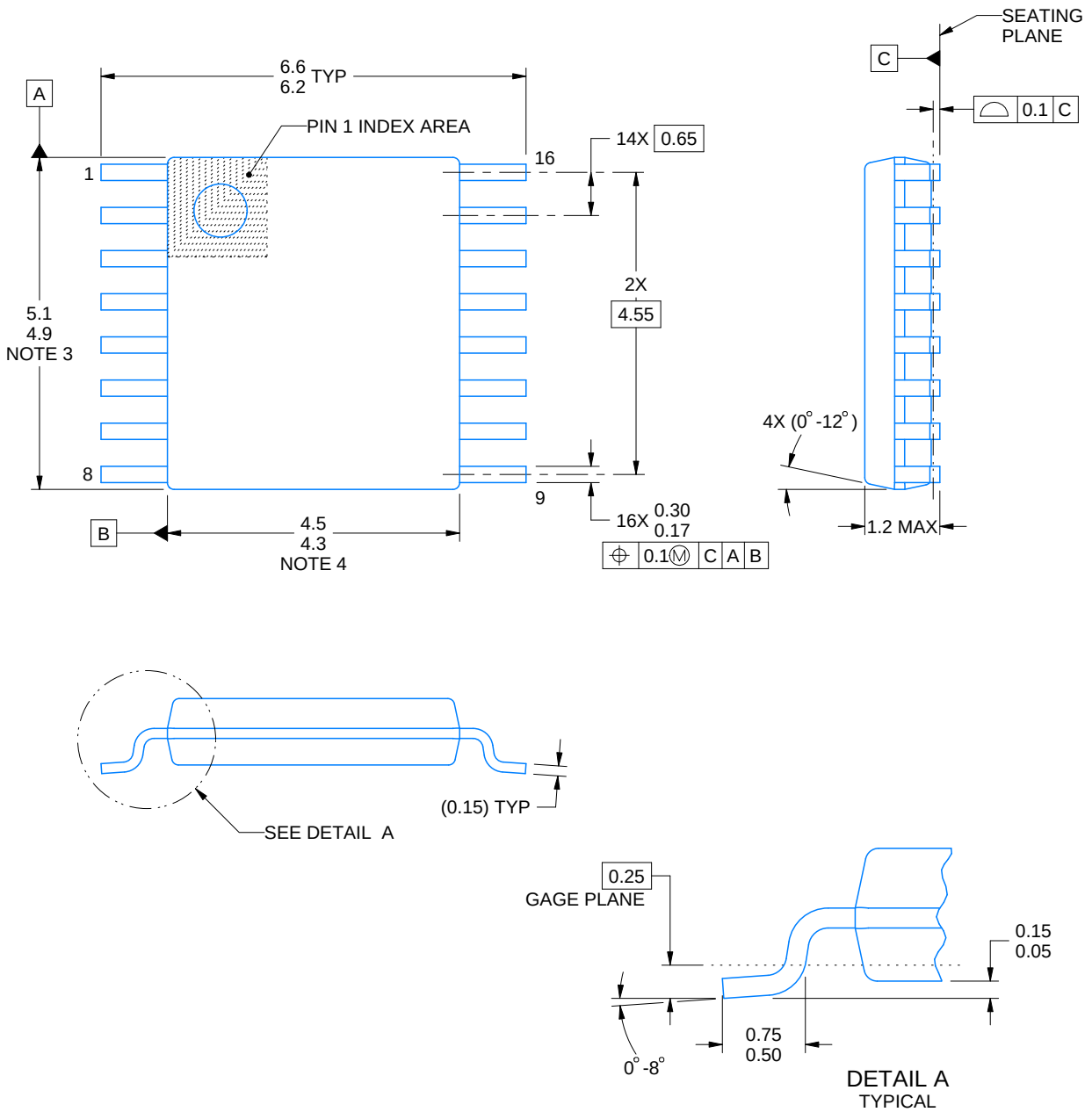
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

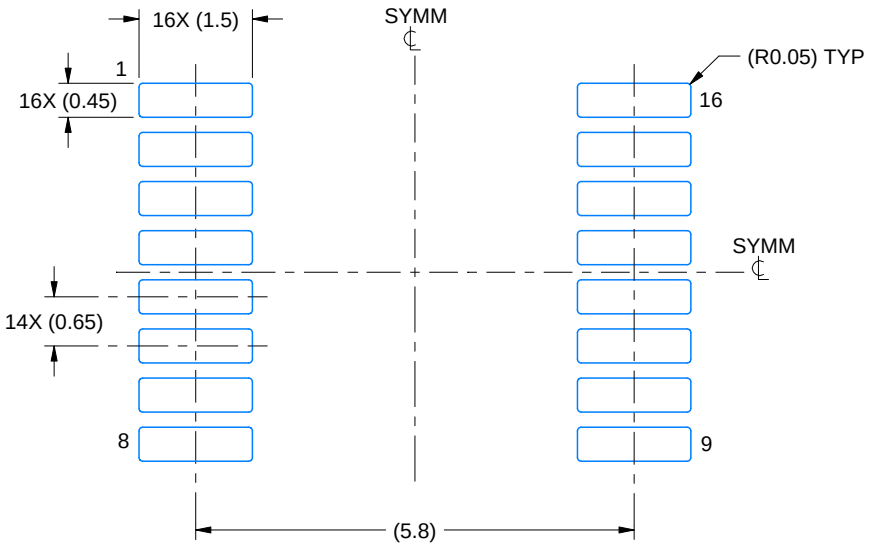
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



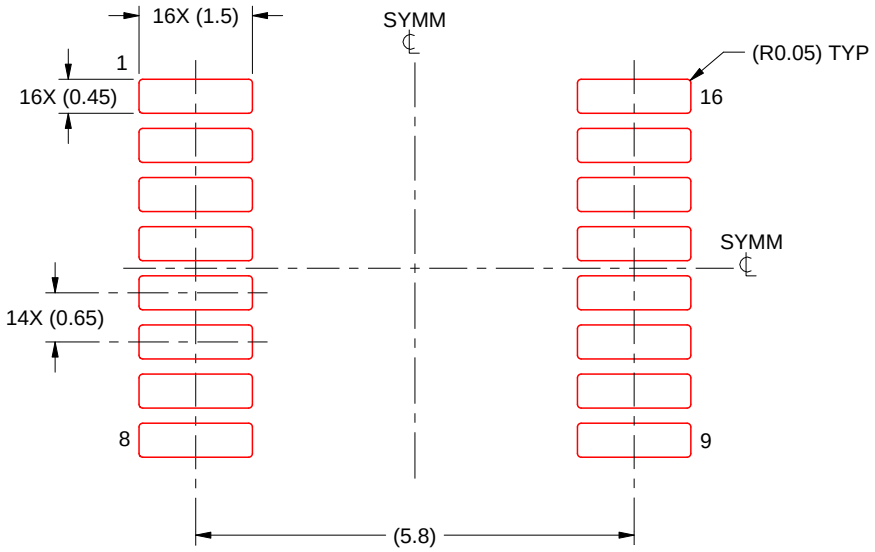
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

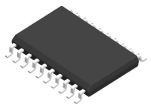


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

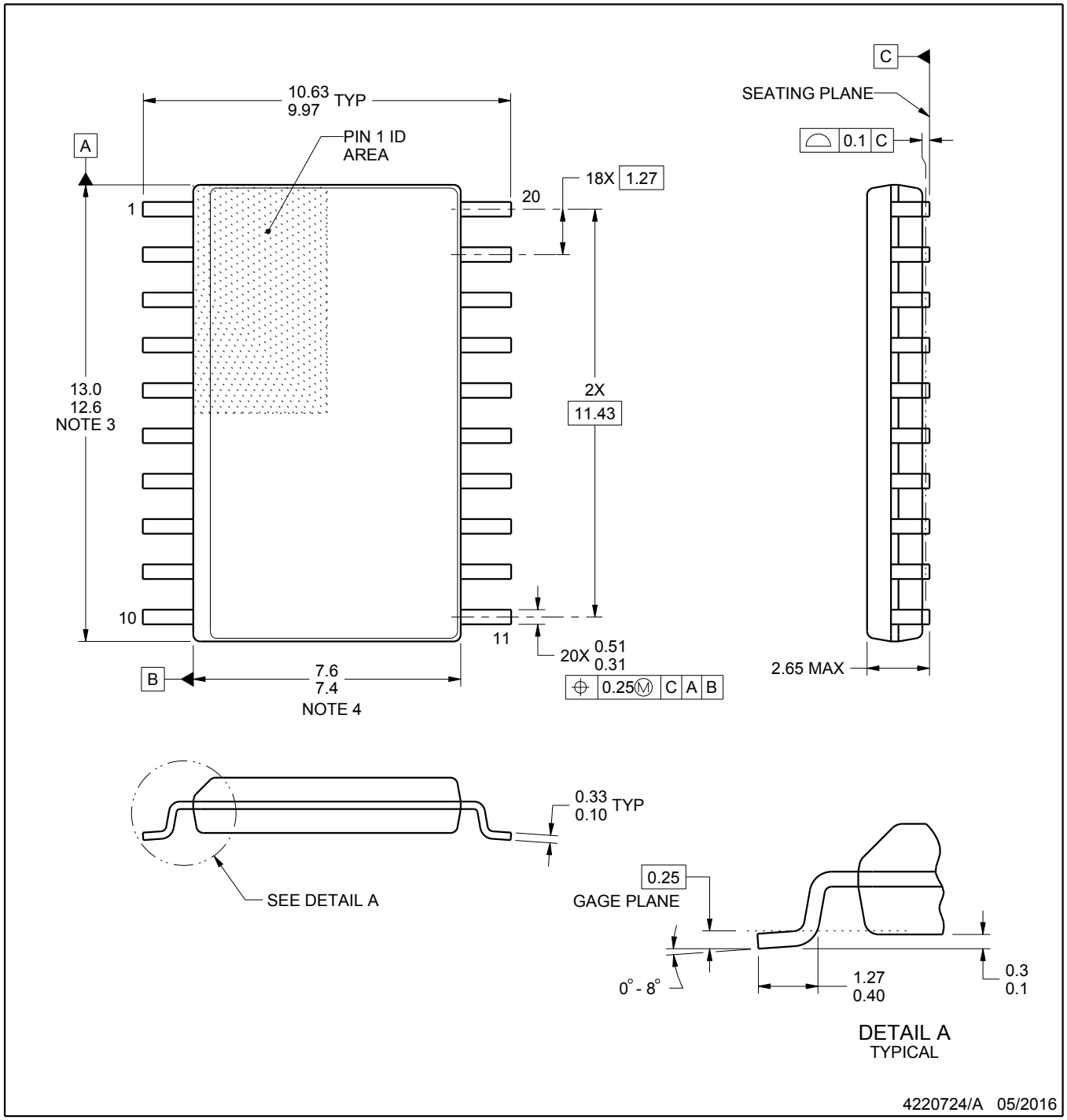


PACKAGE OUTLINE

DW0020A

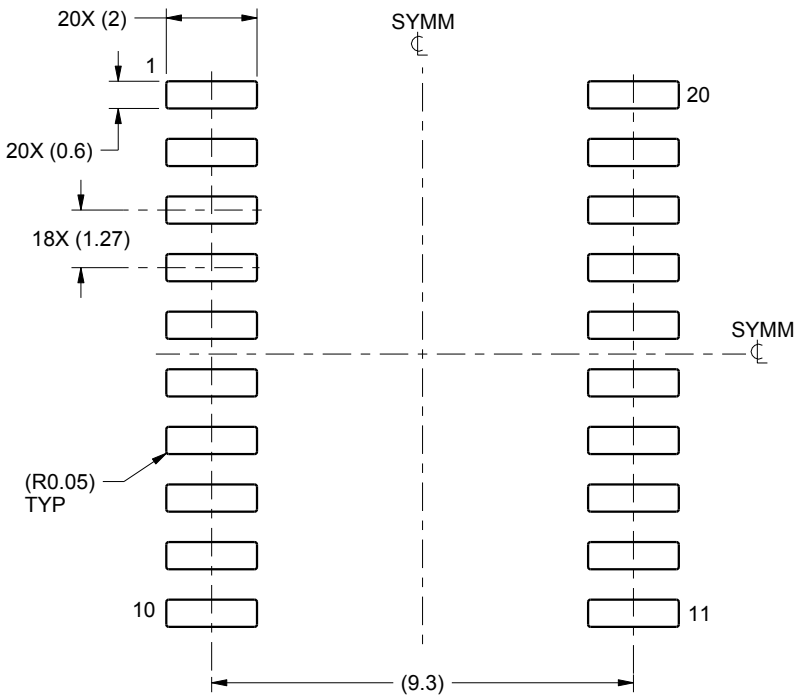
SOIC - 2.65 mm max height

SOIC

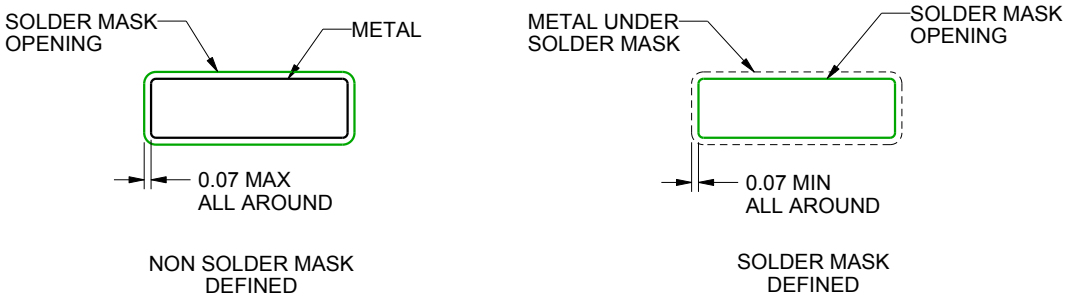


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

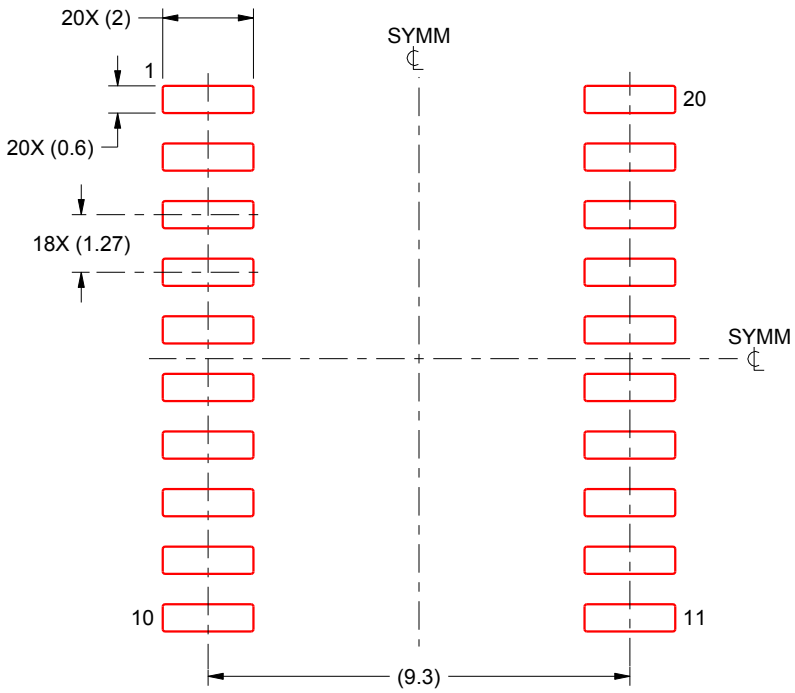


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

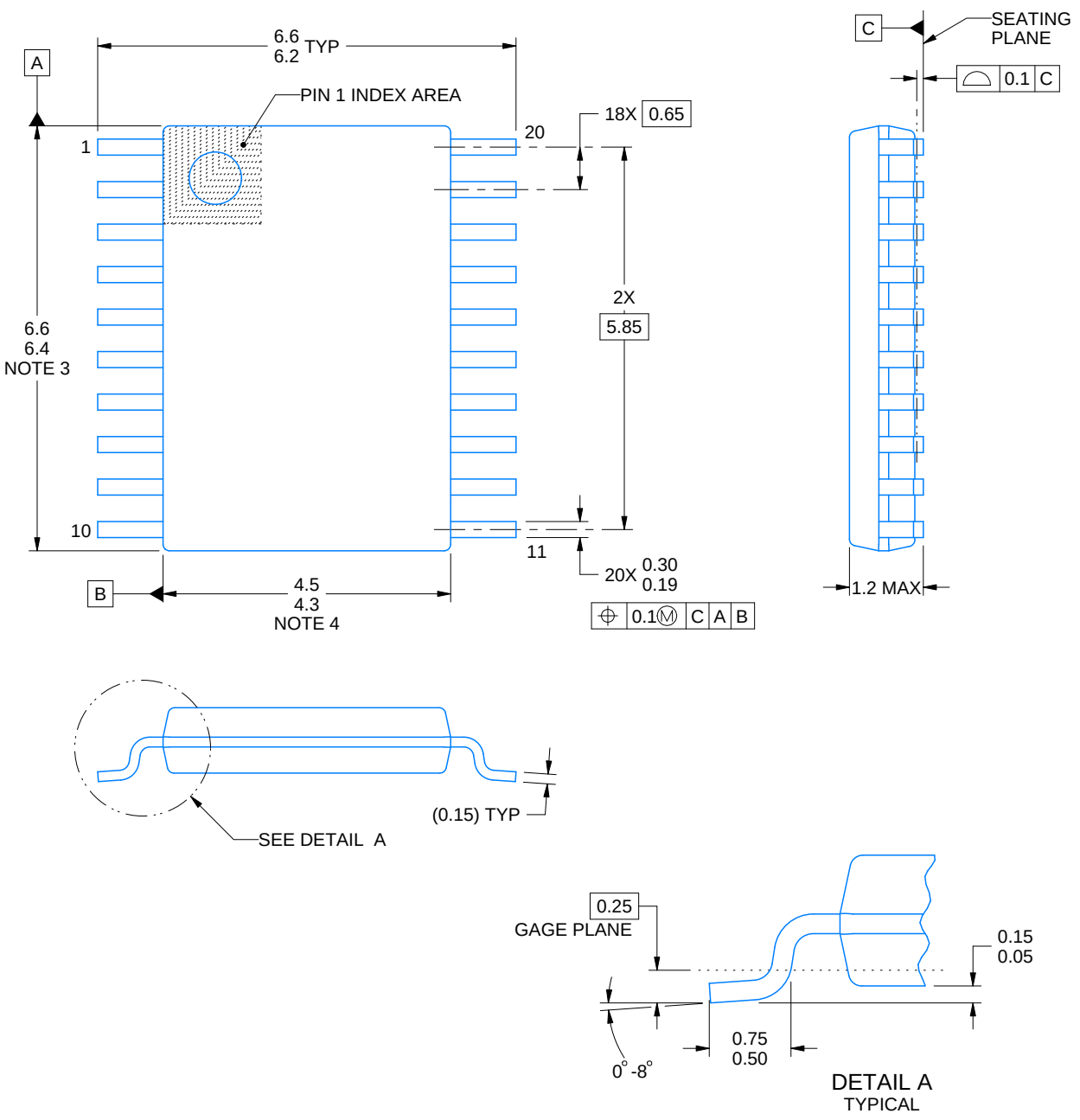
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

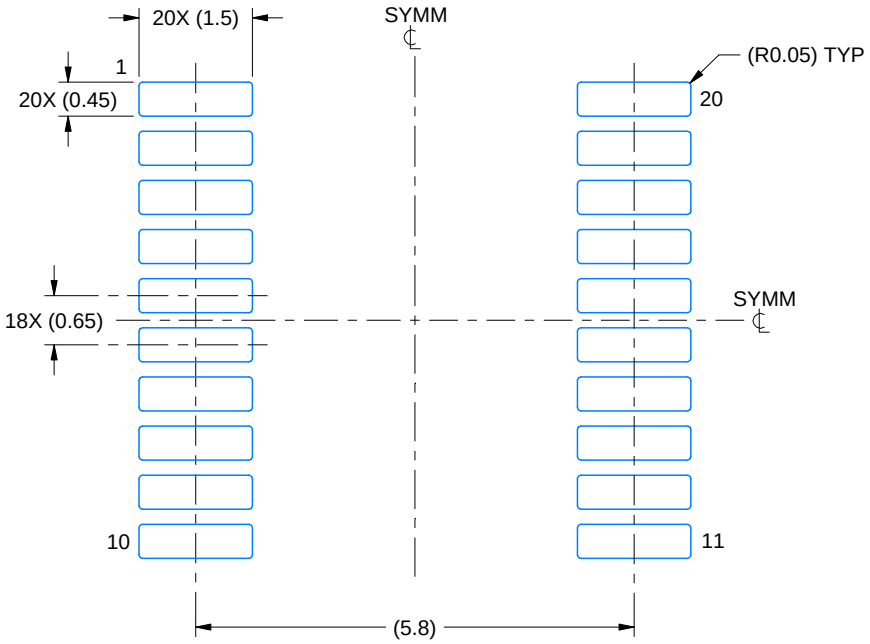
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



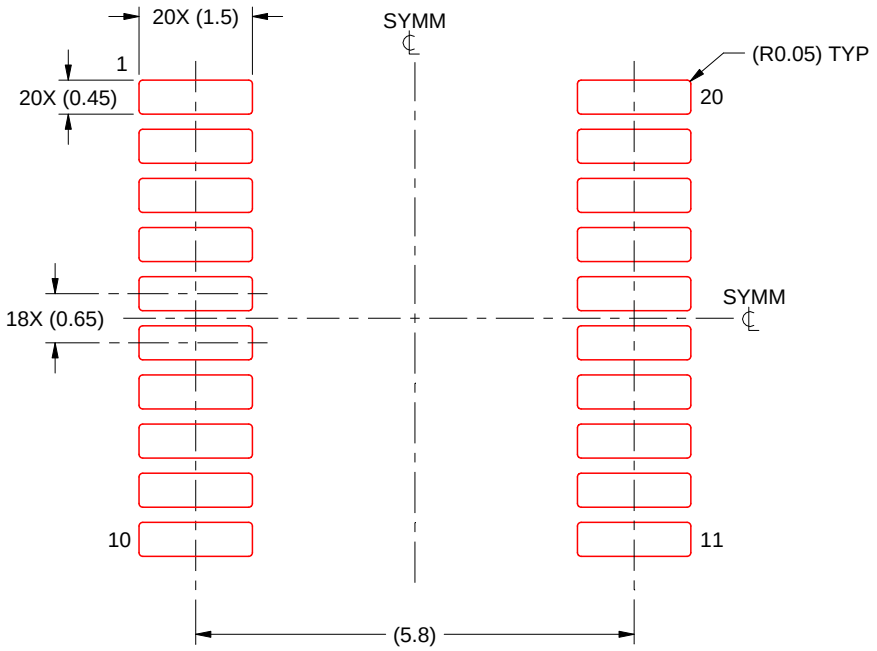
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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