TLC227x-Q1 Advanced, Rail-To-Rail, LinCMOS™ Operational Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design (TLC2272-Q1)
  - Documentation available to aid functional safety system design (TLC2272A-Q1)
- Output swing includes both supply rails
- Low noise: 9 nV/√Hz typical at f = 1 kHz
- Low input bias current: 1 pA typical
- Fully specified for both single-supply and split-supply operation
- Common-mode input voltage range includes negative rail
- High-gain bandwidth: 2.2 MHz typical
- High slew rate: 3.6 V/µs typical
- Low input offset voltage: 950 µV maximum at T_A = 25°C
- Macromodel included

2 Applications

- Body control module
- Battery management system
- Car audio
- DC/DC converter
- Electric power steering
- Engine control unit
- Gasoline engine
- Instrument clusters
- Inverter and motor control
- On-board charger
- Telematics control unit
- Transmission control
- White goods (refrigerators, washing machines)

3 Description

The TLC227x-Q1 are dual and quad, LinCMOS™ operational amplifiers. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x-Q1 family offers 2 MHz of bandwidth and 3 V/µs of slew rate for higher-speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS op amps. The TLC227x-Q1 has a noise voltage of 9 nV/√Hz—two times lower than competitive solutions.

The TLC227x-Q1, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

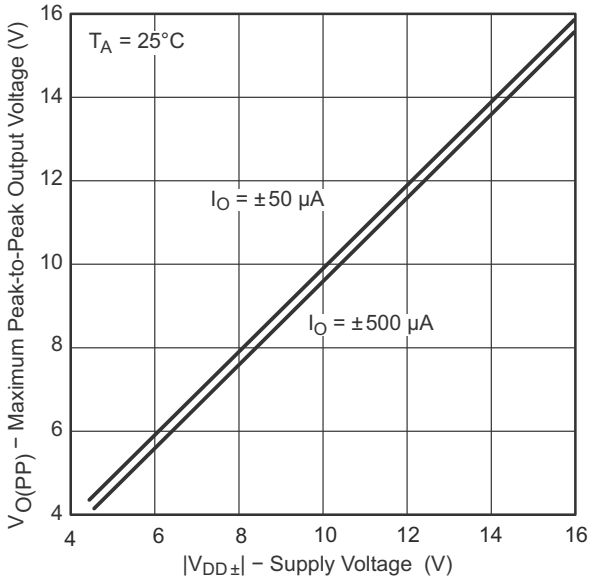
For precision applications, the TLC227xA-Q1 family is available with a maximum input offset voltage of 950 µV. This family is fully characterized at 5 V and ±5 V.

These devices offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows the TLC227x-Q1 to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432-Q1 and TLV2442-Q1. All the parameters of the TLC227x-Q1 family enables these devices to be applicable in most automotive applications.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TLC2272-Q1, TLC2272A-Q1	SOIC (8)	4.90 mm x 3.91 mm
	TSSOP (8)	3.00 mm × 4.40 mm
TLC2274-Q1, TLC2274A-Q1	SOIC (14)	8.65 mm x 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Maximum Peak-To-Peak Output Voltage vs Supply Voltage

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (March 2016) to Revision G (August 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added functional safety information to *Features* bullets	1

Changes from Revision E (January 2012) to Revision F (March 2016)	Page
• Added *Pin Configuration and Functions* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout*section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added *ESD ratings* table	4

Changes from Revision D (March 2009) to Revision E (January 2012)	Page
• Deleted *ESD ratings* table	4

5 Pin Configuration and Functions

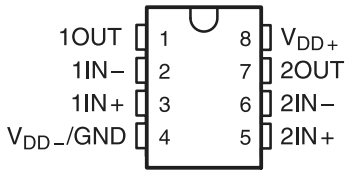


Figure 5-1. TLC2272-Q1 and TLC2272A-Q1: D (8-Pin SOIC) or PW (8-Pin TSSOP) Packages, Top View

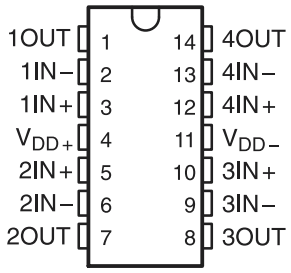


Figure 5-2. TLC2274-Q1 and TLC2274A-Q1: D (14-Pin SOIC) or PW (14-Pin TSSOP) Packages, Top View

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	TLC2272-Q1, TLC2272A-Q1	TLC2274-Q1, TLC2274A-Q1		
1IN+	3	3	Input	Noninverting input, channel 1
1IN–	2	2	Input	Inverting input, channel 1
1OUT	1	1	Output	Output, channel 1
2IN+	5	5	Input	Noninverting input, channel 2
2IN–	6	6	Input	Inverting input, channel 2
2OUT	7	7	Ouput	Output, channel 2
3IN+	—	10	Input	Noninverting input, channel 3
3IN–	—	9	Input	Inverting input, channel 3
3OUT	—	8	Output	Output, channel 3
4IN+	—	12	Input	Noninverting input, channel 4
4IN–	—	13	Input	Inverting input, channel 4
4OUT	—	14	Output	Output, channel 4
V_{DD+}	8	4	Input	Positive (highest) supply
$V_{DD–}$	4	11	Input	Negative (lowest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, $V_{DD}+$(2)			8	V
$V_{DD}–$(2)		–8		V
Differential input voltage, V_{ID} (3)			±16	V
Input voltage, V_I(any input)(2)		$V_{DD–}$ − 0.3	V_{DD+}	V
Input current, I_I (any input)			±5	mA
Output current, I_O			±50	mA
Total current into V_{DD+}			±50	mA
Total current out of $V_{DD–}$			±50	mA
Duration of short-circuit current at (or below) 25°C(4)		Unlimited		
Operating free-air temperature range, T_A		–40	125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or PW package		260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.3*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and $V_{DD–}$.
(3) Differential voltages are at IN+ with respect to IN–. Excessive current will flow if input is brought below $V_{DD–}$ − 0.3 V.
(4) The output can be shorted to either supply. Temperature or supply voltages must be limited so that the maximum dissipation rating is not exceeded.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{DD±}$	Supply voltage	±2.2	±8	V
V_I	Input voltage	$V_{DD–}$	V_{DD+} −1.5	V
V_{IC}	Common-mode input voltage	$V_{DD–}$	V_{DD+} −1.5	V
T_A	Operating free-air temperature	−40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLC2272-Q1, TLC2272A-Q1		TLC2274-Q1, TLC2274A-Q1		UNIT
		D (SOIC)	PW (TSSOP)	D (SOIC)	PW (TSSOP)	
		8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.6	175.8	83.8	111.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.8	58.8	43.2	41.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.9	104.3	38.4	54.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.3	5.9	9.4	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	55.4	102.3	38.1	53.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_{DD} = 5 V (TLC2272-Q1 and TLC2272A-Q1)

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	TLC2272-Q1	T_A = 25°C		300	2500	µV
			TLC2272A-Q1			300	950	
			TLC2272-Q1	Full Range[1]			3000	
			TLC2272A-Q1				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift[2]	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		0.5	60	pA
				Full Range[1]			800	
I_{IB}	Input bias current	V_{IC} = 0 V, $V_{DD\pm}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		1	60	pA
				Full Range[1]			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\lvert V_{IO} \rvert \le$ 5 mV		T_A = 25°C	–0.3	2.5	4	V
				Full Range[1]	0	2.5	3.5	
V_{OH}	High-level output voltage	I_{OH} = −20 µA				4.99		V
		I_{OH} = −200 µA		T_A = 25°C	4.85	4.93		
				Full Range[1]	4.85			
		I_{OH} = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range[1]	4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA			0.01		V
			I_{OL} = 500 µA	T_A = 25°C		0.09	0.15	
				Full Range[1]			0.15	
			I_{OL} = 5 mA	T_A = 25°C		0.9	1.5	
				Full Range[1]			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ[3]	T_A = 25°C	10	35		V/mV
				Full Range[1]	10			
			R_L = 1 MΩ[3]			175		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		T_A = 25°C	70	75		dB
				Full Range[1]	70			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD} / 2, no load		T_A = 25°C	80	95		dB
				Full Range[1]	80			

6.5 Electrical Characteristics: V_{DD} = 5 V (TLC2272-Q1 and TLC2272A-Q1) (continued)

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	V_O = 2.5 V, no load	T_A = 25°C		2.2	3	mA
			Full Range[1]			3	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ[3], C_L = 100 pF[3]	T_A = 25°C	2.3	3.6		V/μs
			Full Range[1]	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz			50		nV/√Hz
		f = 1 kHz			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			1		μV
		f = 0.1 Hz to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ[3]	A_V = 1		0.0013%		
			A_V = 10		0.004%		
			A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ[3], C_L = 100 pF[3]			2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ[3], C_L = 100 pF[3]			1		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ[3], Step = 0.5 V to 2.5 V, C_L = 100 pF[3]	To 0.1%		1.5		μs
			To 0.01%		2.6		
φ_m	Phase margin at unity gain	R_L = 10 kΩ[3], C_L = 100 pF[3]			50°		
	Gain margin	R_L = 10 kΩ[3], C_L = 100 pF[3]			10		dB

(1) T_A = –40°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 0 V.

6.6 Electrical Characteristics: $V_{DD±}$ = ±5 V (TLC2272-Q1 and TLC2272A-Q1)

at specified free-air temperature, $V_{DD±}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	TLC2272-Q1	T_A = 25°C		300	2500	μV
			TLC2272A-Q1			300	950	
			TLC2272-Q1	Full Range[1]			3000	
			TLC2272A-Q1				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				2		μV/°C
	Input offset voltage long-term drift[2]	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				0.002		μV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		0.5	60	pA
				Full Range[1]			800	
I_{IB}	Input bias current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		1	60	pA
				Full Range[1]			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\lvert V_{IO} \rvert \le$ 5 mV		T_A = 25°C	–5.3	0	4	V
				Full Range[1]	–5	0	3.5	
V_{OM+}	Maximum positive peak output voltage	I_O = −20 μA				4.99		V
		I_O = −200 μA		T_A = 25°C	4.85	4.93		
				Full Range[1]	4.85			
		I_O = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range[1]	4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V	I_O = 50 μA			–4.99		V
			I_O = 500 μA	T_A = 25°C	–4.85	–4.91		
				Full Range[1]	–4.85			
			I_O = 5 mA	T_A = 25°C	–3.5	–4.1		
				Full Range[1]	–3.5			

6.6 Electrical Characteristics: $V_{DD±}$ = ±5 V (TLC2272-Q1 and TLC2272A-Q1) (continued)

at specified free-air temperature, $V_{DD±}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	T_A = 25°C	20	50		V/mV
				Full Range[1]	20			
			R_L = 1 MΩ			300		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = –5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C	75	80		dB
				Full Range[1]	75			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD+} = 2.2 V to ±8 V, V_{IC} = 0 V, no load		T_A = 25°C	80	95		dB
				Full Range[1]	80			
I_{DD}	Supply current	V_O = 0 V, no load		T_A = 25°C		2.4	3	mA
				Full Range[1]			3	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF		T_A = 25°C	2.3	3.6		V/µs
				Full Range[1]	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		µV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = ±2.3, f = 20 kHz, R_L = 10 kΩ		A_V = 1		0.0011%		
				A_V = 10		0.004%		
				A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF				2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF				0.54		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ, Step = –2.3 V to 2.3 V, C_L = 100 pF		To 0.1%		1.5		µs
				To 0.01%		3.2		
$φ_m$	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF				52°		
	Gain margin	R_L = 10 kΩ, C_L = 100 pF				10		dB

(1) T_A = –40°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6.7 Electrical Characteristics: V_{DD} = 5 V (TLC2274-Q1 and TLC2274A-Q1)

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω	TLC2274-Q1	T_A = 25°C		300	2500	µV
			TLC2274A-Q1			300	950	
			TLC2274-Q1	Full Range[1]			3000	
			TLC2274A-Q1				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift[2]	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		0.5	60	pA
				Full Range[1]			800	
I_{IB}	Input bias current	V_{IC} = 0 V, $V_{DD±}$ = ±2.5 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		1	60	pA
				Full Range[1]			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\|V_{IO}\|$ ≤ 5 mV		T_A = 25°C	–0.3	2.5	4	V
				Full Range[1]	0	2.5	3.5	
V_{OH}	High-level output voltage	I_{OH} = −20 µA				4.99		V
		I_{OH} = −200 µA		T_A = 25°C	4.85	4.93		
				Full Range[1]	4.85			
		I_{OH} = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range[1]	4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 50 µA			0.01		V
			I_{OL} = 500 µA	T_A = 25°C		0.09	0.15	
				Full Range[1]			0.15	
			I_{OL} = 5 mA	T_A = 25°C		0.9	1.5	
				Full Range[1]			1.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ[3]	T_A = 25°C	10	35		V/mV
				Full Range[1]	10			
			R_L = 1 MΩ[3]			175		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				140		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		T_A = 25°C	70	75		dB
				Full Range[1]	70			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.4 V to 16 V, V_{IC} = V_{DD} / 2, no load		T_A = 25°C	80	95		dB
				Full Range[1]	80			
I_{DD}	Supply current	V_O = 2.5 V, no load		T_A = 25°C		4.4	6	mA
				Full Range[1]			6	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ[3], C_L = 100 pF[3]		T_A = 25°C	2.3	3.6		V/µs
				Full Range[1]	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz				50		nV/√Hz
		f = 1 kHz				9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz				1		µV
		f = 0.1 Hz to 10 Hz				1.4		
I_n	Equivalent input noise current					0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 10 kΩ[3]		A_V = 1		0.0013%		
				A_V = 10		0.004%		
				A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ[3], C_L = 100 pF[3]				2.18		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, A_V = 1, R_L = 10 kΩ[3], C_L = 100 pF[3]				1		MHz

6.7 Electrical Characteristics: V_{DD} = 5 V (TLC2274-Q1 and TLC2274A-Q1) (continued)

at specified free-air temperature, V_{DD} = 5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_s	Settling time	A_V = –1, R_L = 10 kΩ(3), Step = 0.5 V to 2.5 V, C_L = 100 pF(3)	To 0.1%		1.5		µs
			To 0.01%		2.6		
φ_m	Phase margin at unity gain	R_L = 10 kΩ(3), C_L = 100 pF(3)			50°		
	Gain margin	R_L = 10 kΩ(3), C_L = 100 pF(3)			10		dB

(1) T_A = –40°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) Referenced to 0 V.

6.8 Electrical Characteristics: $V_{DD±}$ = ±5 V (TLC2274-Q1 and TLC2274A-Q1)

at specified free-air temperature, $V_{DD±}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω	TLC2274-Q1	T_A = 25°C		300	2500	µV
			TLC2274A-Q1			300	950	
			TLC2274-Q1	Full Range(1)			3000	
			TLC2274A-Q1				1500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				2		µV/°C
	Input offset voltage long-term drift(2)	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω				0.002		µV/mo
I_{IO}	Input offset current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		0.5	60	pA
				Full Range(1)			800	
I_{IB}	Input bias current	V_{IC} = 0 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C		1	60	pA
				Full Range(1)			800	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω; $\lvert V_{IO} \rvert \le$ 5 mV		T_A = 25°C	–5.3	0	4	V
				Full Range(1)	–5	0	3.5	
V_{OM+}	Maximum positive peak output voltage	I_O = −20 µA				4.99		V
		I_O = −200 µA		T_A = 25°C	4.85	4.93		
				Full Range(1)	4.85			
		I_O = −1 mA		T_A = 25°C	4.25	4.65		
				Full Range(1)	4.25			
V_{OM-}	Maximum negative peak output voltage	V_{IC} = 0 V	I_O = 50 µA			–4.99		V
			I_O = 500 µA	T_A = 25°C	–4.85	–4.91		
				Full Range(1)	–4.85			
			I_O = 5 mA	T_A = 25°C	–3.5	–4.1		
				Full Range(1)	–3.5			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V	R_L = 10 kΩ	T_A = 25°C	20	50		V/mV
				Full Range(1)	20			
			R_L = 1 MΩ			300		
r_{id}	Differential input resistance					10^{12}		Ω
r_i	Common-mode input resistance					10^{12}		Ω
c_i	Common-mode input capacitance	f = 10 kHz, P package				8		pF
z_o	Closed-loop output impedance	f = 1 MHz, A_V = 10				130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = –5 V to 2.7 V, V_O = 0 V, R_S = 50 Ω		T_A = 25°C	75	80		dB
				Full Range(1)	75			
k_{SVR}	Supply-voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD+} = 2.2 V to ±8 V, V_{IC} = 0 V, no load		T_A = 25°C	80	95		dB
				Full Range(1)	80			
I_{DD}	Supply current	V_O = 0 V, no load		T_A = 25°C		4.8	6	mA
				Full Range(1)			6	

6.8 Electrical Characteristics: $V_{DD±}$ = ±5 V (TLC2274-Q1 and TLC2274A-Q1) (continued)

at specified free-air temperature, $V_{DD±}$ = ±5 V; T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	T_A = 25°C	2.3	3.6		V/μs
			Full Range[1]	1.7			
V_n	Equivalent input noise voltage	f = 10 Hz			50		nV/√Hz
		f = 1 kHz			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz			1		μV
		f = 0.1 Hz to 10 Hz			1.4		
I_n	Equivalent input noise current				0.6		fA/√Hz
THD+N	Total harmonic distortion + noise	V_O = ±2.3, f = 20 kHz, R_L = 10 kΩ	A_V = 1		0.0011%		
			A_V = 10		0.004%		
			A_V = 100		0.03%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ, C_L = 100 pF			2.25		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 4.6 V, A_V = 1, R_L = 10 kΩ, C_L = 100 pF			0.54		MHz
t_s	Settling time	A_V = –1, R_L = 10 kΩ, Step = –2.3 V to 2.3 V, C_L = 100 pF	To 0.1%		1.5		μs
			To 0.01%		3.2		
φ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF			52°		
	Gain margin	R_L = 10 kΩ, C_L = 100 pF			10		dB

(1) T_A = –40°C to 125°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

6.9 Typical Characteristics

Table 6-1. Table of Graphs

			FIGURE(1)
V_{IO}	Input offset voltage	Distribution	1, 2, 3, 4
		vs Common-mode voltage	5, 6
α_{VIO}	Input offset voltage temperature coefficient	Distribution	7, 8, 9, 10 (2)
I_{IB} /I_{IO}	Input bias and input offset current	vs Free-air temperature	11 (2)
V_I	Input voltage	vs Supply voltage	12
		vs Free-air temperature	13 (2)
V_{OH}	High-level output voltage	vs High-level output current	14 (2)
V_{OL}	Low-level output voltage	vs Low-level output current	15, 16 (2)
V_{OM+}	Maximum positive peak output voltage	vs Output current	17 (2)
V_{OM-}	Maximum negative peak output voltage	vs Output current	18 (2)
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	19
I_{OS}	Short-circuit output current	vs Supply voltage	20
		vs Free-air temperature	21 (2)
V_O	Output voltage	vs Differential input voltage	22, 23
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	24
	Large-signal differential voltage amplification and phase margin	vs Frequency	25, 26
	Large-signal differential voltage amplification	vs Free-air temperature	27 (2), 28 (2)
z_0	Output impedance	vs Frequency	29, 30
CMRR	Common-mode rejection ratio	vs Frequency	31
		vs Free-air temperature	32
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	33, 34
		vs Free-air temperature	35 (2)
I_{DD}	Supply current	vs Supply voltage	36 (2), 37 (2)
		vs Free-air temperature	38 (2), 39 (2)
SR	Slew rate	vs Load Capacitance	40
		vs Free-air temperature	41 (2)
V_O	Inverting large-signal pulse response		42, 43
	Voltage-follower large-signal pulse response		44, 45
	Inverting small-signal pulse response		46, 47
	Voltage-follower small-signal pulse response		48, 49
V_n	Equivalent input noise voltage	vs Frequency	50, 51
	Noise voltage over a 10-second period		52
	Integrated noise voltage	vs Frequency	53
THD+N	Total harmonic distortion + noise	vs Frequency	54
	Gain-bandwidth product	vs Supply voltage	55
		vs Free-air temperature	56 (2)
φ_m	Phase margin	vs Load capacitance	57
	Gain margin	vs Load capacitance	58

(1) For all graphs where V_{DD} = 5 V, all loads are referenced to 2.5 V.
(2) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

6.9 Typical Characteristics (continued)

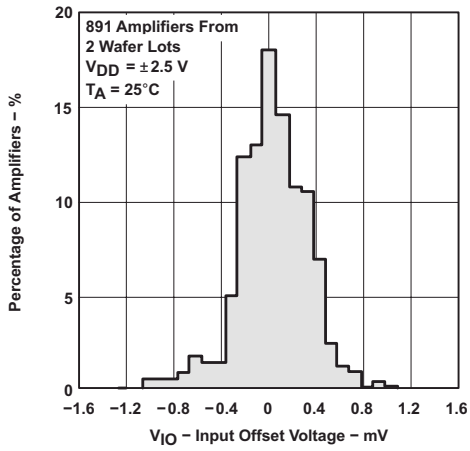


Figure 6-1. Distribution of TLC2272-Q1 Input Offset Voltage

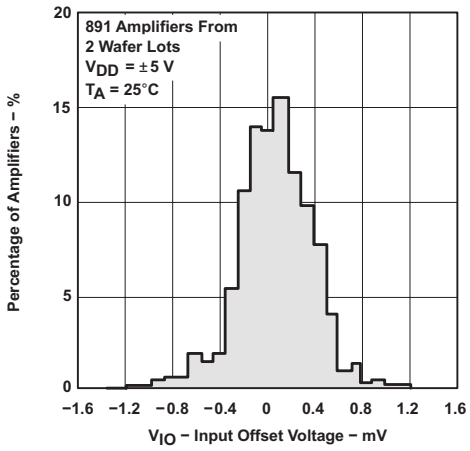


Figure 6-2. Distribution of TLC2272-Q1 Input Offset Voltage

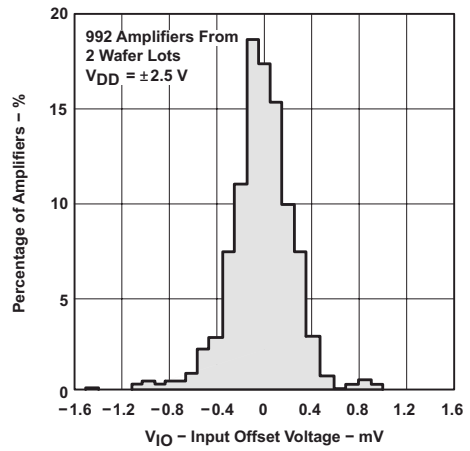


Figure 6-3. Distribution of TLC2274-Q1 Input Offset Voltage

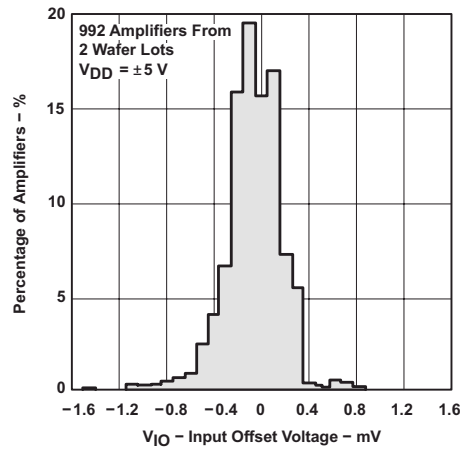


Figure 6-4. Distribution of TLC2274-Q1 Input Offset Voltage

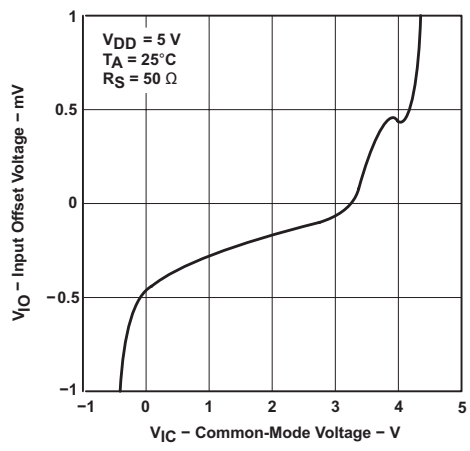


Figure 6-5. Input Offset Voltage vs Common-Mode Voltage

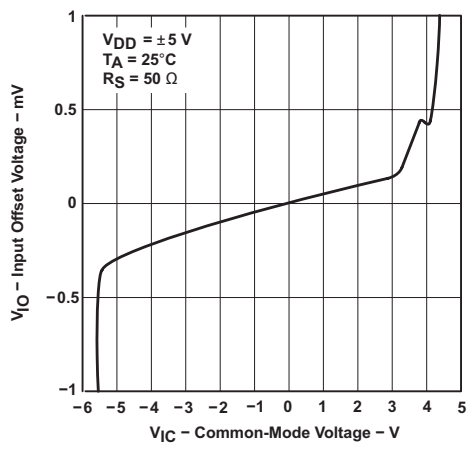


Figure 6-6. Input Offset Voltage vs Common-Mode Voltage

6.9 Typical Characteristics (continued)

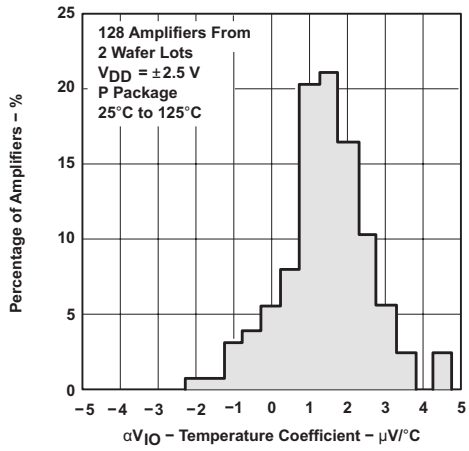


Figure 6-7. Distribution of TLC2272-Q1 vs Input Offset Voltage Temperature Coefficient

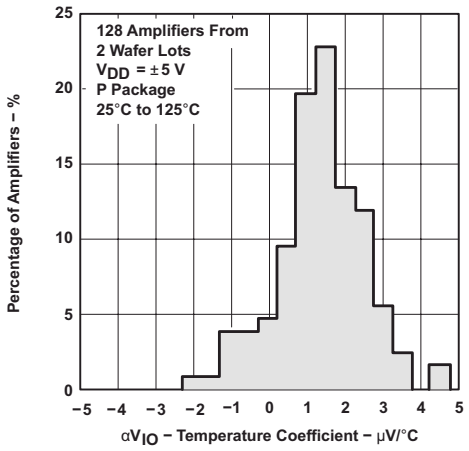


Figure 6-8. Distribution of TLC2272-Q1 vs Input Offset Voltage Temperature Coefficient

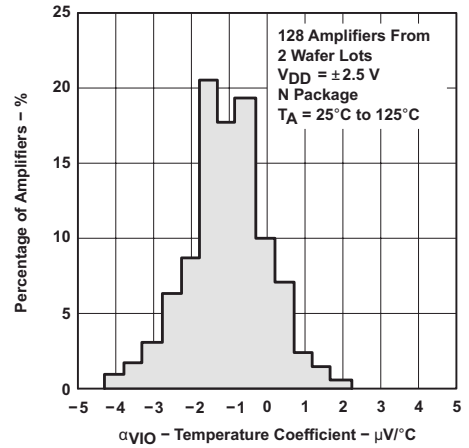


Figure 6-9. Distribution of TLC2274-Q1 vs Input Offset Voltage Temperature Coefficient

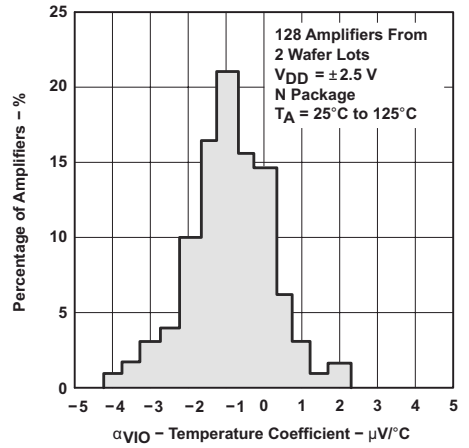


Figure 6-10. Distribution of TLC2274-Q1 vs Input Offset Voltage Temperature Coefficient

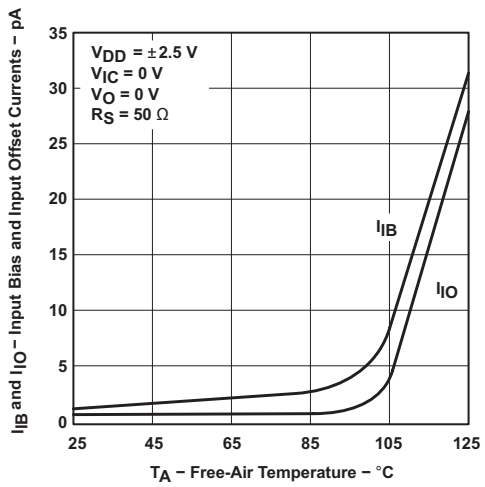


Figure 6-11. Input Bias and Input Offset Current vs Free-Air Temperature

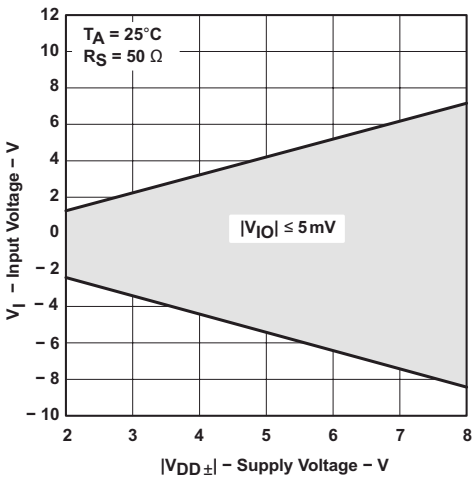


Figure 6-12. Input Voltage vs Supply Voltage

6.9 Typical Characteristics (continued)

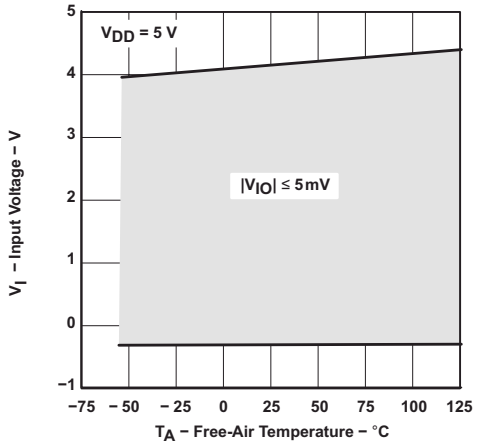


Figure 6-13. Input Voltage vs Free-Air Temperature

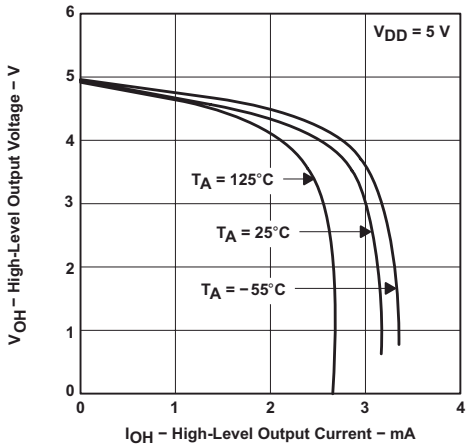


Figure 6-14. High-Level Output Voltage vs High-Level Output Current

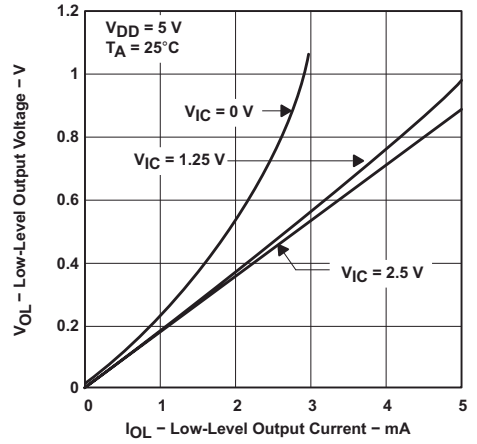


Figure 6-15. Low-Level Output Voltage vs Low-Level Output Current

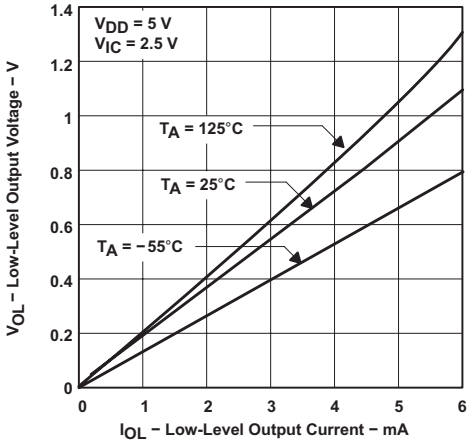


Figure 6-16. Low-Level Output Voltage vs Low-Level Output Current

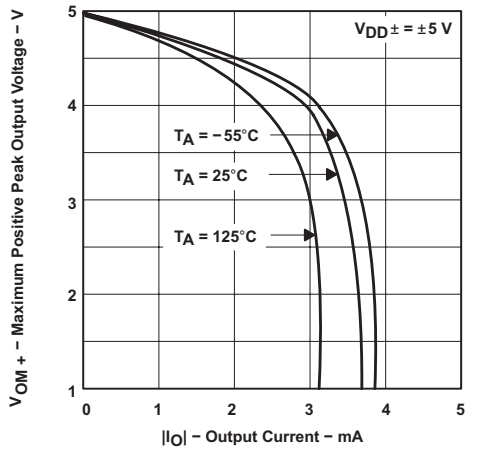


Figure 6-17. Maximum Positive Peak Output Voltage vs Output Current

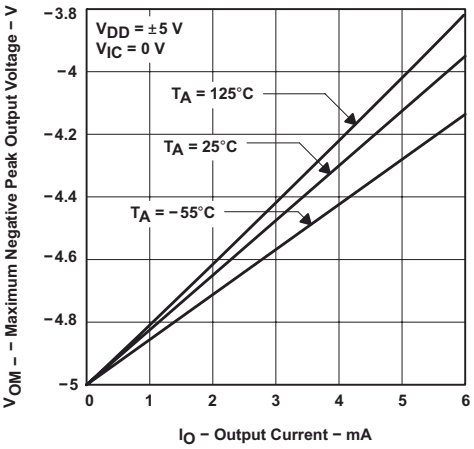


Figure 6-18. Maximum Positive Peak Output Voltage vs Output Current

6.9 Typical Characteristics (continued)

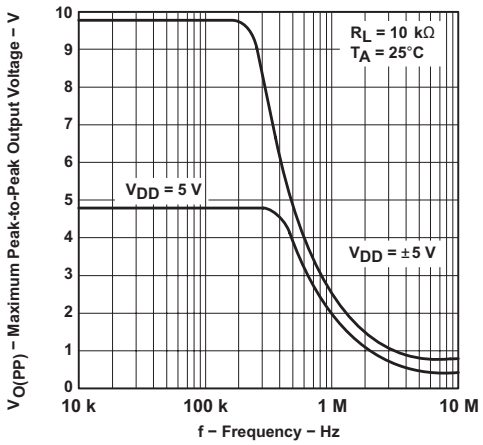


Figure 6-19. Maximum Peak-to-Peak Output Voltage vs Frequency

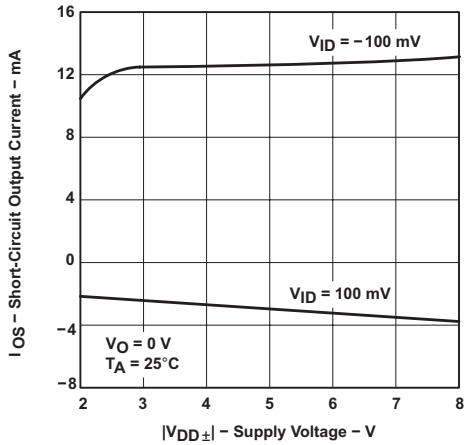


Figure 6-20. Short-Circuit Output Current vs Supply Voltage

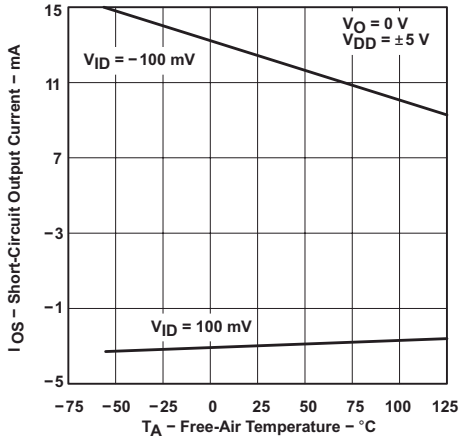


Figure 6-21. Short-Circuit Output Current vs Free-Air Temperature

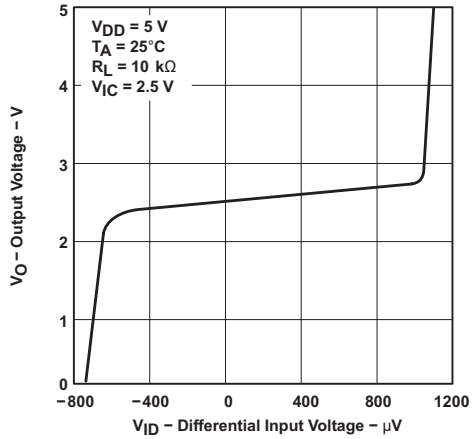


Figure 6-22. Output Voltage vs Differential Input Voltage

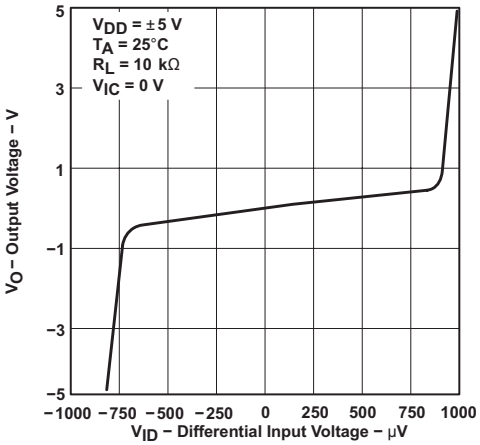


Figure 6-23. Output Voltage vs Differential Input Voltage

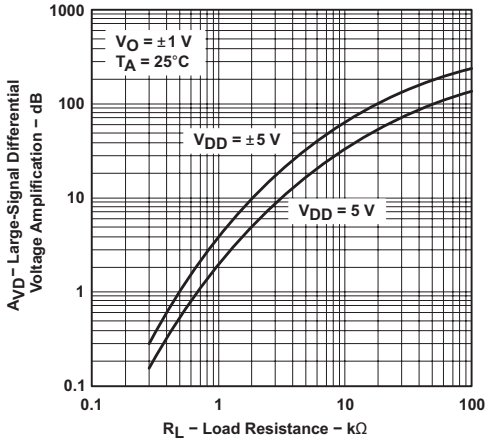


Figure 6-24. Large-Signal Differential Voltage Amplification vs Load Resistance

6.9 Typical Characteristics (continued)

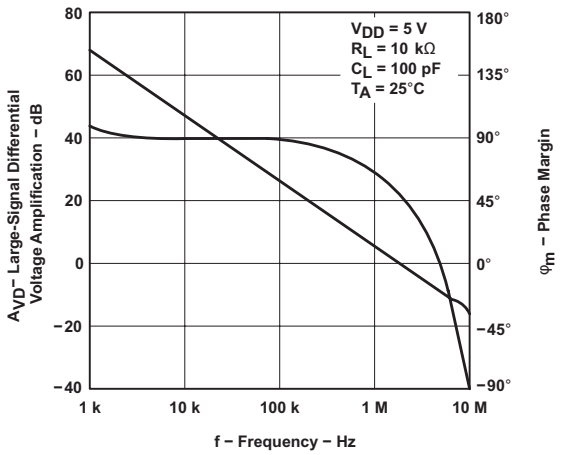


Figure 6-25. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

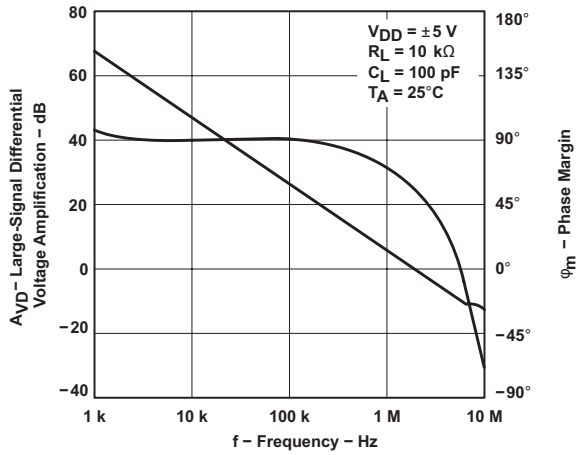


Figure 6-26. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency

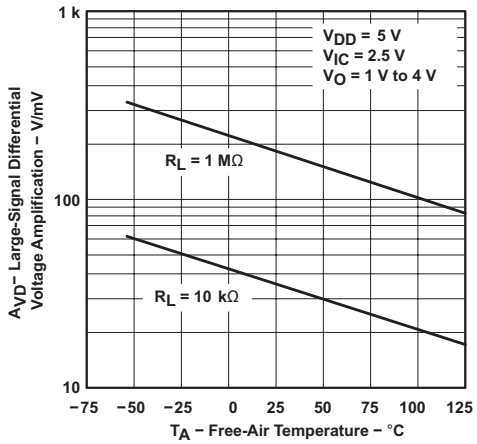


Figure 6-27. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

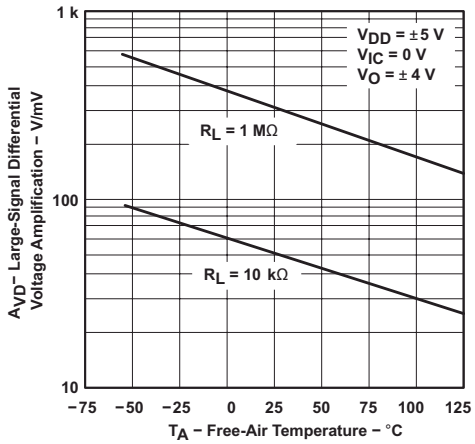


Figure 6-28. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

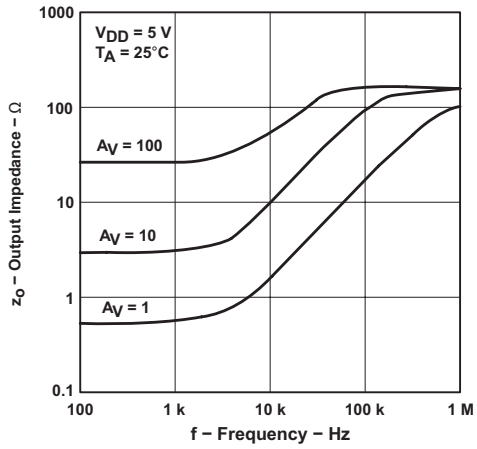


Figure 6-29. Output Impedance vs Frequency

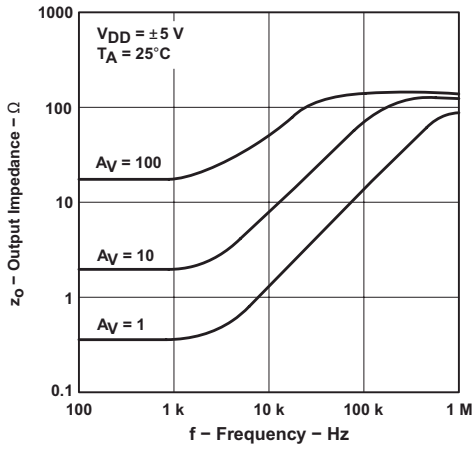


Figure 6-30. Output Impedance vs Frequency

6.9 Typical Characteristics (continued)

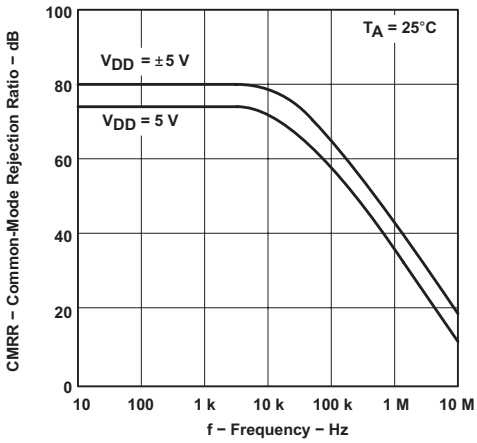


Figure 6-31. Common-Mode Rejection Ratio vs Frequency

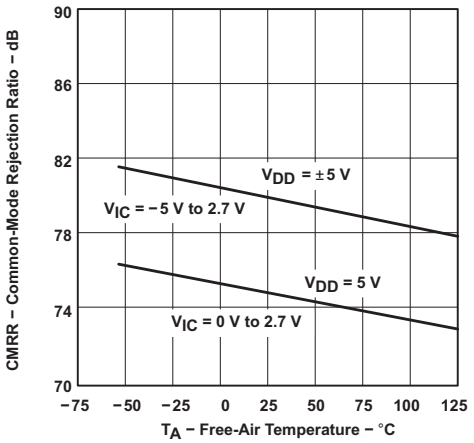


Figure 6-32. Common-Mode Rejection Ratio vs Free-Air Temperature

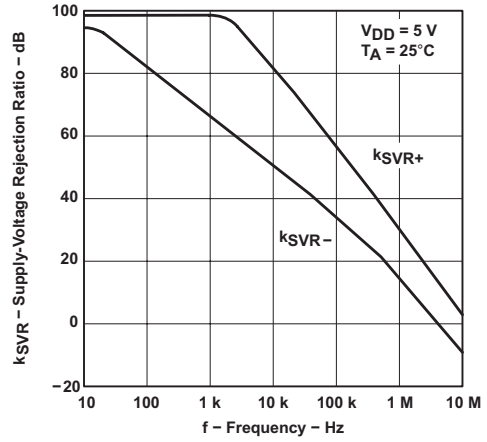


Figure 6-33. Supply-Voltage Rejection Ratio vs Frequency

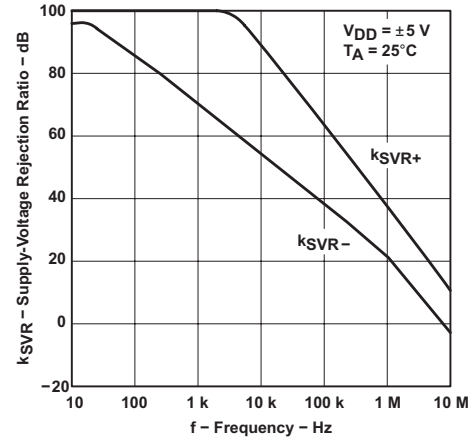


Figure 6-34. Supply-Voltage Rejection Ratio vs Frequency

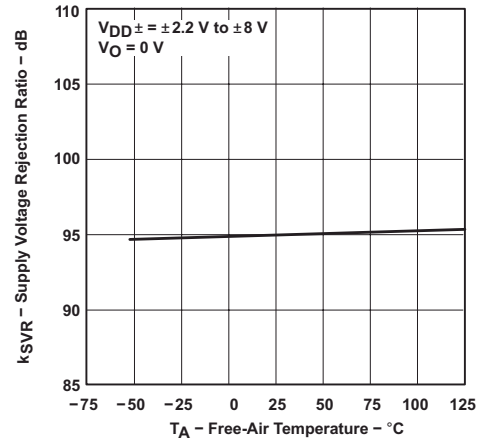


Figure 6-35. Supply-Voltage Rejection Ratio vs Free-Air Temperature

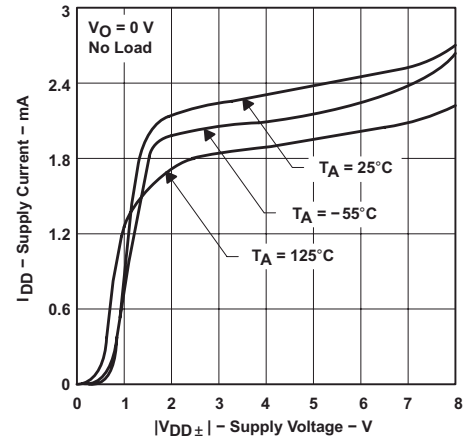


Figure 6-36. TLC2272-Q1 Supply Current vs Supply Voltage

6.9 Typical Characteristics (continued)

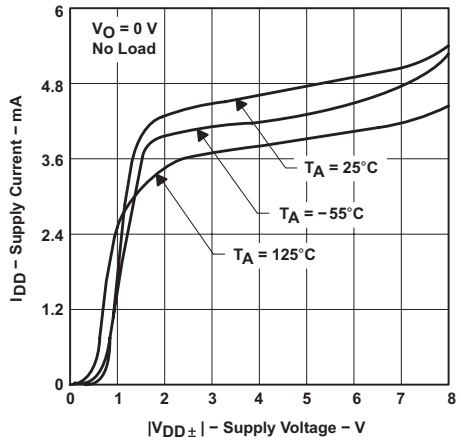


Figure 6-37. TLC2274-Q1 Supply Current vs Supply Voltage

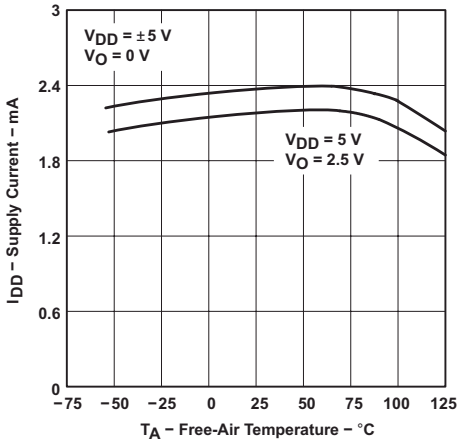


Figure 6-38. TLC2272-Q1 Supply Current vs Free-Air Temperature

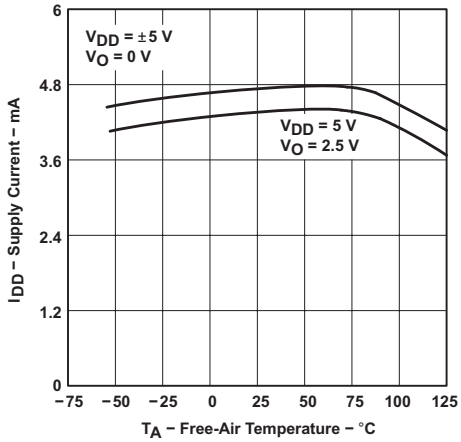


Figure 6-39. TLC2274-Q1 Supply Current vs Free-Air Temperature

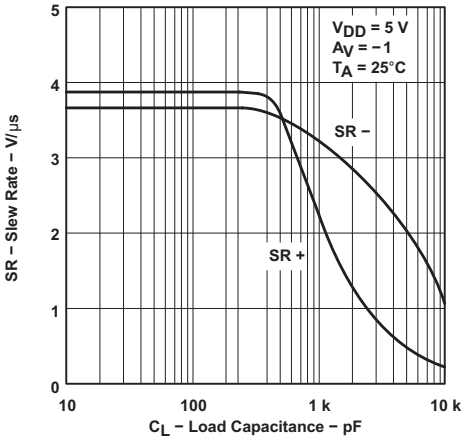


Figure 6-40. Slew Rate vs Load Capacitance

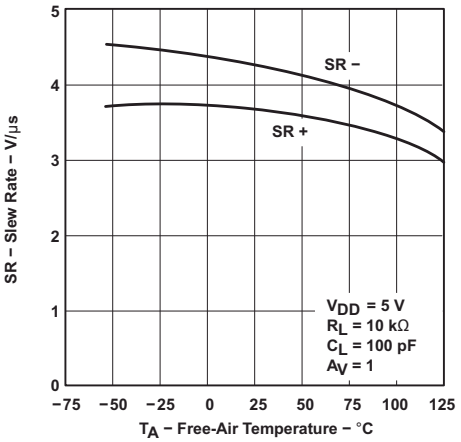


Figure 6-41. Slew Rate vs Free-Air Temperature

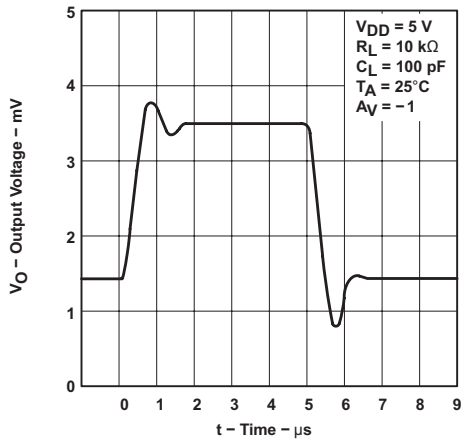


Figure 6-42. Inverting Large-Signal Pulse Response

6.9 Typical Characteristics (continued)

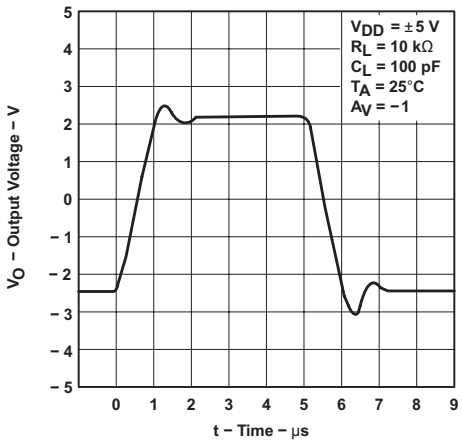


Figure 6-43. Inverting Large-Signal Pulse Response

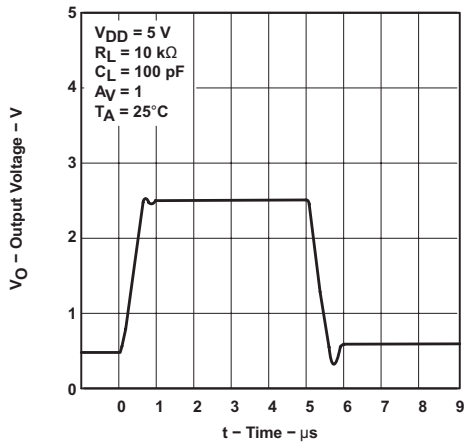


Figure 6-44. Voltage-Follower Large-Signal Pulse Response

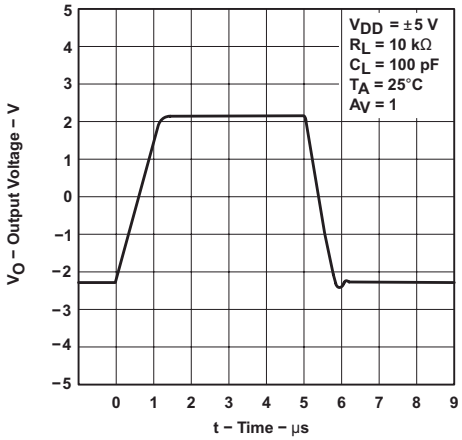


Figure 6-45. Voltage-Follower Large-Signal Pulse Response

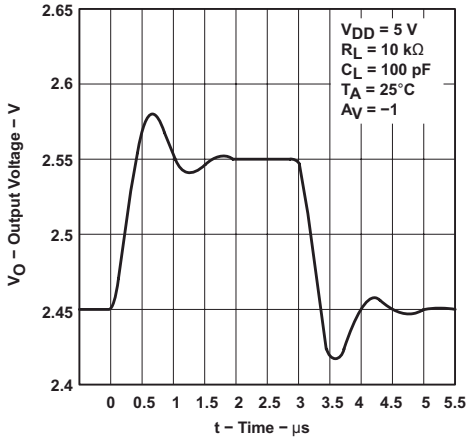


Figure 6-46. Inverting Small-Signal Pulse Response

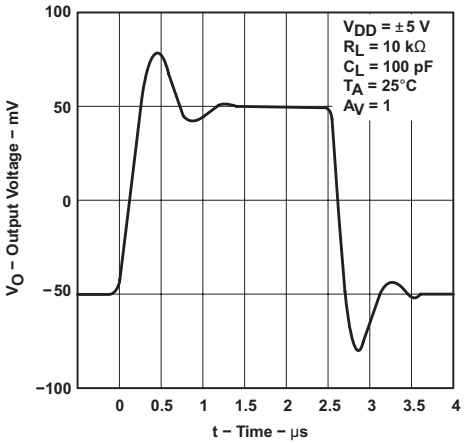


Figure 6-47. Inverting Small-Signal Pulse Response

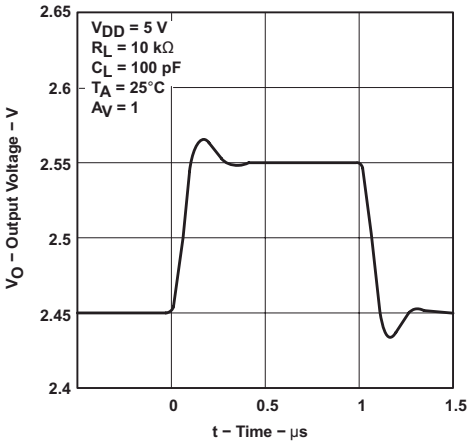


Figure 6-48. Voltage-Follower Small-Signal Pulse Response

6.9 Typical Characteristics (continued)

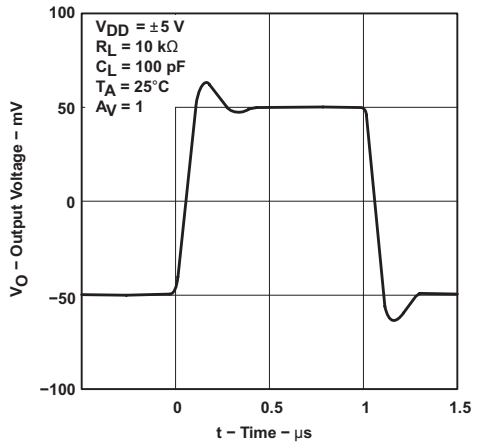


Figure 6-49. Voltage-Follower Small-Signal Pulse Response

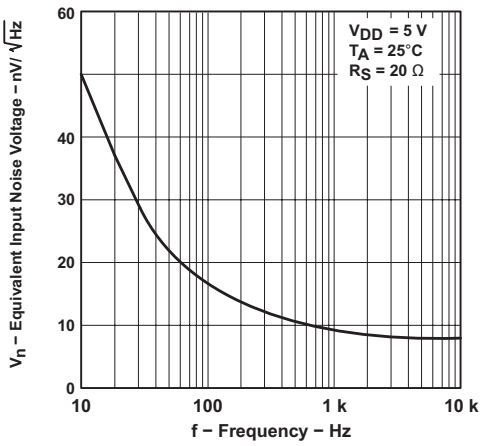


Figure 6-50. Equivalent Input Noise Voltage vs Frequency

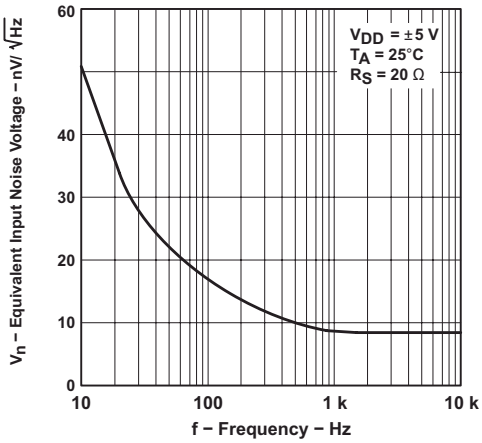


Figure 6-51. Equivalent Input Noise Voltage vs Frequency

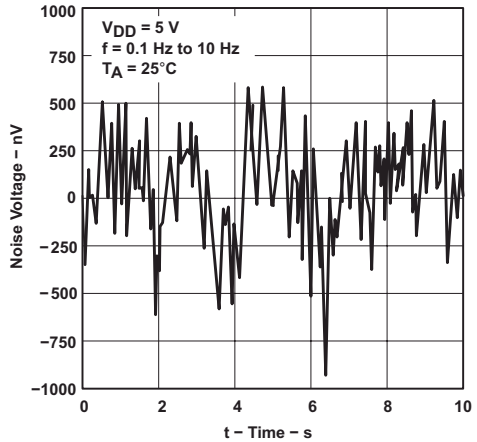


Figure 6-52. Noise Voltage Over a 10 Second Period

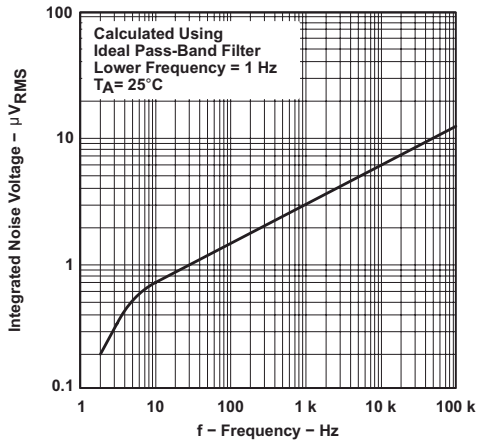


Figure 6-53. Integrated Noise Voltage vs Frequency

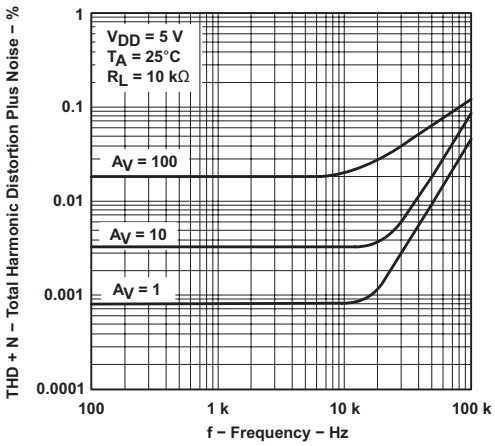


Figure 6-54. Total Harmonic Distortion + Noise vs Frequency

6.9 Typical Characteristics (continued)

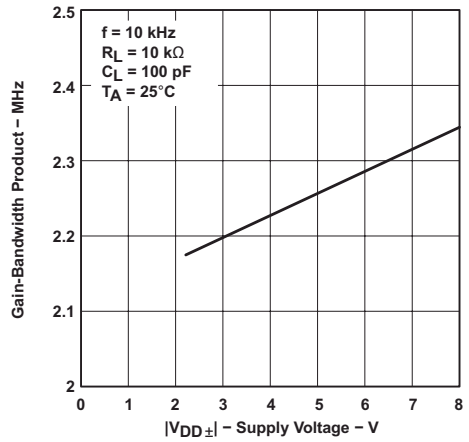


Figure 6-55. Gain-Bandwidth Product vs Supply Voltage

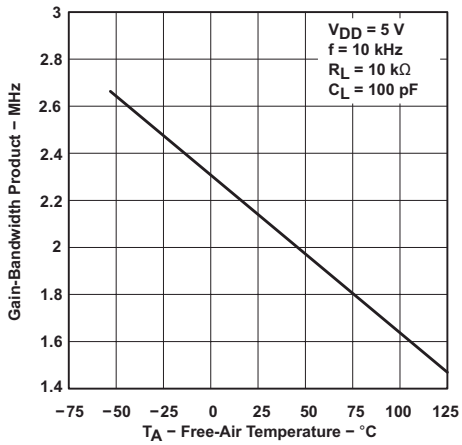


Figure 6-56. Gain-Bandwidth Product vs Free-Air Temperature

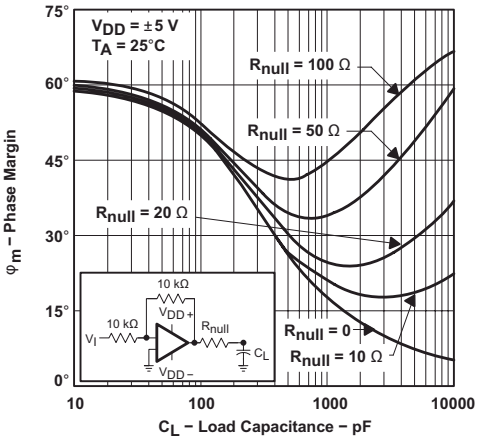


Figure 6-57. Phase Margin vs Load Capacitance

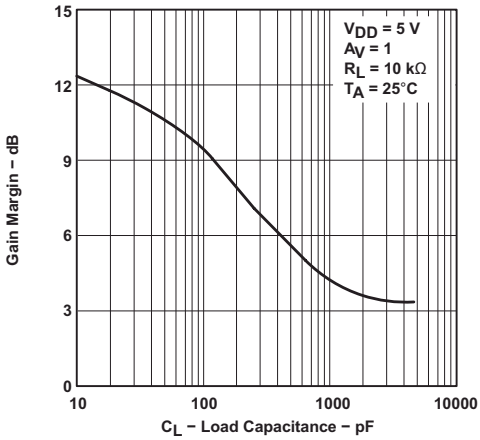


Figure 6-58. Gain Margin vs Load Capacitance

7 Detailed Description

7.1 Overview

The TLC227x-Q1 devices are a rail-to-rail output operational amplifiers. These devices operate from a 4.4-V to 16-V single supply and a ±2.2-V ±8-V dual supply, are unity-gain stable, and are an excellent choice for a wide range of general-purpose applications.

7.2 Functional Block Diagram

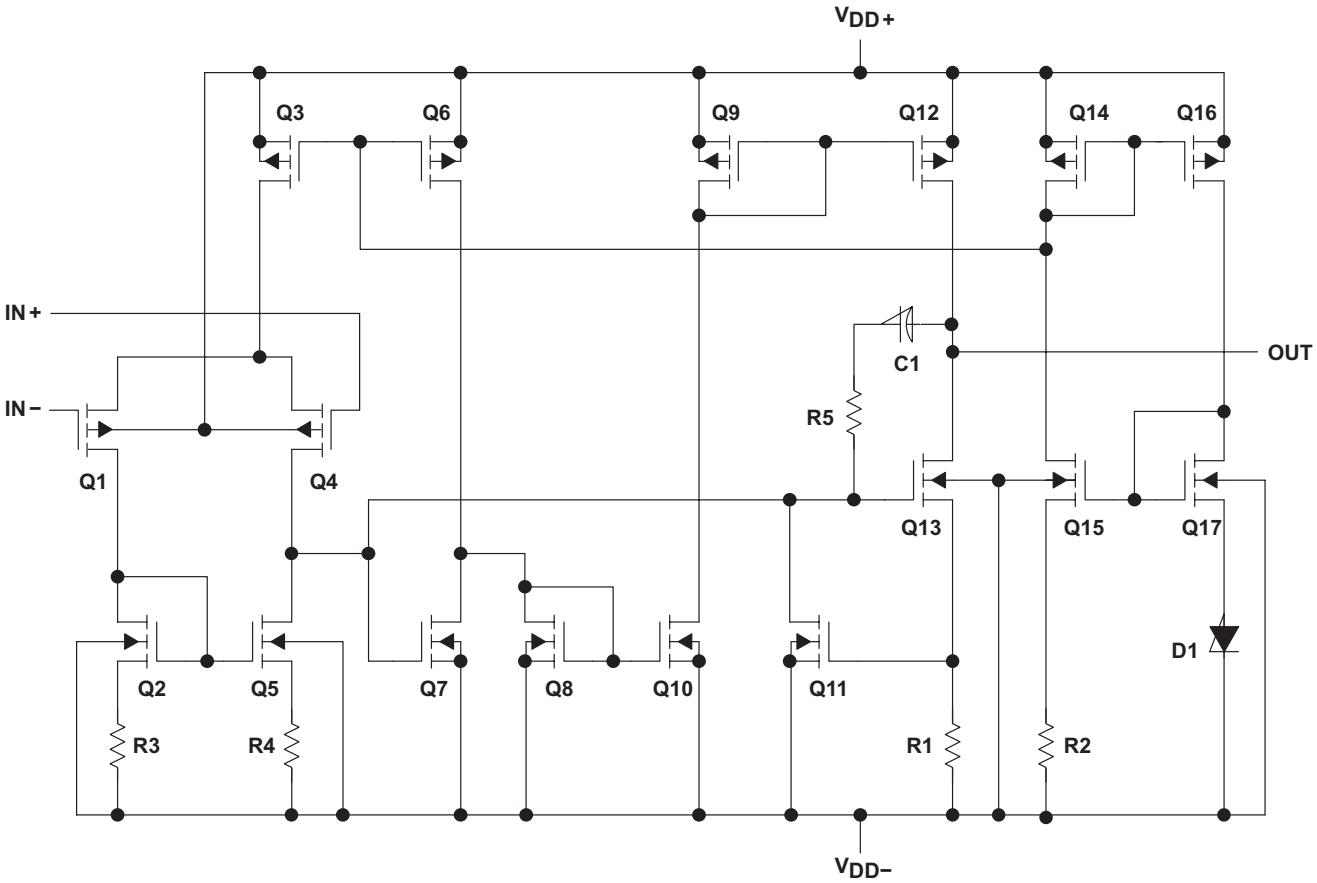


Table 7-1. Actual Device Component Count(1)

COMPONENT	TLC2272-Q1	TLC2274-Q1
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

7.3 Feature Description

The TLC227x-Q1 family features 2-MHz bandwidth and voltage noise of 9 nV/√Hz with performance rated from 4.4 V to 16 V across an automotive temperature range (–40°C to +125°C). LinMOS is a great choice for a wide range of audio, automotive, industrial, and instrumentation applications.

7.4 Device Functional Modes

The TLC227x-Q1 family of devices is powered on when the supply is connected. The device can operate with single or dual supply, depending on the application. The device is in full performance after the supply is greater than the recommended value.

8 Application and Implementation

Note

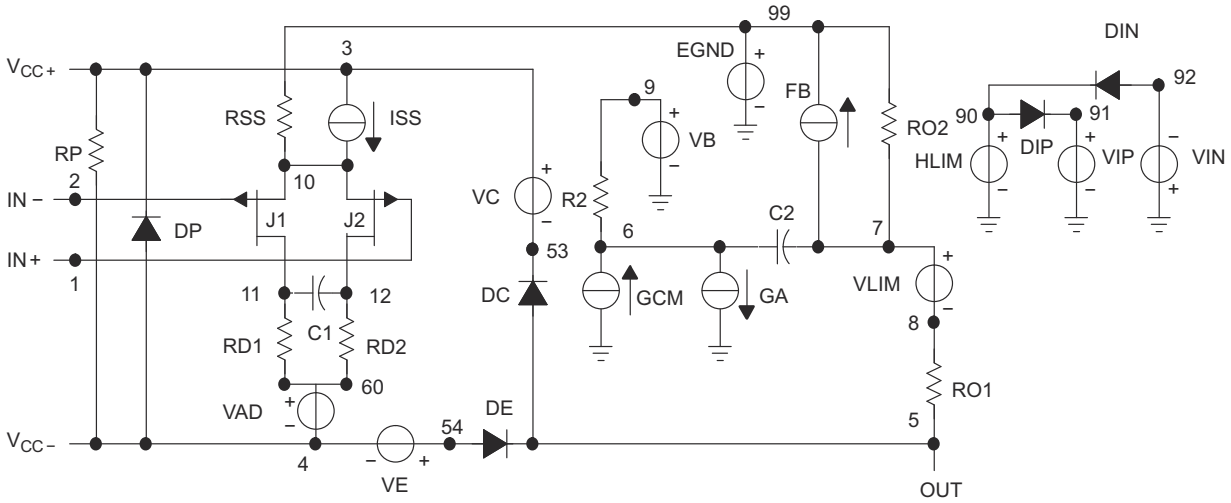
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Macromodel Information

Macromodel information provided was derived using MicroSim Parts, the model generation software used with PSpice®. The Boyle macromodel (see also *Section 9.2.1*) and subcircuit in Figure 8-1 were generated using the TLC227x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit




```
.SUBCKT TLC227x 1 2 3 4 5
C1      11      12      1214E−12
C2      6       7       760.00E−12
DC      5       53      53DX
DE      54      5       5DX
DLP     90      91      91DX
DLN     92      90      90DX
DP      4       3       3DX
EGND    99      0       0POLY (2) (3,0) (4,) 0 .5 .5
FB      99      0       0POLY (5) VB VC VE VLP VLN 0
+ 984.9E3 −1E6 1E6 1E6 −1E6
GA      6       0       011 12 377.0E−6
GCM 0 6 10 99 134E−9
ISS     3       10      10DC 216.OE−6
HLIM    90      0       0VLIM 1K
J1      11      12      210 JX
J2      12      110 JX
R2      6       9100.OE3
RD1     60      112.653E3
RD2     60      122.653E3
R01     8       550
R02     7       9950
RP      3       44.310E3
RSS     10      99925.9E3
VAD     60      4−.5
VB      9       0DC 0
VC 3 53 DC .78
VE      54      4DC .78
VLIM    7       8DC 0
VLP     91      0DC 1.9
VLN     0       92DC 9.4
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=1.500E−12BETA=1.316E-3
+ VTO=−.270)
.ENDS
```

Figure 8-1. Boyle Macromodels and Subcircuit

8.2 Typical Application

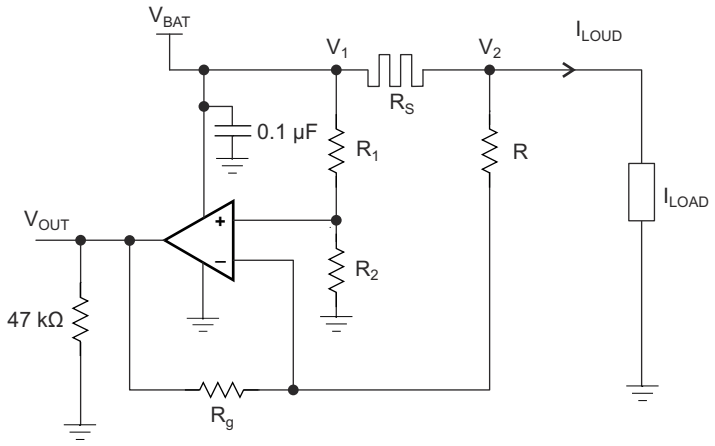


Figure 8-2. High-Side Current Monitor Equivalent Schematic (Each Amplifier)

8.2.1 Design Requirements

For this design example, use these parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

PARAMETER		VALUE
V_{BAT}	Battery voltage	12 V
R_{SENSE}	Sense resistor	0.1 Ω
I_{LOAD}	Load current	0 A to 10 A
	Operational amplifier	Set in differential configuration with gain = 10

8.2.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with a 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

8.2.2.1 Differential Amplifier Equations

Equation 1 and Equation 2 are used to calculate V_{OUT}.

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times\frac{V_1+V_2}{2}+\frac{1+\frac{1}{2}\left(\frac{R_1}{R_2}+\frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}}(V_1-V_2)\right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R}\left(\frac{\frac{R}{R_g}-\frac{R_1}{R_2}}{1+\frac{R_1}{R_2}}\times V_{BAT}+\frac{1+\frac{1}{2}\left(\frac{R_1}{R_2}+\frac{R}{R_g}\right)}{1+\frac{R_1}{R_2}}\times R_S\times I_{Load}\right) \quad (2)$$

In an ideal case, Equation 3 then calculates $R_1 = R$ and $R_2 = R_g$, and V_{OUT}:

$$V_{OUT} = \frac{R_g}{R}\times R_S\times I_{Load} \quad (3)$$

However, the resistors have tolerances; therefore, the resistors cannot be perfectly matched.

$R_1 = R \pm \Delta R_1$

$R_2 = R_2 \pm \Delta R_2$

$R = R \pm \Delta R$

$R_g = R_g \pm \Delta R_g$

$$Tol = \frac{DR}{R} \tag{4}$$

Equation 5 shows that by developing the equations and neglecting the second order, the worst case is when the tolerances add up:

$$V_{OUT} = \pm (4\ Tol)\frac{R_g}{R + R_g} \times V_{BAT} + \left(1 \pm 2\ Tol\left(1 + \frac{2R}{R + R_g}\right)\right)\frac{R_g}{R} \times R_S \times I_{LOAD} \tag{5}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1%

If the resistors are perfectly matched, then Tol = 0 and Equation 6 calculates V_{OUT}:

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{LOAD} \tag{6}$$

The highest error is from the common mode:

$$4\ (Tol)\frac{R_g}{R + R_g} \times V_{BAT} \tag{7}$$

Gain of 10, R_g / R = 10, and Tol = 1%:

Common mode error = ((4 × 0.01) / 1.1) × 12 V = 0.436 V

Gain of 10 and Tol = 0.1%:

Common mode error = 43.6 mV

The resistors were chosen from 2% batches.

R_1 and R 12 kΩ

R_2 and R_g 120 kΩ

Ideal Gain = 120 / 12 = 10

The measured value of the resistors:

R_1 = 11.835 kΩ

R = 11.85 kΩ

R_2 = 117.92 kΩ

R_g = 118.07 kΩ

8.2.3 Application Curves

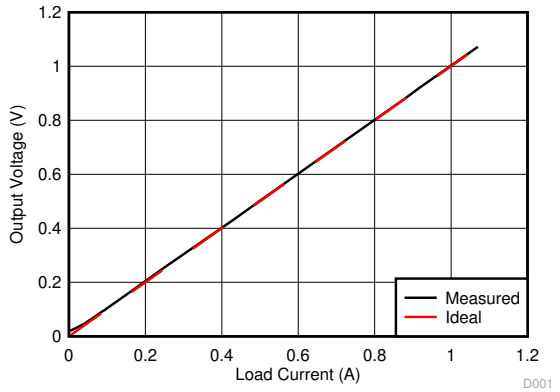


Figure 8-3. Output Voltage Measured vs Ideal (0 A to 1 A)

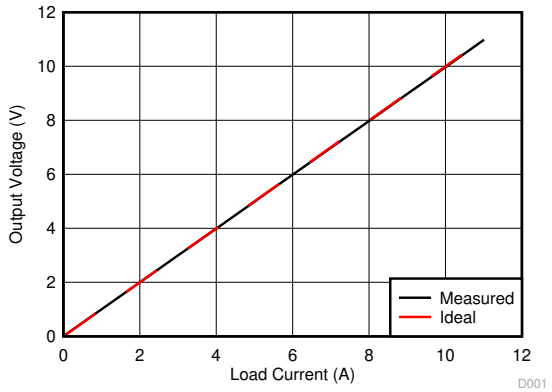


Figure 8-4. Output Voltage Measured vs Ideal (0 A to 10 A)

8.3 Power Supply Recommendations

Supply voltage is 4.4 V to 16 V for single supply and ±2.2 V to ±8 V for dual. In the high-side sensing application, the supply is connected to a 12-V battery.

8.4 Layout

8.4.1 Layout Guidelines

The TLC227x-Q1 is a wideband amplifier. To realize the full operational performance of the device, good high frequency printed-circuit-board (PCB) layout practices are required. Low-loss 0.1-µF bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces must be designed for minimum inductance.

8.4.2 Layout Example

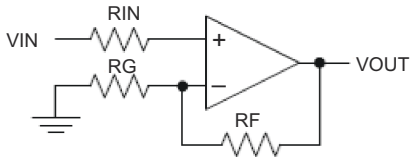


Figure 8-5. Schematic Representation

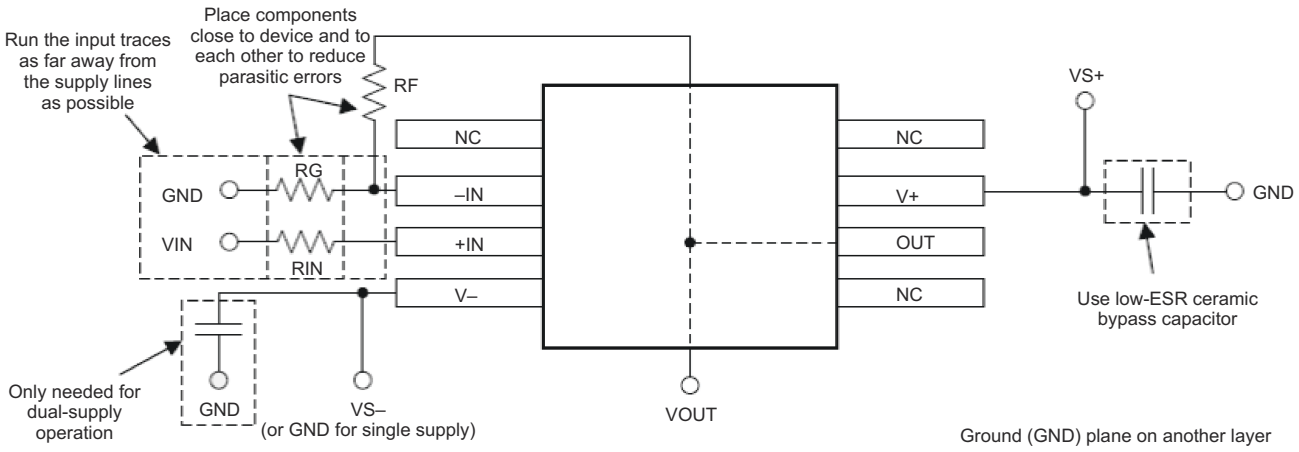


Figure 8-6. Operational Amplifier Board Layout for Noninverting Configuration

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- G.R. Boyle, D.O. Pederson, B.M. Cohn, J.E. Solomon (Dec. 1974). *Macromodeling of Integrated Circuit Operational Amplifiers*. IEEE Journal of Solid-State Circuits, Volume 9, Issue 6, pages 353–364. Retrieved from https://ieeexplore.ieee.org/document/1050528

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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PSpice® is a registered trademark of Cadence Design Systems, Inc.
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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2272AQDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQDRG4Q1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQPWRG4Q1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQPWRG4Q1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272AQPWRQ1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ
TLC2272QDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QDRG4Q1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QPWRG4Q1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QPWRG4Q1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QPWRG4Q1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QPWRQ1	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QPWRQ1.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2272QPWRQ1.B	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1
TLC2274AQDRG4Q1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQDRG4Q1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQDRG4Q1.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC2274AQDRQ1.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQPWRG4Q1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQPWRG4Q1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQPWRG4Q1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274AQPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1
TLC2274QDRG4Q1	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	2274Q1
TLC2274QDRQ1	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 125	2274Q1
TLC2274QPWRG4Q1	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	-40 to 125	2274Q1
TLC2274QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1
TLC2274QPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1
TLC2274QPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLC2272-Q1, TLC2272A-Q1, TLC2274-Q1, TLC2274A-Q1 :

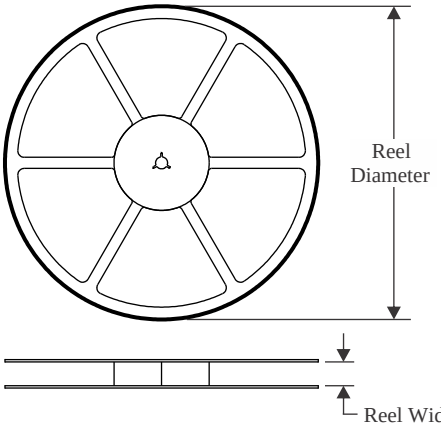
- Catalog : TLC2272, TLC2272A, TLC2274, TLC2274A
- Enhanced Product : TLC2272A-EP, TLC2274-EP, TLC2274A-EP
- Military : TLC2272M, TLC2272AM, TLC2274AM

NOTE: Qualified Version Definitions:

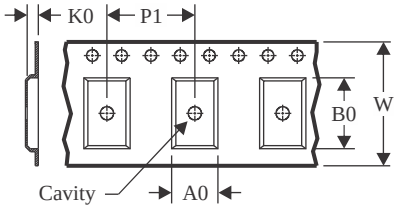
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

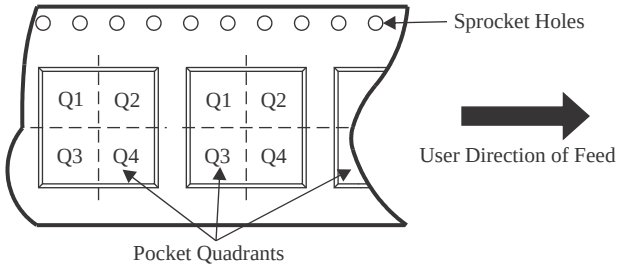


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

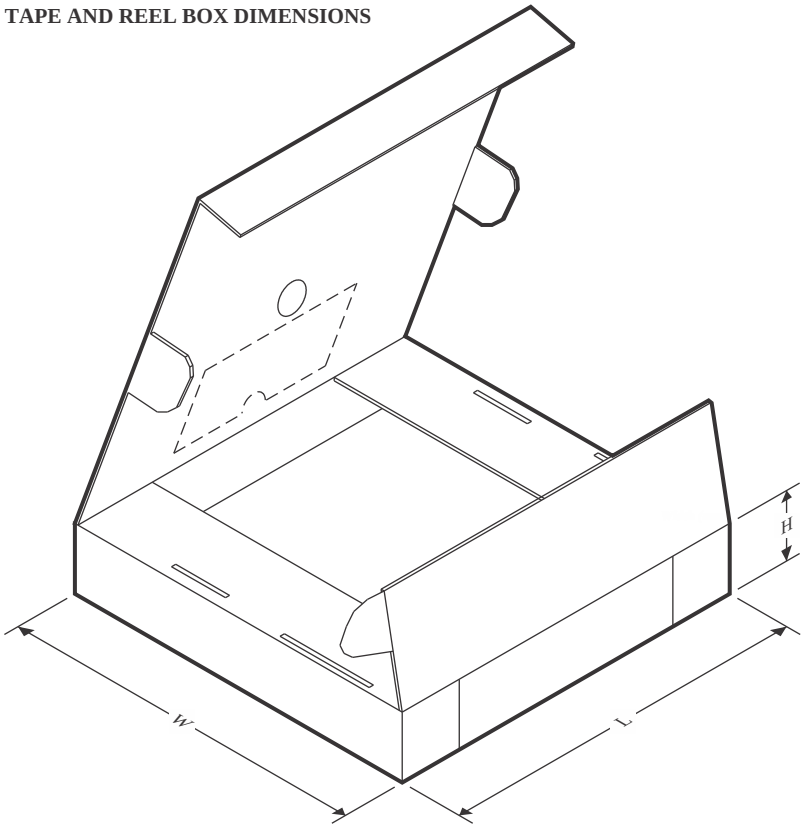
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

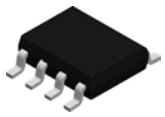
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2272AQPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272AQPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272QPWRG4Q1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2272QPWRQ1	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2272AQPWRG4Q1	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2272AQPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2272QPWRG4Q1	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2272QPWRQ1	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2274AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
TLC2274QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

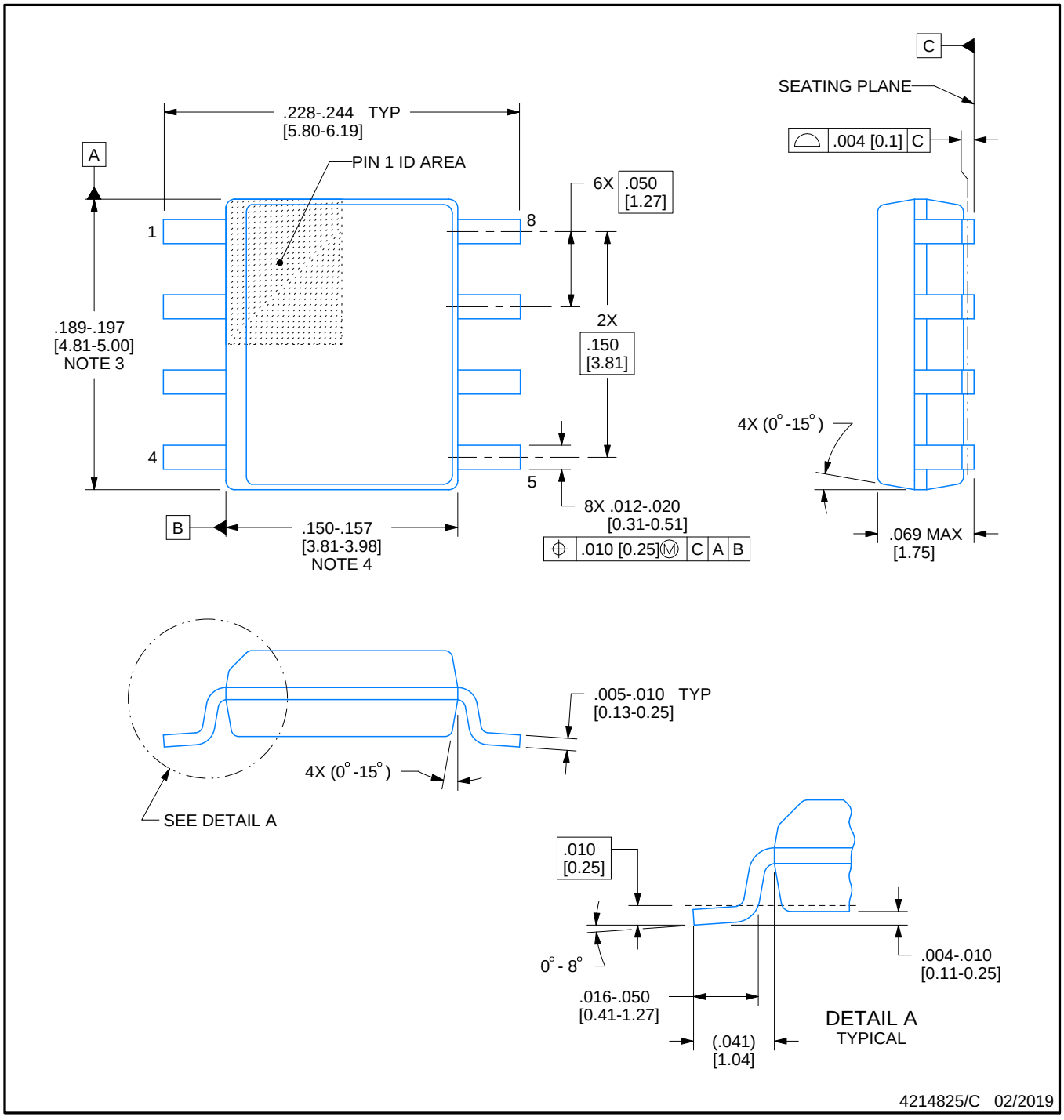


PACKAGE OUTLINE

D0008A

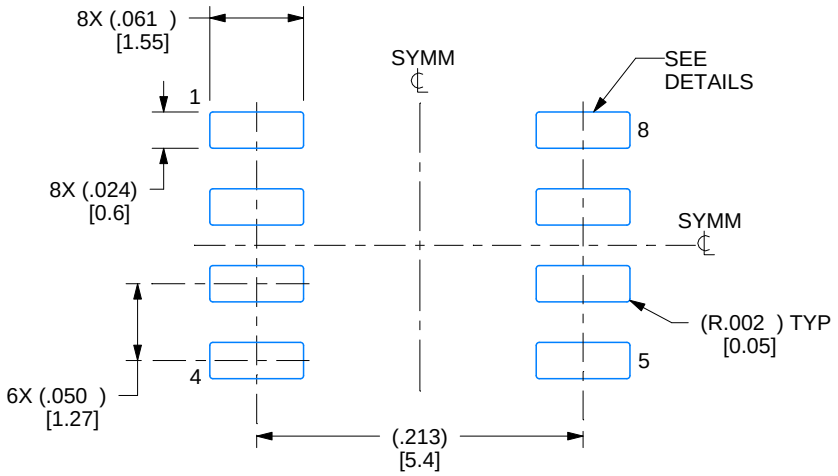
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

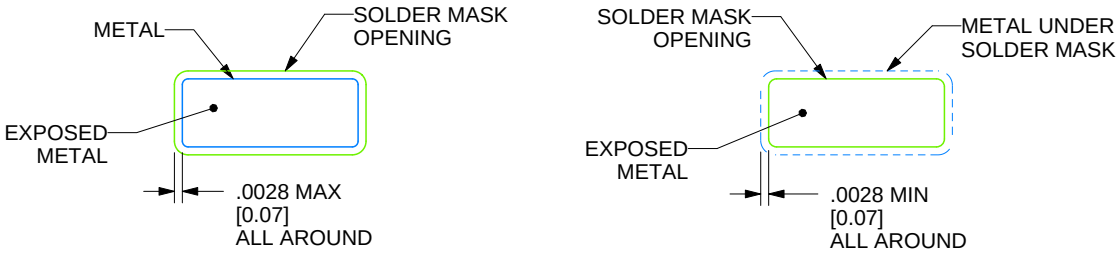


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

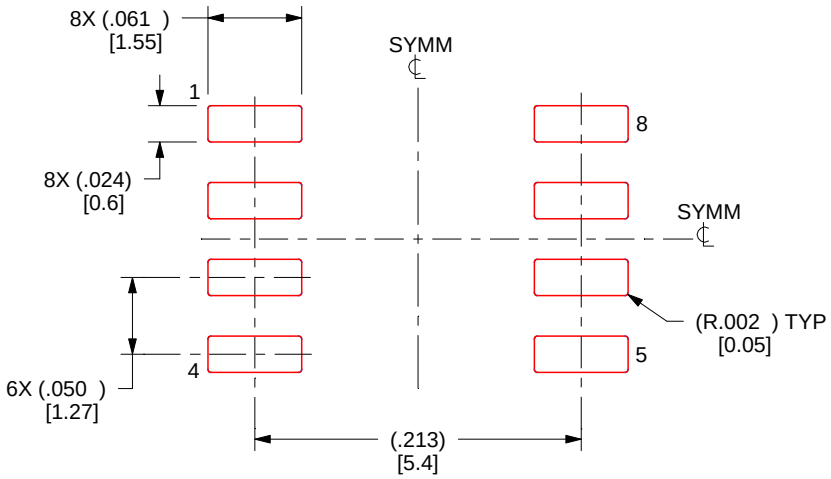
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

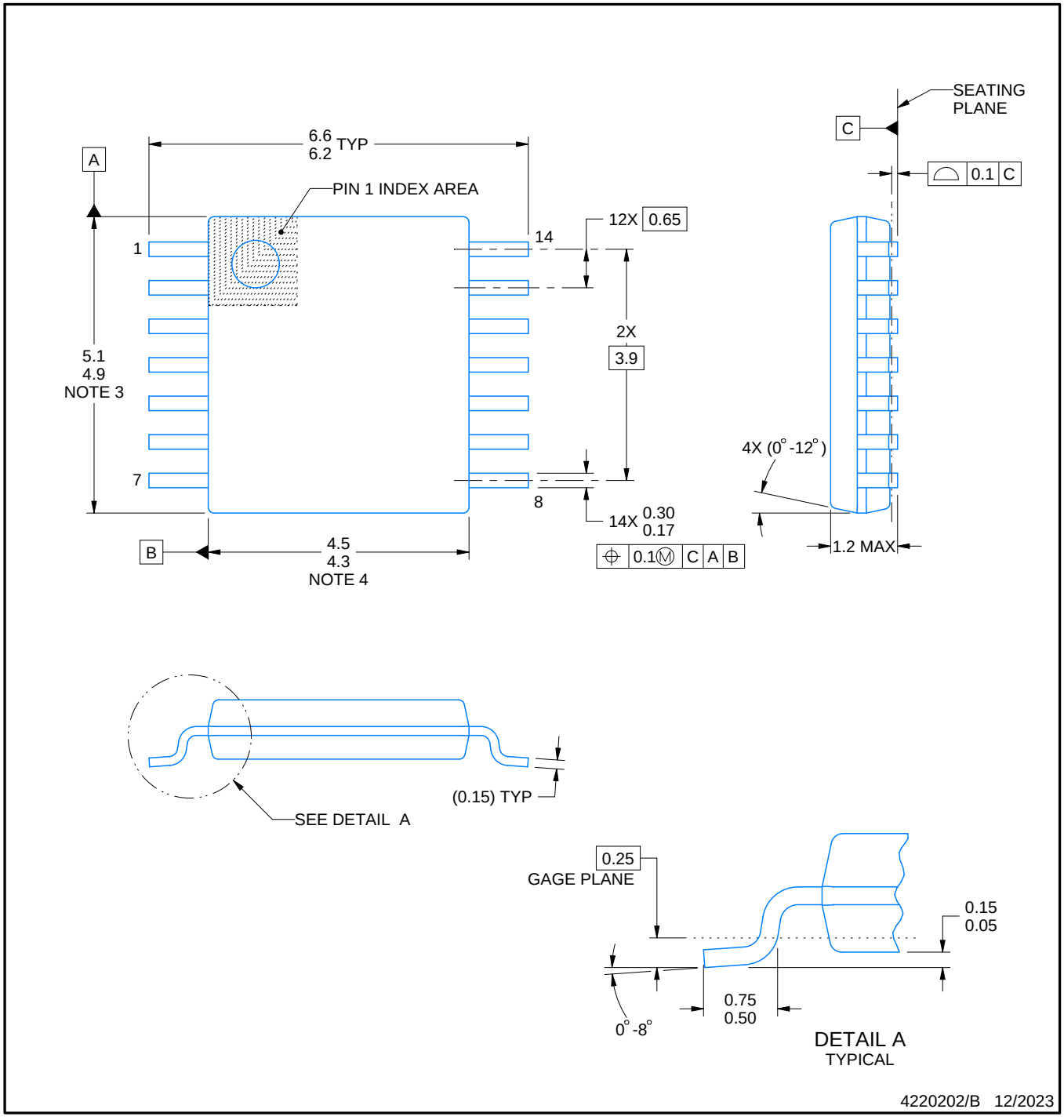
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

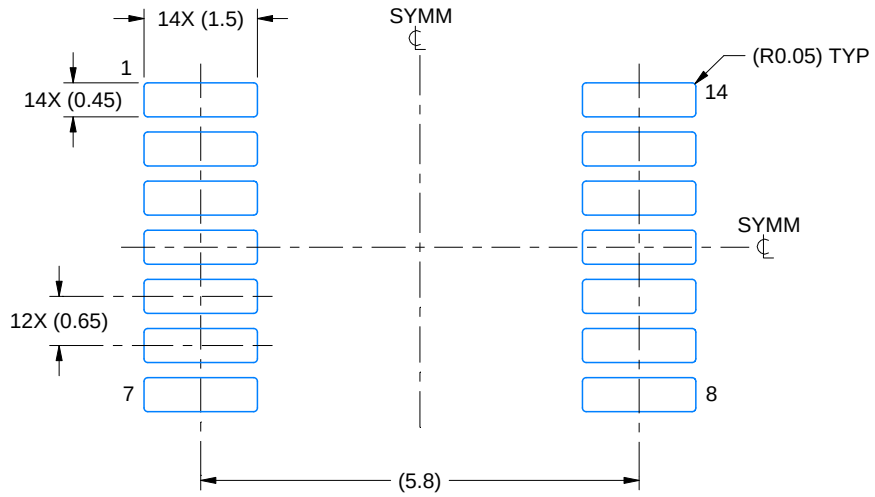
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

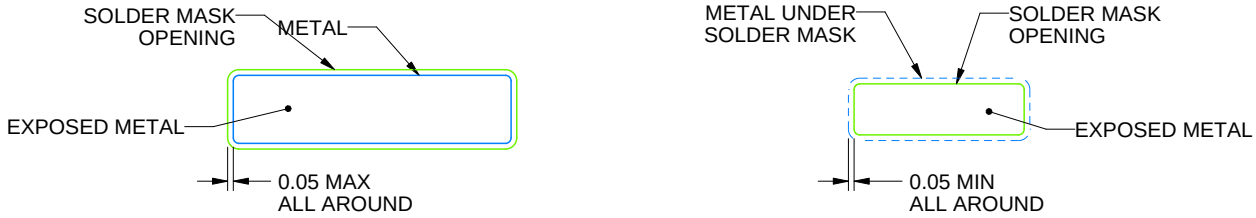


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

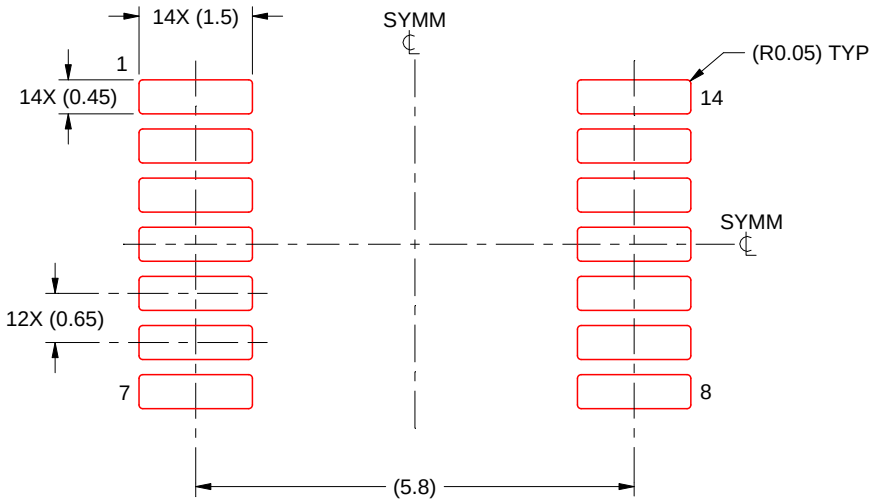


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

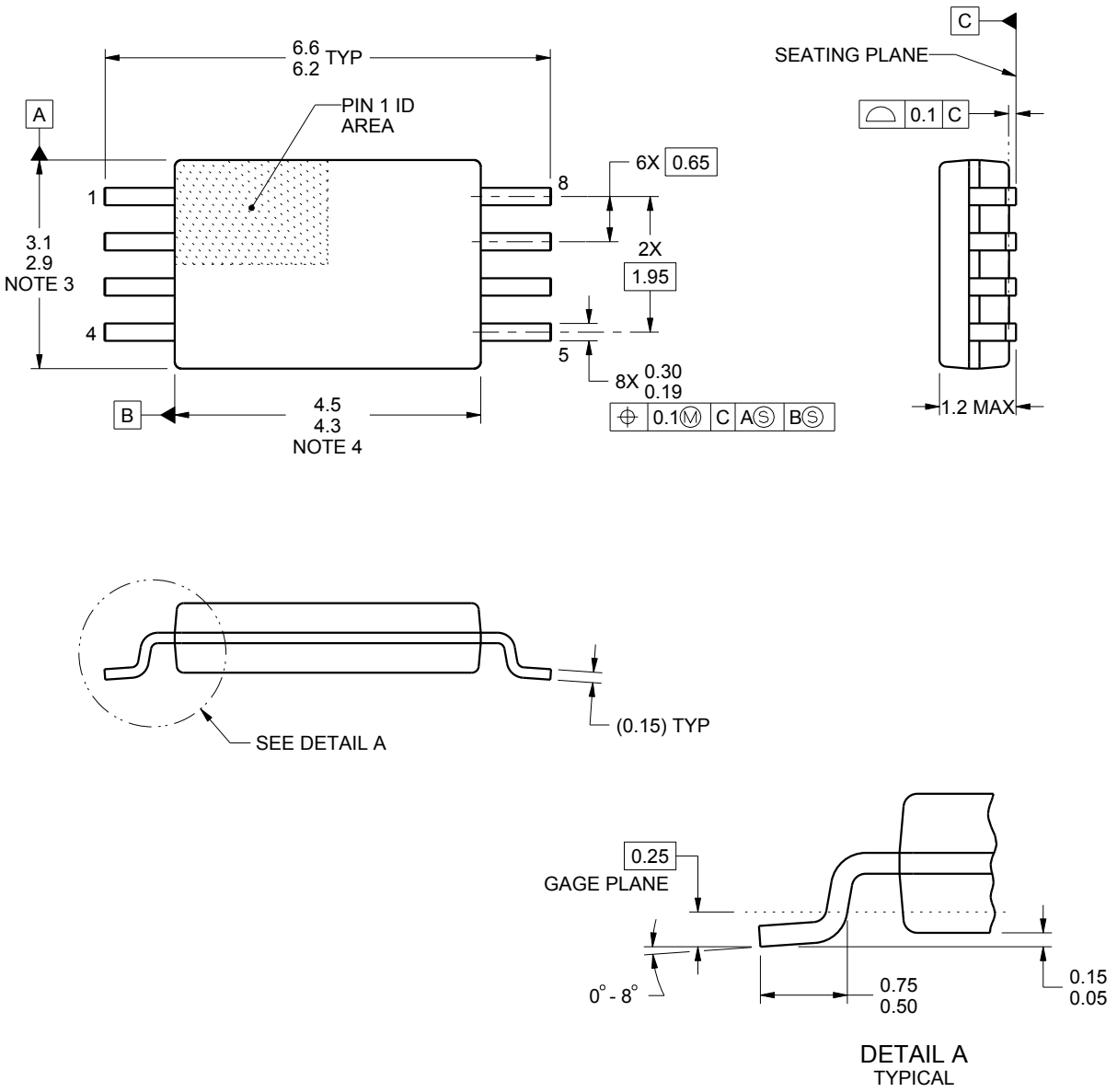
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

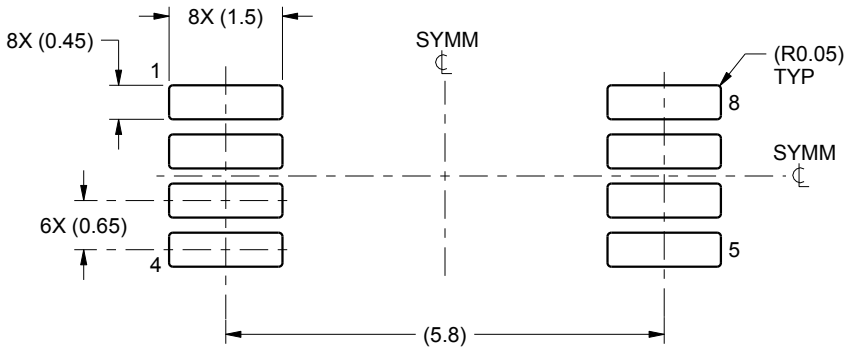
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

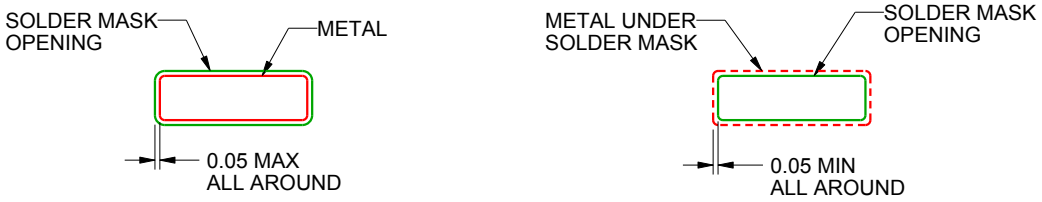


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

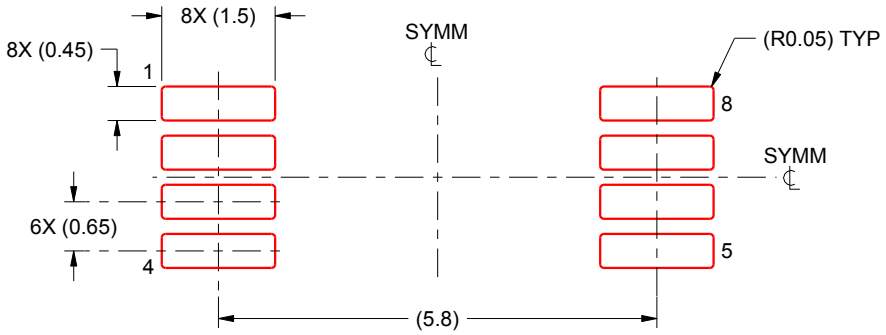


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

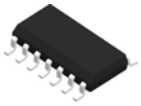


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

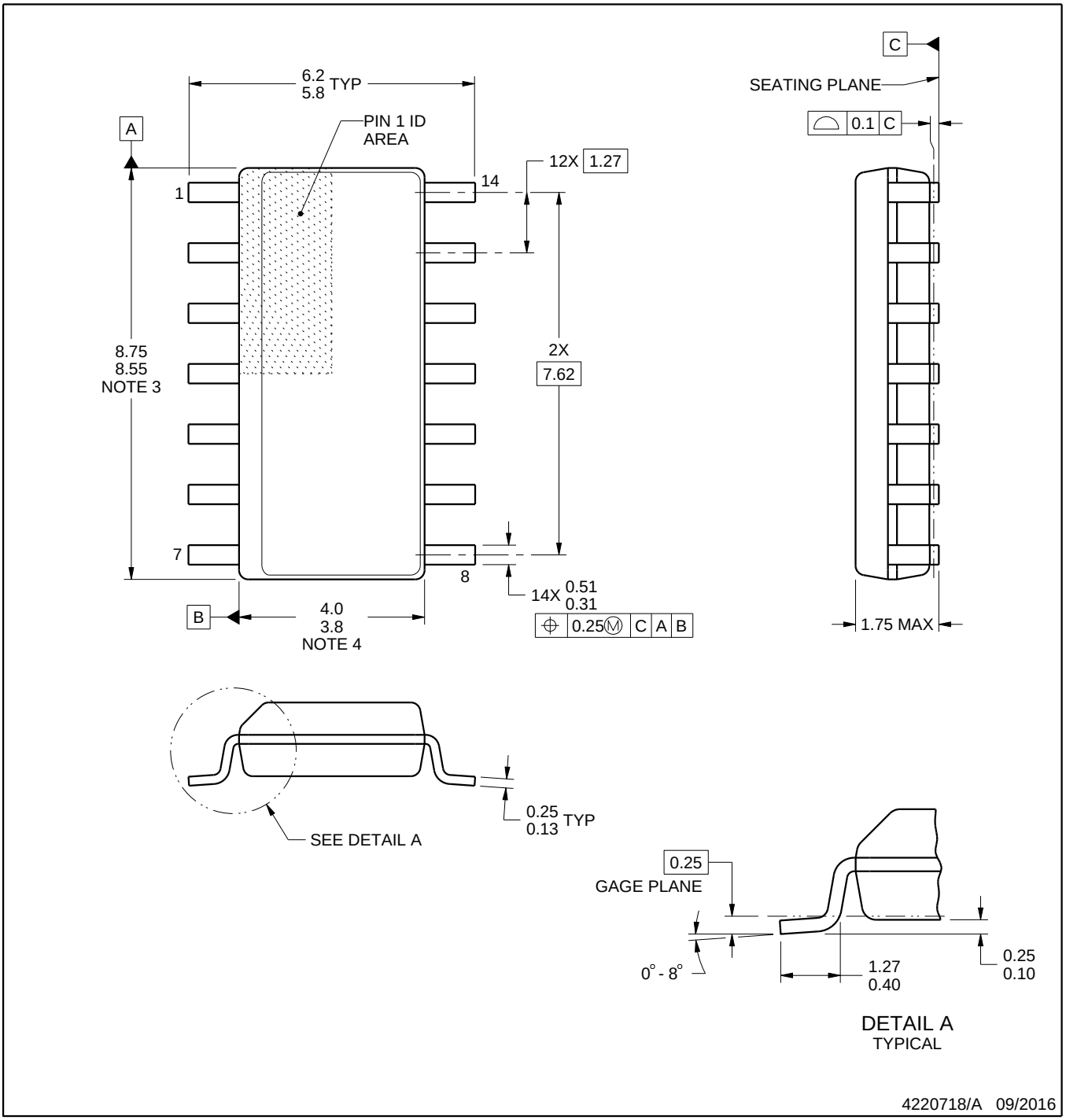


PACKAGE OUTLINE

D0014A

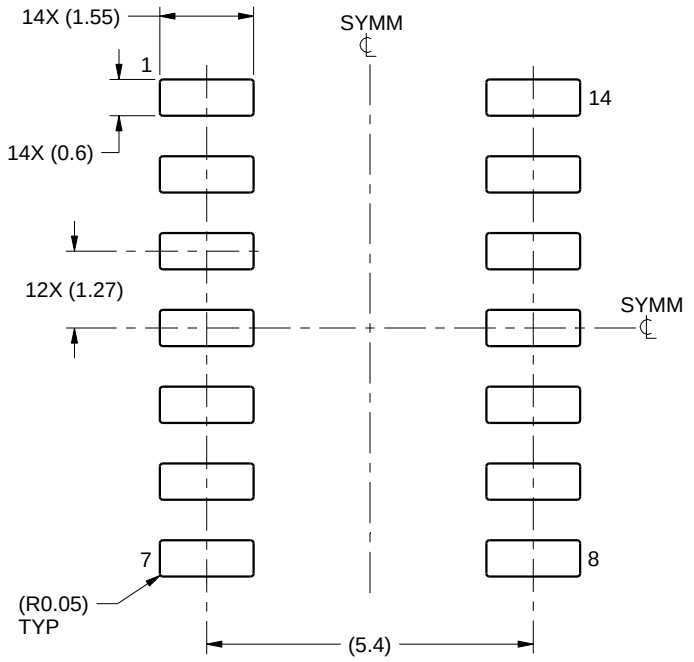
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

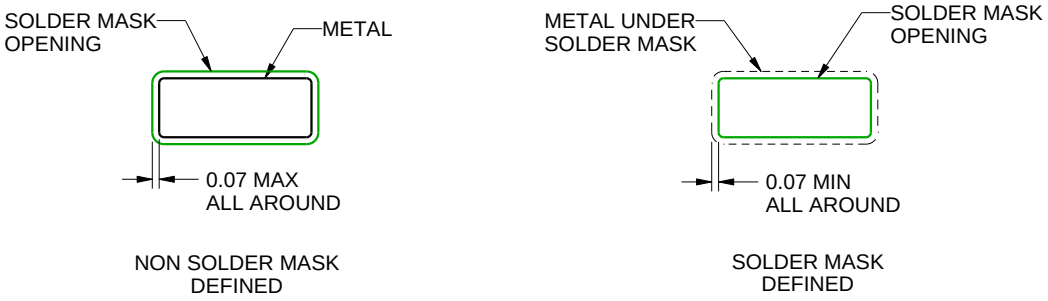


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

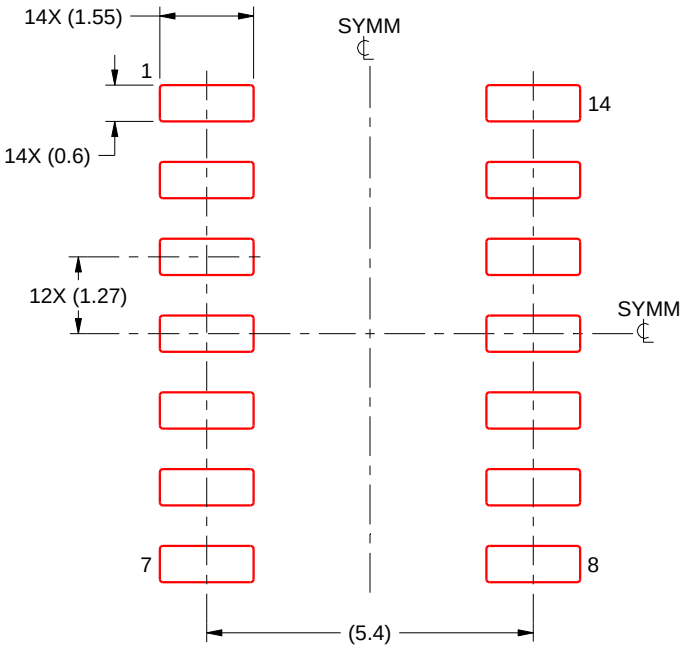
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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