### TL714C HIGH-SPEED DIFFERENTIAL COMPARATOR

SLCS015A - DECEMBER 1988 - REVISED AUGUST 2003

- Operates From a 5-V Supply
- Self-Biasing Inputs
- Hysteresis . . . 10 mV Typ
- Response Time . . . 6 ns Typ
- Maximum Operating Frequency... 50 MHz Typ

#### 

NC - No internal connection

### description/ordering information

The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics.

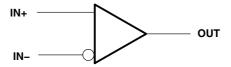
The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

#### **ORDERING INFORMATION**

T <sub>A</sub>	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	PDIP (P)	Tube of 50	TL714CP	TL714CP	
0°C to 70°C	COIC (D)	Tube of 75	TL714CD	TI 74.40	
	SOIC (D)	Reel of 2500	TL714CDR	TL714C	

<sup>&</sup>lt;sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### symbol

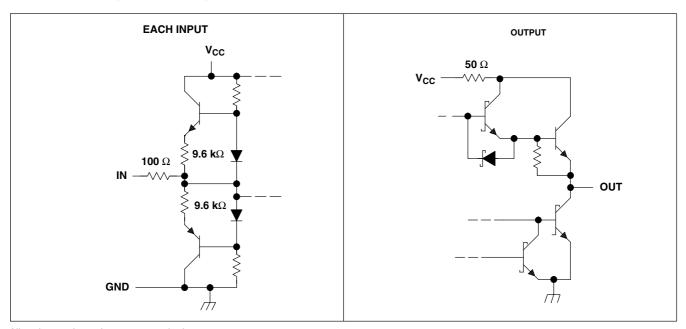




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### schematic of inputs and outputs



All resistor values shown are nominal.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub> (see Note 1)	7 V
Differential input voltage, V <sub>ID</sub> (see Note 2)	
Input voltage range, V <sub>I</sub>	V <sub>CC</sub> to GND
Low-level output current, I <sub>OL</sub>	40 mA
Package thermal impedance, θ <sub>JA</sub> (see Notes 3 and 4): D package	97°C/W
P package	85°C/W
Operating virtual junction temperature, T <sub>J</sub>	150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T <sub>stg</sub>	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltage, are with respect to the network ground.
  - 2. Differential voltage values are at IN+ with respect to IN-.
  - 3. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  - 4. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5.25	V
V <sub>IC</sub>	Common-mode input voltage	1.4 to V <sub>CC</sub> -1.4		٧
I <sub>OH</sub>	High-level output current		-1	mA
I <sub>OL</sub>	Low-level output current		16	mA
T <sub>A</sub>	Operating free-air temperature	0	70	°C



# electrical characteristics over free-air operating temperature range, $V_{CC}$ = 5 V (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS	MIN	TYP†	MAX	UNIT
$V_{T}$	Threshold voltage ( $V_{T+}$ and $V_{T-}$ )	$V_{IC} = 1.4 \text{ V to } 3.6$	6 V	-75 <sup>‡</sup>		75	mV
V <sub>hys</sub>	Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )			2	10	30	mV
$V_{OH}$	High-level output voltage	$V_{ID} = 100 \text{ mV},$	$I_{OH} = -1 \text{ mA}$	2.7	3.4		V
$V_{OL}$	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	I <sub>OL</sub> = 16 mA		0.4	0.5	V
Ios	Short-circuit output current			-30		-110	mA
rį	Differential input resistance			2.9			kΩ
I <sub>CC</sub>	Supply current	$V_{ID} = -100 \text{ mV},$	I <sub>O</sub> = 0		7	12	mA

<sup>&</sup>lt;sup>†</sup> All typical values are at  $T_A = 25$ °C.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	MIN	TYP†	MAX	UNIT	
f <sub>max</sub>	Maximum operating frequency	$V_{ID} = \pm 250 \text{ mV},$ $C_L = 25 \text{ pF},$	$t_r = t_f = 4 \text{ ns},$ Input duty cycle = 50%		50		MHz
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	$V_{ID} = \pm 100 \text{ mV},$	C <sub>L</sub> = 25 pF,		6	12	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output	See Figures 1 and 2	·		6	12	ns
t <sub>r</sub>	Rise time	$V_{ID} = \pm 100 \text{ mV},$	C <sub>L</sub> = 25 pF,		4	8	ns
t <sub>f</sub>	Fall time	See Figure 3			4	8	ns

<sup>†</sup> All typical values are at  $T_A = 25$ °C.

### PARAMETER MEASUREMENT INFORMATION

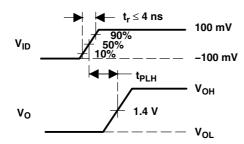


Figure 1. Propagation Delay Time, Low to High (t<sub>PLH</sub>)

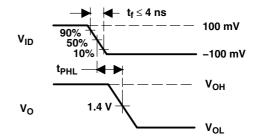


Figure 2. Propagation Delay Time, High to Low (t<sub>PHL</sub>)

<sup>&</sup>lt;sup>‡</sup> The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

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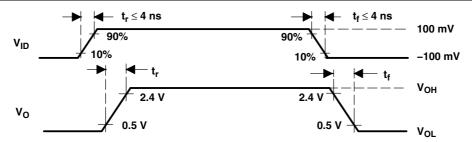


Figure 3. Rise and Fall Times (t<sub>r</sub>, t<sub>f</sub>)

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
TL714CD	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CD.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CDR	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CP	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL714CP
TL714CP.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL714CP

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



# **PACKAGE OPTION ADDENDUM**

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# **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

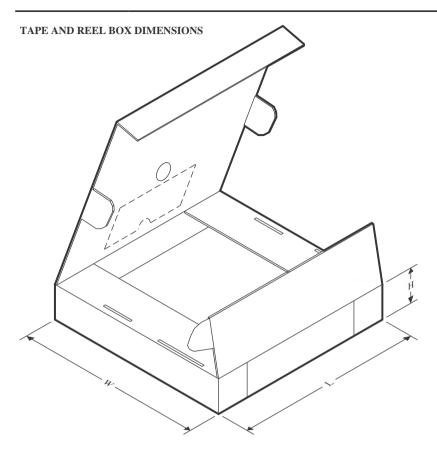
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL714CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TL714CDR	SOIC	D	8	2500	353.0	353.0	32.0	

# **PACKAGE MATERIALS INFORMATION**

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### **TUBE**



### \*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL714CD	D	SOIC	8	75	507	8	3940	4.32
TL714CD.A	D	SOIC	8	75	507	8	3940	4.32
TL714CP	Р	PDIP	8	50	506	13.97	11230	4.32
TL714CP.A	Р	PDIP	8	50	506	13.97	11230	4.32



SMALL OUTLINE INTEGRATED CIRCUIT



### NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



# P (R-PDIP-T8)

### PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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