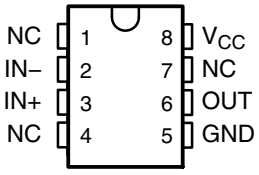
TL714C
HIGH-SPEED DIFFERENTIAL COMPARATOR

SLCS015A – DECEMBER 1988 – REVISED AUGUST 2003

- **Operates From a 5-V Supply**
- **Self-Biasing Inputs**
- **Hysteresis . . . 10 mV Typ**
- **Response Time . . . 6 ns Typ**
- **Maximum Operating Frequency . . . 50 MHz Typ**

D OR P PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The TL714C is a high-speed differential comparator fabricated with bipolar Schottky process technology. The circuit has differential inputs and a TTL-compatible logic output with symmetrical switching characteristics.

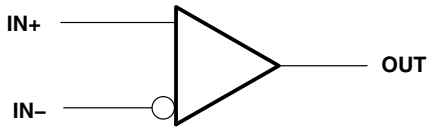
The device operates from a single 5-V supply and is useful as a disk-memory read-chain data comparator.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 50	TL714CP	TL714CP
	SOIC (D)	Tube of 75	TL714CD	TL714C
		Reel of 2500	TL714CDR	

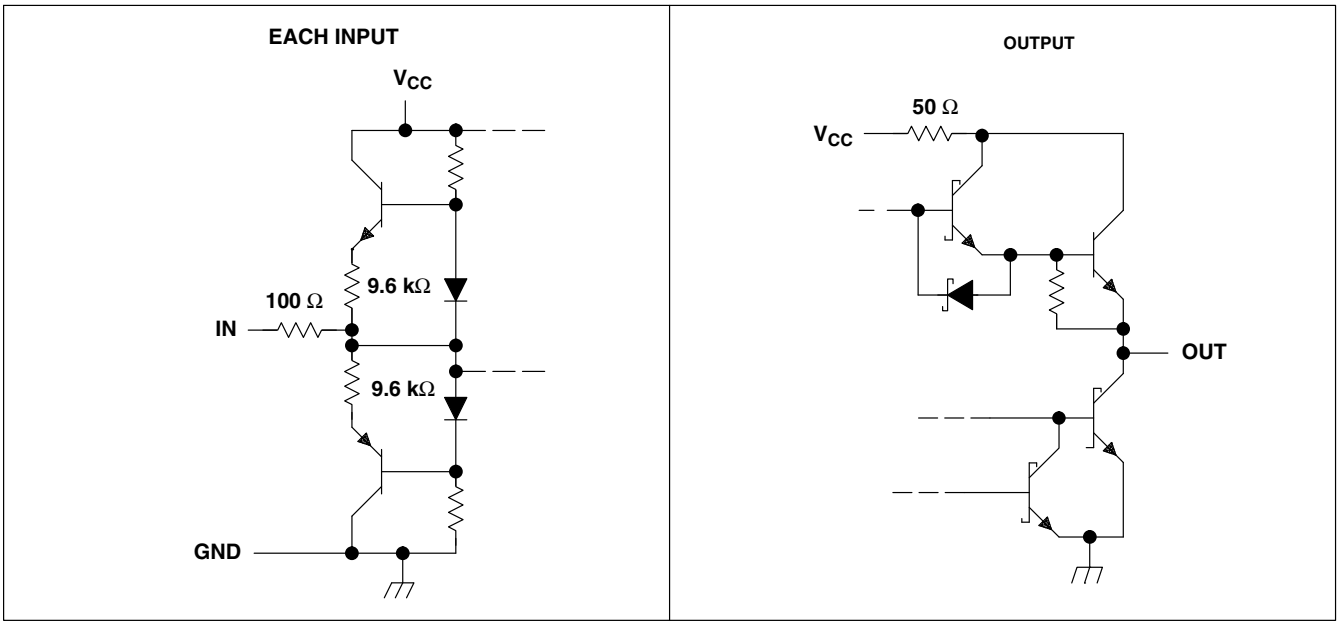
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

schematic of inputs and outputs



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±5 V
Input voltage range, V_I . . . . . V_{CC} to GND
Low-level output current, I_{OL} . . . . . 40 mA
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D package . . . . . 97°C/W
P package . . . . . 85°C/W
Operating virtual junction temperature, T_J . . . . . 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltage, are with respect to the network ground.
2. Differential voltage values are at IN+ with respect to IN–.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
4. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.75	5.25	V
V_{IC}	Common-mode input voltage	1.4 to V_{CC}–1.4		V
I_{OH}	High-level output current		–1	mA
I_{OL}	Low-level output current		16	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over free-air operating temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_T	Threshold voltage (V_{T+} and V_{T-})	V_{IC} = 1.4 V to 3.6 V		–75‡		75	mV
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)			2	10	30	mV
V_{OH}	High-level output voltage	V_{ID} = 100 mV,	I_{OH} = –1 mA	2.7	3.4		V
V_{OL}	Low-level output voltage	V_{ID} = –100 mV,	I_{OL} = 16 mA		0.4	0.5	V
I_{OS}	Short-circuit output current			–30		–110	mA
r_i	Differential input resistance			2.9			kΩ
I_{CC}	Supply current	V_{ID} = –100 mV,	I_O = 0		7	12	mA

† All typical values are at T_A = 25°C.
‡ The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
f_{max}	Maximum operating frequency	V_{ID} = ±250 mV, C_L = 25 pF,	$t_r = t_f$ = 4 ns, Input duty cycle = 50%		50		MHz
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = ±100 mV, See Figures 1 and 2	C_L = 25 pF,		6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output				6	12	ns
t_r	Rise time	V_{ID} = ±100 mV, See Figure 3	C_L = 25 pF,		4	8	ns
t_f	Fall time				4	8	ns

† All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

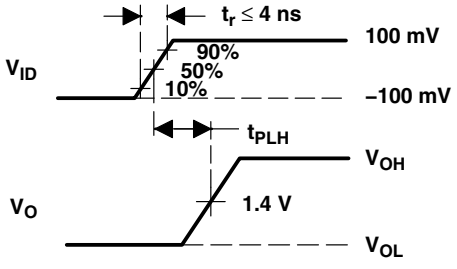


Figure 1. Propagation Delay Time, Low to High (t_{PLH})

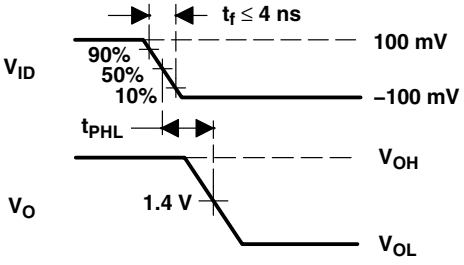


Figure 2. Propagation Delay Time, High to Low (t_{PHL})

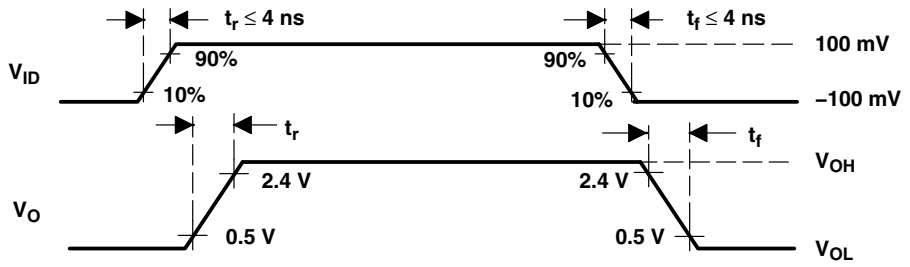


Figure 3. Rise and Fall Times (t_r, t_f)

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL714CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL714C
TL714CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL714CP
TL714CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL714CP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

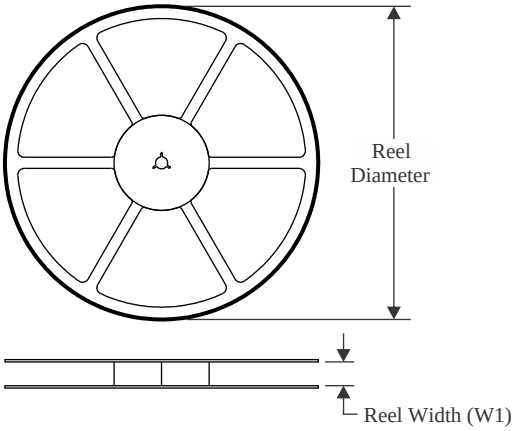
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

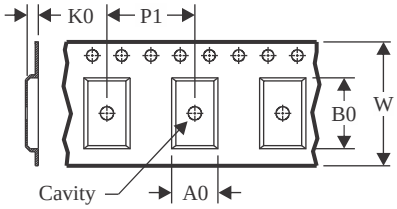
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

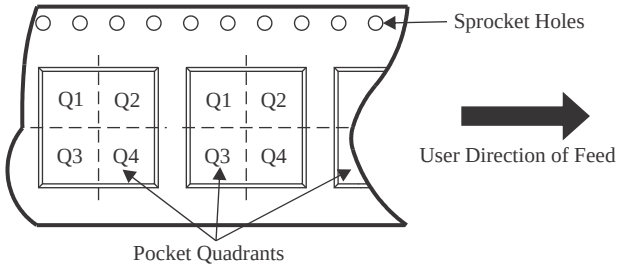


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

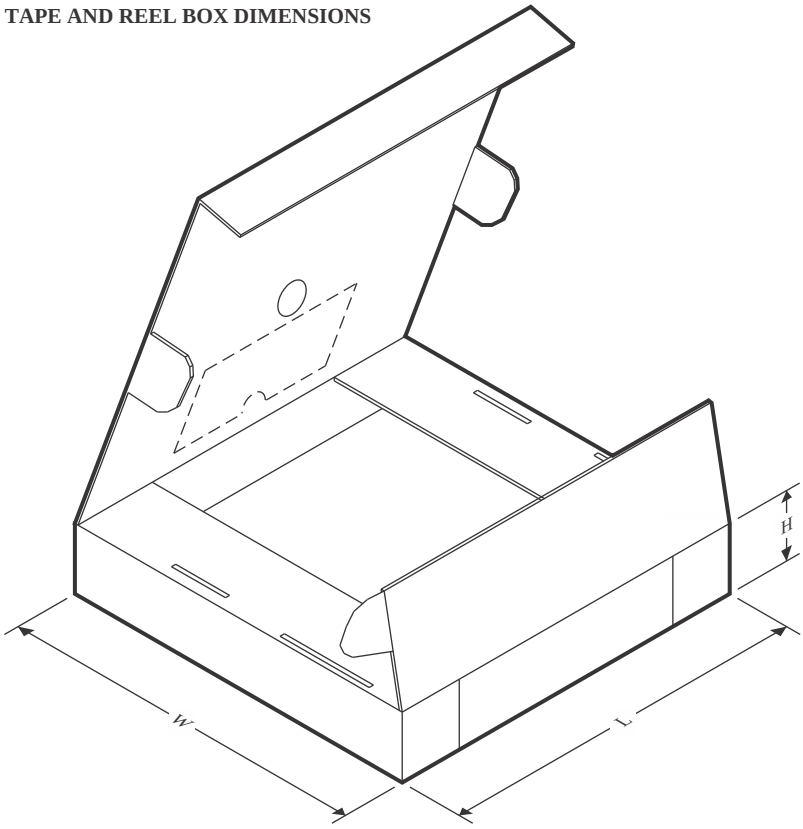
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL714CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

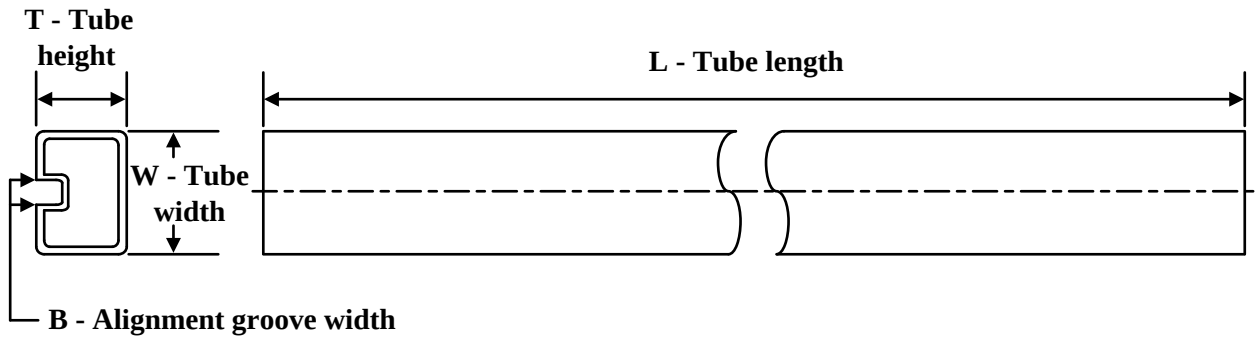
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

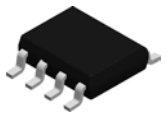
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL714CDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL714CD	D	SOIC	8	75	507	8	3940	4.32
TL714CD.A	D	SOIC	8	75	507	8	3940	4.32
TL714CP	P	PDIP	8	50	506	13.97	11230	4.32
TL714CP.A	P	PDIP	8	50	506	13.97	11230	4.32

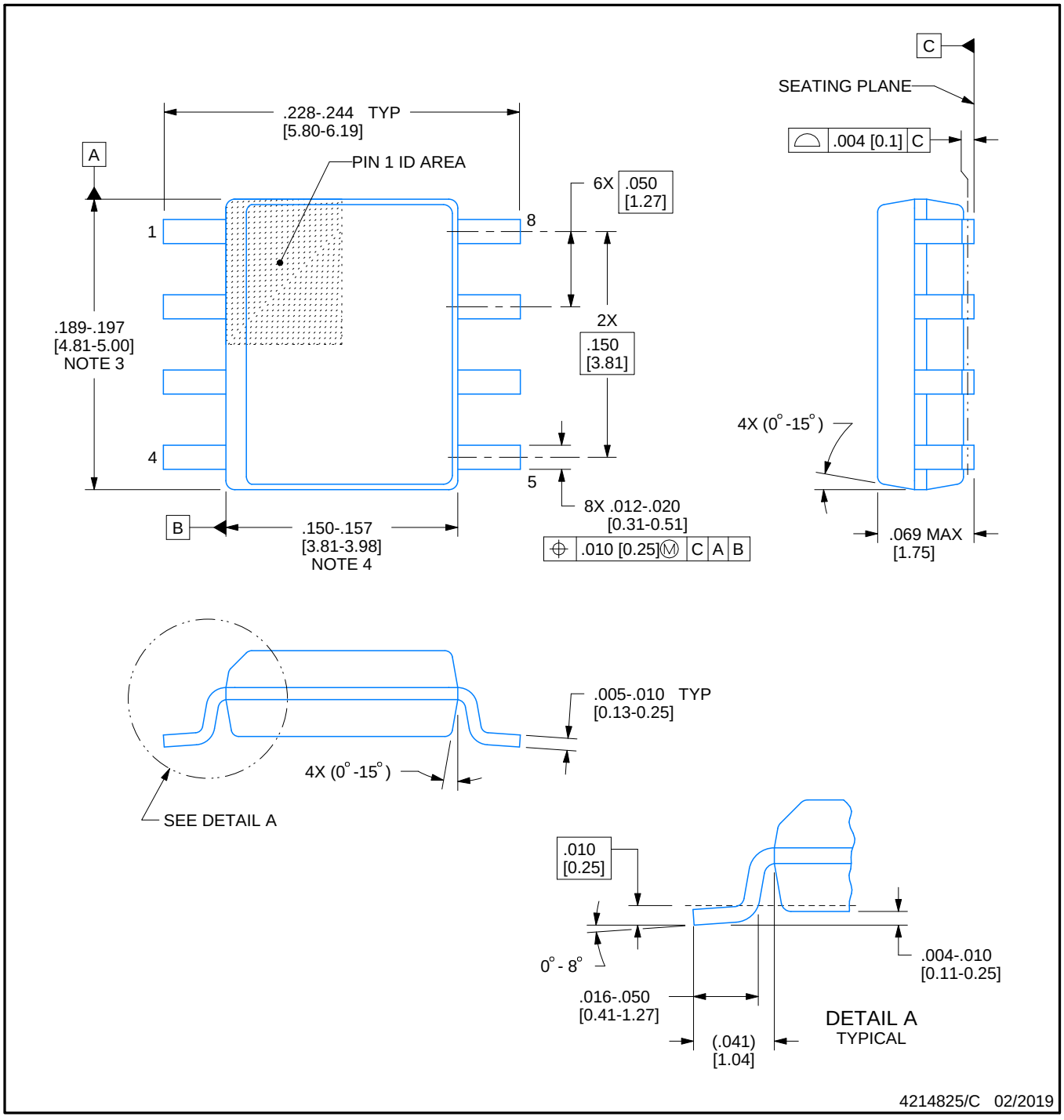


PACKAGE OUTLINE

D0008A

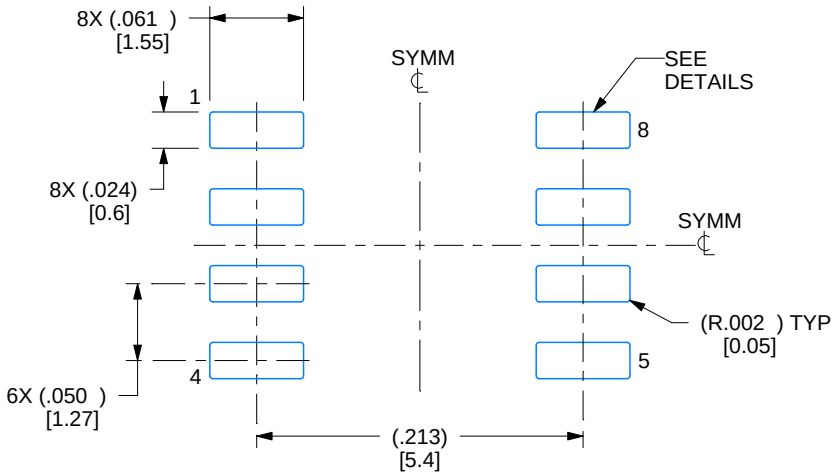
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

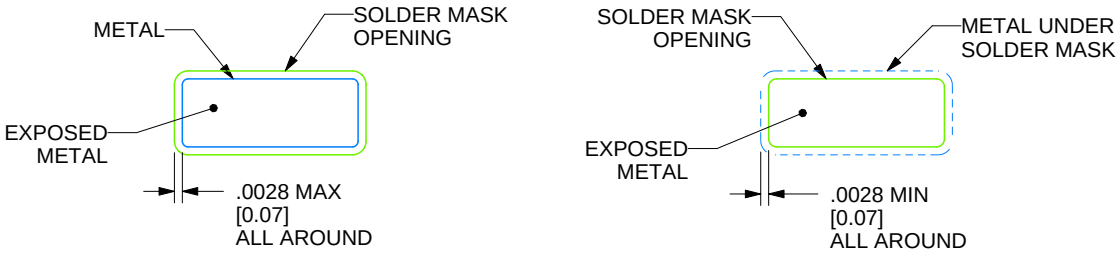


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

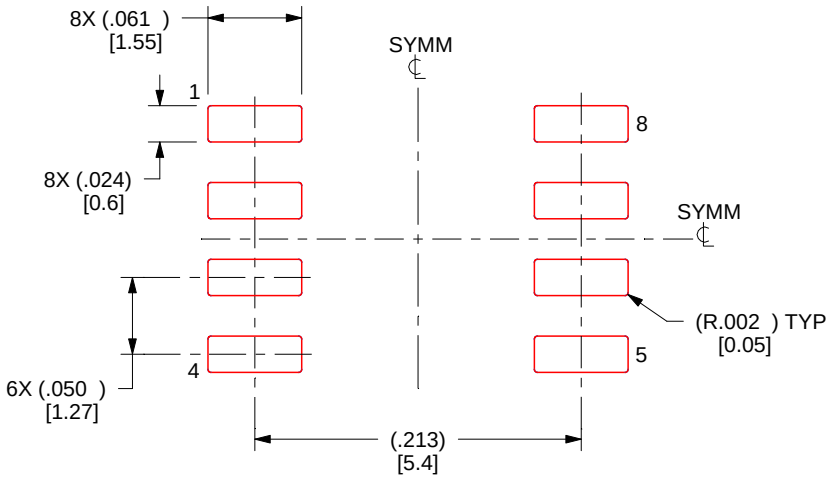
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



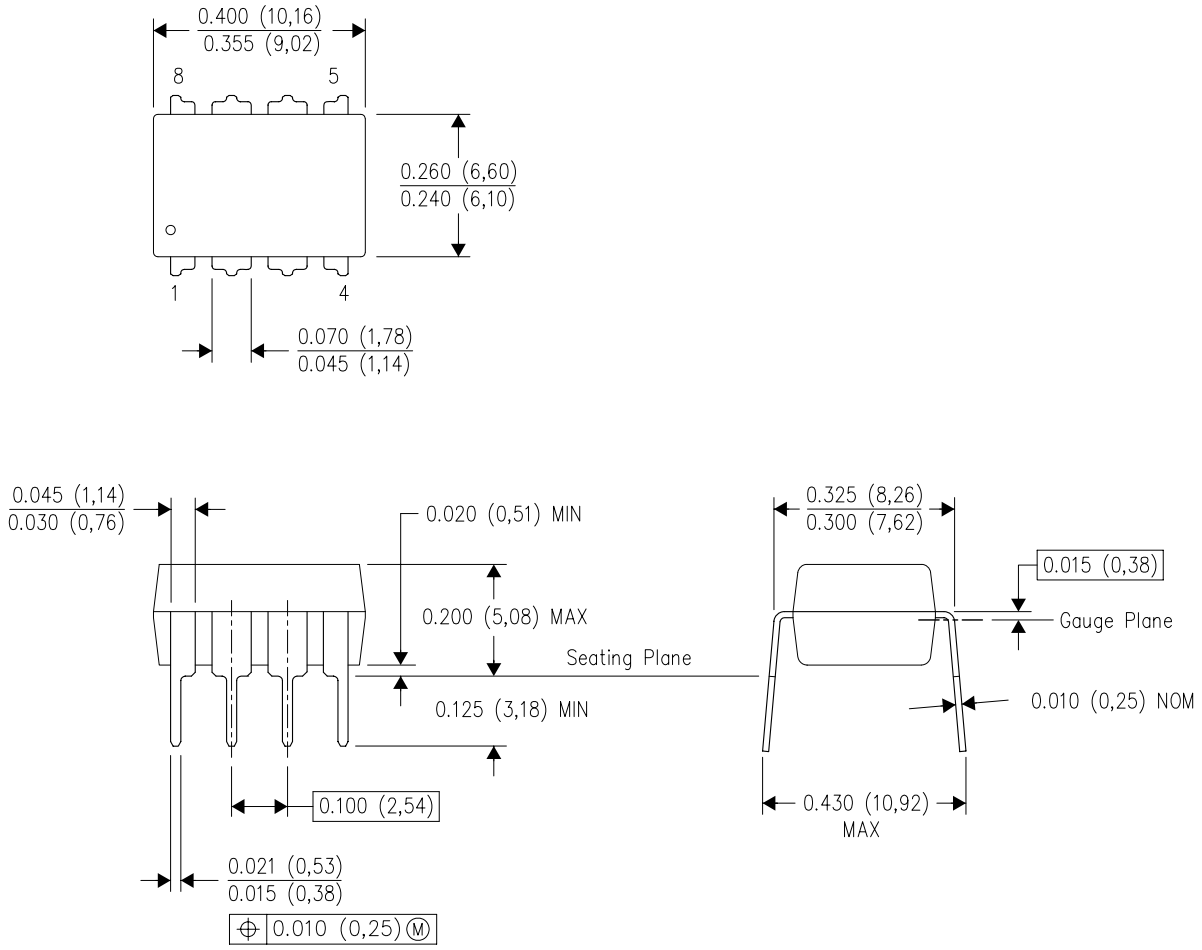
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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